The Santa Clara Valley (Silicon Valley) Chapters:

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE Photonics Society

IEEE Reliability Society

HETEROGENEOUS INTEGRATION ROADMAP

# Heterogeneous Integration (HI) Reliability

## IEEE HIR Reliability TWG

# Acknowledgement to Current Members of HIR Reliability TWG

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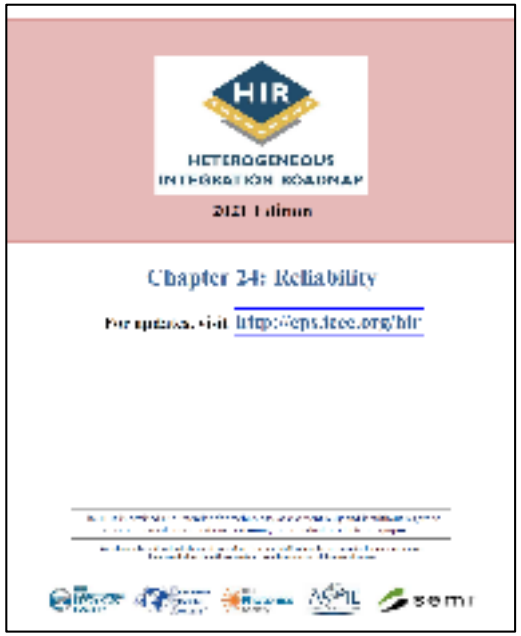

# Course Outline

- Introduction of Heterogenous Integration System
- Heterogenous Integration Reliability
- Reliability Assurance Activities
- Reliability Challenges
- Reliability Assurance Example
    - Chip to Package Interaction Reliability
    - Silicon Photonics Package Reliability

# Technology Roadmapping for Creating a Common Vision and Collaboration

The National Technology Roadmap for Semiconductors (NTRS) was initiated by SIA Technology Committee chaired by **Dr Gordon Moore**, working together with SRC and SEMATECH. In November 1992, 179 semiconductor technologists met in Irving Texas to create a common vision and collaboration (industry, suppliers, customers, academia, government & national laboratories). of semiconductor technology over the next 15 years. The report published in 1993 constitute the first open-source Semiconductor Technology Roadmap.

In 1998 the NIRS roadmap work was joined by four other regional SIAs: Taiwan, South Korea, Japan and Europe to become *International Technology Roadmap for Semiconductors (ITRS)*, In 2014 decision was made by SIA to end ITRS. The last edition of ITRS was published July 8, 2016.

The Heterogeneous Integration team in ITRS in 2014 learnt of the closure of ITRS decided to continue the Technology Roadmap effort towards shared vision and collaboration for the next era of Moore's Law progress for Electronics Resurgence into the Future Decades.

# Heterogeneous Integration Roadmap (HIR)

Launched 10-10-2019
24 chapters
590 Pages
Free download
Download Link
https://eps.ieee.org/technology/heterogeneous-integration-roadmap

- Sponsored by IEEE Electronics Packaging Society (EPS), SEMI, IEEE Electron Devices Society, IEEE Photonics Society and ASME Electronics & Photonics Division
- Comprehensively covers the complete microelectronics technology ecosystem: Industry, academia, and government organizations.
- Articulates state-of-the-art Advances in Technology & Science, Future directions, Roadblocks & Potential solutions
- Heterogeneous Integration Roadmap is the Roadmap for the Next Era of Moore's Law paving the way towards Electronics Industry Resurgence decades into the future.

# Heterogeneous Integration Roadmap (HIR)

- HIR was founded with initiative from several IEEE Societies
  - Electronics Packaging Society
  - Electron Devices Society
  - Photonics Society
- SEMI (Semiconductor Equipment and Materials International)
- ASME EPPD (Electronic and Photonic Packaging Division)
- Dedicated to embrace innovation wherever it arises and promote collaboration wherever possible to accelerate progress in the microelectronics market landscape.

# Heterogeneous Integration Roadmap Chapters

## Covering the Microelectronics Systems Products & Technology Ecosystem

HETEROGENEOUS INTEGRATION ROADMAP

### HI Systems & Market Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Microelectronics Ecosystem
23 Technical Working Groups
Working in Collaboration

### Cross Cutting topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- **Reliability (formed 2021)**

### Heterogeneous Integration Components

- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communication & Beyond

### Integration Processes

- SiP & Module
- 3D +2D & Interconnect
- Wafer Level Packaging (fan in and fan out)

### Co-Design + Simulation

- Co-Design
- Simulation

Kanad Ghose

John Shalf

Madhu Iyengar

Azmat Malik

Weihua Tang

Ravi Mahajan

Subu Iyer

Bill Bottoms

Amr Amry

Ken Butler

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Jose Schutt-Aine

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Mark Poliks

Nancy Stoffel

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Richard Rao

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Veer Dhandapani

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Mary Anne Maher

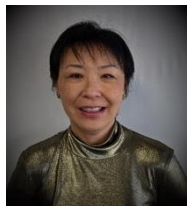
Siva Sivasankar

Kitty Pearsal

Paul Trio

Pat. McKluskey

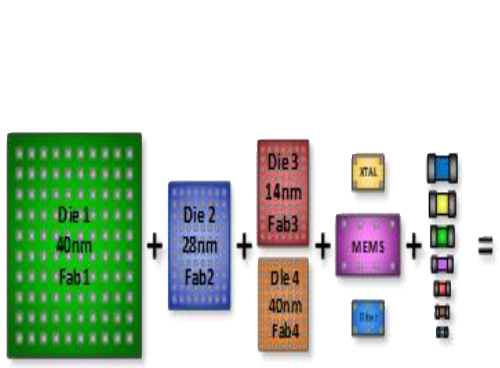
Doug Hopkins


Annette Teng

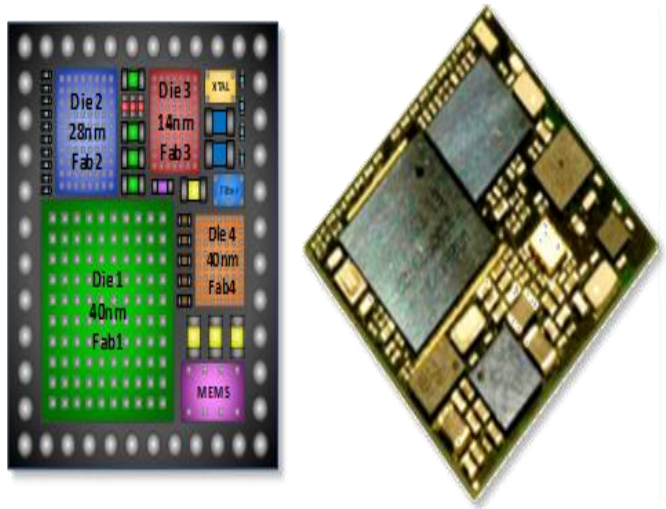
Melissa Grupen-Shemansky

# Heterogeneous Integration Roadmap Technical Working Groups Chairs & Co-Chairs

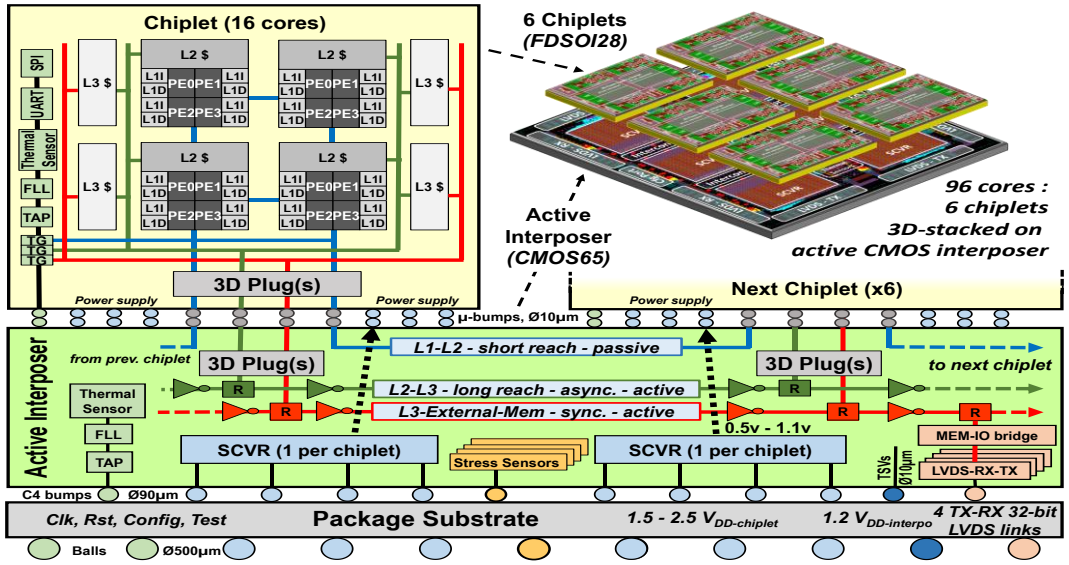
# The Definition of Heterogeneous Integration




Die + Heterogeneous

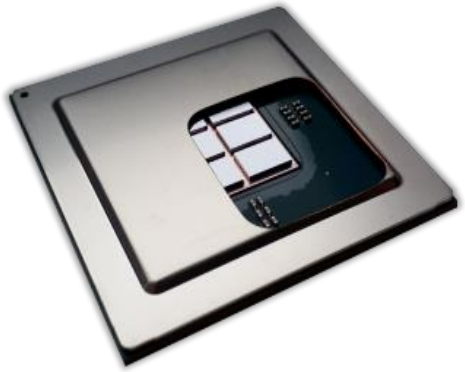


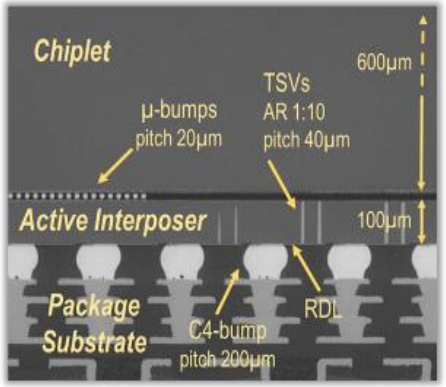

System in Package (SiP)




**Heterogeneous by multi-scale and multiphysics:**

- **Material**
- **Component type (IC, Photonics, MEMS, sensors)**
- **Circuit type (DRAM, Serdes, logic, RF, Power)**
- **Si Node**
- **Level/method of bonding/interconnection**

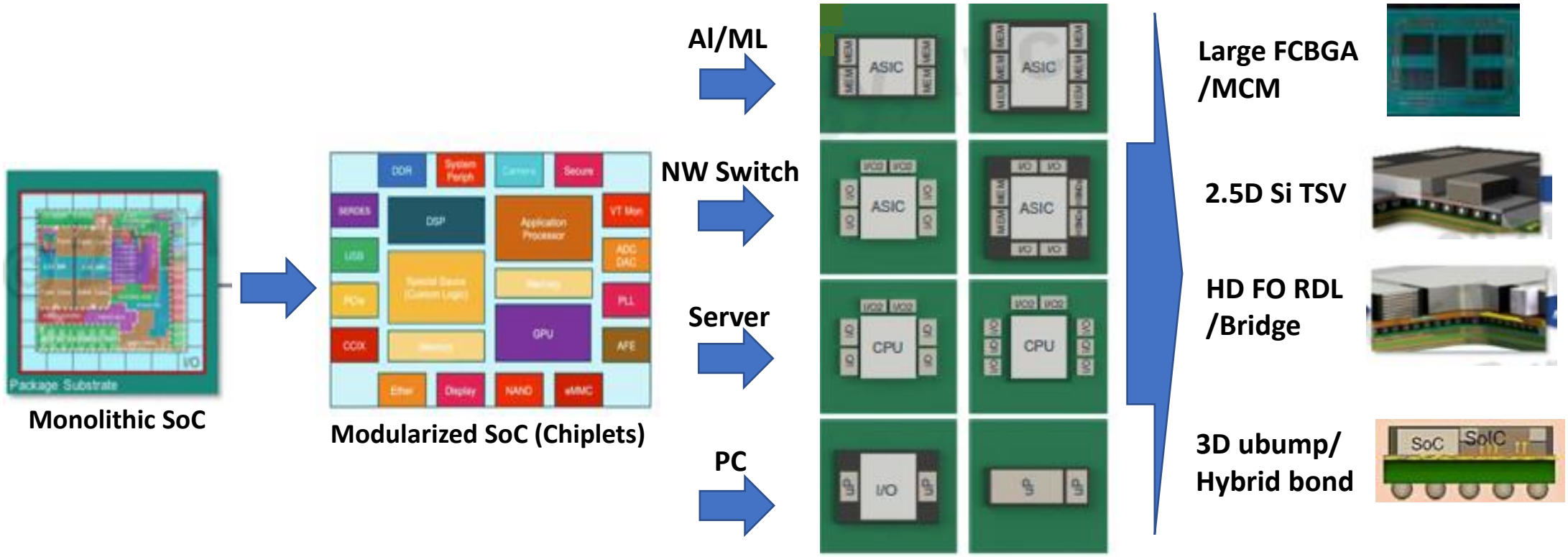





Source: 2020 ISSC

# Chiplets – Heterogeneous Integration

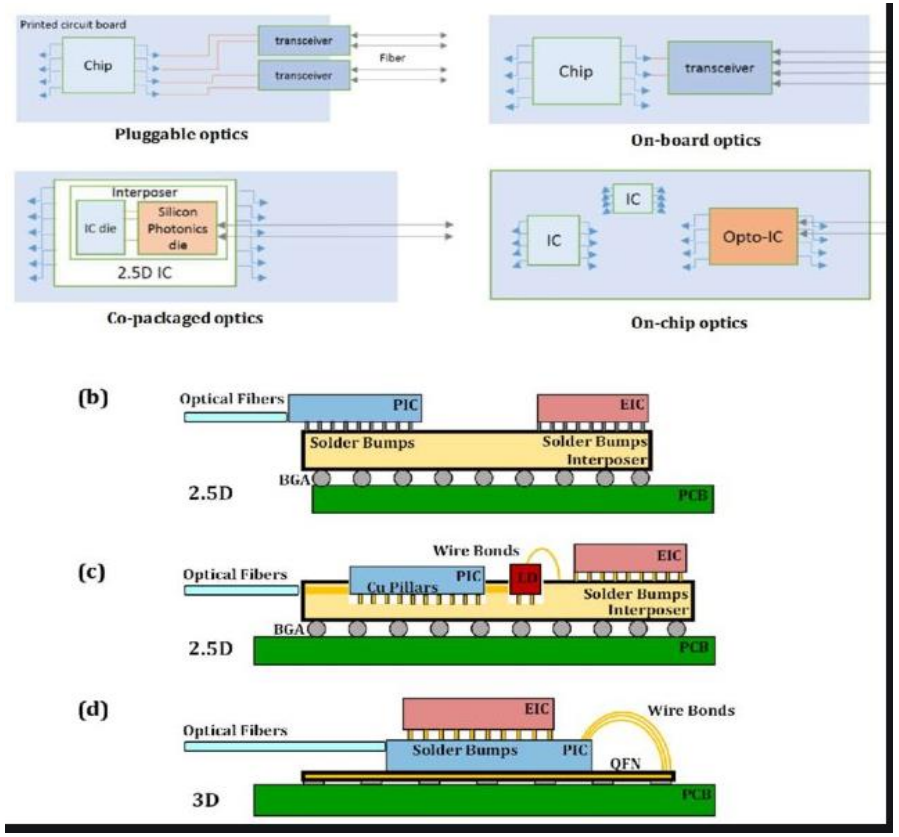
## Chiplet integration becoming mainstream for HPC through Advanced Packaging Platforms

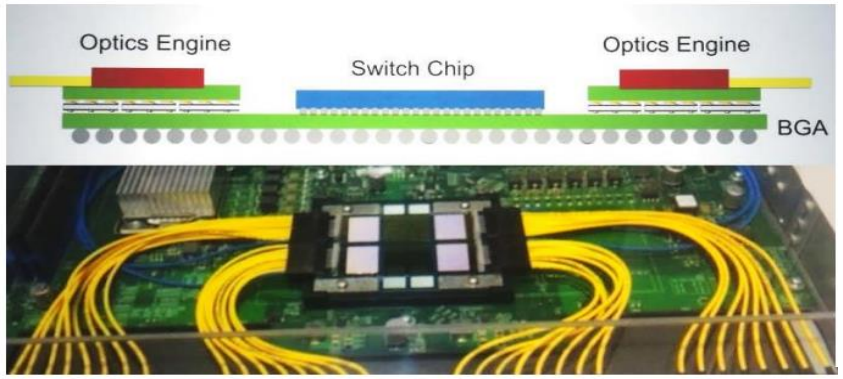


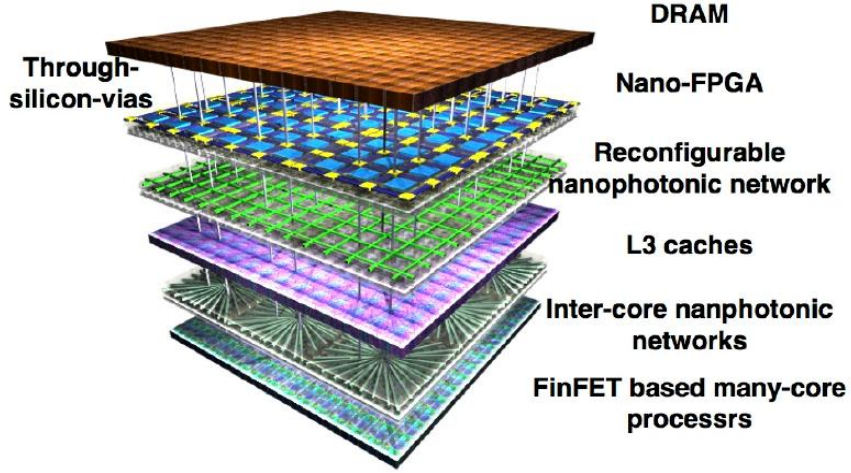

Reference: ”The March Towards Chiplets” Ed Sperling & Karen Heyman, December 15, 2022. Semiconductor Engineering

# Heterogenous Integration of Electronics and Photonics

- Evolution of Photonics Packaging
  - Heterogenous integration of passive/active photonics devices and IC devices from board level to package and wafer levels
  - Co-Packaged Optics (CPO) Using 2.5D and 3D Packaging technology

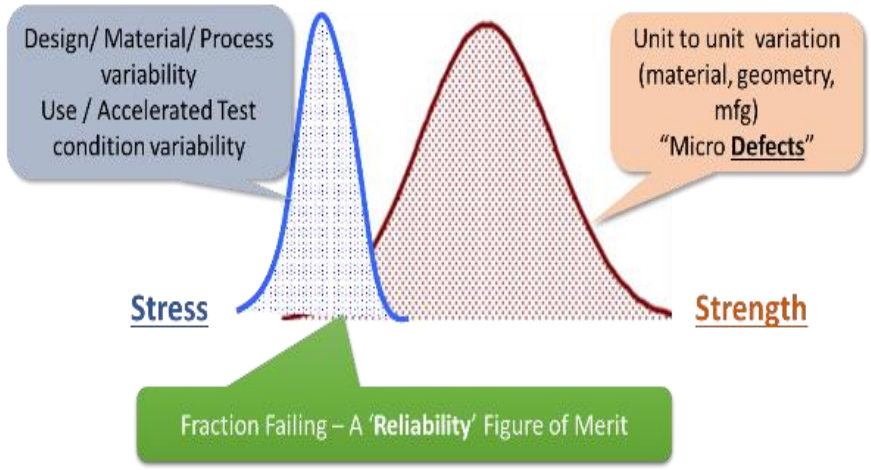


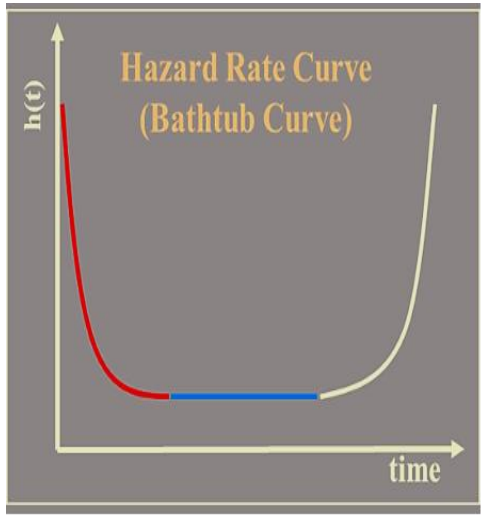



# Heterogenous Integration System Reliability Introduction

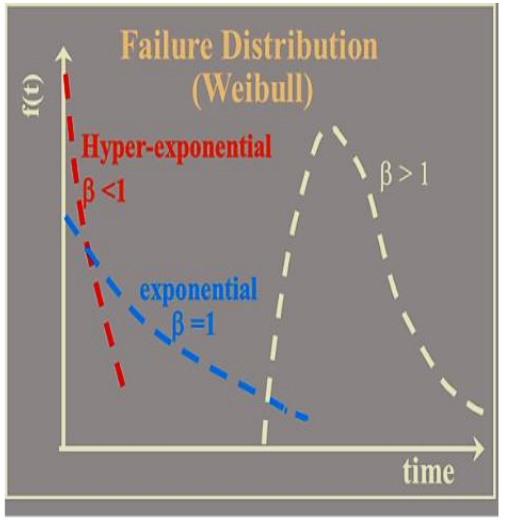
- Systems with heterogeneous integration (HI) will experience new multiscale chip-package interactions and multi-physics failure modes
- Managing reliability of HI systems will require holistic cradle-to-grave methodology
- HI system reliability depends on aggregation of multiple degradation modes



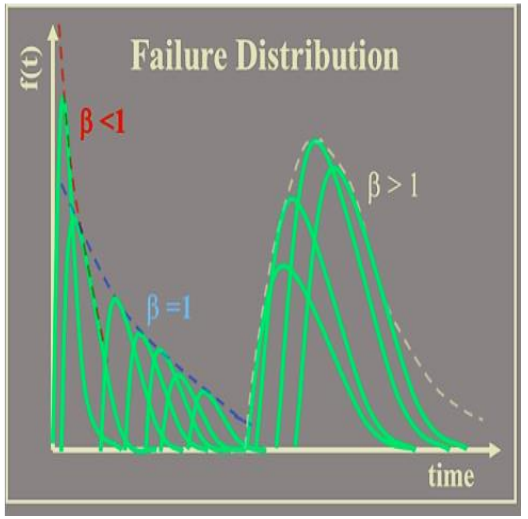

Definition of Reliability Failure




Typical Bathtub Curve based on hazard rates




System-level Bathtub Curve expressed as Weibull Failure Distribution



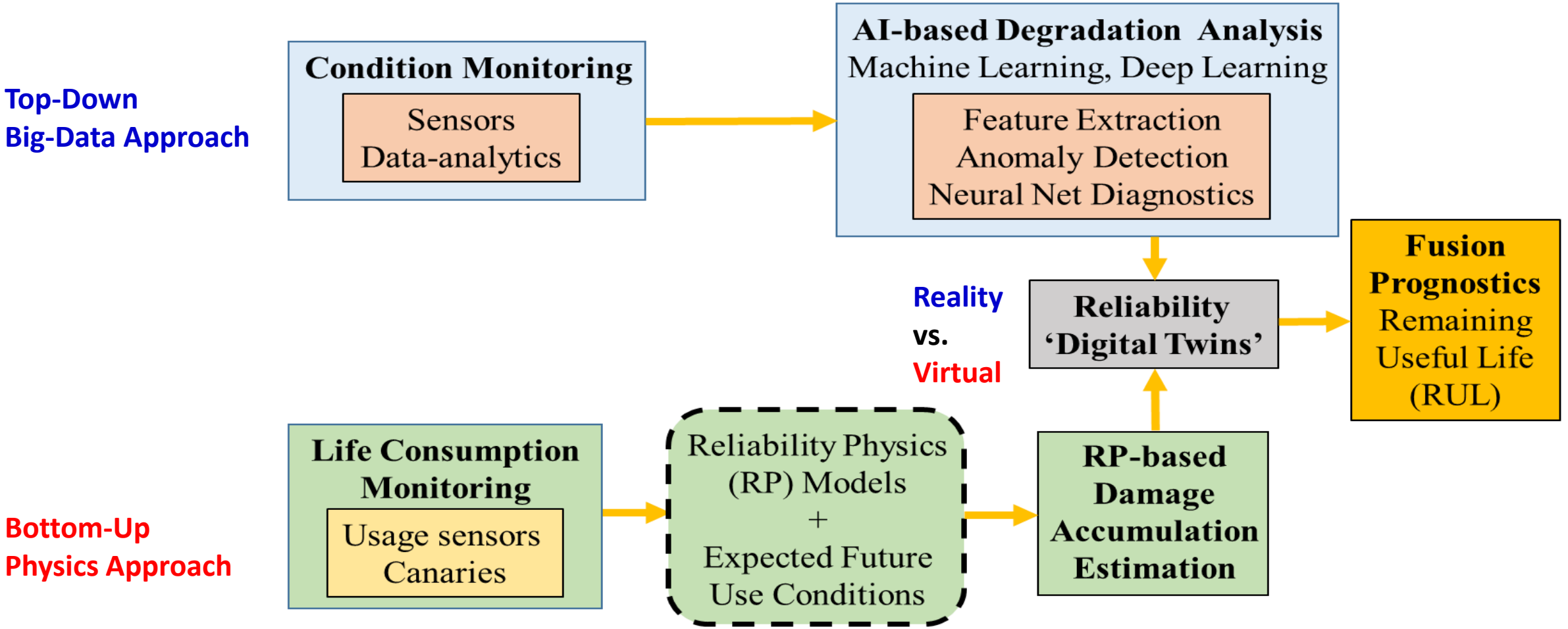

HI Systems Bathtub curve is the result of Multiple Competing Failure Modes

- **In this era of Chiplets and multi-devices packages, innovations and collaborations in Reliability Technology and Science will be crucial for the semiconductor and microelectronics industries decades into the future.**

# Reliability Methodology of HI Systems

HETEROGENEOUS INTEGRATION ROADMAP

- ‘Digital Twins’ for managing reliability will rely on fusion methods that combine bottom-up physics and top-down big-data approaches

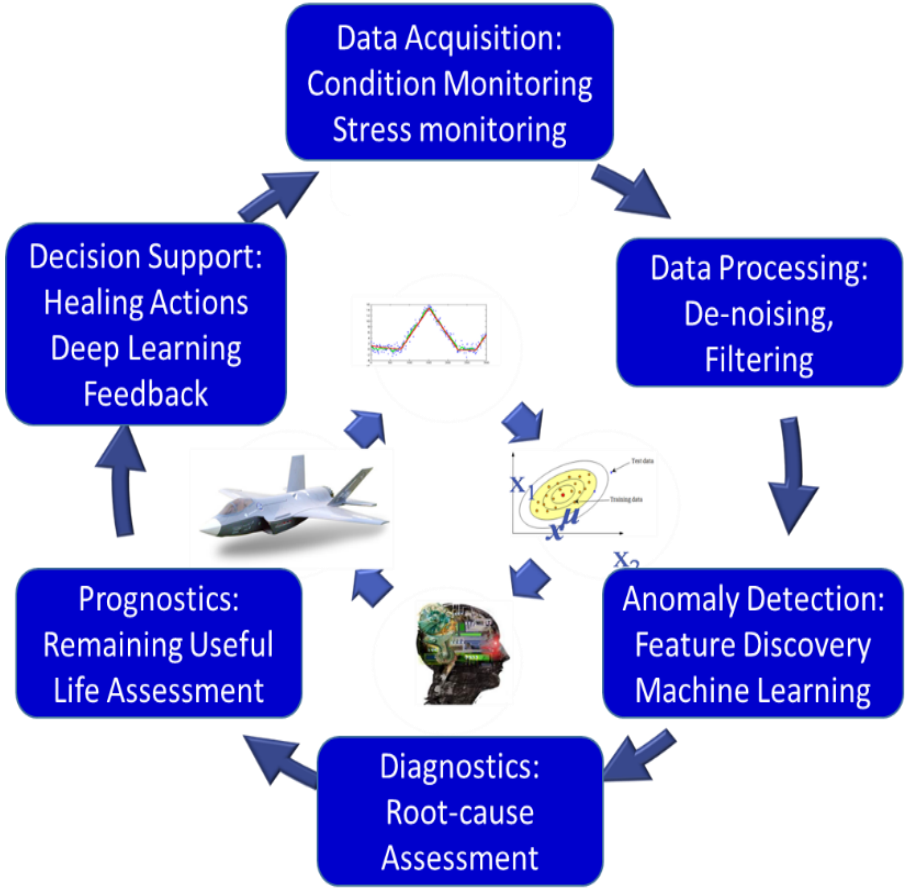


# Detailed Flow for Bottom-Up and Top-Down Approaches

## Methodology for Reliability Assurance

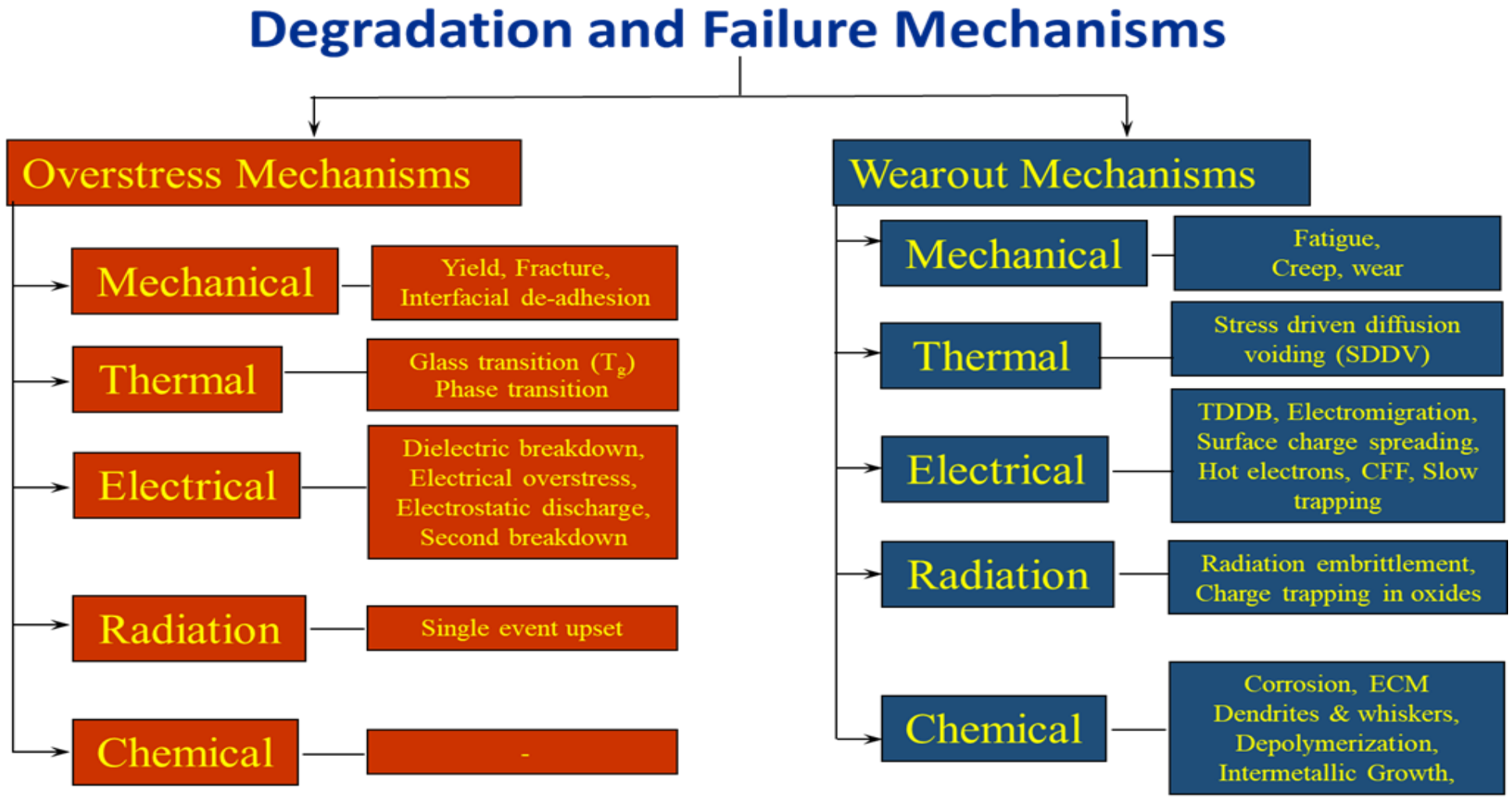
- Reliability Targets
- Life Cycle Conditions
- Design for Reliability
- Manufacturing for Reliability
- Knowledge based Testing for Qualification
- Product Health Management
- Supply chain Integration

**Bottom-Up**
**Physics Approach**

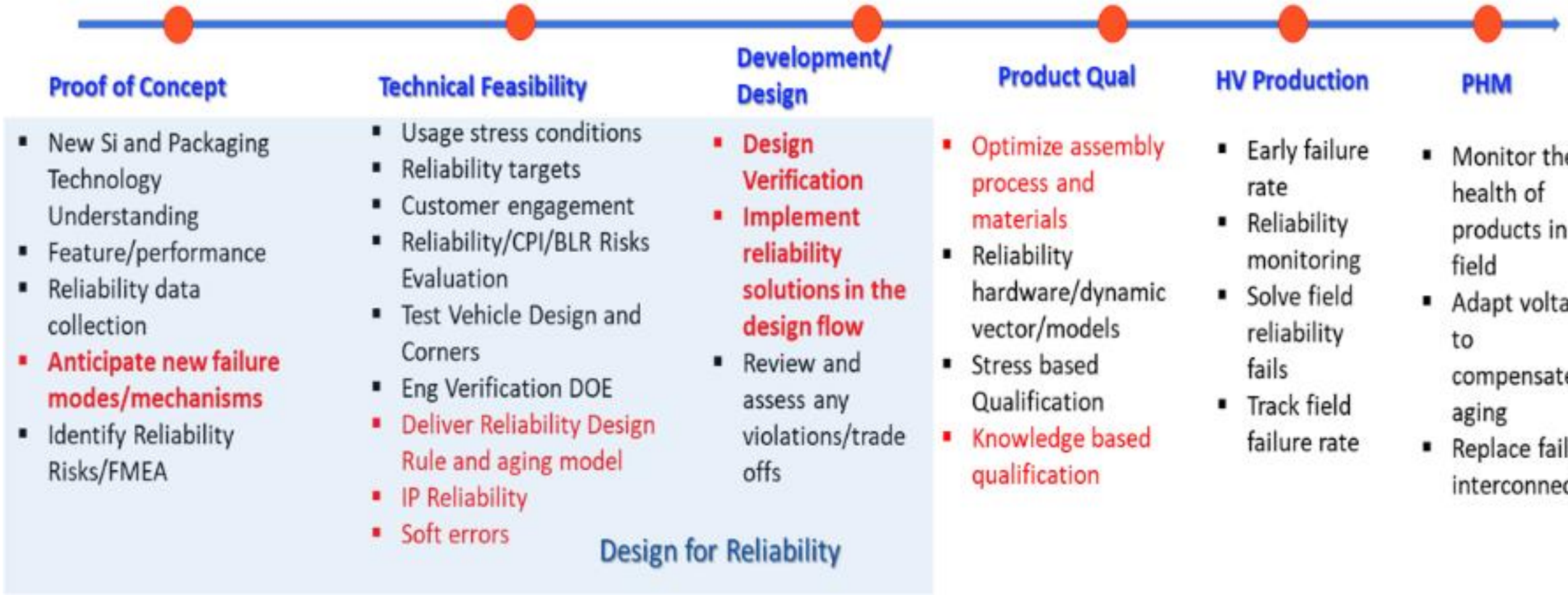



**Top-Down**
**Big-Data Approach**

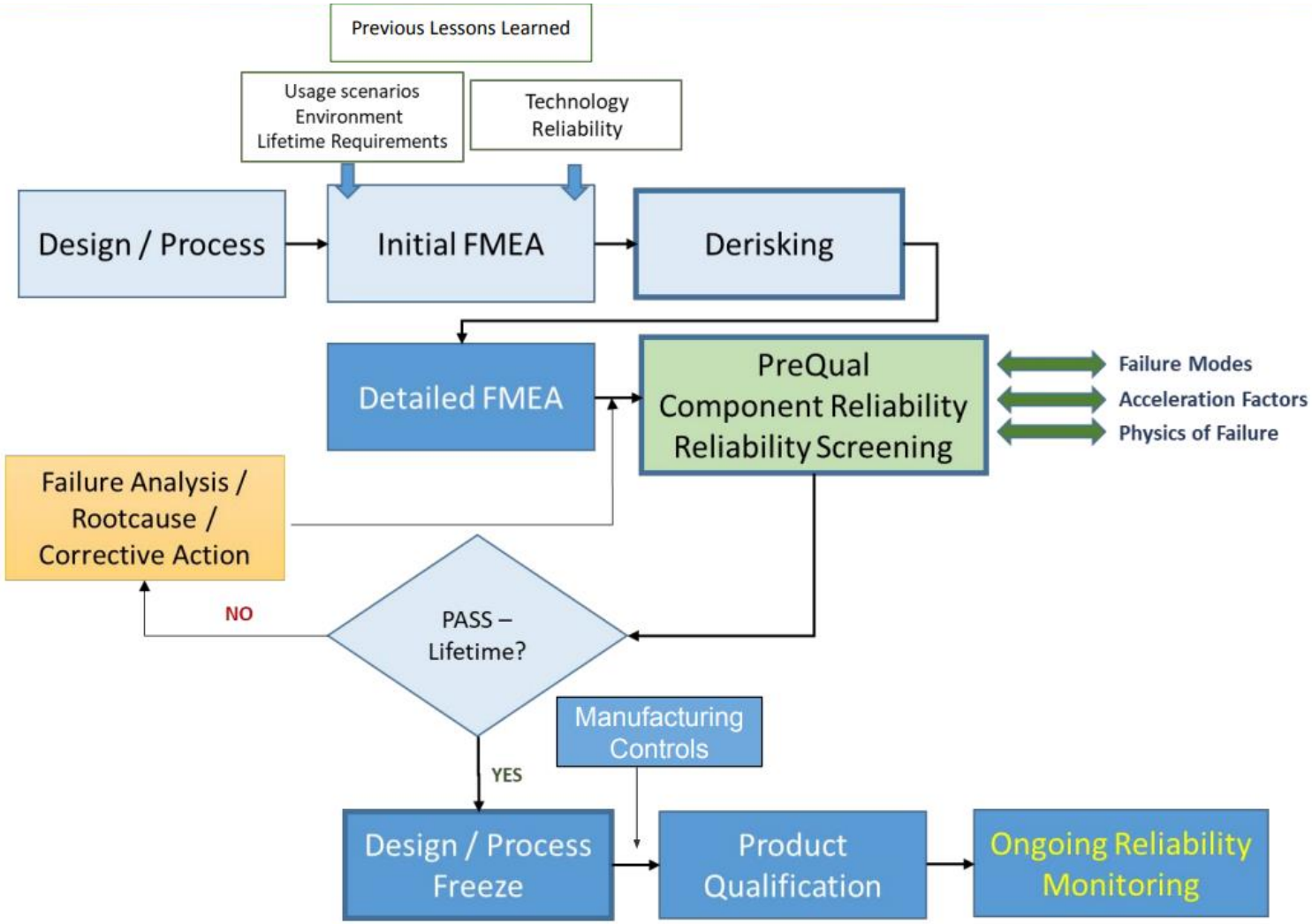
# HI Reliability Physics



# Reliability Functions in Product Lifecycle



# Design for Reliability (DfR) Program-Key Components



# Product Development Considerations

## Operational

- Usage Scenarios - continuous on, xx hrs per day, cyclic
- Environmental - (Controlled, Uncontrolled, Commercial, Industrial, …)
- Lifetime: (Automotive, Telecom, Datacenter, Consumer, ..)
- Stability and Drift Requirements
- Failure Rate Requirements

## Wafer Fabrication

- Established Foundry Technology - DRC, PDK, Reliability model, PCM
- New Technology Fab - Process Development, Reliability Development, Screening, Manufacturing Control

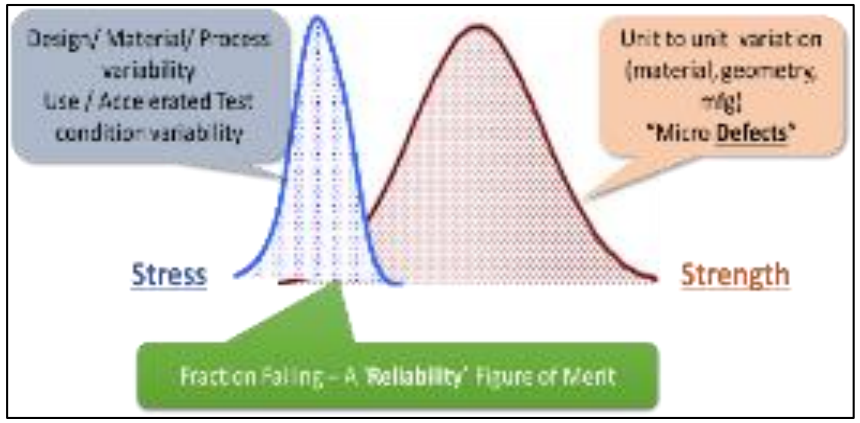
## Supplier Strategy

- Component
- Assembly
- Test
- Reliability Execution
- Volume Manufacturing

## Controls Strategy

- Sensing and Control Elements
- Control Firmware - In-field adjustment capability
- Monitoring Capability

# Reliability Assurance Activities




**Reliability Targets**

**Life Cycle Conditions**

**Design for Reliability**

**Manufacturing for Reliability**

**Knowledge based Testing for Qualification**

**Product Health Management**

**Supply chain Integration**

# Hardware Reliability Topic Matrix

## ❑ Reliability road-map of HI systems requires coordination across all TWGs

| | Reliability Targets | Life Cycle Conditions | Design for Reliability | Manufacturing for Reliability | KBT[4] for Reliability Qualification: EV/DV/PV[1] | PHM[5] | Supply Chain |
|---|---|---|---|---|---|---|---|
| **SiP Technologies** | TWGs: SCM/MCM , Photonics, MEMS, Power, RF/Analog | | TWGs: Electromigration; Materials; Co-Design and Simulation Topic Teams: Electrical System Performance; Thermal Management; Mechanical Structure and Mechanics | TWGs: SCM/MCM; Photonics; MEMS/Sensors; Power; RF/Analog; Test | Test TWG | Security TWG | Supply Chain TWG |
| **Package Integration** | TWGs: WLP, 2.5D/3D, Interconnects, SIP Topic Teams: WST; Substrate | | | TWGs: WLP; 2.5D/3D; Interconnects; SIP, Test; Topic Teams: WST; Substrate; Board Assembly | | | |
| **Applications** | TWGs: Mobile, IoT, MHW, Automotive, HPC, Aerospace | | | TWGs: Mobile; IoT; MHW; Automotive; HPC; Aerospace; Test | | | |

# Reliability roadmap will be synchronized with different

## Application Segments: Example - Automotive HI Systems Challenges

- **Drive Electrification**
- **Connectivity**
- **Autonomous Driving**
- **Smart Mobility**

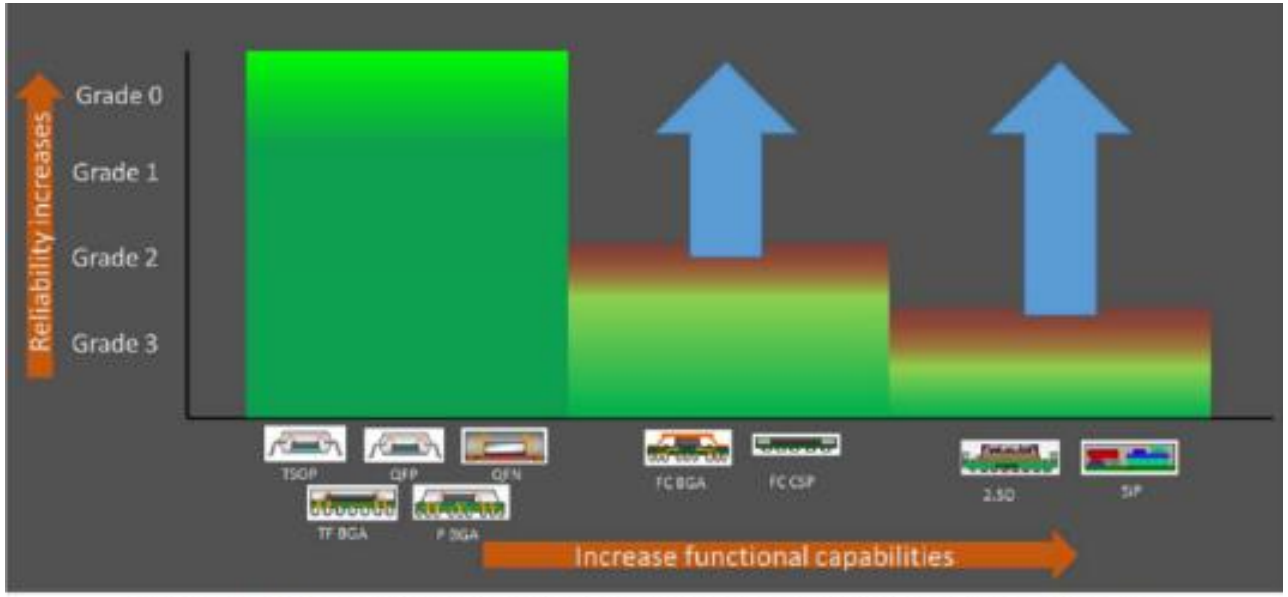
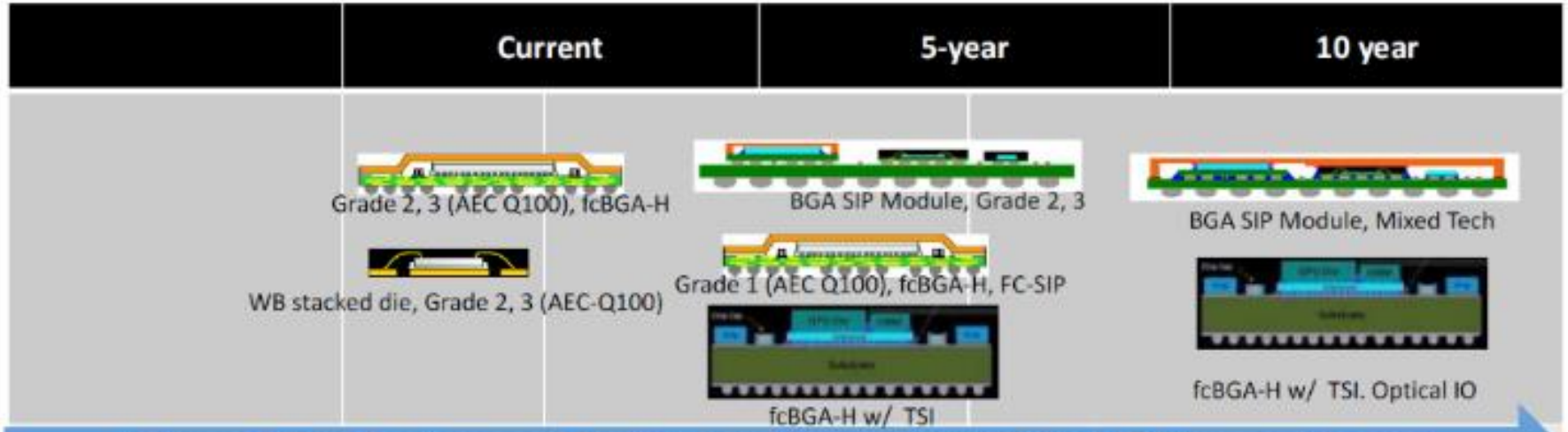



*Figure 9. Role of Reliability Requirements and Functional Capabilities*

Source: Automotive Chapter, HIR, 2020

- New materials
- Infotainment/ADAS:
- Processor/memory integration
- Thermal requirements, ambient conditions
- Qualification requirement, especially safety for ADAS
- Sensors
- Cost effective packaging
- Performance requirements
- E/HEV segment
- Highly efficient power packaging

# Reliability roadmap will be synchronized with different Application Segments: Example - Automotive HI Processor Roadmap

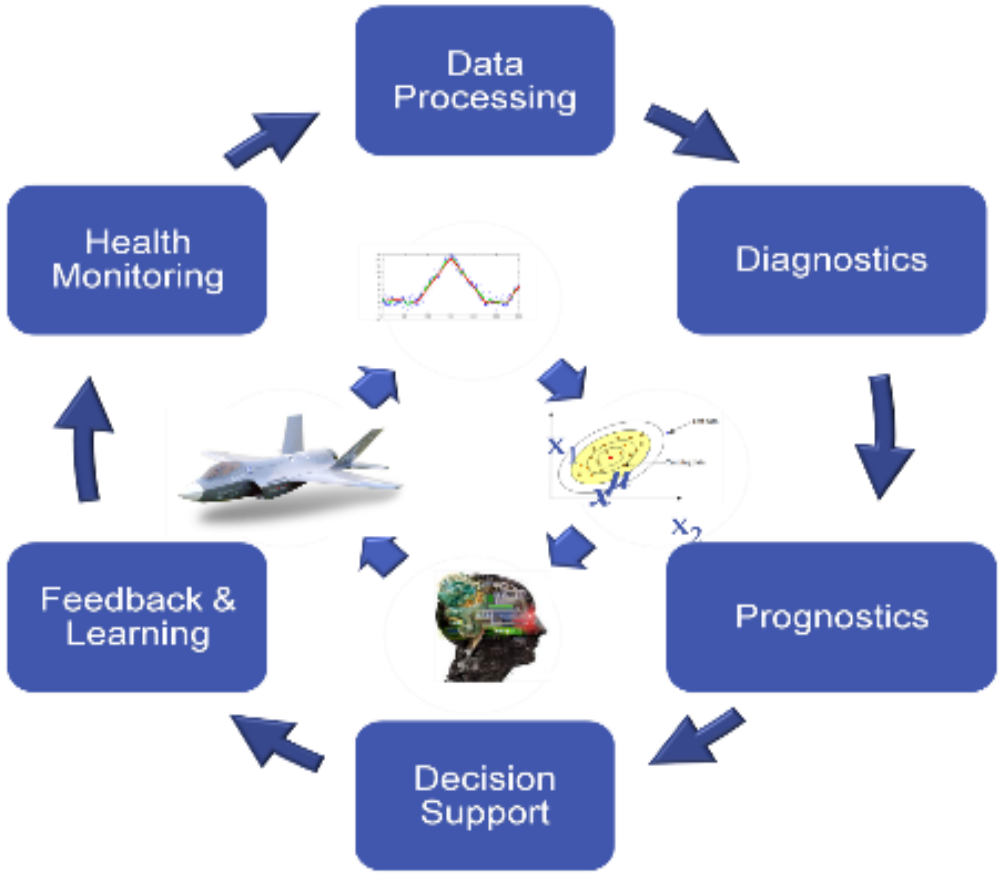



| | | | |
|---|---|---|---|
| Si Node | 40nm/28nm/14nm/10nm/7nm | | 5nm/3nm/2nm |
| Interface Speed (parallel), opto | High end 128 bit (32bit X 4 channels) →Massive parallelism<br>Mid-end 64 bit (32bit X2 channel) | | |
| Bump pitch | 150um/130um/110um | | <100um |
| Mounting structure | PCB Attach | | SIP/Module |
| Reliability | AEC Q100 Grade 3/2/1 | AEC Q100 Grade 2/1<br>AEC Q006 Grade 1 | AEC Q100 Grade 1<br>AEC Q-104 for SIP |
| Safety | ASIL-B | ASIL-D? | |

*Figure 4. Automotive Processor Roadmap*

Source: Automotive Chapter, HIR, 2020

# Top Down: Data-Based System-Level Prognostics and Health Management



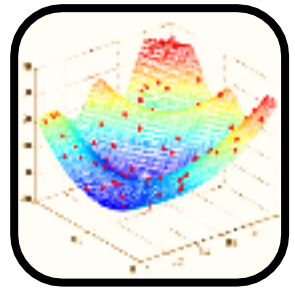

PHM methods can work with:

- Physical data
- Simulated data
- Physics models

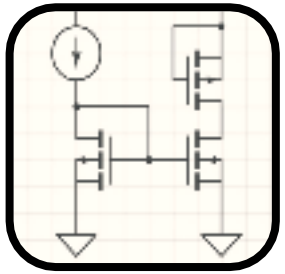
Canaries can be developed for early warning

PHM methods being developed are very suitable for Digital Twins

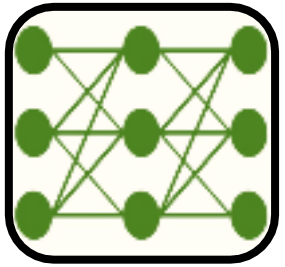
**Design of Experiments**



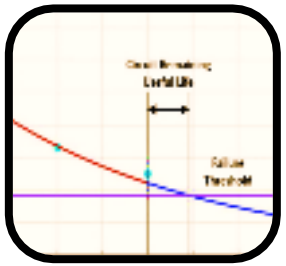
**Circuit Simulations**



**Fault Diagnosis**

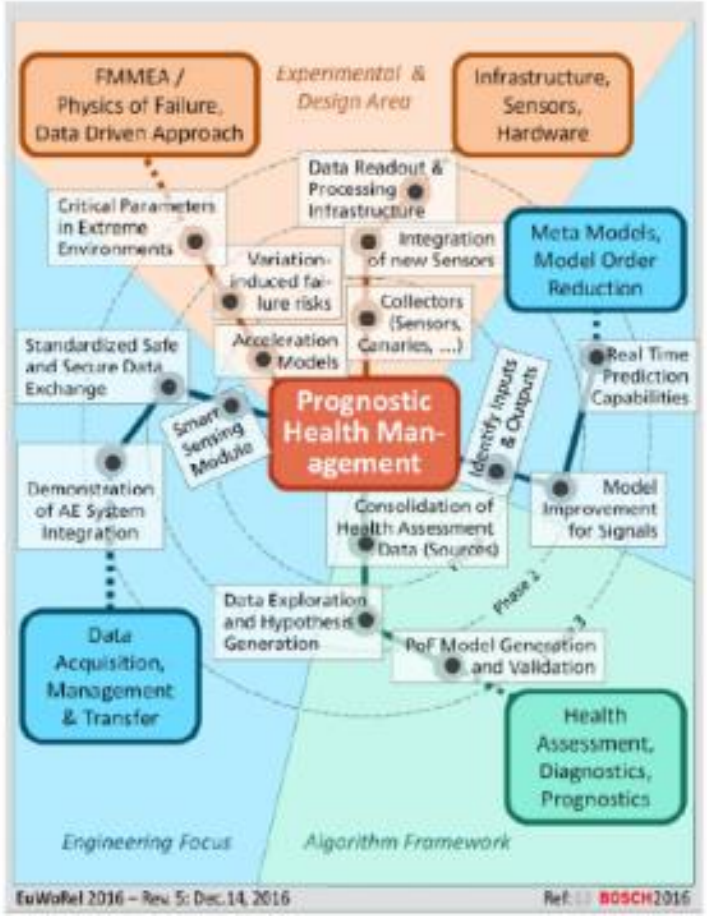


**Fault Prognosis**



# Automotive TWG: PHM for Life-Cycle Reliability Assurance

- **Electrification**
- **Autonomous Driving**
- **Connectivity**
- **Smart Mobility**




Source: Automotive Chapter, HIR, 2020

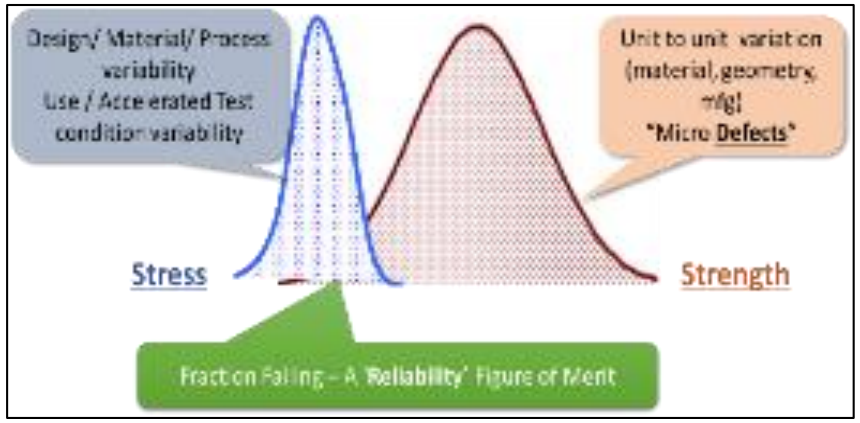
**Data-driven approach requires:**

- Available/new **sensors** for in-situ monitoring of device/system life;
- Identification of **failure pre-cursors for different degradation modes** for in-situ monitoring during the lifetime of electronic products
- AI/ML-based algorithms for **anomaly detection and failure identification**;
- Hierarchical, local (at device level) and global (at ECU level) state of **health evaluation** schemes that will enable a damage calculation for each single ECU level;

**Reliability Physics model-based approach requires:**

- A generalized multi-domain and multi-scale simulations flow for **virtual design and testing** under accelerated and field conditions;
- AI/ML-based algorithm for compact models and **digital twins** of electronic components, modules, and complete ECUs for coupled-field, nonlinear and transient effects;
- Deeper physical understanding of the **root cause of damage**, especially under multi-domain (electrical/thermal/mechanical/chemical) loading conditions that design elements experience in the field

# Reliability Assurance Activities




**Reliability Targets**

**Life Cycle Conditions**

**Design for Reliability**

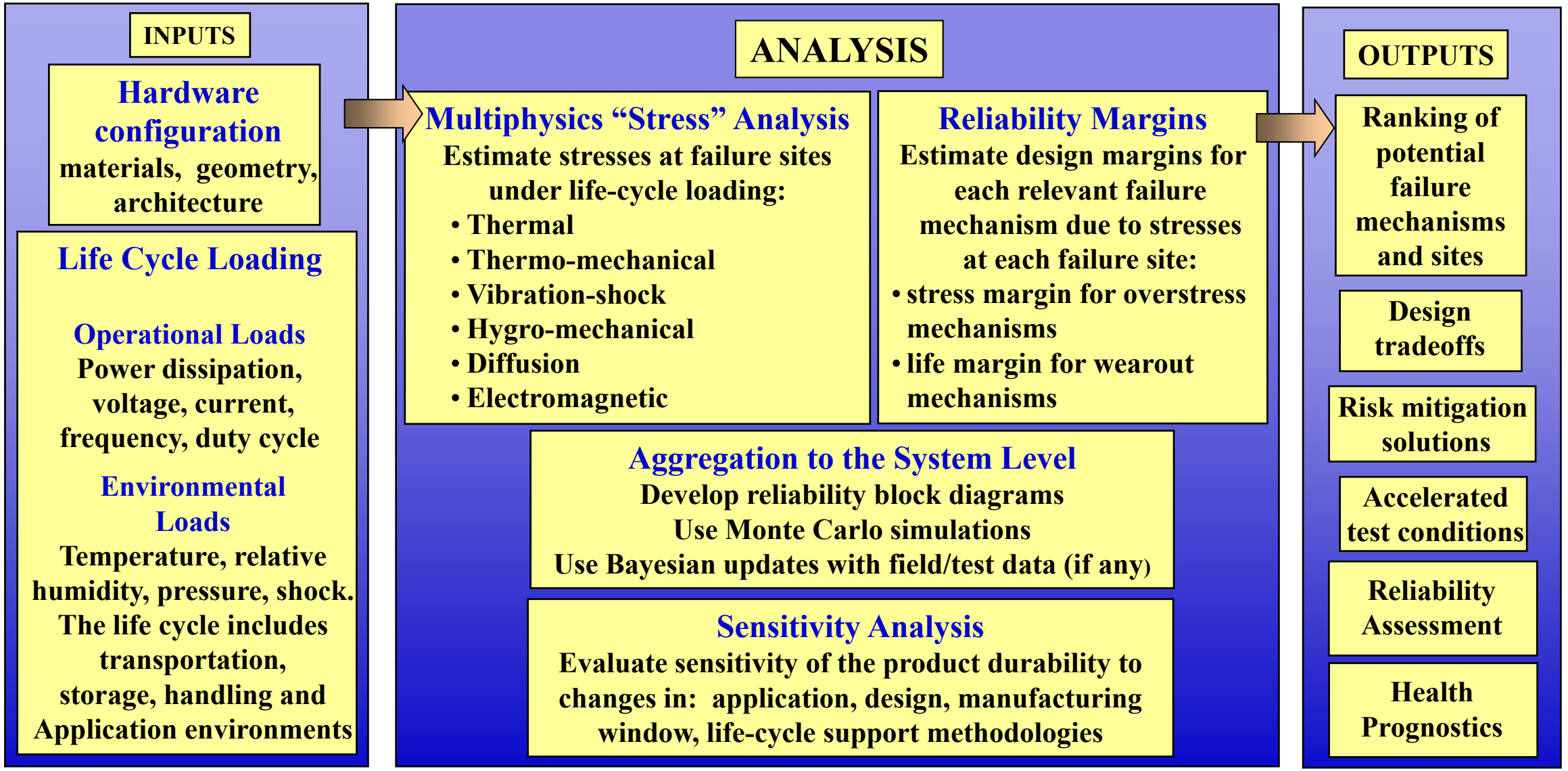
**Manufacturing for Reliability**

**Knowledge based Testing for Qualification**

**Product Health Management**

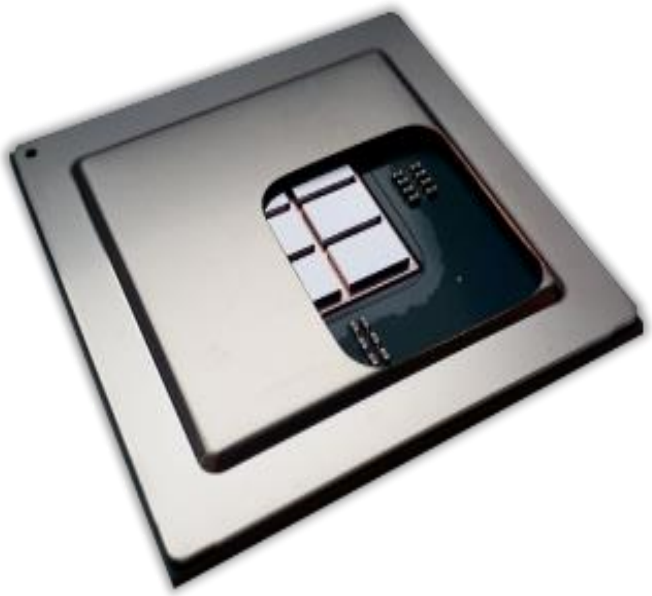
**Supply chain Integration**

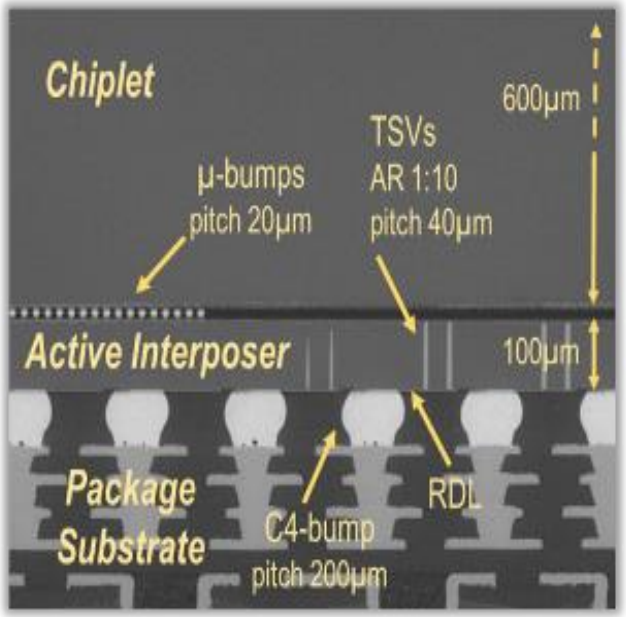
# Designing for Reliability: Reliability-Physics Process



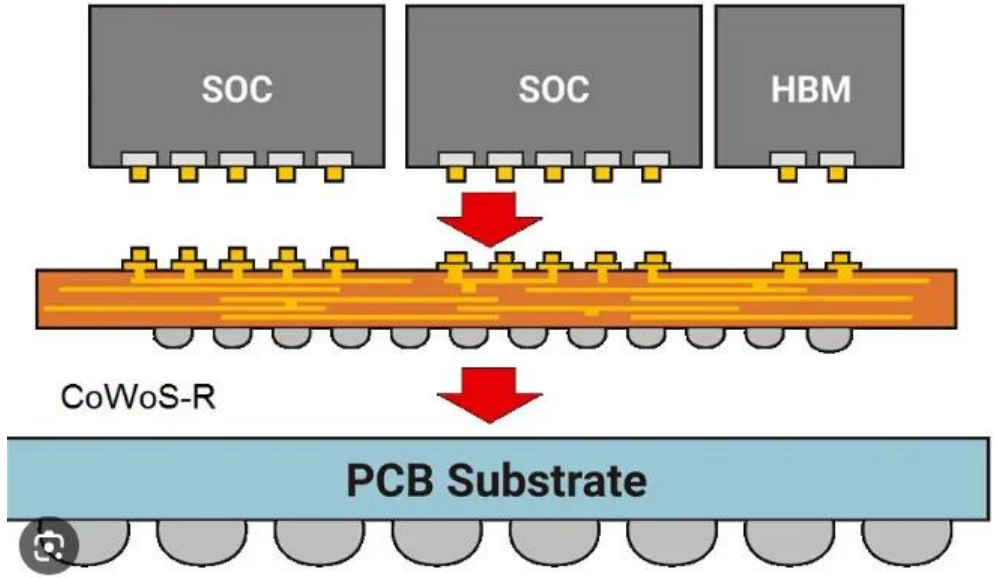
# Advanced Packages

3D Package

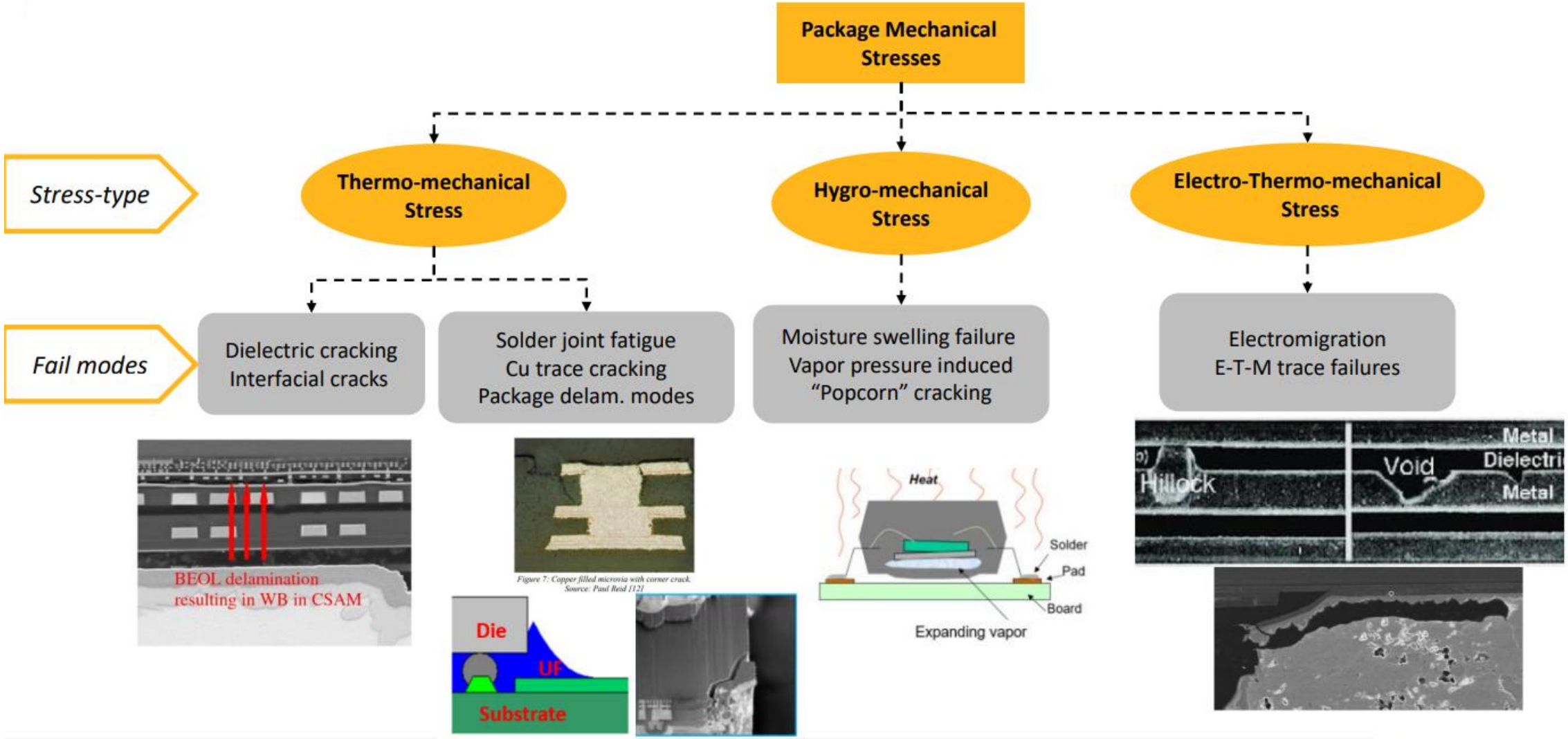





Enhance 2D Package
(2.5D CoWoS-R/S)



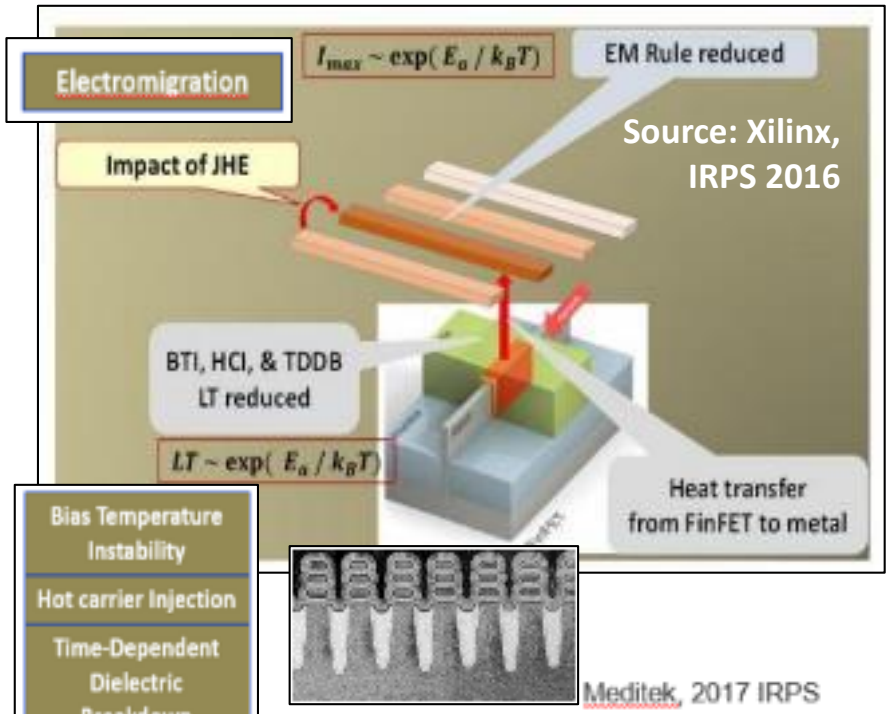
# Package Mechanical Stress and Failure Modes




Source: ANSYS

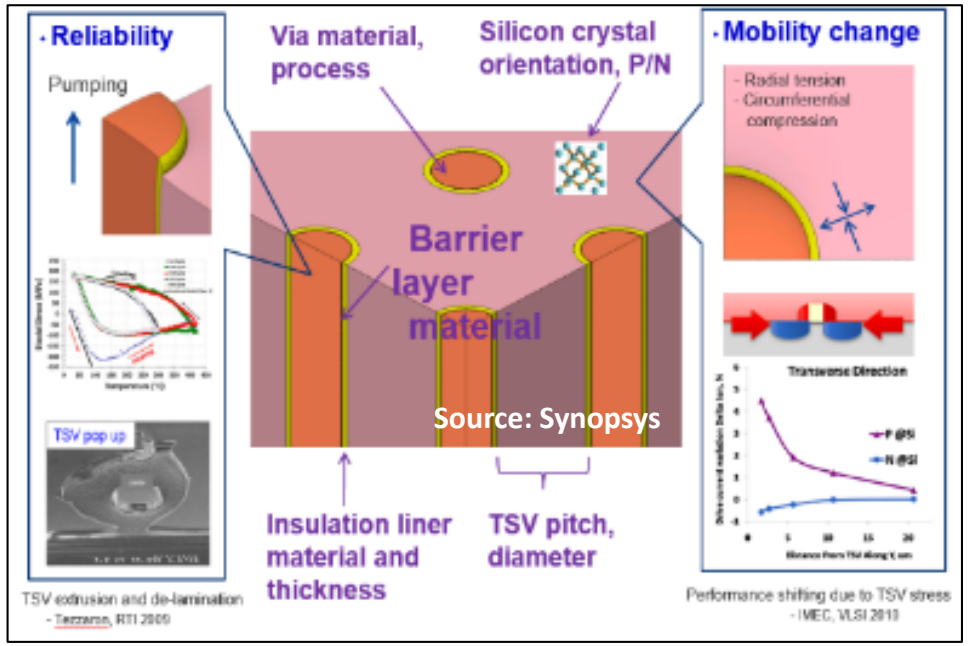
# CBPI-induced Stresses and degradation/failure modes

## SHE-induced FEOL failure modes



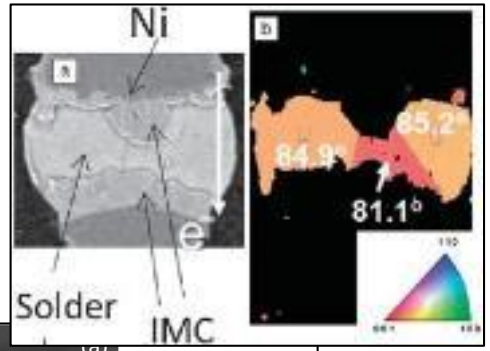

Meditek, 2017 IRPS

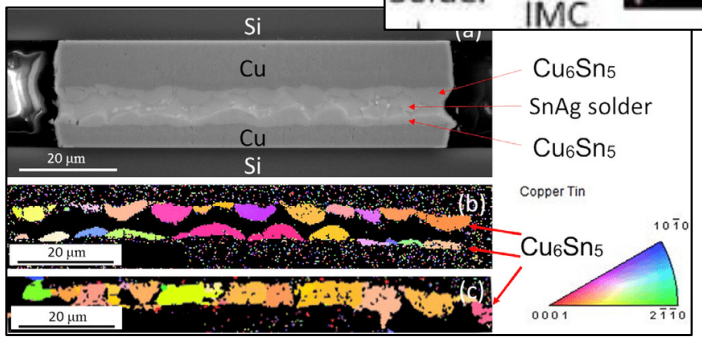
## CPI-induced MEOL/BEOL failure modes (interposers, bridges, RDLs)



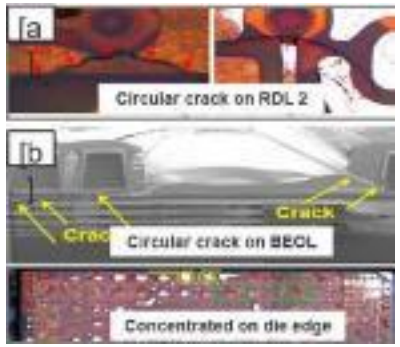

## Microbumps:

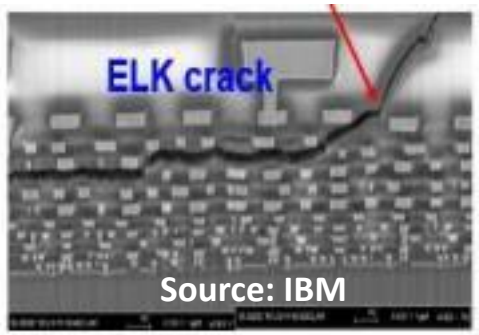
- Material anisotropy
- Length-scale effects




DOI:10.1016/j.scriptamat.2020.01.005
DOI.org/10.1557/mrs.2015.29

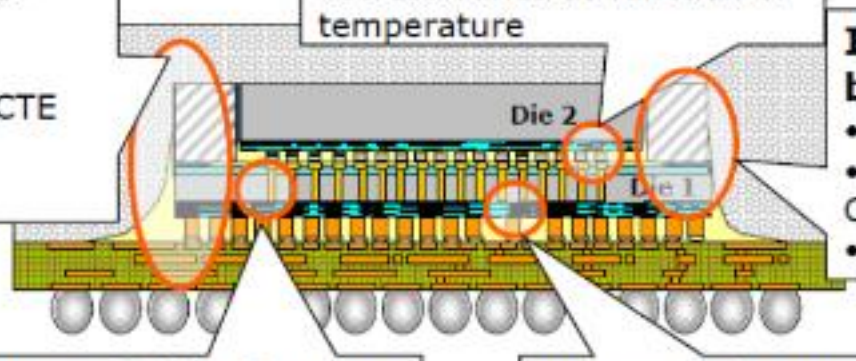


# HI Systems Reliability Failure Modes

**Impact of Flip Chip Package on 3D chip-stack (CPI)**
- Stress induced by Cu-pillars on low-K
- Stress induced by overmold, laminates CTE mismatch
- …

**Impact of TSV/uBump on top die**
- Built-in stress
- Stress varies as function of temperature



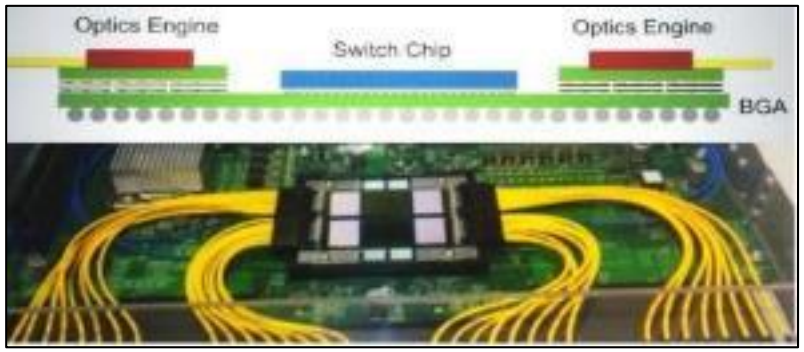

**Impact of 3D-SIC bonding on dies**
- Stress during bonding
- Stress due to underfill CTE mismatch
- …

**Impact of die thinning**
- Releases stress
- Strength of die
- …

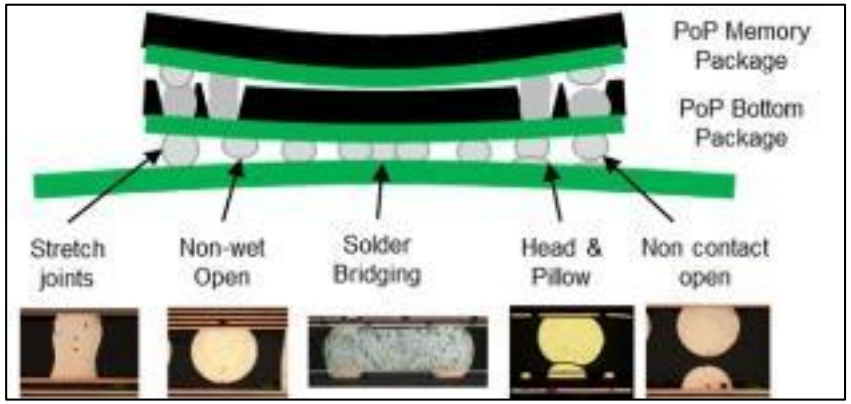
**Impact of TSV on bottom die**
- Built-in stress
- Stress varies as function of temperature
- …

**Stress/strain can lead to**
- mechanical failures due to delamination, peel, fatigue, …
- electrical Impact due to parameter shifts, increased variability, EM,…

**Multi-scale**



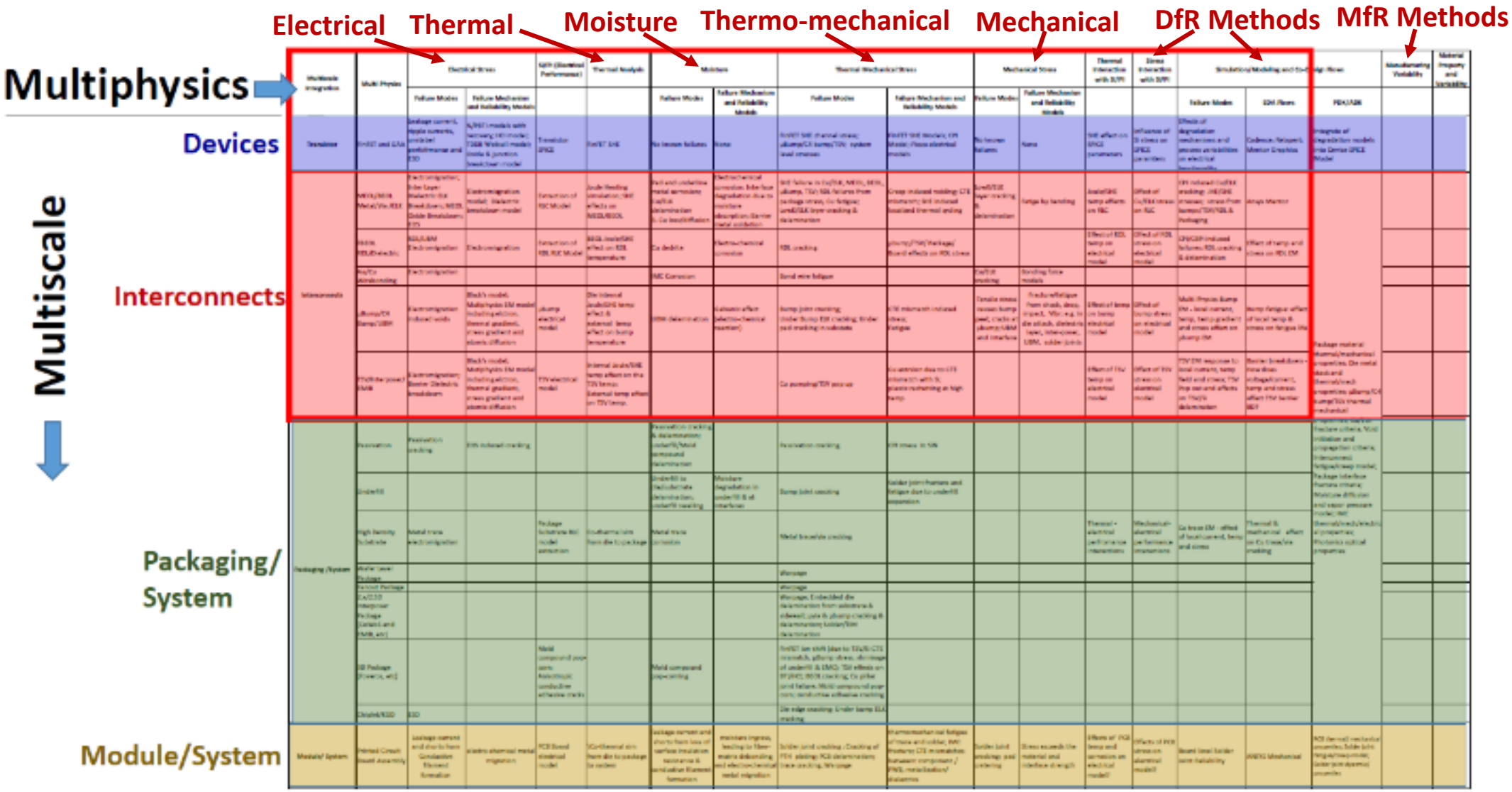

Photonic switching devices/SIP concepts




**Package on package warpage induced defects and failures**

**Source: IMEC**

# Modes/Mechanisms/Models for Degradation & Failure



# HI Failure Mechanisms and Modelling

| ELEMENT | Failure mechanisms | Test | Test regimes | Modeling approaches |
|---|---|---|---|---|
| Thin die | Warpage-induced stress effect on device performance, TSV/Si delamination and silicon cracking, misalignment, deterioration of of BEoL reliability (TDDB) by Cu diffusion from the back side | Ultrasonic microscopy; chain structures; ring oscillators (RO); test for leakage; capacitance measurements, capacitance-time method (C-t) | Temperature -accelerated (T-accelerated) (Constant T anneal for diffusion-driven failures and T-cycles for CTE-mismatch driven failures) | FEA/compact modeling |
| TSV | Si cracks, BEoL cracks/ delaminations, TSV-stress effects device performance, EM/SM | RO, Test for leakage, capacitance measurements, resistance | T&I (current) accelerated | FEA, compact modeling |
| Chip-to-chip (C2C) connection/underfill (UF) | Stress generated by chip stacking effects device performance, delamination / BEoL crakcs. | Ultrasonic microscopy, chain structures, RO, Test for leakage, capacitance | T-accelerated | FEA |
| | | measurements | | |
| Die backside redistribution layer (BRDL) | Stress-induced cracking/delamination, Cu contamination on the back surface of the thinned wafer/stress-enhanced Cu diffusion | Ultrasonic microscopy, chain structures, RO, Test for leakage, capacitance measurements, C-t | T-accelerated | FEA, CAD |
| Micro-bumps/UBM | Cracking, EM/SM, electrical resistance | Wheatstone bridge + XCT, resistance | T&I-accelerated | FEA/compact modeling |
| Large volume of Cu | Cu contamination on the backside surface of the thinned die/stress-enhanced diffusion | Bending Beam, C-t | Use conditions | FEA |
| Large thermal gradients | Chip performance, BEoL cracking | Ultra sound spectroscopy, chain structures, RO, Test for leakage, capacitance measurements | Use conditions | FEA/compact modeling |

# HI Failure Mechanisms and Modelling

| Failure Mechanisms | Driving forces | Outcome | Test | Test regimes | Modeling approaches |
|---|---|---|---|---|---|
| 1. TSV-induced stress effect on device performance | CTE mismatch | Device performance degradation | RO, device in the vicinity of TSV arrays | Use conditions | FEA, compact modeling |
| 2. TSV effect on BEoL | CTE mismatch | Interface delamination (adhesive failure), ILD cracking (cohesive failure) | chain structures (open/shorts detection) | T-accelerated | FEA |
| 3. Electromigration and stress migration | TSV voids | Resistance increase | Wheatstone Bridge + X-ray microscopy/ tomography, Kelvin/chain structures | T & I– Accelerated | FEA, compact modeling |
| 4. Barrier/oxide liner integrity | CTE mismatch; deposition, interface conditions | Signal propagation | Test for leakage | T-accelerated | FEA |
| 5. Stress-induced corrosion | "Out-of-spec" stress effecting migration/ reaction rates | Metal voiding, delamination | Combined corrosion + stress test | T-accelerated | |
| 6. Interfacial failures: Cu/barrier, barrier/oxide | CTE | BEoL metal/ULK and TSV metal/Si delamination/ cracking | Capacitance measurements; continuity structures (shorts & opens) | T-accelerated | |
| 7. TSV pop-out | CTE mismatch | TSV/Si interface delamination and cracking, TSV bottom voids | nano-XCT | T-accelerated | FEA |
| 8. Copper/TSV CMP process | Interaction with W contacts | Contacts failure | Resistance measurements | Use conditions | CMP models |
| 9. Cu contamination on the backside surface of the thinned die, stress-enhanced diffusion | Cu atoms originated from Cu TSV | Deterioration of device characteristics | C-t | Use conditions | |

# HI Failure Mechanisms and Modelling

| Failure Mechanisms | Driving forces | Outcome | Test | Test regimes | Modeling approaches |
|---|---|---|---|---|---|
| 1. Effect of bump proximity on transistor; role of underfill (UF) | CTE mismatch | Performance degradation | RO, device in the vicinity of TSV arrays | Use conditions | FEA, compact modeling |
| 2. IMC: formation of intermetallic phases | Metal-physical processes | Voiding, cracking, EM, power, electrical resistance | Energy-disperive X-ray (EDX) spectroscopy, Auger electron spectroscopy (AES); cross-sectional SEM; Bump shear test and tensile chip pull test; resistance measurements | Use conditions | |
| 3. W2W or C2C joining process | Warpage-induced stress; CTE mismatch, UF/bump-induced pressure | Device performance, IC delamination/cracking, misalignment | Ultra sound spectroscopy, chain structures, RO, Test for leakage, capacitance measurements | T-accelerated | FEA |
| 4. Under bump metallization (UBM) | Metal-physical processes, stress | Voiding, cracking, EM, electrical resistance | Ultrasonic microscopy, X-ray microscopy/ tomography, chain structures (open/shorts detection); Wheatstone Bridge + X-ray; resistance measurements | | |
| 5. Cu contamination on the backside surface of the thinned die/stress-enhanced diffusion | Cu atoms originated from micro-bumps | Deterioration of device characteristics | C-t | Use conditions | |
| 6. Electromigration and stress migration in on-chip interconnects and TSVs | TSV voids | Resistance increase | Wheatstone Bridge + X-ray microscopy/ tomography | T & I– Accelera-ted | FEA, compact modeling |

# HI Failure Mechanisms and Modelling

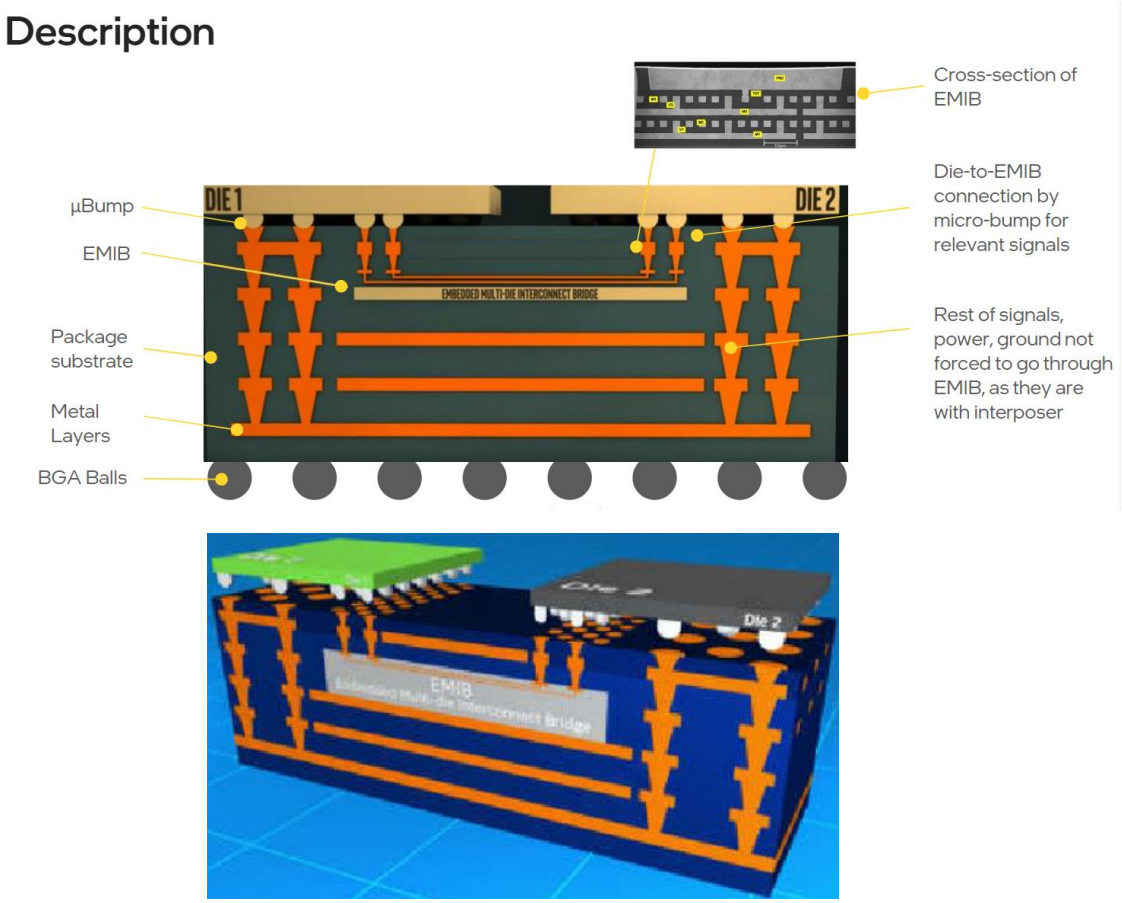
| Failure Mechanisms | Driving forces | Outcome | Test | Test regime | Modeling approaches |
|---|---|---|---|---|---|
| 1. Interfacial RDL/BCB-polymer delamination | CTE | Delamination | Capacitance measurements | T-accelerated | |
| 2. TSV effect on RDL | CTE mismatch | Interface delamination | Ultrasonic microscopy, chain structures (open/shorts detection) | Temperature T-accelerated | FEA |
| 3. Cu contamination on the backside surface of the thinned die/stress-enhanced diffusion | Cu atoms originated from Cu TSV | Deterioration of device characteristics | C-t | Use conditions | |

| Failure Mechanisms | Driving forces | Outcome | Test | Test regime | Modeling approaches |
|---|---|---|---|---|---|
| 1. W2W or C2C joining process | Warpage-induced stress; CTE mismatch, UF/bump-induced pressure | Device performance, BEoL cracking | Ultrasonic microscopy, chain structures, RO, Test for leakage, capacitance measurements | T-accelerated | FEA |
| 2. Cu contamination on the backside surface of the thinned wafer/stress-enhanced diffusion | Cu atoms originated from Cu TSV/micro-bumps; wafer or die thinning can remove intrinsic and extrinsic gettering regions (IG & EG) | Deterioration of device characteristics due to reduction of the minority carrier lifetime by impurity levels generated by Cu-atoms | C-t | Use conditions | |

# 3D Package Reliability Failure Modes and Mechanism

| AREA OF FAILURES | DESCRIPTION | EXPECTED RELIABILITY FAILURE MODE | FAILURE STIMULI for the FAILURE MECHANISM (description of the driving factor to the failure |
|---|---|---|---|
| **FEOL** | Change of electrical characteristics of all devices | Devices/system out of specs | Global mechanical stress -induced in silicon by 3D processing. This stress is mainly caused by CTE mismatch |
| **FEOL** | Change of local device electrical characteristics | Device/system out of specs | Local mechanical stress induced in silicon near 3D processing components (TSVs, micro-solder bumps, Cu pads and pillars). |
| **Interconnect** | Micro bump IMC growth | Increase in interconnect resistance over time | IMC growth over time (enhanced by temperature) |
| **Interconnect** | Micro bump delamination | Electrical open | IMC growth over time (enhanced by temperature) resulting in UBM consumption. |
| **Interconnect** | Micro bump crack in Cu-UBM/Sn based solders | Electrical open | Micro bumps fracture during mechanical impact due to a weak interface caused by Kirkendall void formation. |
| **Stacking** | Increased chip temperature. | Temperature accelerated failures | Increased thermal resistance due to a thick BEOL stack or due to many stacked chips with a thinner BEOL stack but many bonding interfaces |
| **Interconnect** | Solder bridging | Electrical short, or XCT or CSAM detection | Ultra-fine micro bump pitch and high density increases the risk of solder bridging during bonding. |
| | | | |
| **Interconnect** | Cu pumping | Damaged BEOL | Cu bulge-out due to thermo-mechanical stresses induced by TSV-anneal during BEOL processing |
| **Interconnect** | Liner integrity | High leakage/copper diffusion | Weak barrier coverage in TSV liners can cause Cu to become mobile in liners and adjacent Si |

# EMIB Failure Modes and Mechanism




| AREA | DESCRIPTION | EXPECTED RELIABILITY FAILURE MODE | FAILURE STIMULI |
|---|---|---|---|
| **EMIB** | Microbump crack | Electrical open during Temp. cycle | Microbumps fail due to difference in package and die and underfill CTE and residual process stressing |
| **EMIB** | Microbump crack | Electrical open during bake or preconditioning or early thermal cycling | Bump solder consumption resulting in brittle intermetallic that cracks with high normal and shear loading. – see Xylinx paper Ramalingham |
| **EMIB** | Underfill cracking at die corner and edges | Open circuit or delamination | High shear force at the corners and edges of the companion dice (distance to neutral point effect) resulting from package displacement relative to the dice during preconditioning and thermal cycling. |

# Fanout Package Failure Modes and Mechanism

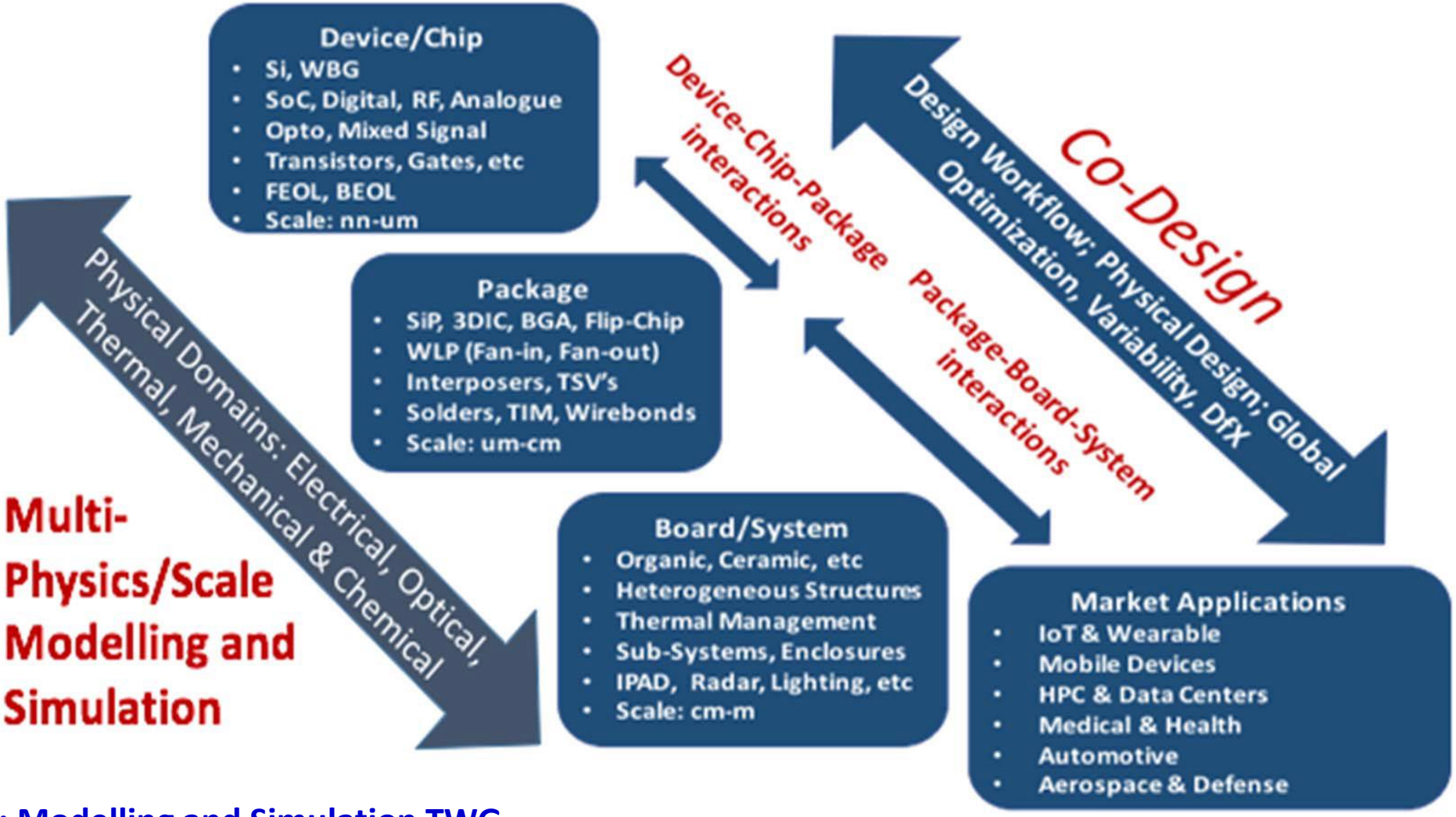
| AREA OF FAILURES | DESCRIPTION | EXPECTED RELIABILITY FAILURE MODE | FAILURE STIMULI for the FAILURE MECHANISM (description of the driving factor to the failure |
|---|---|---|---|
| **RDL** | RDL Cracking | Electrical open during Temp. cycling and drop tests on board | Large die induced high local stress due to CTE mismatch between die, RDL and board |
| **RDL** | RDL Delamination and Lifted | Electrical open during drop test on board | Localized high stress and poor adhesion between RDL and dielectric polymer |
| **RDL** | RDL and microvia Electromigration | Electrical open during high temperature and current | Localized current crowding and scaling of RDL and microvia size |
| **RDL** | RDL Crrosion | Electrical short during biased HAST test | Reduced RDL spacing and UF stress breaking UBM sealing |
| **Under Bump ILD** | ILD Damage under Cu pillars | Electrical open during flip chip and during Temp cycling test | RDL first process incuded planarization issue<br>Bonding force during TCNCP process |
| **Microbump** | Cracking | Electrical open during temp cycling | Global/local CTE mismatch induced stress in microbumps |
| **Microbump** | Voiding | Electrical open during elcromigration test | Temperature and high current density particarly the current crowding at RDL/Bump intersection |
| **Overall Package** | Warpage | Chip first RDL Lithograph<br>Board level SMT Issue | Large size panel<br>Material properties<br>Process flow and parameters<br>Die size and thickness |

# Reliability Bottom-Up Status

| Key Elements for DfR Flow | Wafer Level DfR | Package and System Level DfR | Chip to Package to Board Interactions |
|---|---|---|---|
| **Thermal Stress** | Localized Self Heating and hot spots | Global Level thermal managements | FEOL/BEOL and systeme level thermal interactions |
| **Failure Modes** | TDDB, HCI, BTI , EM and SM, etc | Warpage, delamination; C4, ubump, DBI, TSV, Optical Via interconnect fatigue and migration failure, etc | Global and local Stress effects on Cu/ELK failure, stress effects on FET's mobility |
| **Failure Mechanism and Reliability Model** | Weibull, Lognormal, Power Law Model, Aging Model, etc | Weibull, Lognormal, multiphysics models, etc; many are under development | Under development |
| **Material Chaterization and Modeling** | Modeling device thermal characteristics (Thermal resistance)<br>Modeling device aging<br>Modeling the impact of stress on device threshold, delay, etc. | To make materials data useable by EDA tools – and enable them to produce accurate and meaningful results – materials data needs to be presented in a machine-readable format and agreed upon with EDA tool vendor. | Modeling multi scale and multi physics failures |
| **Process Design Kit** | Foundry Design Kit | Assembly Process Design Kit | Under development |
| **EDA Flow** | Cadence Spectre/HSPICE, etc | Ansys/Mentor, etc | Mentor/Synopsys |
| **Circuit/System Reliability** | HCI/BTI and EM Available; TDDB and SM not Available | Under development | Under development |

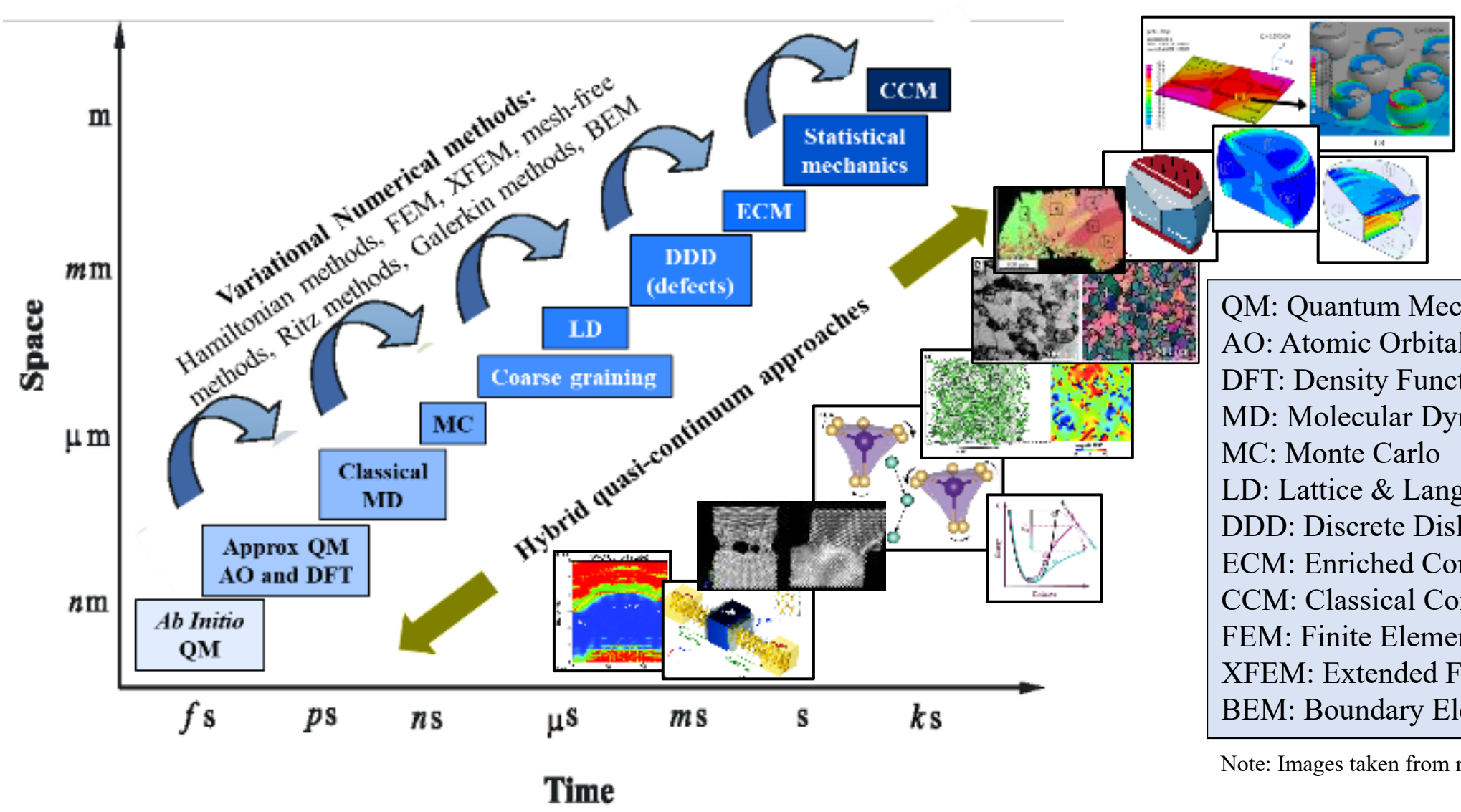
| |
|---|
| Established |
| Partially Established |
| Under development or Not Available |

# Physics-based Modeling Simulation and Co-design




Source: HIR; Modelling and Simulation TWG

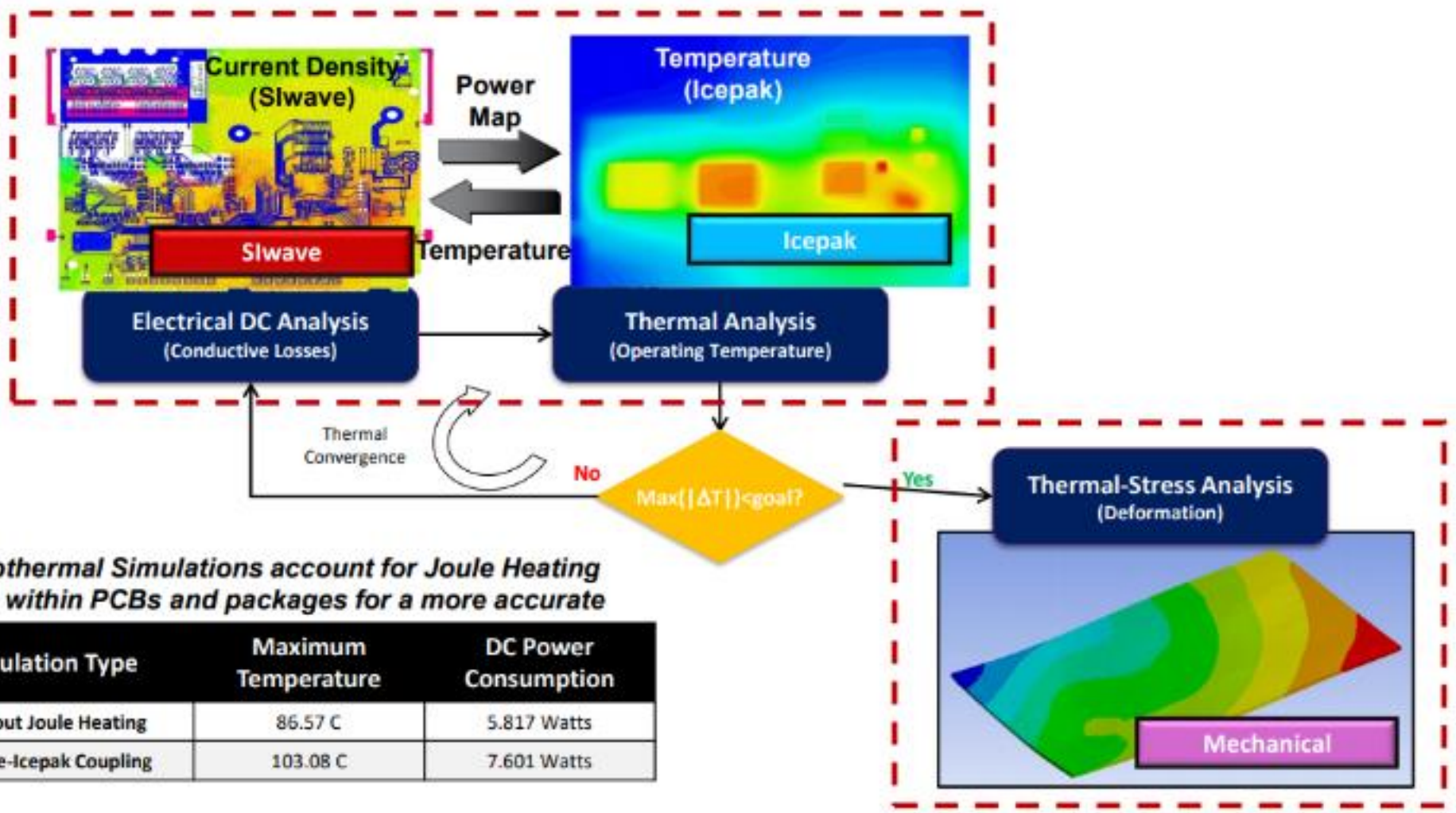
# Multi-scale Modeling and Simulation




QM: Quantum Mechanics
AO: Atomic Orbital
DFT: Density Functional Theory
MD: Molecular Dynamics
MC: Monte Carlo
LD: Lattice & Langevin Dynamics
DDD: Discrete Dislocation Dynamics
ECM: Enriched Continuum Mechanics
CCM: Classical Continuum Mechanics
FEM: Finite Element Method
XFEM: Extended Finite Element Method
BEM: Boundary Element Method

Note: Images taken from multiple public-domain sources

# System-level Multiphysics Simulations




***Electrothermal Simulations account for Joule Heating losses within PCBs and packages for a more accurate***

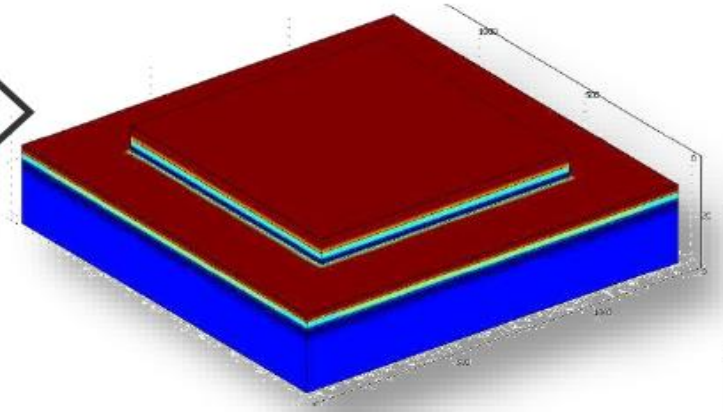
| Simulation Type | Maximum Temperature | DC Power Consumption |
|---|---|---|
| Without Joule Heating | 86.57 C | 5.817 Watts |
| SIwave-Icepak Coupling | 103.08 C | 7.601 Watts |

**Source: ANSYS**

# Multi-Scale and Multi-Physics CPI Flow

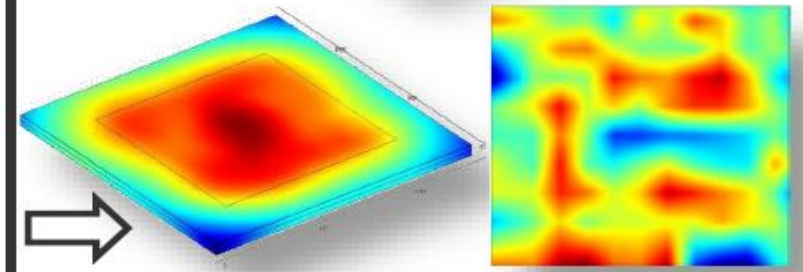
**Package-scale simulation (FEA)**
**Input**: geometry; material properties; smeared mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

**Output**: field of displacement components on the die faces.



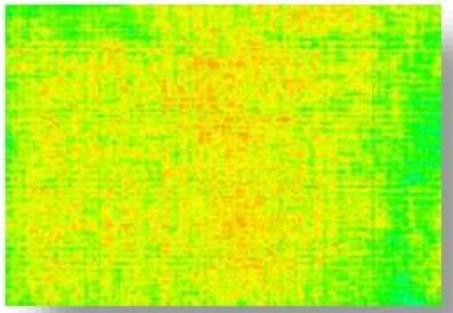
**Die-scale simulation (FEA)**
**Input**: geometry; field of displacements on the die faces; coordinate-dependent mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

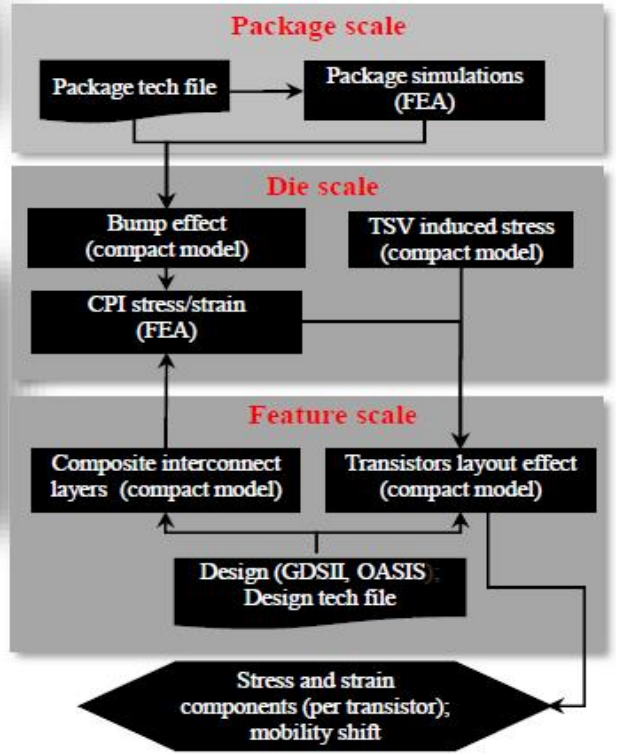
**Output**: Distribution of the strain components across device layer.



**Layout-scale w/feature-scale resolution (compact model):**
**Input**: GDS; distribution of the strain components across device layer.

**Output**: Transistor-to-transistor variation in stress components



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# Canonical Thermal Heterogeneous Integration Problems

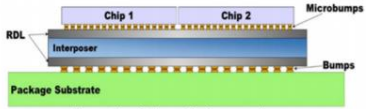


Figure 3a: Schematic for case 1.

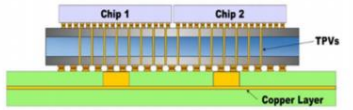


Figure 3b: Schematic for case 2.

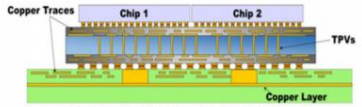


Figure 3c: Schematic for case 3.

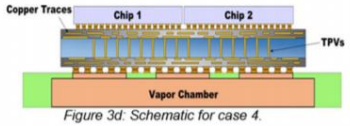
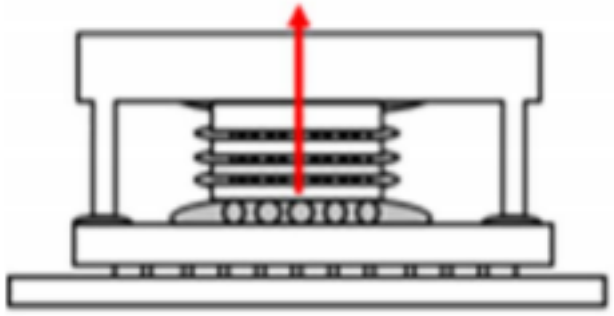
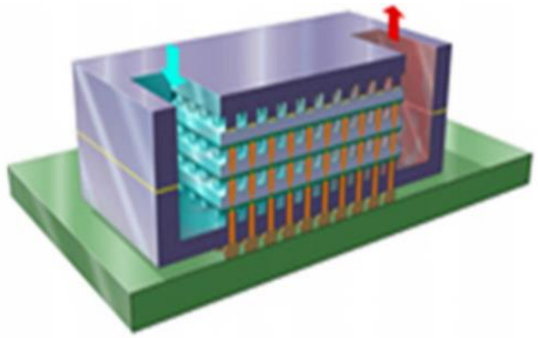


Figure 3d: Schematic for case 4.

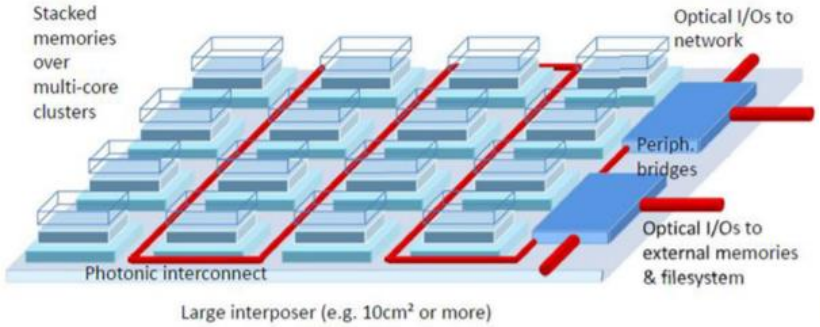
1. 2D chip with stacked memory on a silicon/glass interposer



2. 3D stacked die with conduction interfaces



3. 3D stacked die with embedded liquid cooling




4. Optics/photonics based Heterogeneous package

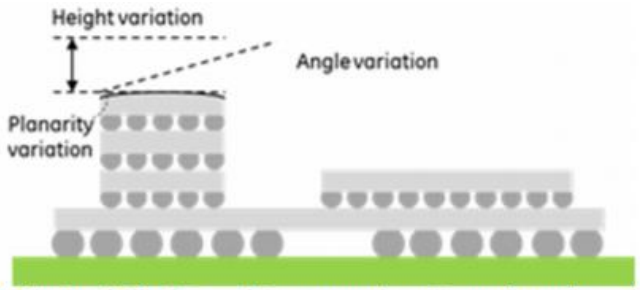


*Figure 11: Notional 3D chip architecture and anticipated topology challenges*

5. Harsh environment (military, aerospace, automobile)

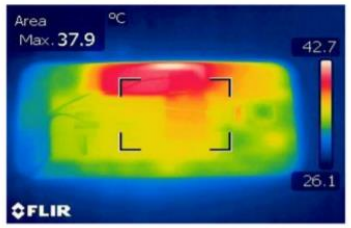


*Figure 14: Temperature contour data for the external surface of a SmartPhone [10]*

6. Mobile application chipset (package on package, fan out, bridge)

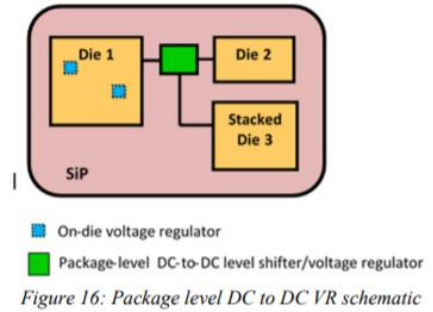


*Figure 16: Package level DC to DC VR schematic*

7. Voltage Regulators in a Heterogenous Package

# Advanced Thermal Technologies & Research

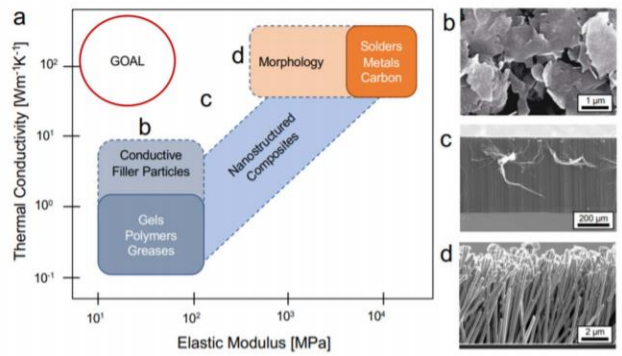
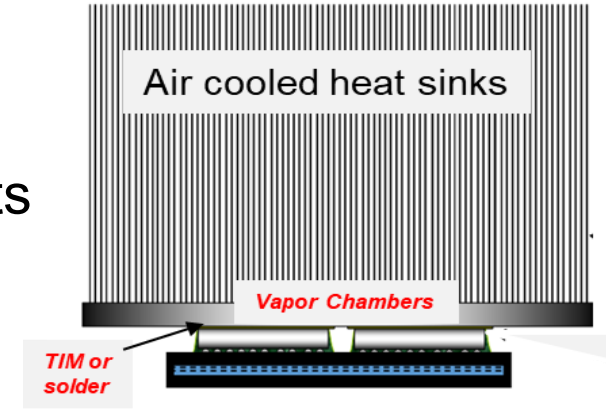
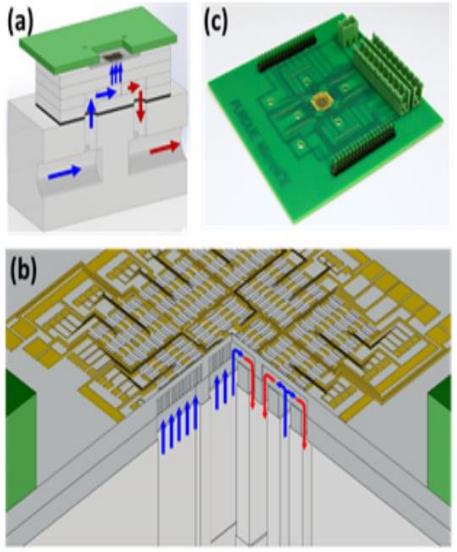



*Figure 17 (a) Two common strategies can be employed to create high-performance TIM composites [14], (b) an example of graphene-polymer composite [15], (c) vertically grown nanotubes [16-17], (d) vertically electrodeposited nanowires [14, 18]*

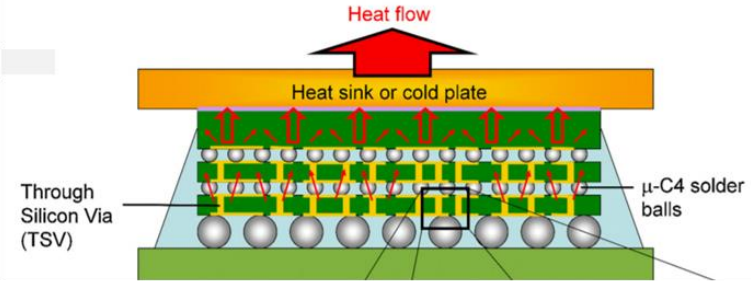
[A] Thermal Interface Materials

[B] System thermal limits for HPC multi-chip modules




[C] Embedded liquid cooling of chip and chip stacks




A 3D chip stack using advanced materials in the conduction heat flow path.

[D] Advanced Thermal Materials for Thermal Management

[E] Thermomechanical Modeling for Heterogeneous Integration

**Design Space Definition**
- Geometrical description
- Material property distributions
- Interface/Boundary conditions across domains

→ Finite element simulation setup and data generation (Electrical, thermal and mechanical models)

→ Field output preparation → Training and Test Split

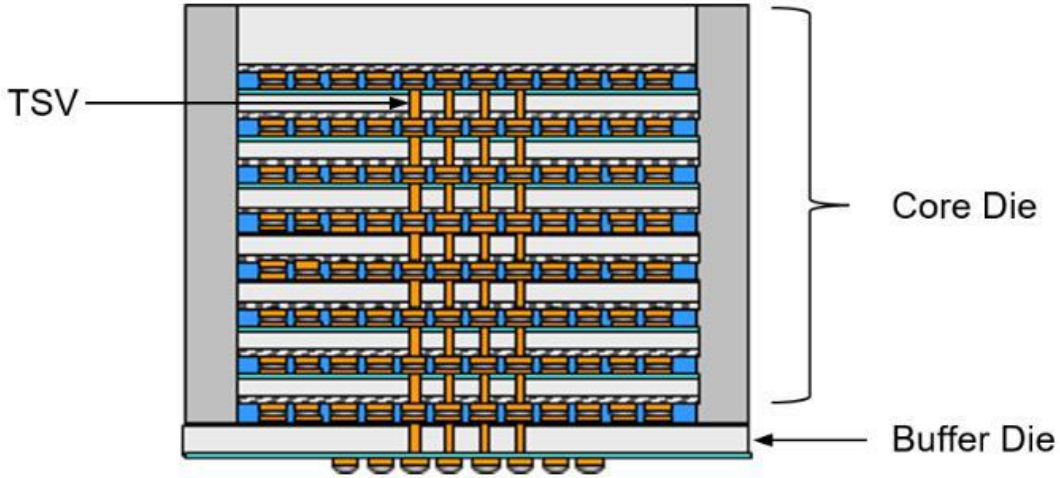
→ DAE training using an ML library

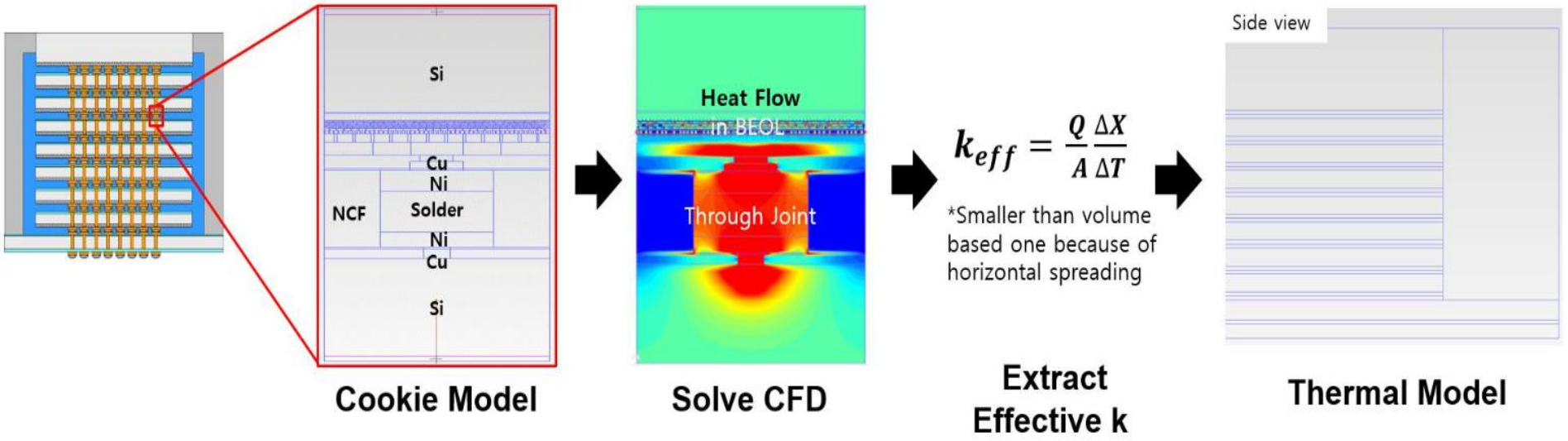
→ Validation and Deployment into design/reliability simulation tools

# *Thermal modeling on the High Bandwidth Memory (HBM)*

HBMs have thermal challenges due to the large stack thermal resistance and thermal coupling from adjacent higher power logic dies.

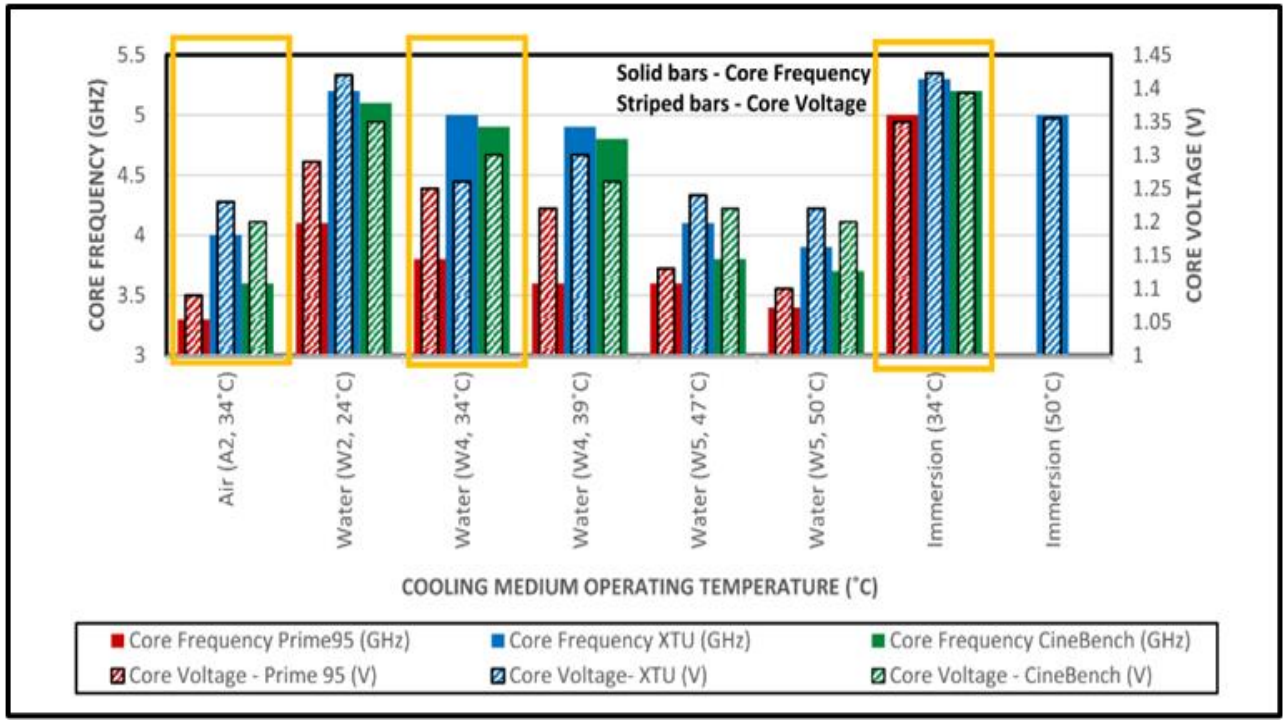
HBM is also not easy to simulate and provide accurate temperature predictions due to its complicated stacking structure.

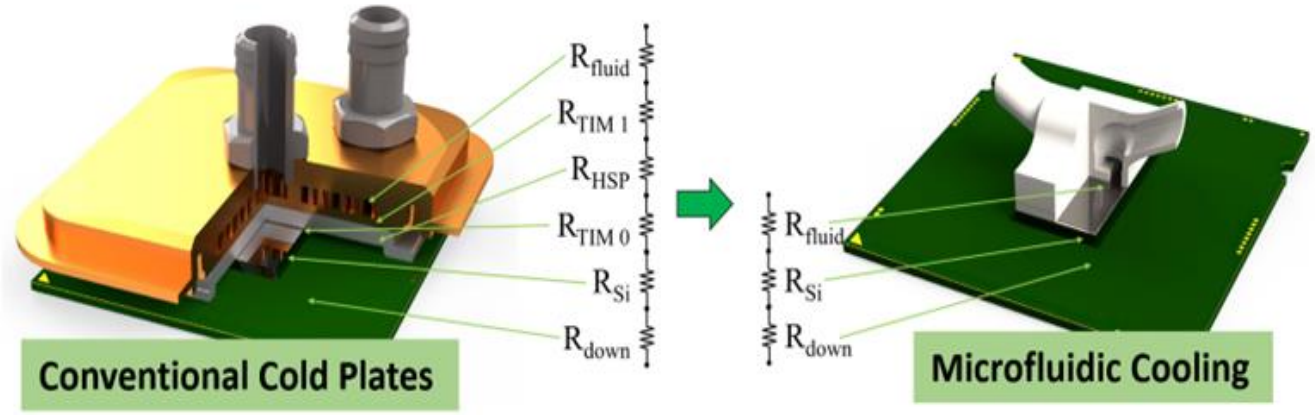


# *Advanced Liquid Cooling for next Generation data center integrated circuits*

When it comes to cooling high density electronic devices including CPUs, GPUs, and FPGAs employed in a data center (DC) server HW infrastructure, two phase (2P) immersion cooling using boiler plates (aka evaporators) and direct contact liquid Cooling using cold plates (aka water cooled microchannel heat sinks) outperform traditional air-cooling techniques.




Demonstrated up to *44.4% reduction in junction-to-inlet thermal resistance* while using only *0.3× of volumetric coolant flow per Watt* of power dissipated in the CPU compared to a conventional cold-plate.

# Reliability Challenges: Future Outlook

| | | Reliability Targets | Life Cycle Conditions | Design for Reliability | Manufacturing for Reliability | Qualification for Reliability | Sustainment for Reliability | Supply Chain |
|---|---|---|---|---|---|---|---|---|
| Applications | Mobile | | | | | | | |
| | IoT | | | | | | | |
| | Medical, Health and wearables | | | | | | | |
| | Automotive | | | | | | | |
| | HPC & Data Centers | | | | | | | |
| | Aerospace and Defense | | | | | | | |
| Package Integration | WLP (FO/FI) | | | | | | | |
| | 2.5D and 3D integration | | | | | | | |
| | Wafer Singulation and Thinning | | | | | | | |
| | Chip-package interactions (CPI) | | | | | | | |
| | Interconnects (TSV8s, µbumps, wirebonds, Flip Chip solder joints) | | | | | | | |
| | Substrates/Interposers | | | | | | | |
| | Board Assembly | | | | | | | |
| | SOC/SIP/SOP[9] formats | | | | | | | |
| Technologies | Microelectronics > 10 nm | | | | | | | |
| | Microelectronics <10 nm | | | | | | | |
| | Photonics & optics | | | | | | | |
| | MEMS and sensors | | | | | | | |
| | Power electronics | | | | | | | |
| | Energy souces (Batteries/PV[6]/FC[7]) | | | | | | | |
| | RF/Analog Devices | | | | | | | |

**1-5 Years**:

Multi-physics fusion approaches for reliability assurance

- Bottom-up *Reliability Physics* based approaches, tools, infrastructure
- Top-down *Machine Learning & AI* based approaches, tools, infrastructure

**5-10 Years**:

Fusion approaches for co-design (based on 'digital twins') and life-cycle PHM of next-gen robust HI systems

- Fault-tolerant systems
- Resilient systems

**10-15 Years**:

Fusion approaches for intelligent, adaptive, reconfigurable products with integrated autonomous life-cycle management capability

- Intelligent, self-cognizant systems
- Self-healing systems