Jet Propulsion Laboratory
California Institute of Technology

Highly Accelerated “Life” Test (HALT) Testing for Use of of COTS Parts on NASA Missions

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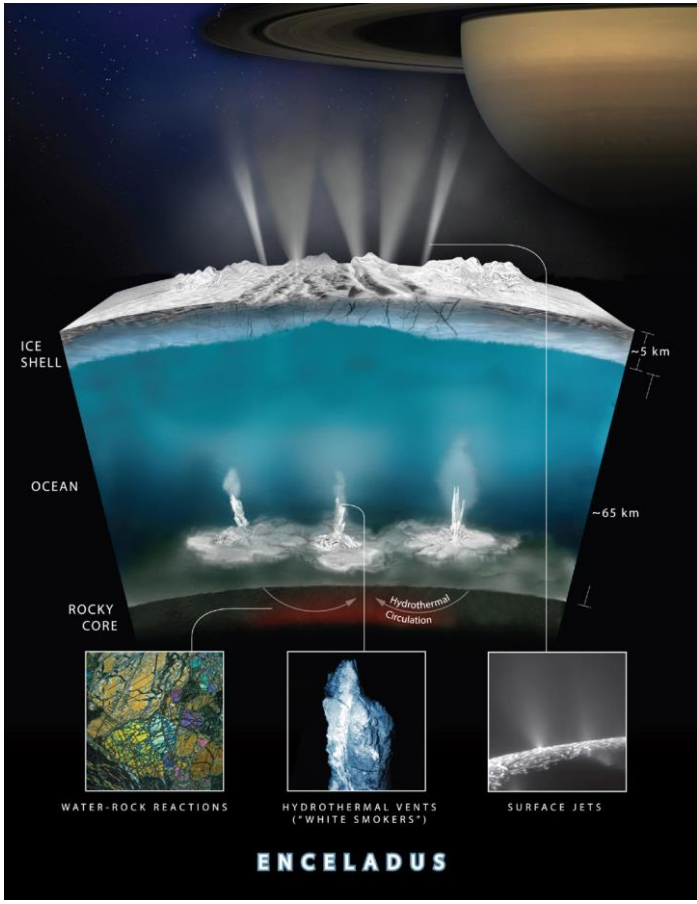


Saturn’s Icy Moon
Courtesy: NASA

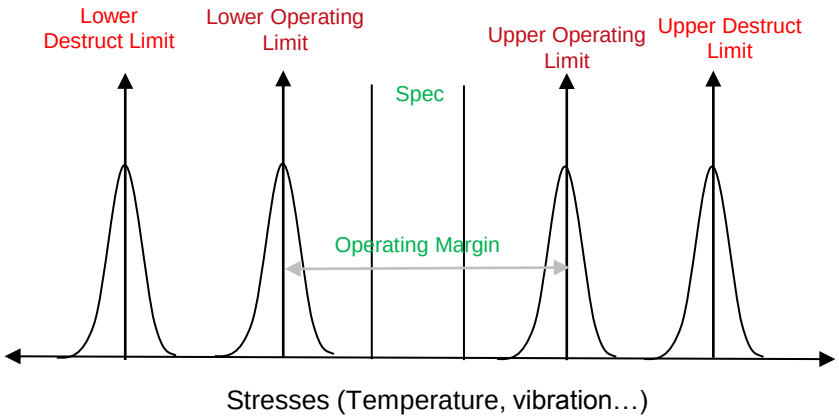
This effort is being sponsored by
NASA Electronic Parts and Packaging Program (NEPP)
under guidance of Ken LaBel and Michael Sampson, NASA/GSFC

HALT Background

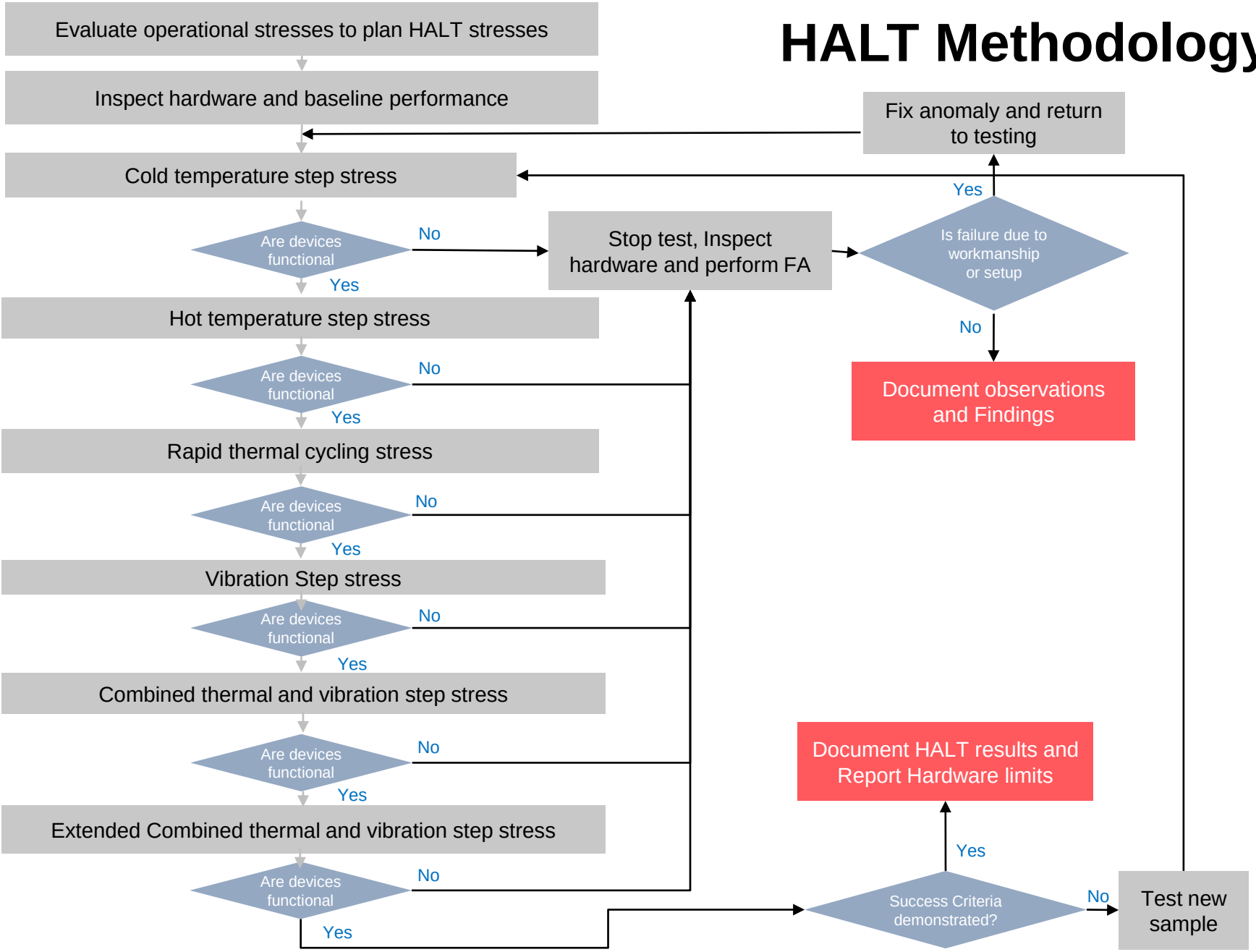
- HALT is a method to identify **latent defects in product design**, workmanship and manufacturing quality early in product development cycle
  - Identify failure modes related to stresses such as thermal, vibration etc…

- Provides opportunity to **screen hardware and improve on its design** and robustness, identify operational and destruct limits.

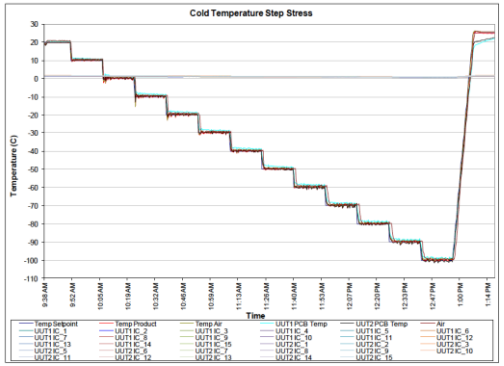
- Provide **faster technology infusion** while minimizing expensive qualification test cost and reduce design cost and time



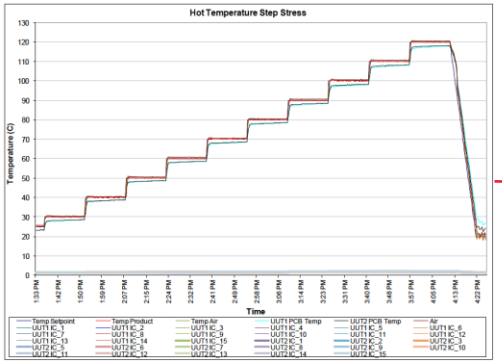
HALT Methodology



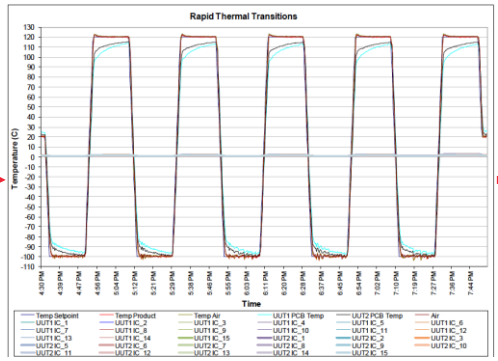
HALT Test Ranges



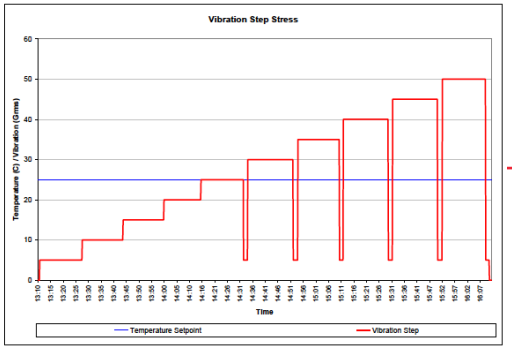
Cold Step Stress



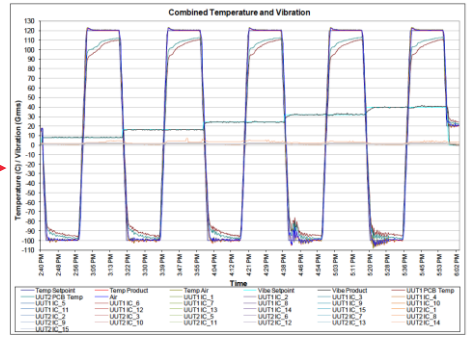
Hot Step Stress



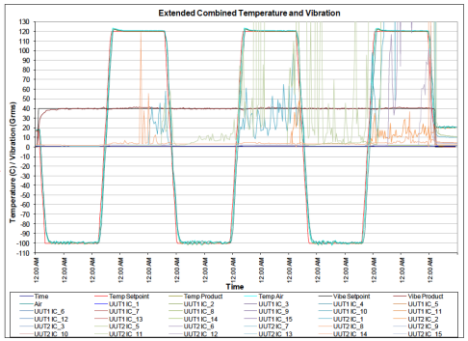
Rapid Thermal cycle stress



Vibration



Combined Thermal Vibration

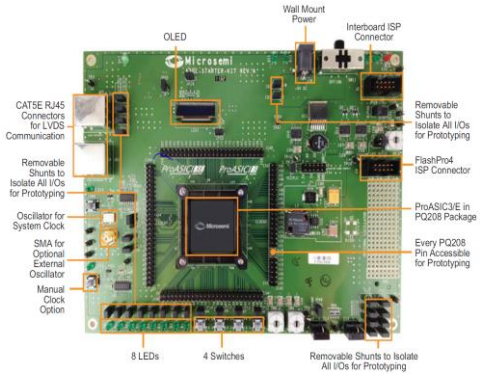


Extended Combined Thermal Vibration

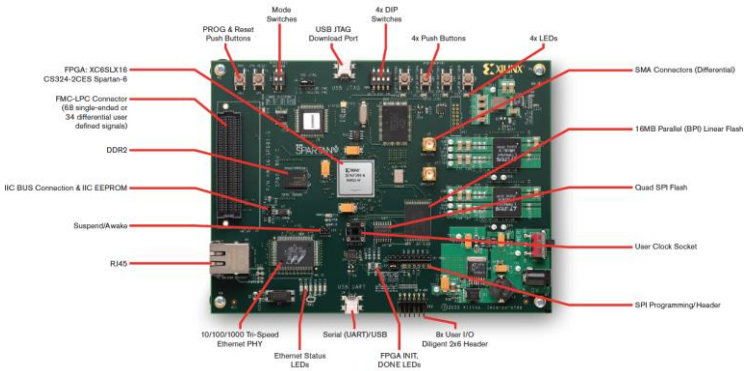
COTS Hardware Tested

COTS Boards - Monitored with Built-In test routine after every stress test

Xilinx Virtex-5 FPGA Board
Case study 1 (1 board tested)

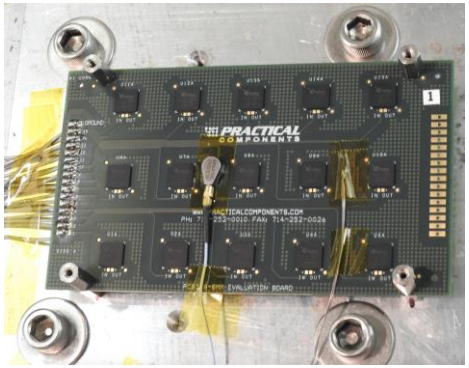


Microsemi ProASIC3/Eval board
Case study 2 (1 board tested)



Xilinx – Spartan 6 FPGA SP601 Board
Case study 3 (2 board tested)

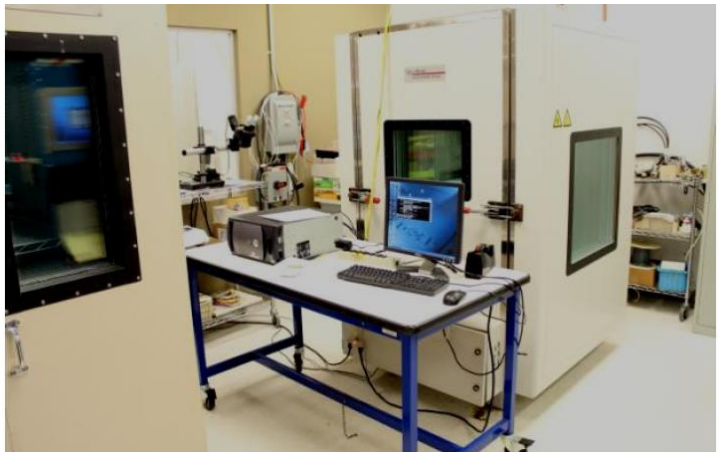
Daisy chain boards – Monitored continuously in situ - resistance continuity check.



15 BGA components Daisy chain boards PCB368 – 0.3 mm Board, ENIG Finish, Pb-free - SAC105 Solder – Case study 4 (4 boards tested- Total 60 BGAs)

Test Setup

Setup at External Lab



HALT Chamber

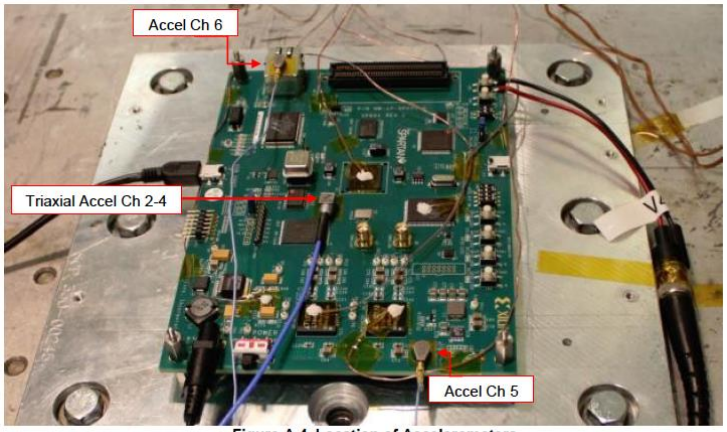
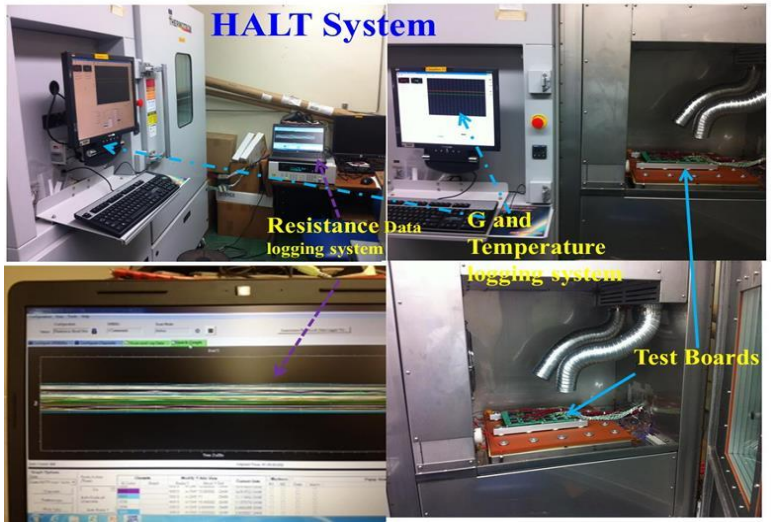


Figure A.4. Location of Accelerometers

Vibration Test Setup with Accelerometers

HALT Setup at JPL

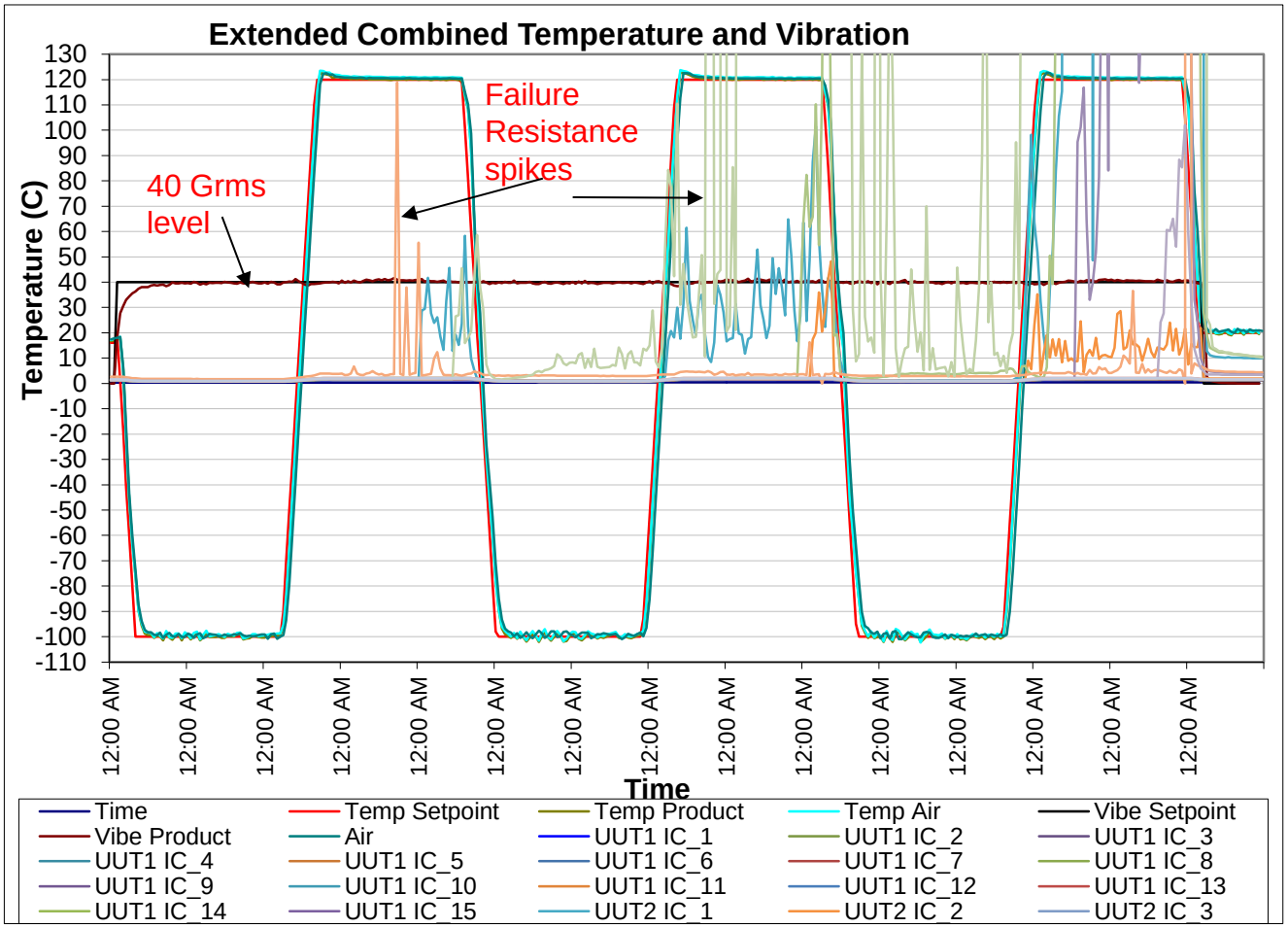
COTS FPGA Board at -65C – Setup at JPL

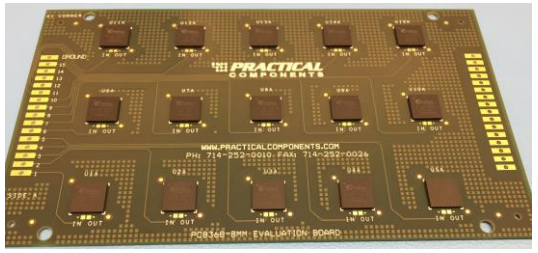


Case Study (#)	Step stress (Cold)	Extended Cold	Step stress (Hot)		Extended Hot	Rapid thermal transition	Extended Rapid Thermal transitions	Vibration Step Stress	Combined Vibration & Thermal
Xilinx ML507 (1)	-30C	-55C, -65C	25C, 50C	75C, 100C	125C	-65C to125C 12-TCT			
Virtex 5	PASS	PASS	PASS	PASS	FAIL	PASS			
USB	PASS	PASS	PASS	PASS	FAIL	FAIL			
DDR RAM	PASS	PASS	PASS	PASS	FAIL	PASS			
SRAM	PASS	PASS	PASS	PASS	FAIL	PASS			
LED	PASS	PASS	PASS	PASS	FAIL	PASS			
DIP Switch	PASS	PASS	PASS	PASS	FAIL	PASS			
LCD	FAIL	FAIL	PASS	FAIL	FAIL	FAIL			
VGA output	PASS	PASS	PASS	PASS	FAIL	PASS			
Peizo transducer	PASS	PASS	PASS	PASS	FAIL	PASS			
Microsemi PROASIC3 (2)	-30C	-55C, -65C	25C	75C, 100C	125C	-65C to125C 12-TCT			
Flashing LEDs	PASS	PASS	PASS	PASS	PASS	PASS			
8-BIT counter	PASS	PASS	PASS	PASS	PASS	PASS			
Xilinx SP601 EVAL (3)	-40C	-100C	25C, 50C	75C, 100C	120C	-40C to 80C			
UART Transmitter	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL
LEDs	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL
Test Timer	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL
Flash Memory	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL
EEPROM	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL
GPIO	PASS	PASS	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL
Memory module	PASS	PASS	PASS	PASS	FAIL	PASS	FAIL	PASS	FAIL
Daisy chain boards PCB368 – 0.3 mm Board (4)	-40C	-100C	25C	80C PASS	120C	-40C to 80C	-100C to 80C	35 Grms	-100C to 80C, 40 Grms
BGA – 368 balls 0.3mm pitch SAC105 balls (Pb-free)	PASS	PASS	PASS	PASS	PASS	PASS	PASS	1/30 FAIL	6/30 FAIL

- COTS boards show range of performance
- Thermal testing highlighted issues on Xilinx boards, while Microsemi boards successfully passed the experiment.
- Combined vibration and thermal stressing is useful in finding marginalities.
- NASA/JPL is investigating std method for HALT

Anomaly Detection – Resistance Spikes

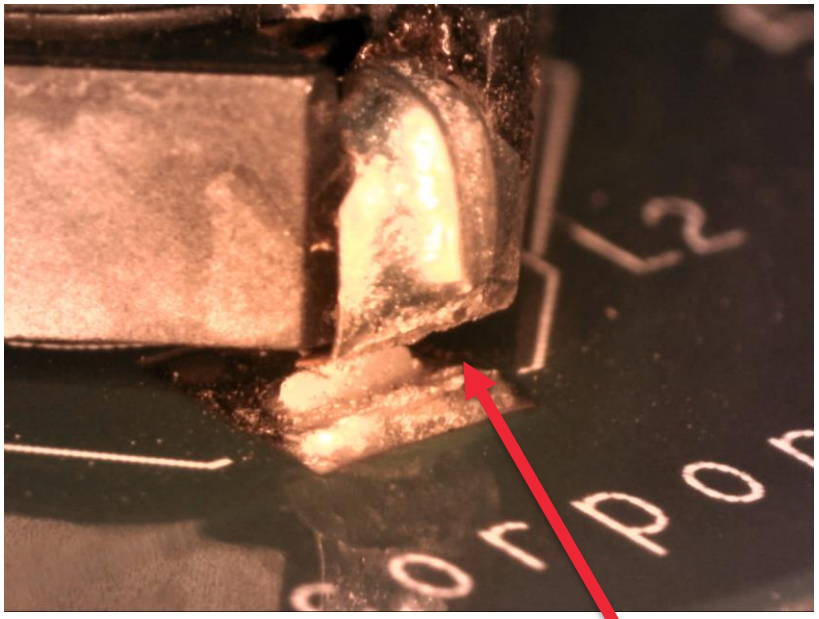


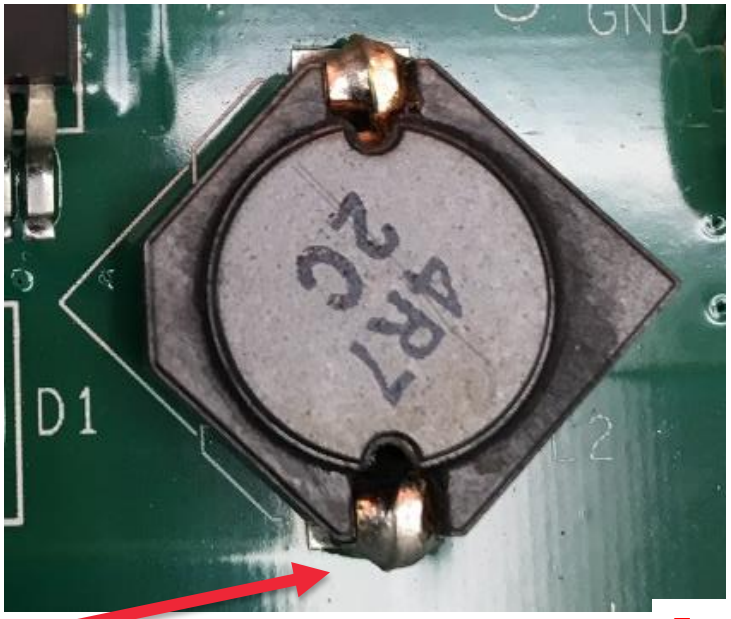


Daisy chain board with 15 BGA was tested with in-situ resistance monitoring during HALT

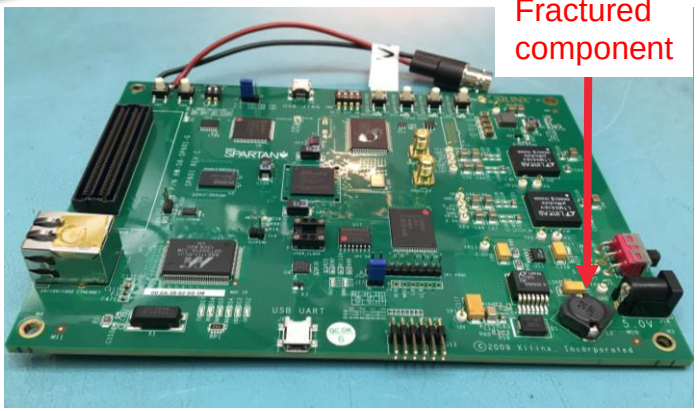
Typical Failure Signature
Resistance increase

Board Inspection – Xilinx Spartan 6 board





Fractured and lifted lead



Xilinx – Spartan 6 FPGA SP601 inspected after HALT testing

- Component shows fractured joint
- Several workmanship defects were observed such as insufficient solder, lack of pretinning etc.

Summary

- NASA/JPL is investigating standard HALT conditions as a means for establishing a benchmark for COTS PCB quality for small sat and other higher risk profile missions.

- NASA/JPL HALT investigations have shown that COTS PCBs have a range of performance.

- HALT methodology demonstrated as a potential screen for COTS boards

- HALT was successful in identifying several workmanship concerns with COTS
  - Insufficient component staking – Component showed fractured joint
  - Insufficient solder coverage for plated thru-hole and leaded packages
  - Lack of pre-tinning and gold removal resulting in poor wetting and solder coverage
- Further development required to build a knowledgebase on HALT application for screening parts to mission requirements.

Acknowledgement

- NASA Electronic Parts and Packaging Program (NEPP) under guidance of Ken LaBel and Michael Sampson, NASA/GSFC

- Douglas Sheldon, Program Technologist
  - Office of Safety and Mission Success, JPL

- Ramesham Rajeshuni
  - Environmental Technologist, JPL

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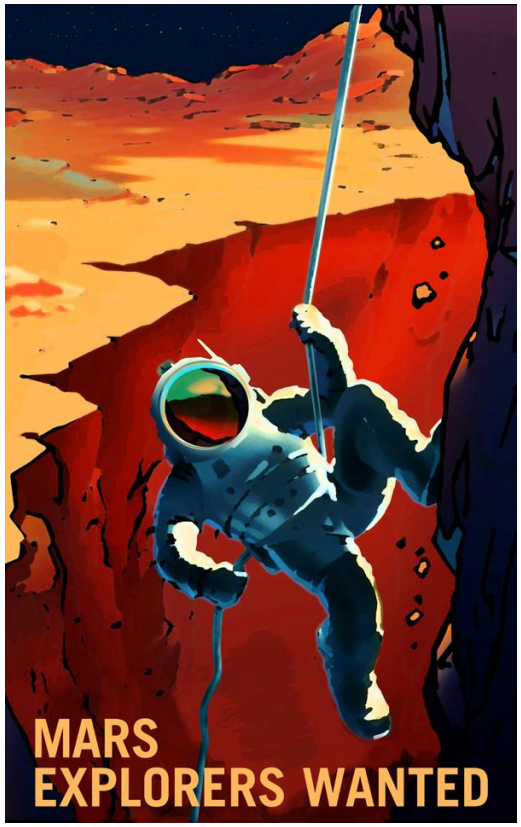

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