Highly Accelerated “Life” Test (HALT) Testing for Use of COTS Parts on NASA Missions

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HALT Background

• HALT is a method to identify **latent defects in product design**, workmanship and manufacturing quality early in product development cycle
  • Identify failure modes related to stresses such as thermal, vibration etc…

• Provides opportunity to **screen hardware and improve on its design** and robustness, identify operational and destruct limits.

• Provide **faster technology infusion** while minimizing expensive qualification test cost and reduce design cost and time
HALT Methodology

Evaluate operational stresses to plan HALT stresses

Cold temperature step stress

Are devices functional

Yes

Stop test, Inspect hardware and perform FA

Fix anomaly and return to testing

Yes

Is failure due to workmanship or setup

No

Document observations and Findings

Fix anomaly and return to testing

Documnet HALT results and Report Hardware limits

Success Criteria demonstrated?

Yes

Test new sample

No
HALT Test Ranges

Cold Step Stress

Hot Step Stress

Rapid Thermal cycle stress

Vibration

Combined Thermal Vibration

Extended Combined Thermal Vibration
COTS Boards - Monitored with Built-In test routine after every stress test

Xilinx Virtex-5 FPGA Board
Case study 1 (1 board tested)

Microsemi ProASIC3/Eval board
Case study 2 (1 board tested)

Xilinx – Spartan 6 FPGA SP601 Board
Case study 3 (2 board tested)

Daisy chain boards – Monitored continuously in situ - resistance continuity check.

15 BGA components Daisy chain boards PCB368 – 0.3 mm Board, ENIG Finish, Pb-free - SAC105 Solder – Case study 4 (4 boards tested- Total 60 BGAs)
Test Setup

Setup at External Lab

HALT Chamber

Vibration Test Setup with Accelerometers

HALT Setup at JPL

COTS FPGA Board at -65C – Setup at JPL

HALT System

Resistance Data
Logging System

G and Temperature
Logging System

Test Boards
<table>
<thead>
<tr>
<th>Case Study (#)</th>
<th>Step stress (Cold)</th>
<th>Extended Cold</th>
<th>Step stress (Hot)</th>
<th>Extended Hot</th>
<th>Rapid thermal transition</th>
<th>Extended Rapid Thermal transitions</th>
<th>Vibration Step Stress</th>
<th>Combined Vibration &amp; Thermal</th>
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<tbody>
<tr>
<td><strong>Xilinx ML507 (1)</strong></td>
<td>-30C</td>
<td>-55C, -65C</td>
<td>25C, 50C</td>
<td>75C, 100C</td>
<td>125C</td>
<td>-65C to 125C 12-TCT</td>
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<td>Virtex 5</td>
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<td>75C, 100C</td>
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<td><strong>Xilinx SP601 EVAL (3)</strong></td>
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<td>25C, 50C</td>
<td>75C, 100C</td>
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<td>-40C to 80C</td>
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<td><strong>Daisy chain boards PCB368 – 0.3 mm Board (4)</strong></td>
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<td>-100C</td>
<td>25C</td>
<td>80C PASS</td>
<td>120C</td>
<td>-40C to 80C</td>
<td>-100C to 80C</td>
<td>35 Grms</td>
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<tr>
<td><strong>BGA – 368 balls 0.3mm pitch SAC105 balls (Pb-free)</strong></td>
<td>PASS</td>
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<td>1/30 FAIL</td>
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</table>

- COTS boards show range of performance
- Thermal testing highlighted issues on Xilinx boards, while Microsemi boards successfully passed the experiment.
- Combined vibration and thermal stressing is useful in finding marginalities.
- NASA/JPL is investigating std method for HALT.
Anomaly Detection – Resistance Spikes

Daisy chain board with 15 BGA was tested with in-situ resistance monitoring during HALT

Typical Failure Signature
Resistance increase
Board Inspection – Xilinx Spartan 6 board

Xilinx – Spartan 6 FPGA SP601 inspected after HALT testing
• Component shows fractured joint
• Several workmanship defects were observed such as insufficient solder, lack of pretinning etc.
Summary

- NASA/JPL is investigating standard HALT conditions as a means for establishing a benchmark for COTS PCB quality for small sat and other higher risk profile missions.

- NASA/JPL HALT investigations have shown that COTS PCBs have a range of performance.

- HALT methodology demonstrated as a potential screen for COTS boards

- HALT was successful in identifying several workmanship concerns with COTS
  - Insufficient component staking – Component showed fractured joint
  - Insufficient solder coverage for plated thru-hole and leaded packages
  - Lack of pre-tinning and gold removal resulting in poor wetting and solder coverage

- Further development required to build a knowledgebase on HALT application for screening parts to mission requirements.
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