THE NEW VALUE FRONTIER

High Performance Packaging for Space

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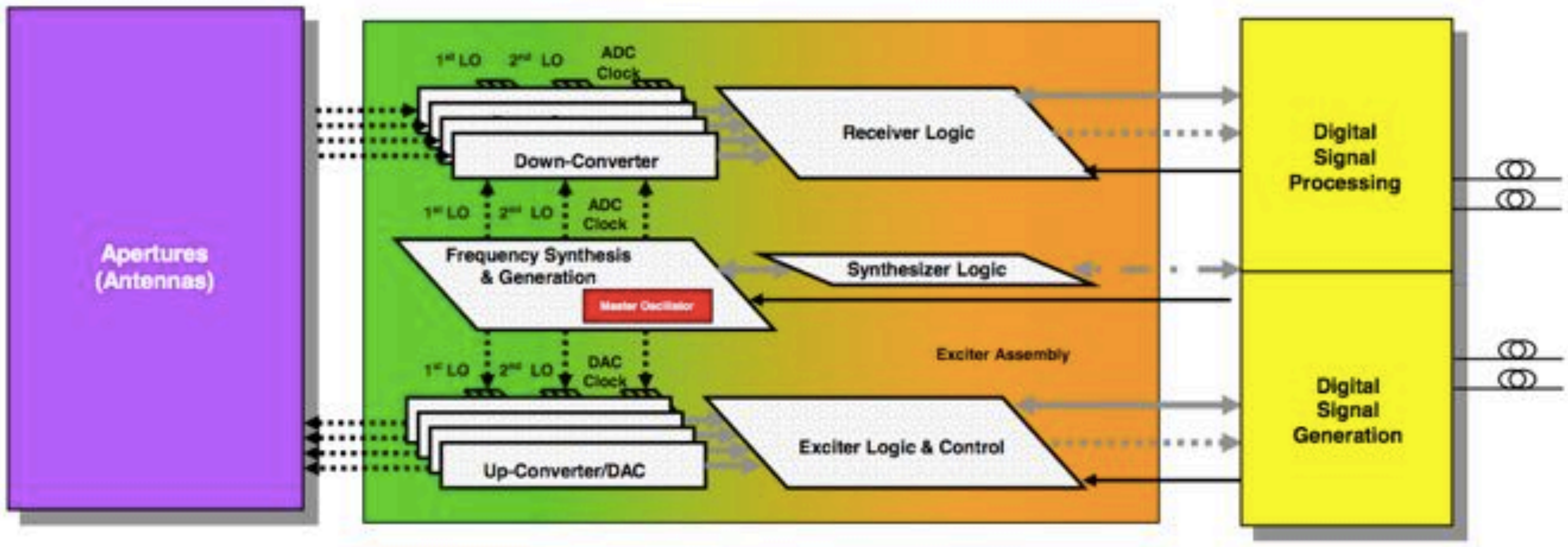
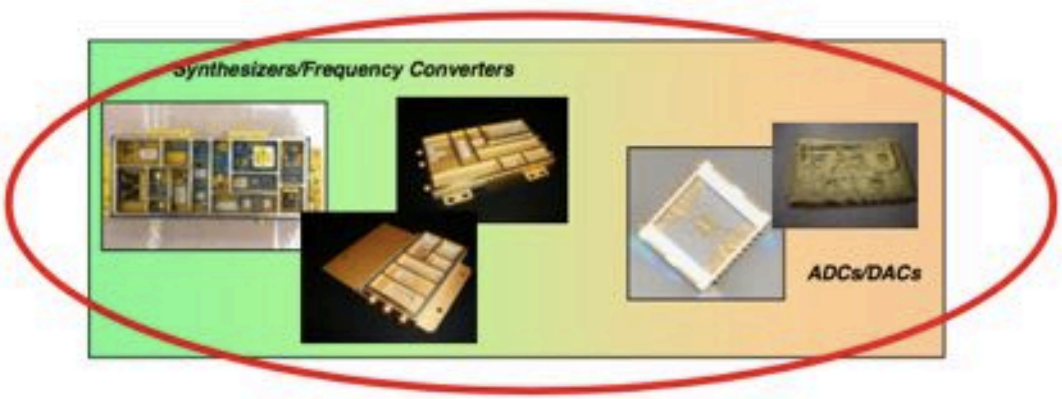
Kyocera International, Inc.

April 2017

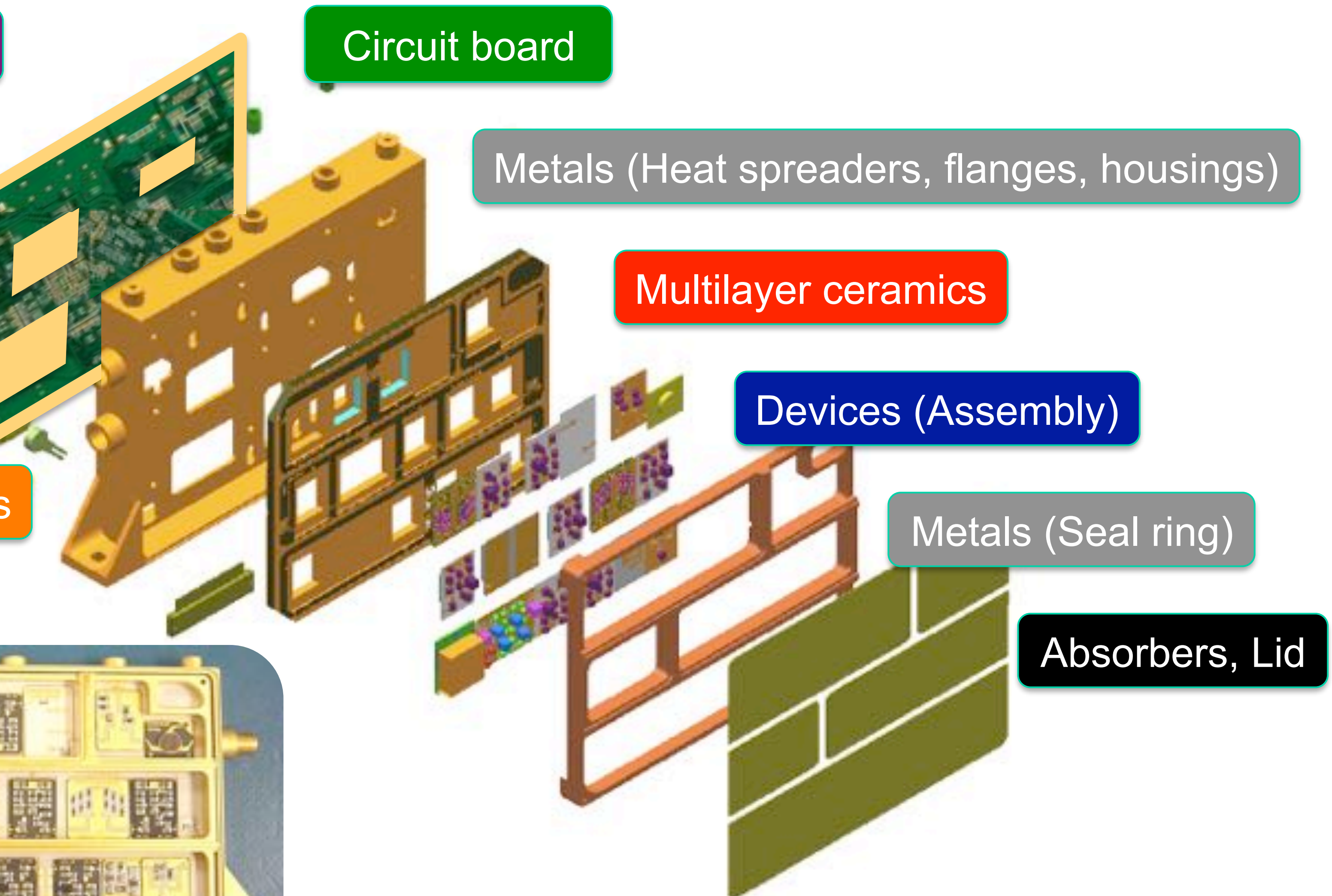
Space Modules and Comm Subsystems



Digital Receiver/Exciter (DREX)

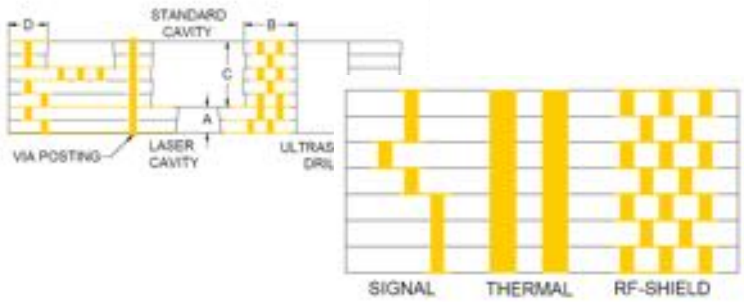


RF modules: KAI’s road map



Benefits of Ceramic Packages

- Unique characteristics of Multilayer and Post-Fired Ceramic technologies can provide a wide variety of solutions.

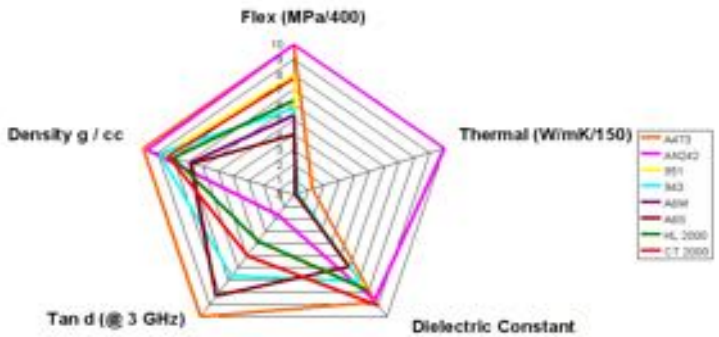


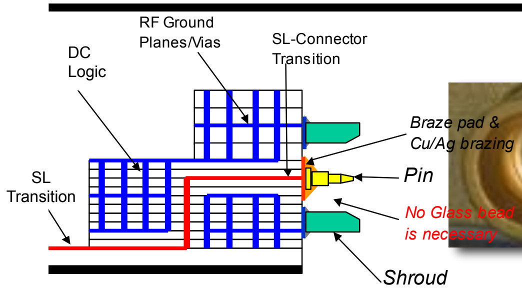
Excellent Design Flexibility

- High Density Design rule
- 3D Structure, Embedded Passives
- Single to Very High Layer Count

Excellent Material Properties

- Physical & Mechanical
- Electrical
- Thermal





Metal Parts Brazing Capability

- Heat Sinks / Seal Rings / Leads
- Many Material Options
- Reliable High Temp Brazing

There are two options for low loss module design: GL331 and AO630

Standard KAI multilayer ceramics

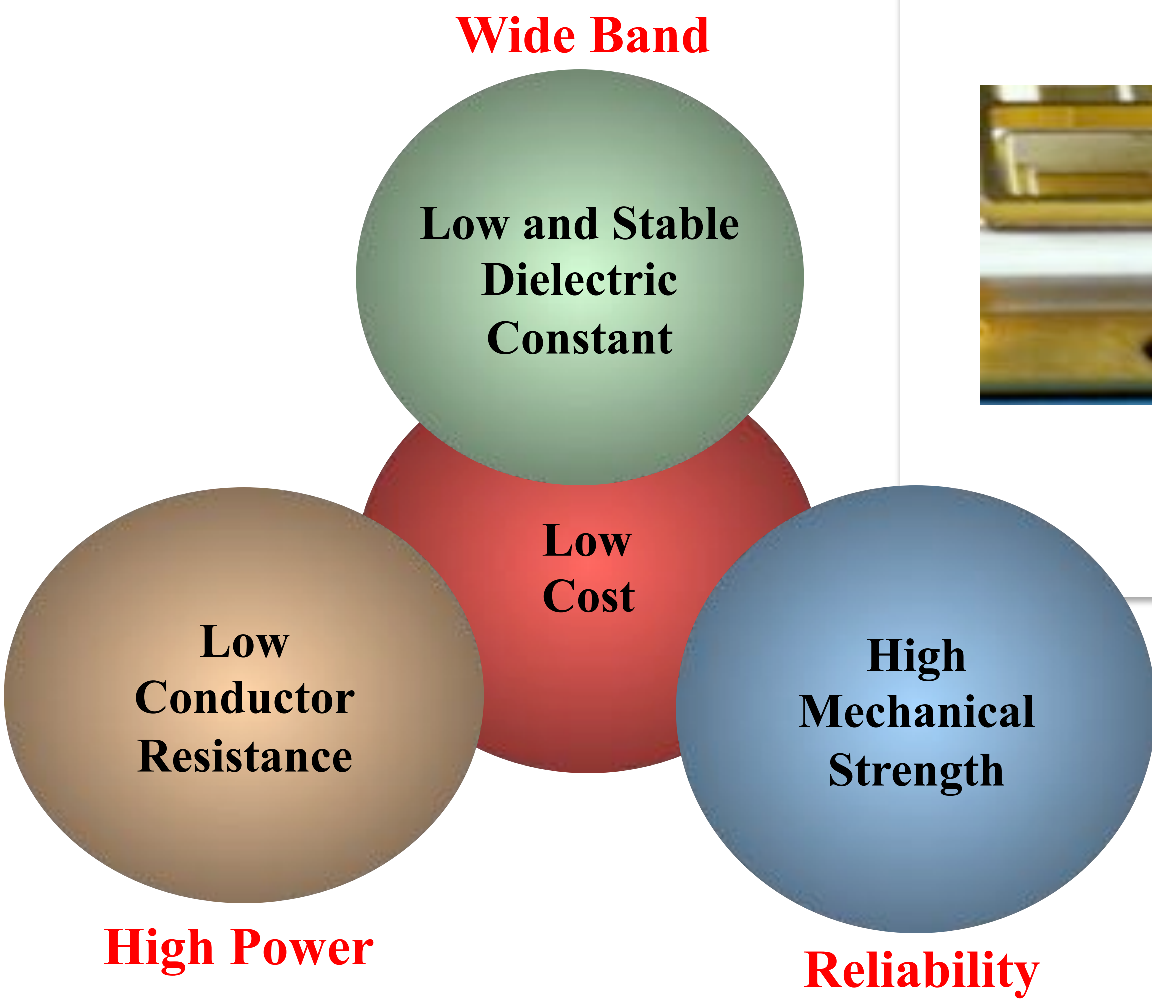
HTCC (High Temp Cofired Ceramic)
Pt: 92% Alumina with Pt conductors

MTCC (Medium Temp Cofired Ceramic)
AO630: Alumina with CuW Conductors

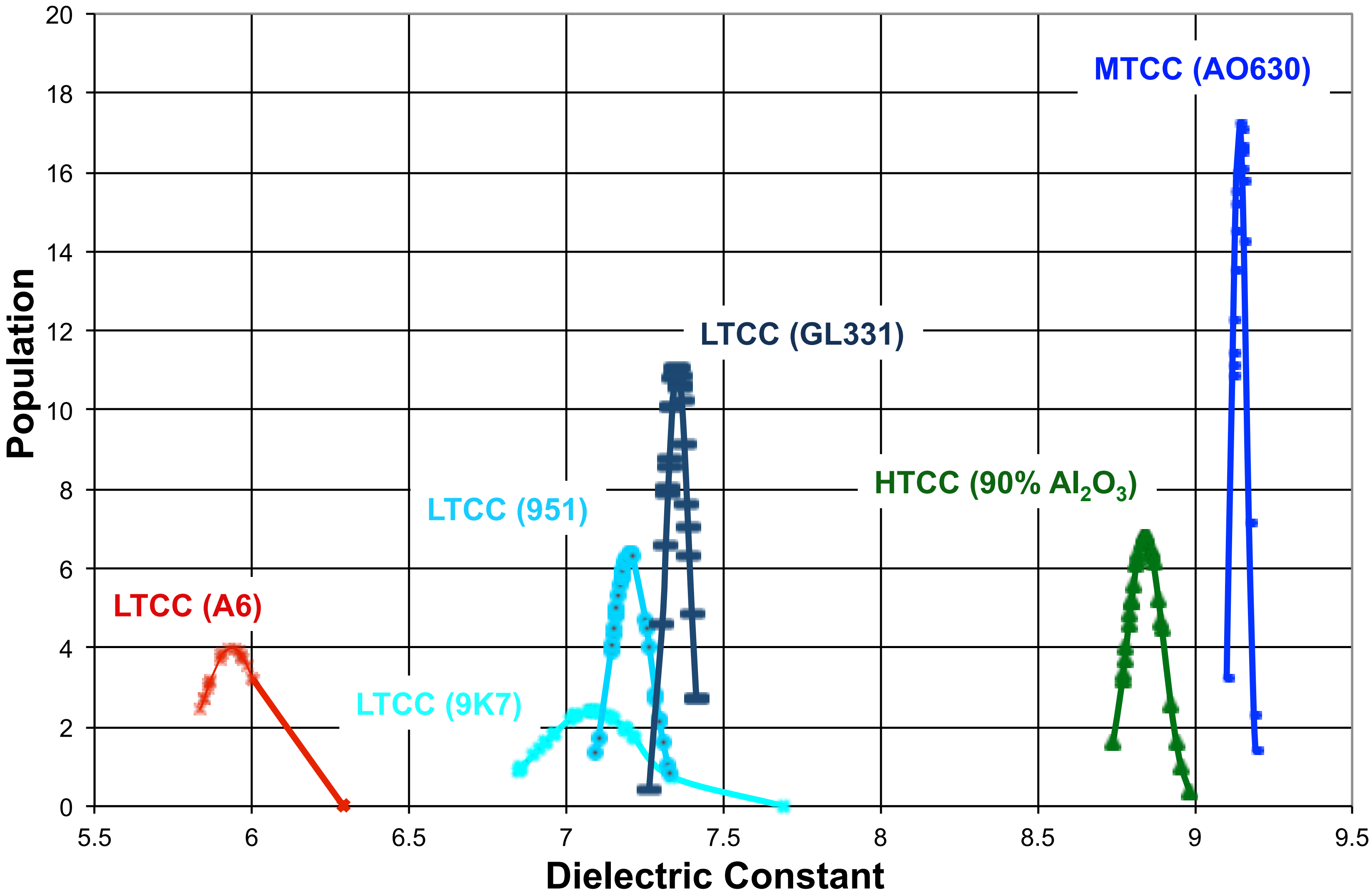
LTCC (Low Temp Cofired Ceramic)
GL331: Filled Glass Ceramic

Materials / Characteristics	HTCC			LTCC			Developmental	
	A440	A473	AN242	Dupont 951	Ferro A6M	GL331	Pt	AO630
Young's Modulus (GPa)	310	270	320	152	92	155	275	275
Flexural Strength (MPa)	400	400	400	320	210	400	440	460
TCE (RT - 400°C, ppm)	7.1	6.9	4.7	5.8	7.0	7.3	6.9	7.0
Thermal Conductivity (W/mK)	14.0	18.0	150	3.0	2.0	3	17	16
Dielectric Const (1Mhz)	9.8	9.1	8.7	7.8	5.9	7.5	9.0	9.3
(3Ghz)	9.6	8.5	8.7	7.8	5.9	7.7	--	9.1
(60Ghz)	--	8.6	-	--	--	7.5	--	9
Dielectric Loss (1Mhz)	24×10^{-4}	5×10^{-4}	1×10^{-4}	10×10^{-4}	12×10^{-4}	4×10^{-4}	6×10^{-4}	5×10^{-4}
(3Ghz)	15×10^{-4}	10×10^{-4}	170×10^{-4}	60×10^{-4}	12×10^{-4}	10×10^{-4}	--	23×10^{-4}
(60Ghz)	--	21×10^{-4}	-	--	12×10^{-4}	16×10^{-4}	--	21×10^{-4}
Conductor/Resistance (mΩ/sq)	W / 8-10	W / 8-10	W / 8-10	Au, Ag / 2-4	Au, Ag / 2-4	Cu/3	Pt /~10-15	CuW/Mo/~4
Brazing Materials	Ag/Cu	Ag/Cu	Ag/Cu	Au/Sn	Au/Sn	Au/Sn	Au	AgCu

Attributes of GL331



Dielectric Constant Uniformity



GL331 Dielectric Constant: Uniformity between and within lots

Lot No.	Tape manufacturing date	Fired layer thickness (mil)	Density (g/cm^3)	Dielectric Constant @12.5GHz* (std. dev.)	Dissipation Factor ($x10^{-4}$)
1	2012	7.57	3.194	7.36 (.03)	22
2	2013	7.82	3.200	7.33 (.04)	22
3	2013	7.73	3.199	7.37 (.02)	23
4	2015	7.52		7.34 (.03)	
Result (±mean)		± 2%	± 0.1%	± 0.3%	± 2%

RF modules and embedded filters: GL331

- **Modules**:

– Structural integrity	*High strength (400MPa)* *Chemical Stability*
– Metals / Connectors	*AuSn brazing of RF connectors* *Hermetic attachment of matched metals (HS,SR)*
– Interconnect	*Wire bonding (15g wire pull (1mil Au))* *BGA (2kg ball shear)*

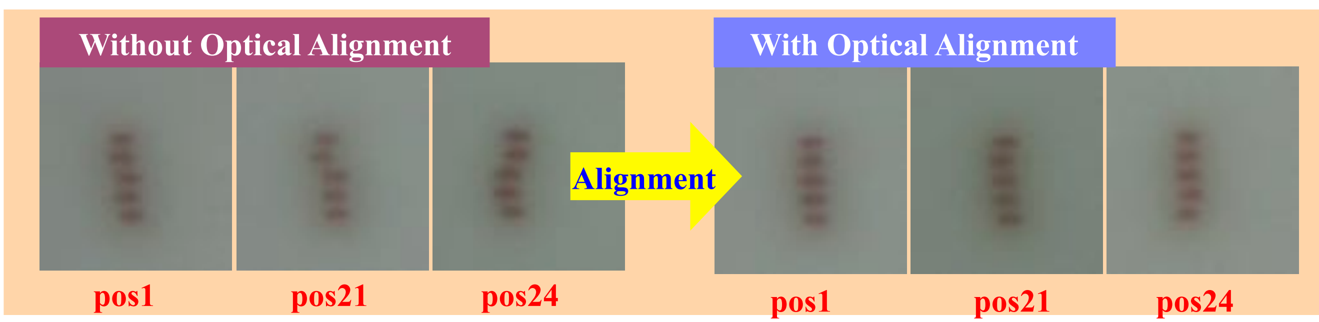
- **Filters**:

– εr	*Stable over frequency, material / firing lots* *Low dielectric and conductor losses*
– Vias	*Uniform diameter, minimal nail-heading* *Fine pitch, slots possible*
– Layer alignment	*Optical alignment (~0.002” possible)*
– Thickness/Shrinkage	*Consistent lot-to-lot*

Layer-to-layer alignment : Critical for filters

- Optical alignment during lamination results in significant improvement
- But, it typically requires:
  - Printed features
  - Tooling modification
  - New group lamination "strategy"

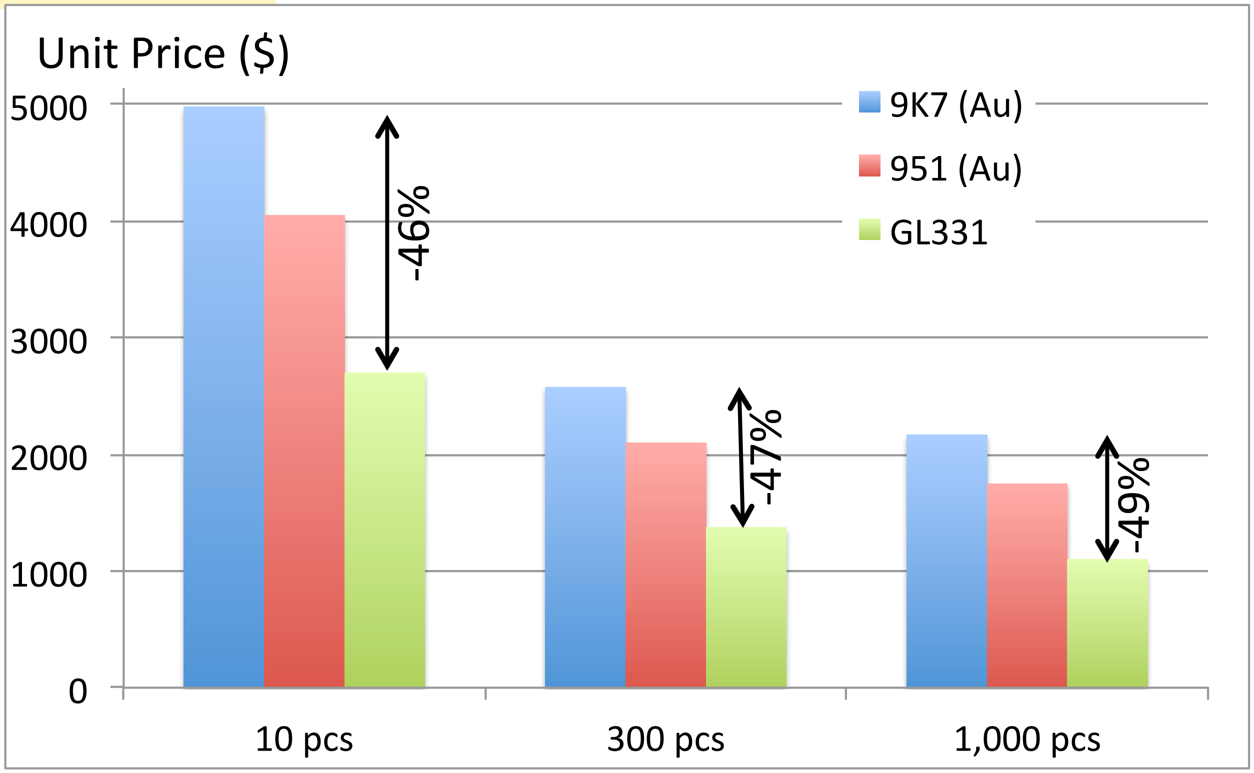
Capable of < 3mil layer-to layer alignment



Comparative Pricing – GL331 is much cheaper than other LTCC materials

Advanced LTCC Module (example)

- 1.5 x 3.5"
- 18 layers
- Ring frame and baseplate
- Edge mounted connectors



Cost comparisons – Candidate Ku-band module

Details: Compare the costs of a package that has been manufactured in volume in **both** LTCC and HTCC. This exercise illustrates the inherent cost differences between the two technologies.

Comparative Package:

1.5 x 0.9 x 0.180"
6 GPPO connectors
FeNiCo seal ring
CuMo/CMC Heat sink

Similar to…

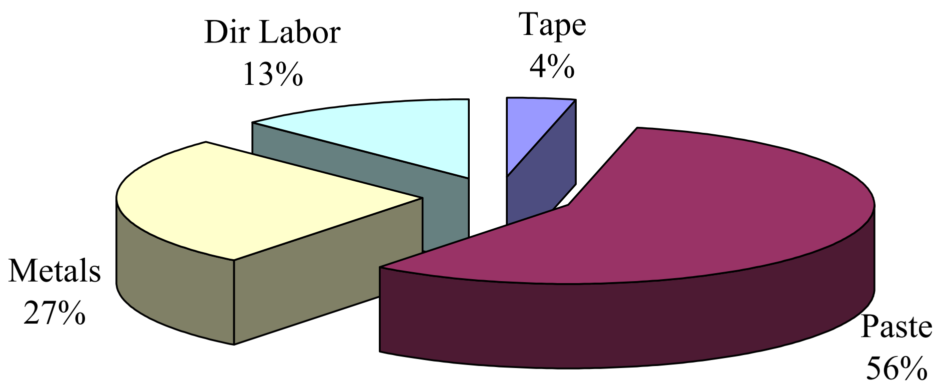
Assumptions:

– Au at $1100/toz
– 75% yield

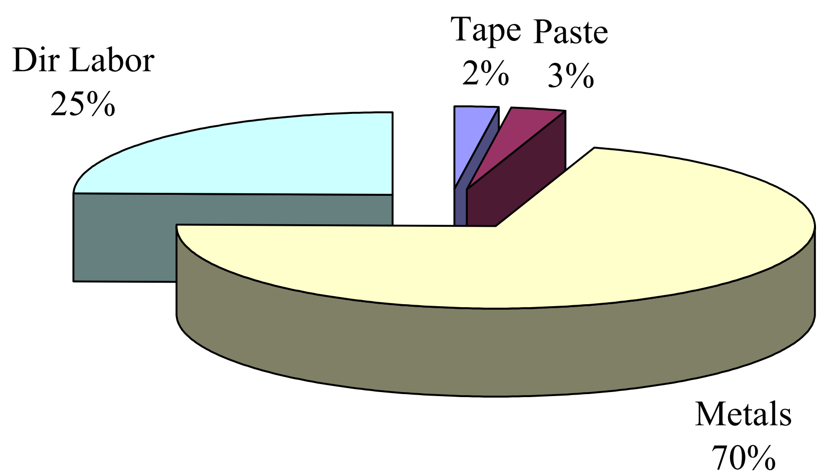
Layer count	23	17
Heat Sink	CuMoCu	CuMo
Metallization	Cofired Au	Cofired W, Ni/Au plate
Brazing	AuSn	CuAg

Cost Details (100k qty)

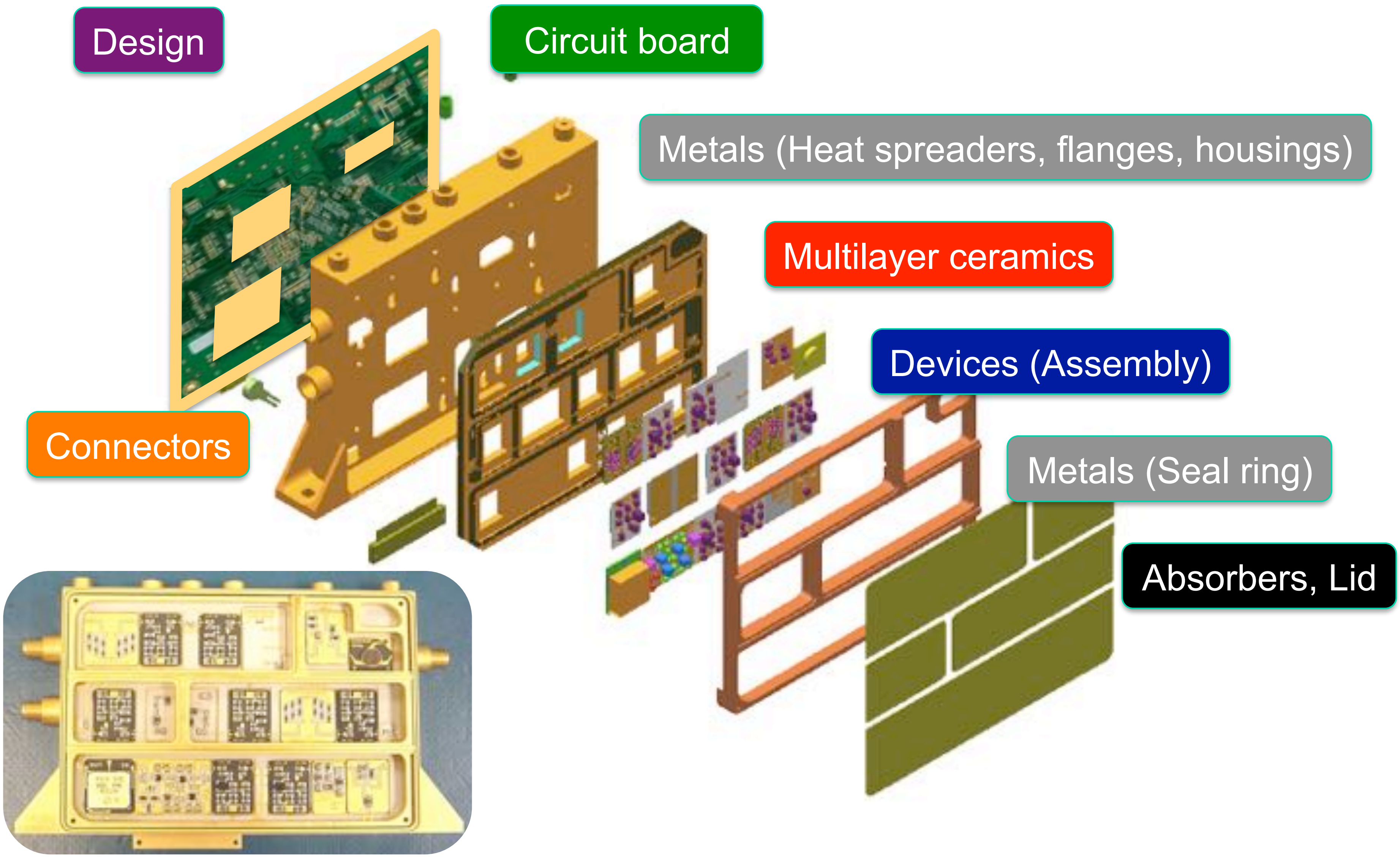
Dupont 951 (LTCC)
$450



92% Al2O3 (HTCC)
$200



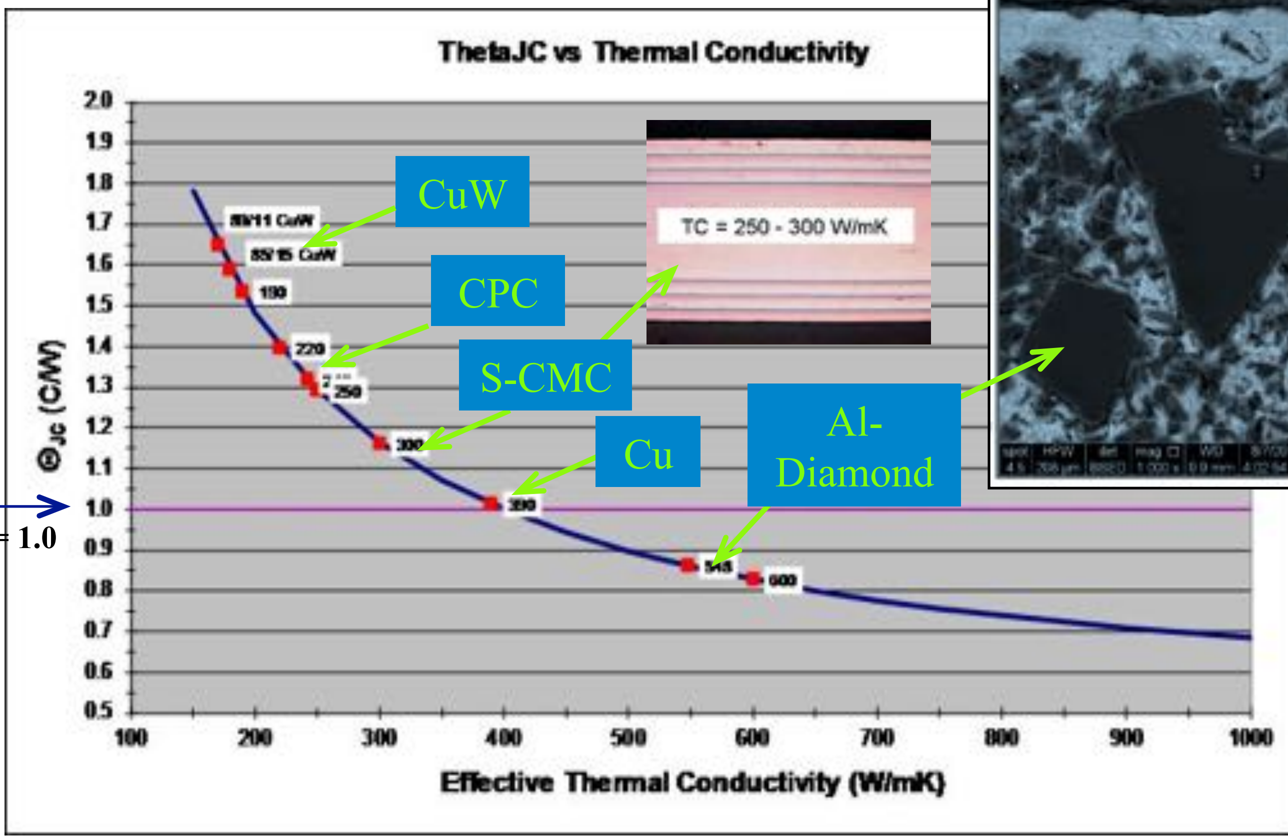
RF modules: KAI's road map

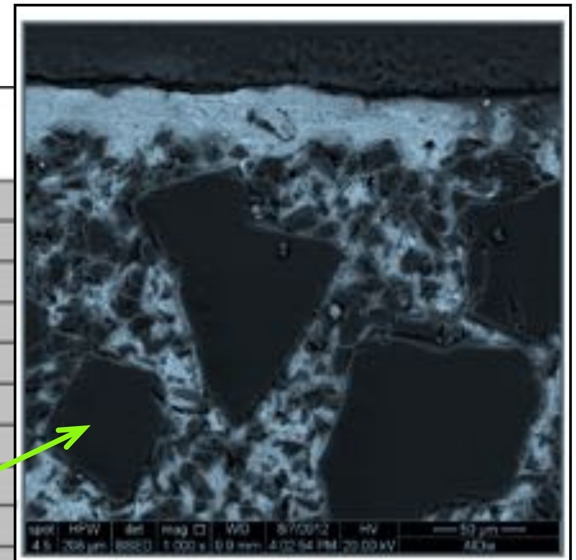


High performance heat sinks

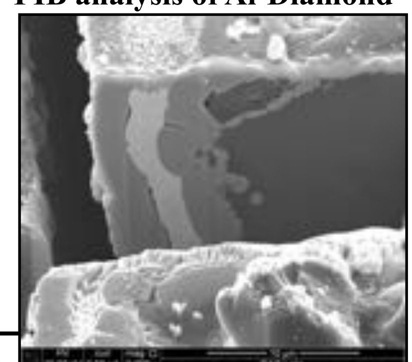
Commercial and defense-based products

Cu = 1.0

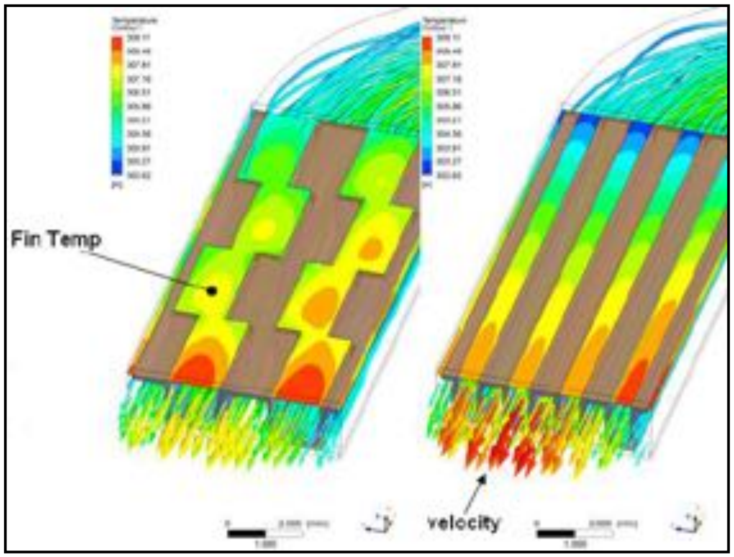




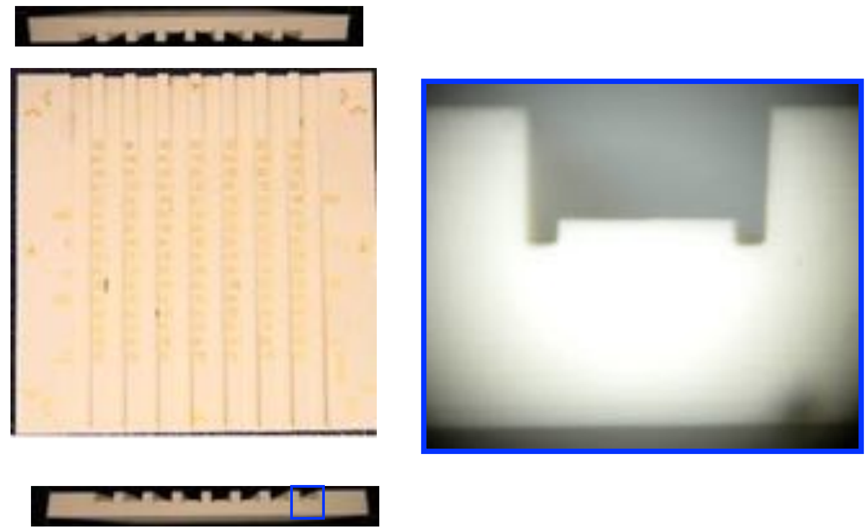
FIB analysis of Al-Diamond



Active cooling – May be required in extreme cases

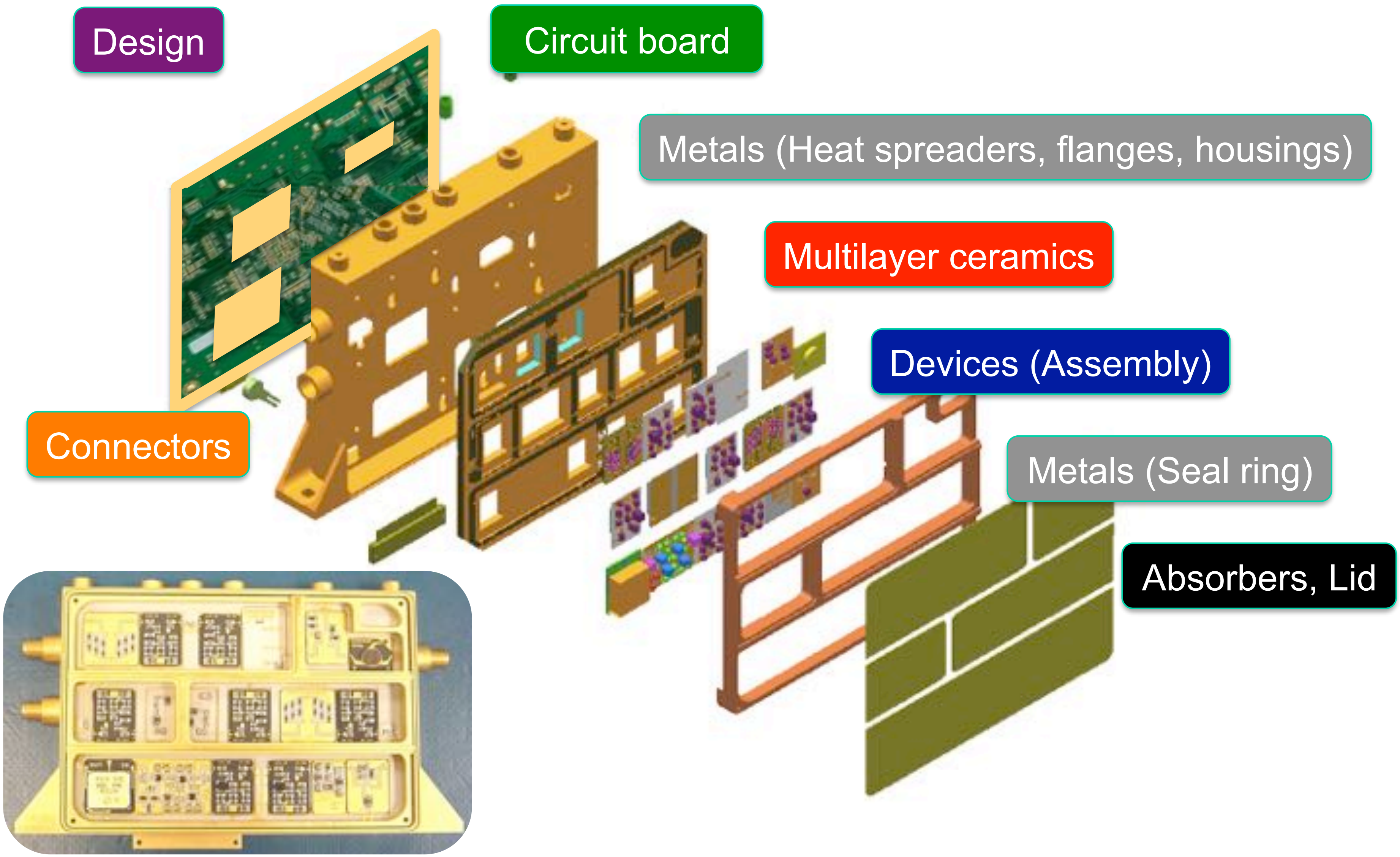


- Fluid delivery design
- Convection models



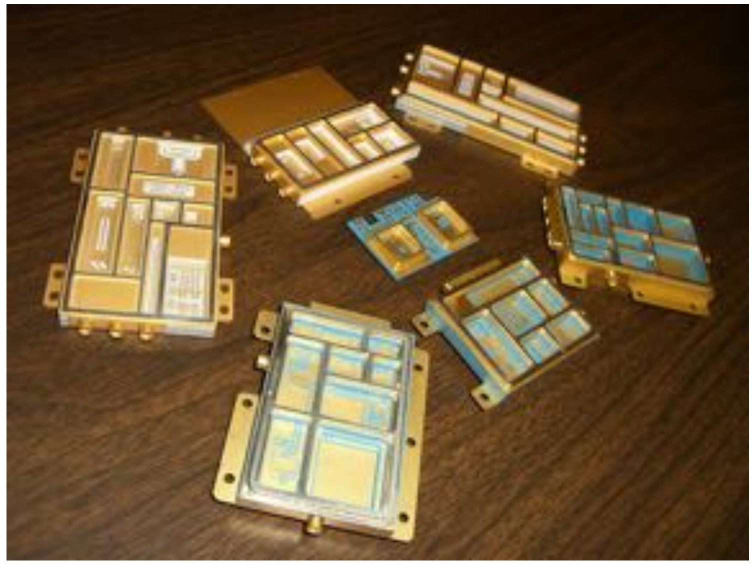
- Machined ceramic
- Unique designs for unique challenges

RF modules: KAI's road map



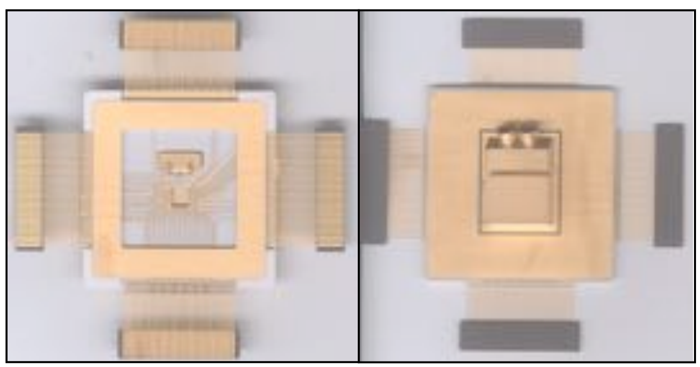
Connectorized RF Pkgs

X-Band Satellite Module

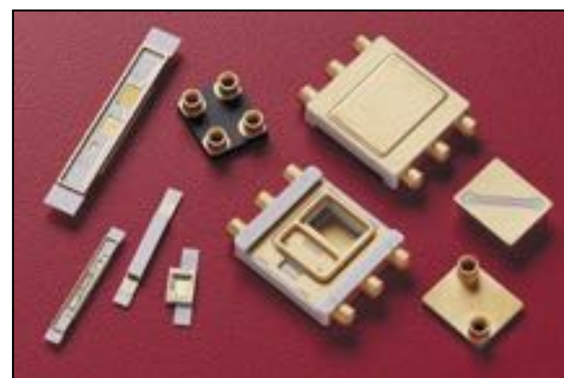


Sat-Com Packages

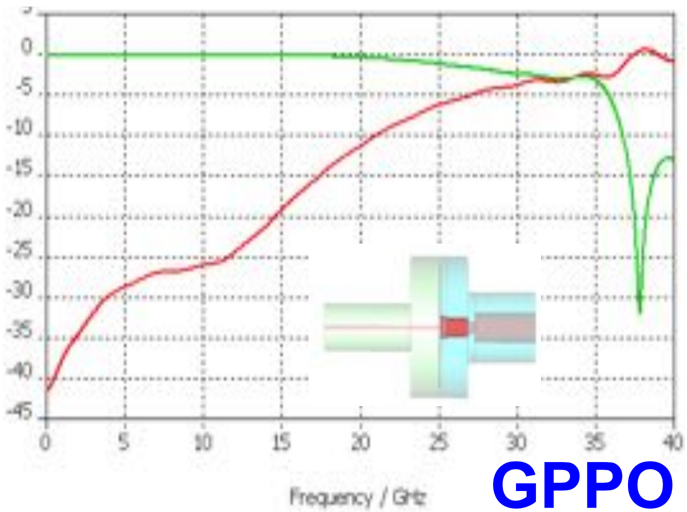
Radar T/R Module

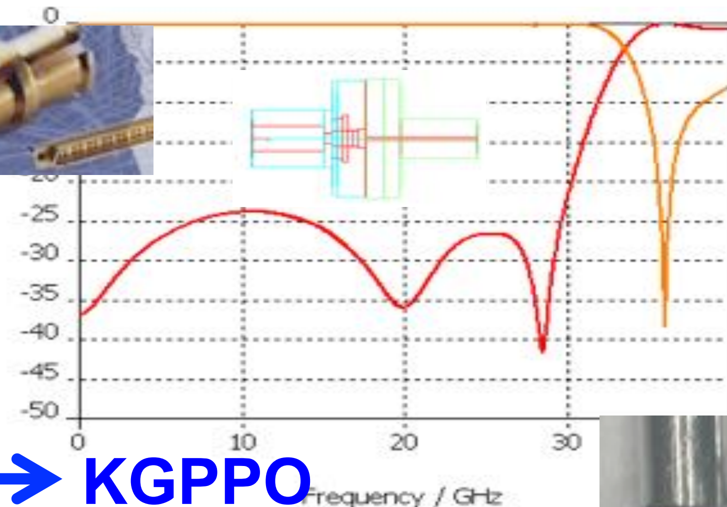


40G Mux/Demux



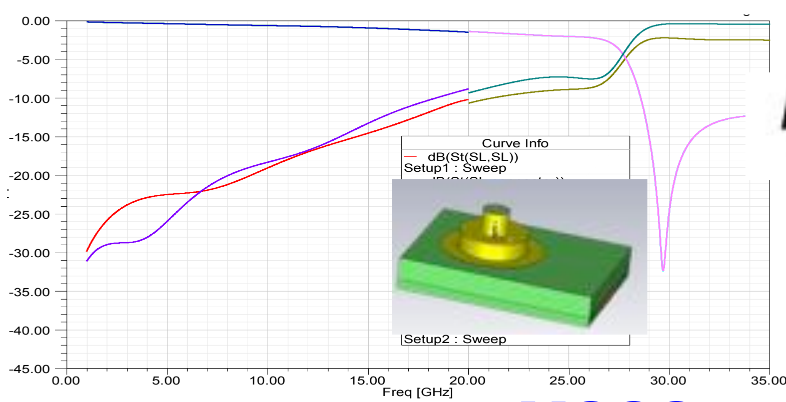
KAI-invented modifications to improve perfomance



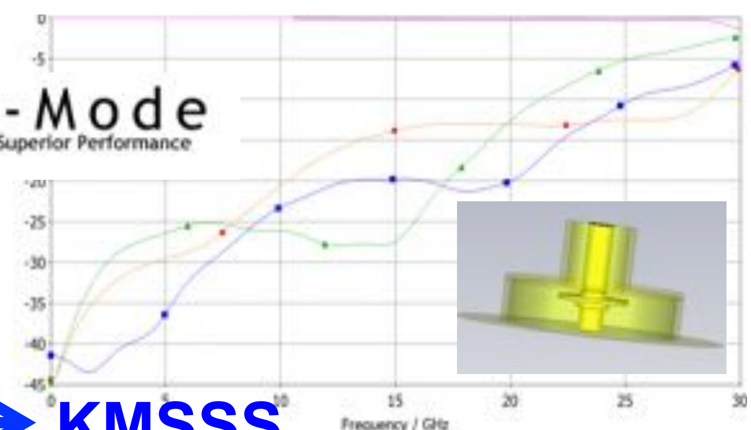


GPPO → KGPPO

~10GHz increased bandwidth

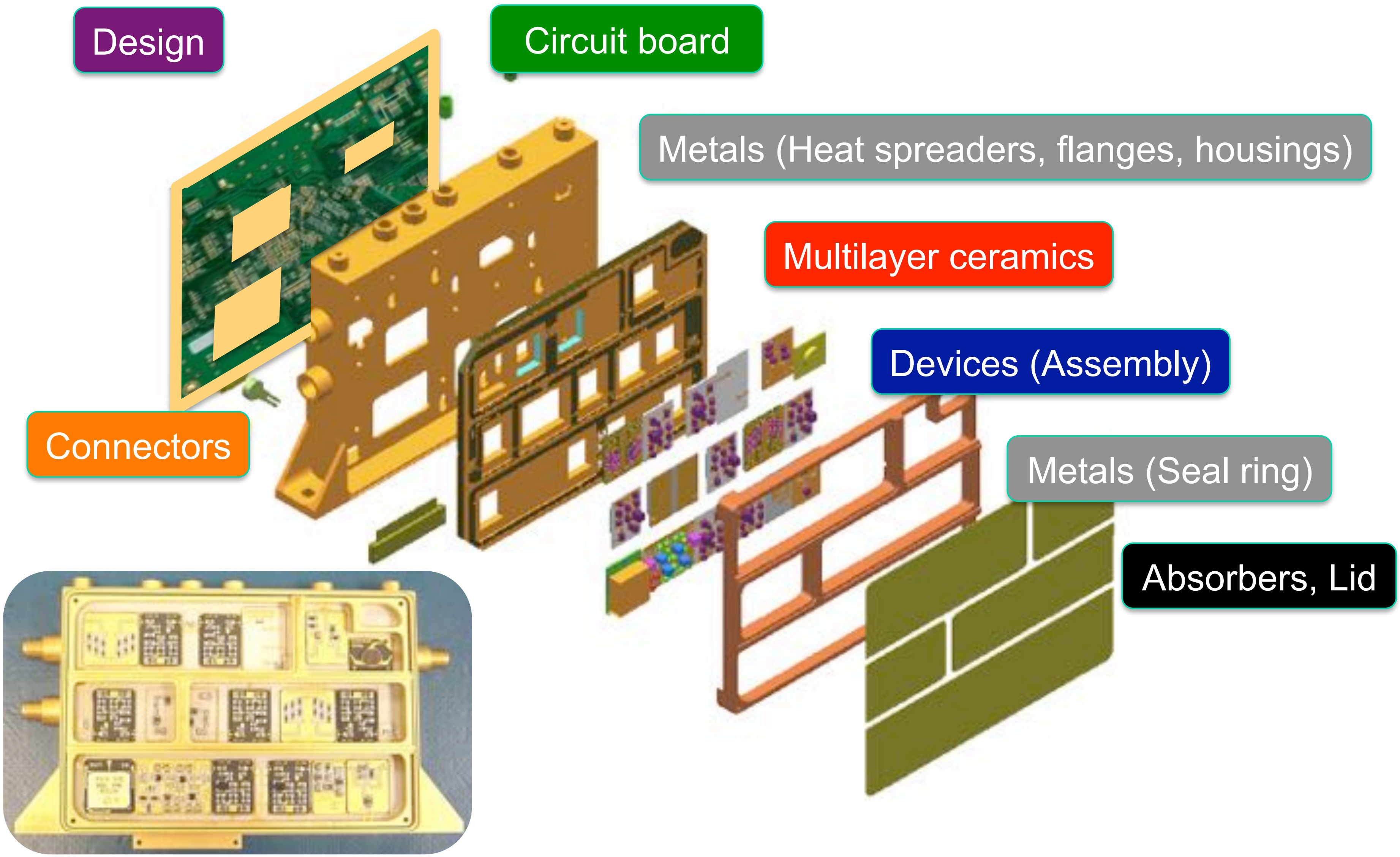


Micro-Mode
Superior Products - Superior Performance



MSSS → KMSSS

RF modules: KAI's road map



FC Assembly Process: QML_V

Wafer Dicing

DISCO DFD_6361

Component Placement

FUJI NXT/NXT-3

FlipChip Placement

DATACON_EVO
MICRON_2 / MRSI_605

Underfill

ASYMTEK

Lidding

Miyachi / SSEC

Electrical Test

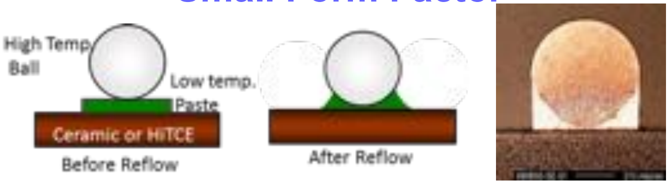
InHouse (consignment)

Outsourced

*Customer**

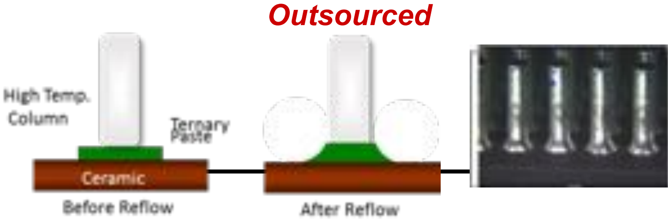
2nd Level Attach

Small Form Factor



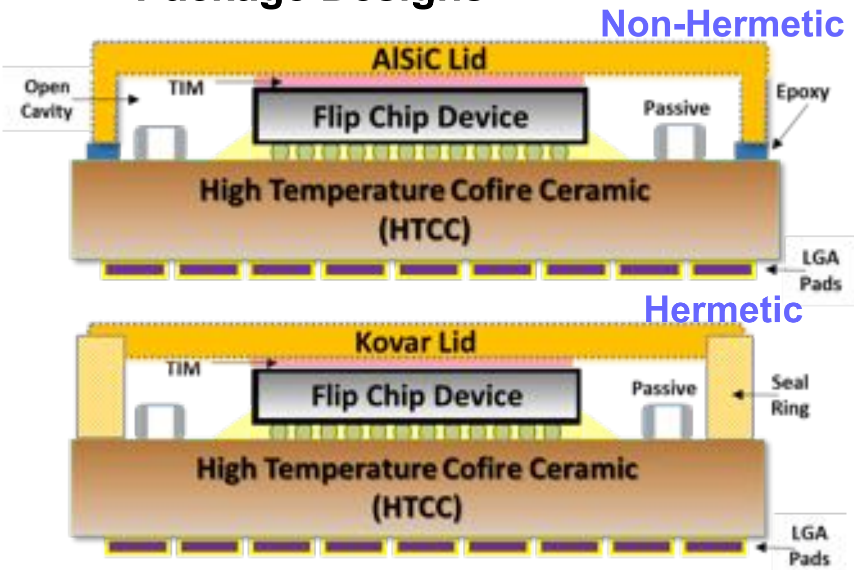
Large Form Factor

Outsourced



Current Status – Space FC

Package Designs



Customers

Package	QML	Customer
Non-Hermetic	Class Y	Customer A
Non-Hermetic	Class Y	Customer B
Non-Hermetic	Class-Y	Customer C*
Hermetic	Class-Q	Customer D
Hermetic	Class-V future	Customer D

*Partial Assembly

High Level Process Flow

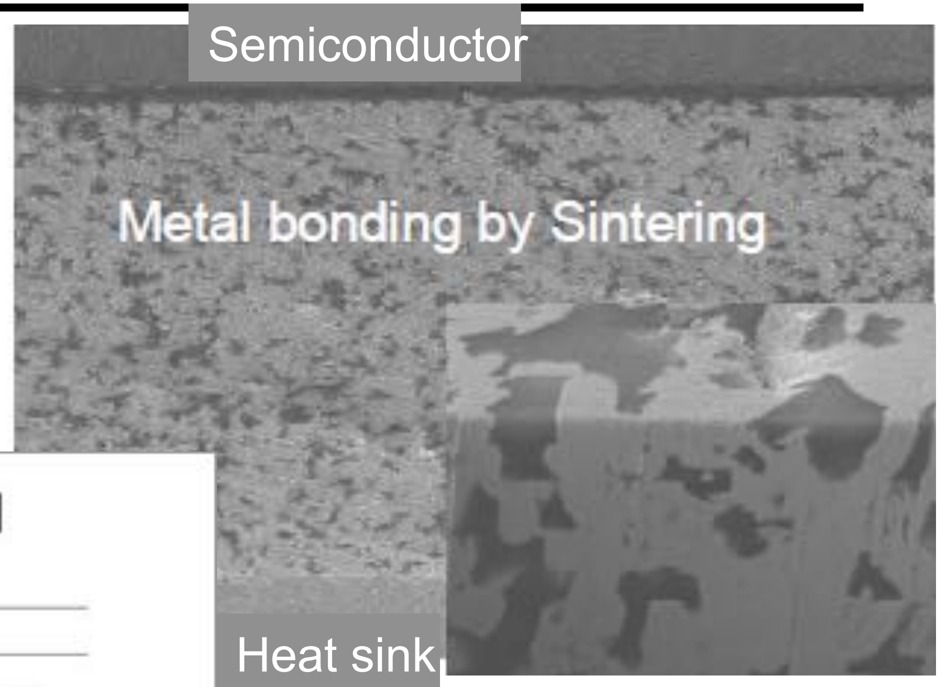
#	Description	Process Development
1	Passive Attach	Completed
2	Die Attach	Completed
3	Cleaning	Completed
4	Underfill	Completed
5	TIM Process	Completed
6	Lid Sealing	Completed
7	Marking	Completed

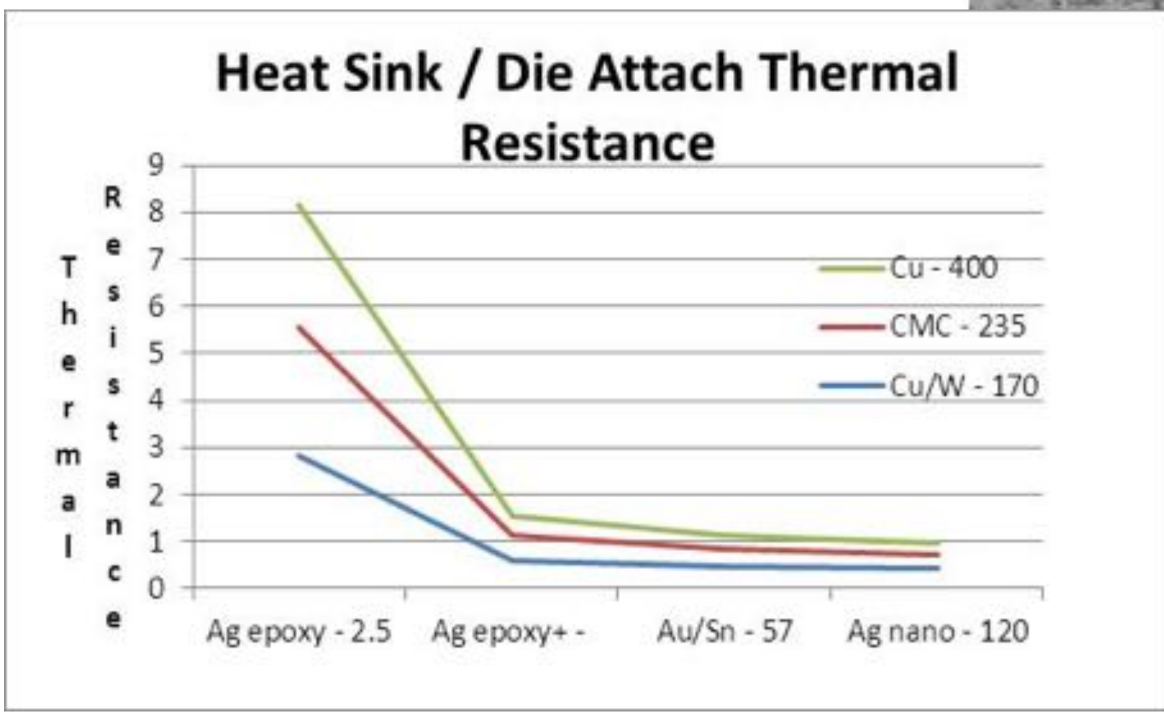
Statement

Kyocera has provided all data required to satisfy the modified Method 5011 and to support customers' PIDTP. Waiting acceptance by customers and DLA.

Sintered silver die attach (KCC)

Highest thermal resistance may be found in the attachment interface between the semiconductor and heat sink





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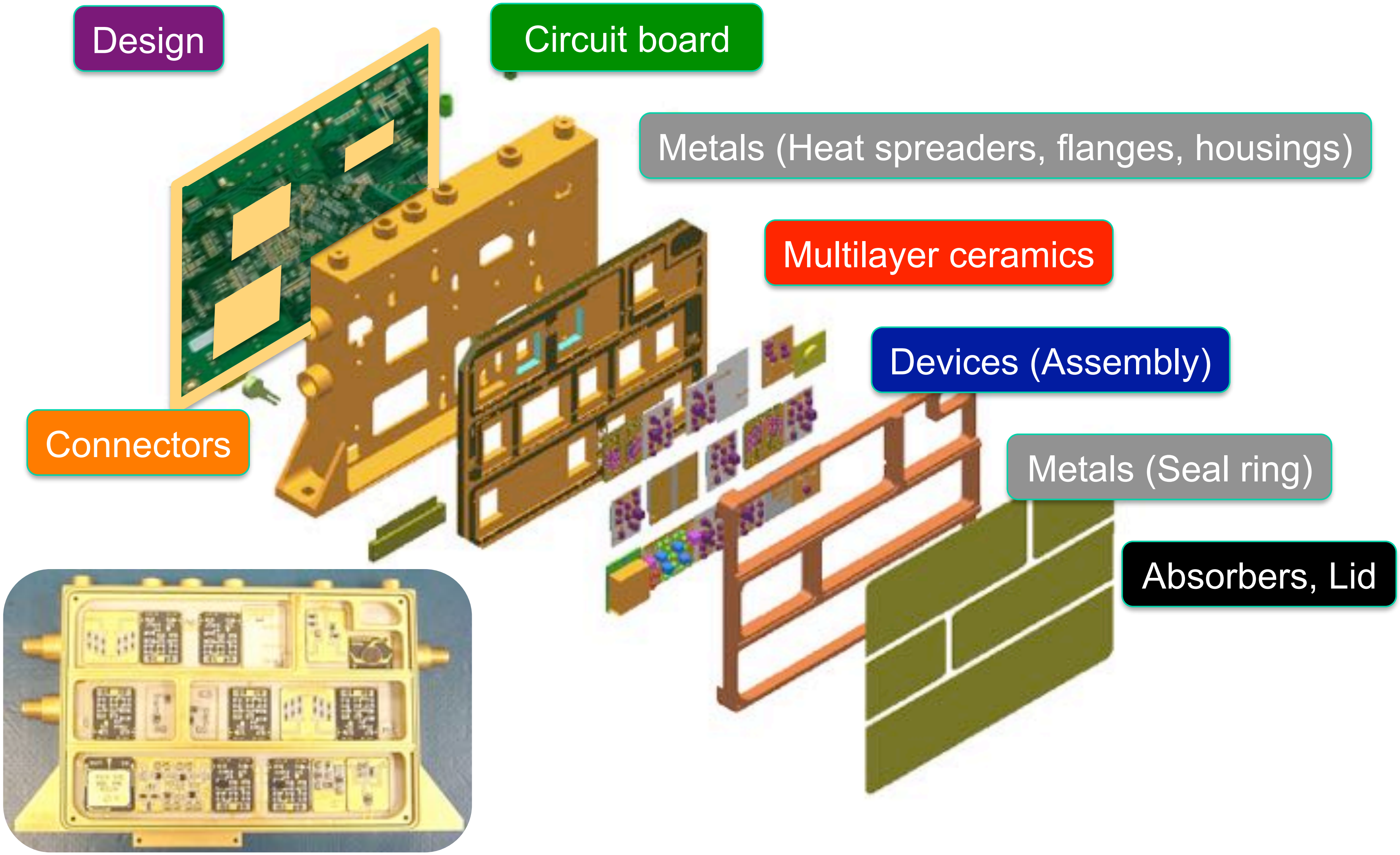
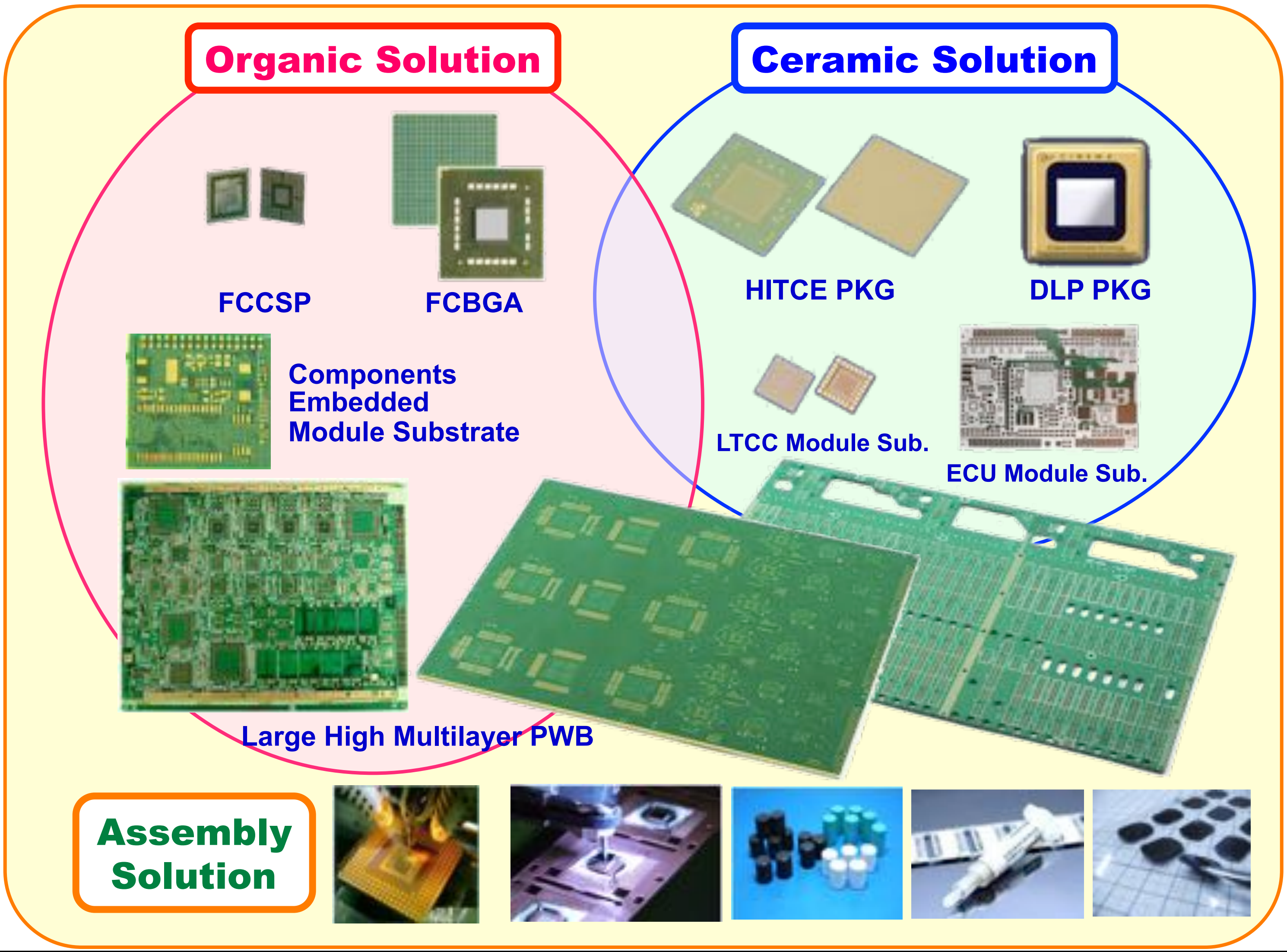


Advanced Packaging Materials

Package

Module Substrate

Mother Board



Example – Hermetic Space MCM

- Kyocera responsible for design, manufacturing, assembly
- Interface with customer and their customer
- Modules are in space

Original SOW: Governing document defining:

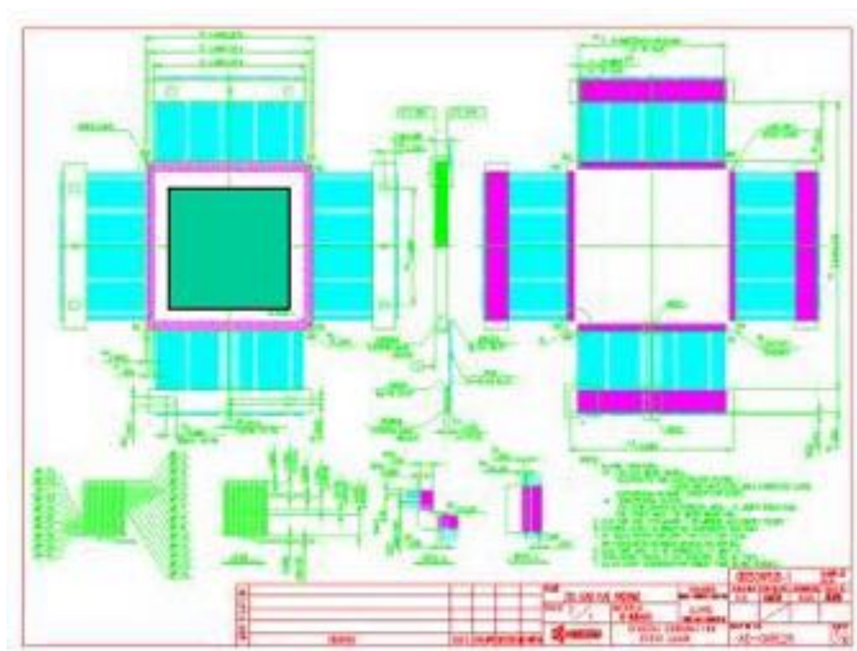
1. Requirements: Electrical, Thermal, Mechanical
2. Package Layout Proposal
3. Reliability Requirements / Estimation
4. Thermal Studies
5. Electrical Simulation / Design
6. Package Production
7. Assembly
8. Testing / Inspection / Shipping
9. Design validation

Original SOW: Governing document defining:

1. **Requirements: Electrical, Thermal, Mechanical**
2. Package Layout Proposal

- Hermeticity – $<10^{-8}$
- Dimensional – x, y, height – tightly spec'd
- Thermal dissipation – theta jc
- Moisture content (underfill, paste) - <1500ppm
- Low inductance
- Signal integrity–dI/dt, decap placement/identity
- RF – RL, isolation

- Brazed leads
- Cup-shaped lid with AuSn seal
- Flip Chip MCM with ~20 passives
- Challenging volume, thermal, electrical requirements



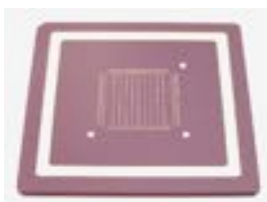
Consideration of:

- 1^{st} level (die-substrate)
- 2^{nd} level (substrate-PWB)
- Lid Seal
- Shock / Vibration / Thermal Cycling
- FIT estimation

Reliability – testing and modeling

Reliability evaluation employing test vehicle…

- Test Package: 29mm sq x 2mm thickness
- Die: Si 15mm sq
- Bump metallization: 95/5 Pb/Sn



…and Literature Data

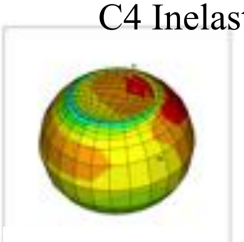
From “Flip Chip Encapsulation Reliability” by Quinones, Babiarz and Lewis, 1998.

Die Size Mm	Temp. Degrees C	Frequency CPD	Cycles to First fail	Die Carrier	Mean Life KCycles
13	0 to 100	72	6,200	50mm white ceramic	203
13	0 to 100	72	11,000	50mm white ceramic	258
13	0 to 100	72	>2,500 <28,600	50mm dark ceramic	-
19.2	-65 to 150	144	>500 <1000	32mm white ceramic	10.4
19.2	-55 to 125	27	>500 <1000	32mm white ceramic	18.4

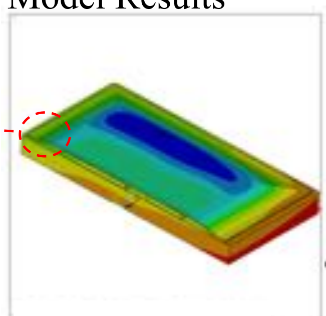
Table 1. Encapsulated Flip Chip Reliability Performance; mean life numbers are normalized to a common constant. (Data published by IBM-Microelectronics [7].)

[7] H.Quinones, "3rd International Conference on Flip-Chip Technology, C4 Encapsulation Fatigue," Center for Management Technology, April 1997.

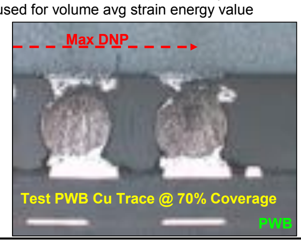
C4 Inelastic FE Model Results



CMOS submodel top 5 μm thick layer in C4 used for volume avg strain energy value



Global Model Deflection plot after three thermal cycles -55-125C, 1.2cph



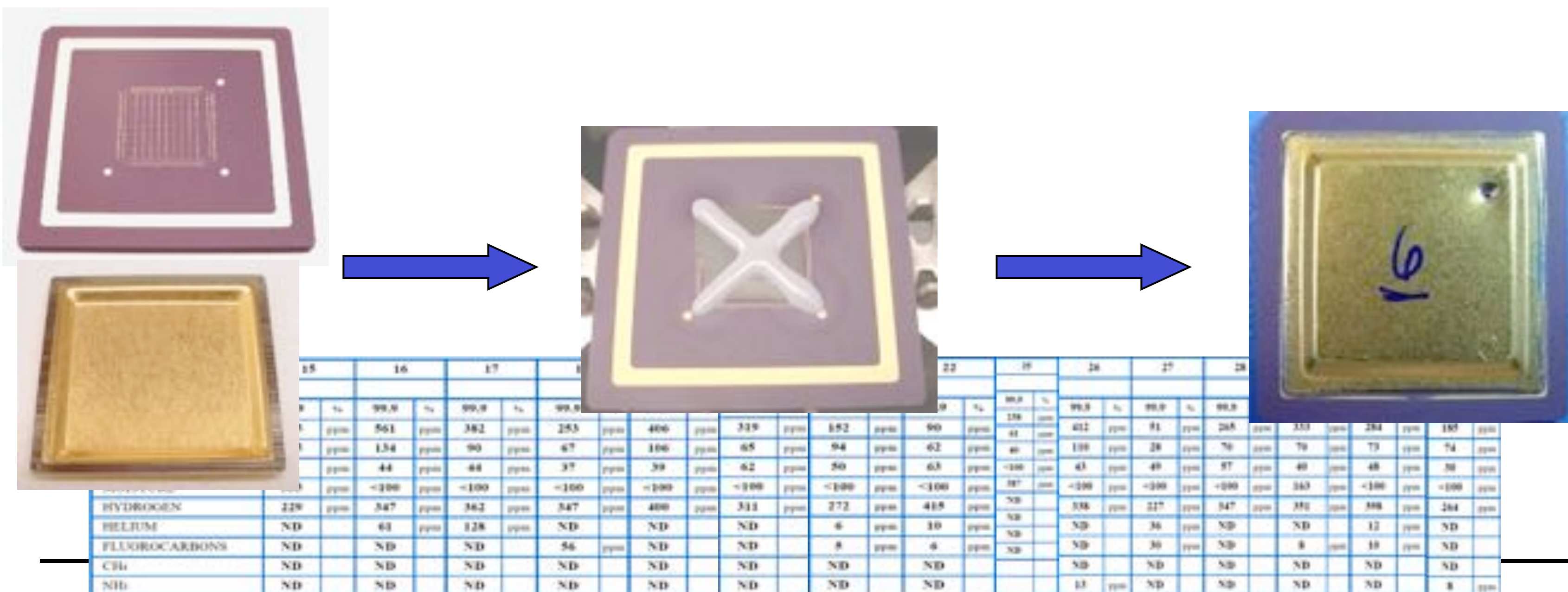
Typical KAI CBGA Fatigue Failure (right), Showing Eutectic Solder Cyclic Creep Ratcheting Behavior (TCT condition: –40-125C)

Lid Seal Reliability:

1. Substrate :	Alumina multilayer package
2. Substrate OD :	27 mm SQ (1.1mm thickness)
3. Die size :	10 mm SQ
4. Bump :	Eutectic bump
5. Underfill :	KAI standard
6. Seal :	AuSn with Seam Seal method
7. Lid:	Kovar dome lid (22mm OD, 0.25mm thick)
8. TCT :	MIL-STD 883, Method 1010 Condition C, 50 cycles
9. Hermeticity :	MIL-STD 883, Method 1014, Fine & Gross leak test

X-ray

- Characterize thermal dissipation – design and materials.
- Identify/characterize outgassing of thermal paste / underfill Focus: Thermal conductivity and Moisture (<5,000 ppm)



Underfill and TIM

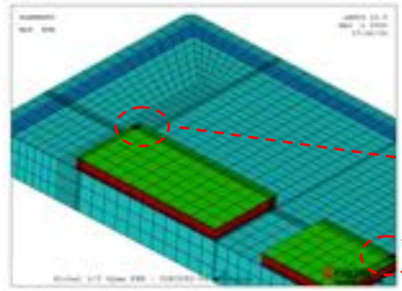
Underfill – Qualification

REF	PHYSICAL PROPERTIES	JM8801 VALUE	Underfill B VALUE	UNITS
	Appearance (Uncured)		Gray	
	Filler Content	63.5	45	%
	Viscosity @ 25°C	60000	35000	cP
	Tg	146	115	°C
	CTE (α1)	22	22	ppm/°C
	CTE (α2)		84	ppm/°C
	Flexural Modulus	10	6.5	GPa
	Ionic Contaminants			
	Na+		10	ppm
	Cl-		20	ppm

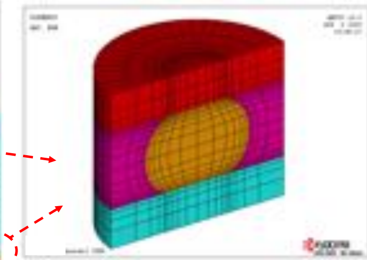
The two materials exhibit equivalent CTE and Modulus!

FE Model Technique For Underfill

Use more accurate 3D submodel technique to investigate underfill/solder interaction effects.



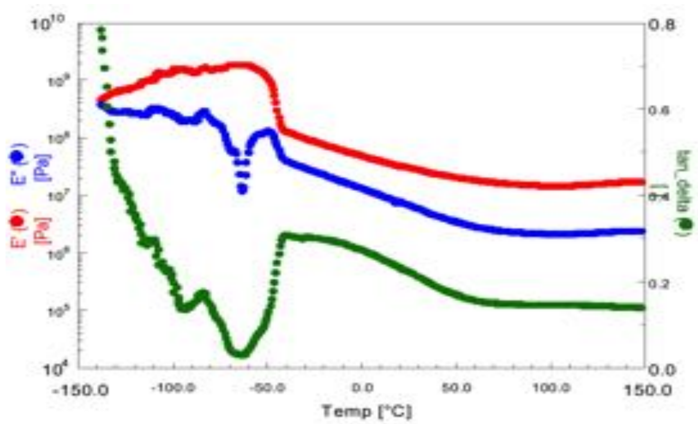
Course global model with Kovar lid removed for clarity.



X-Sectional View of Detailed Submodel

Theory: Submodeling is also known as the cut-boundary displacement method. The cut boundary is the boundary of the submodel which represents a cut through the global model. Displacements calculated on the cut boundary of the coarse model are specified as boundary conditions for the submodel. Submodeling is based on St. Venant's principle. This implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the submodel are far enough away from the stress concentration, reasonably accurate results can be calculated in the submodel.

Thermal Compounds: Modulus vs. Temp



AI#11 – Thermal Paste

RELIABILITY DATA

Reliability experiments were performed using Al-Si sandwiches prepared with 10 psi of assembly pressure and cured for 2 hours at 150C. Thermal diffusivity measurements, made using a laser flash diffusivity instrument (Netzsch Instruments Microflash 300) were used to calculate thermal resistance.

Thermal Shock

After 1000 (AATS) Cycles (Air-to-Air Thermal Shock) **(-55 to 125°C, 20mins cycles)**	Thermal Resistance, delta	-2.5%

Temperature/Humidity Aging

After 250 Hours Conditioning (85°C / 85%RH)	Thermal Resistance, delta	-5.2%

Moisture Sensitivity Level (MSL)

After 168 Hours at 85°C / 85%RH	Thermal Resistance, delta	-0.28%

* Level 1 – 85C / 85%RH + 3 Post Condition Reflow Cycles (260C Peak / Lead-Free Profile)

These data show the stability of the paste thermal resistance and, thus bond integrity, with thermal shock and exposure to humidity

Adhesion Strength-Reliability*

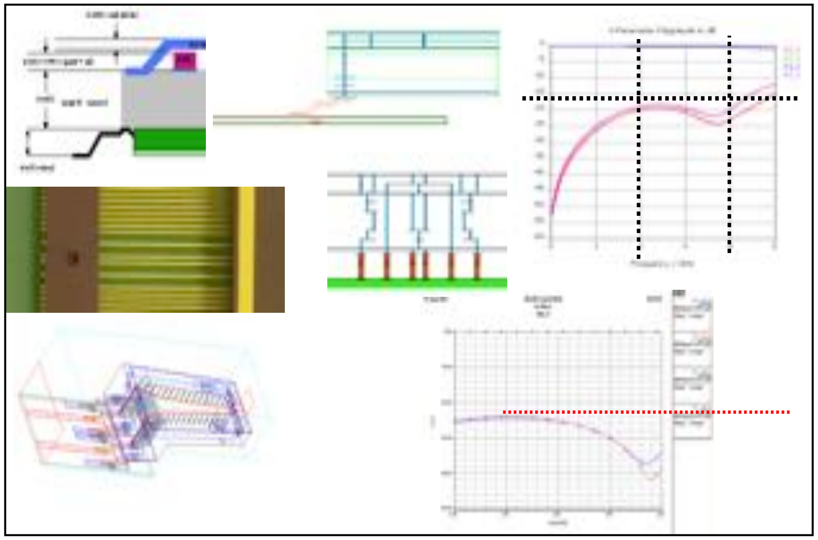
After 500 AATC Cycles	Die Shear Adhesion, delta	+21%

There is an actual increase in adhesion over time. This is likely not inherent to thermal shock.

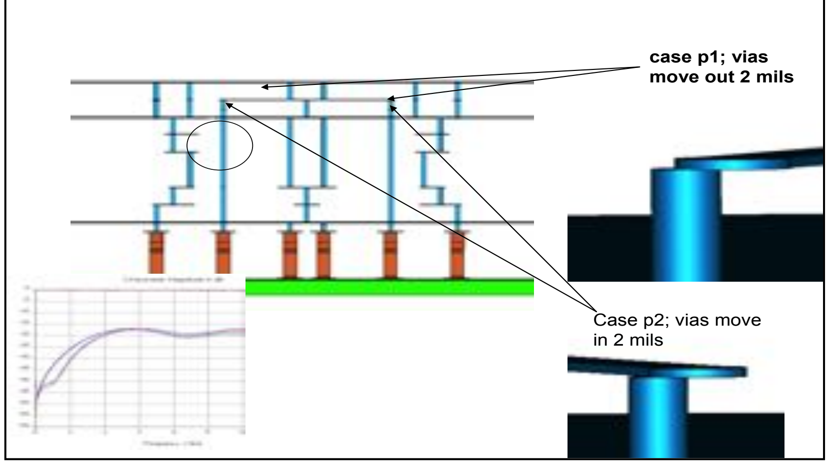
* Die-Shear Test with Silicon Die on Aluminum Substrates
** 500 Air-to-Air Thermal Cycles (-55 to 125°C, 20 minute transition)

1. **RF signal differential pair design** – MWS, HFSS
2. **di/dt analysis** – Speed2000
3. x-talk analysis – Speed2000
4. isolation analysis – Speed2000
5. Rdc analysis
6. S-parameters – Speed2000
7. Impedance Measurement Validation

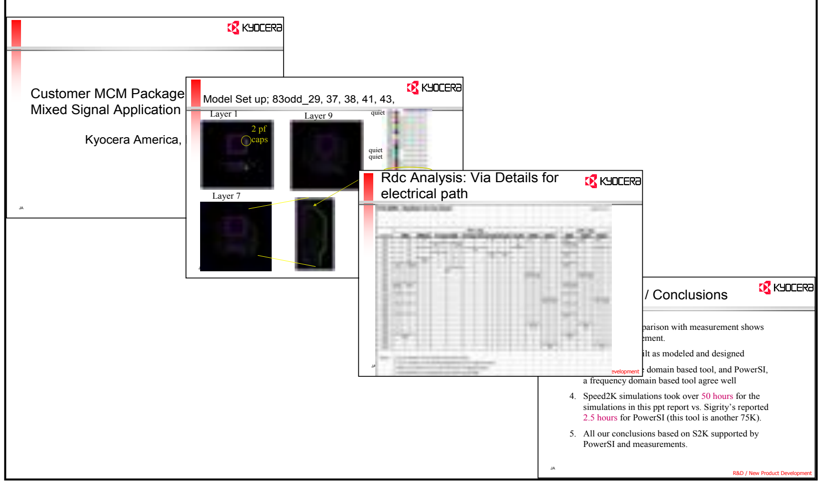
Simulation and Design



Sensitivity Analyses – How is performance affected by process variations?

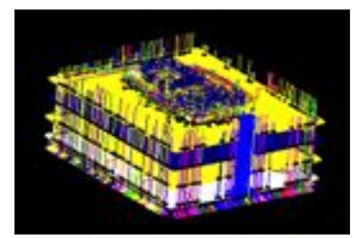


Results – Typically ppt format

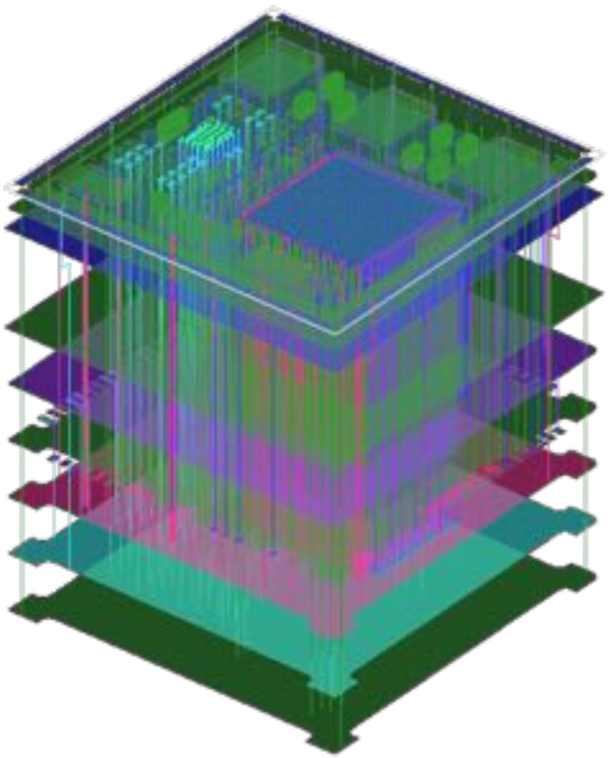


Package Layout – Challenges

- Design:
  - Fine pitch FC
  - Height
  - Hermeticity (lid choice)
  - Lead configuration – bottom vs. top
- Routing
- Net list modifications
- Conductor length
- Design rules



Power Analysis – Typical Requirements



Zin for each power net

- Pwr/Gnd impedance vs. location study
- Impact of decoupling capacitors
  - First question: Can using board decoupling scheme work as drop-in for ceramic package?

    Strategy:Place large value capacitors outside MCM, place smaller value capacitors close to device
  - Next question: How much decoupling is being provided by capacitors on Layer 8?
- What must we do to meet device power delivery requirements?
  - Reselect decoupling capacitors based on package parasitics
  - Reposition decoupling capacitors based on full layout specifics

Package Production / Design Validation

Manufacturing Flow Chart

Substrate Thickness / Flatness

Ceramic Substrate Thickness

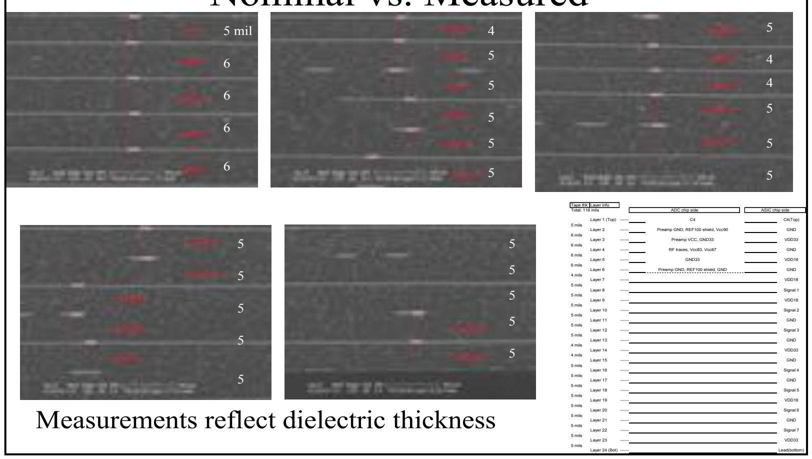
	Thickness[mm]	Thickness[in]
Max.	2.954	0.1163
Min.	2.929	0.1153
Average	2.94	0.1157
STD	0.008	0.0003
Cpk	7.83	
1	2.937	0.1156
2	2.954	0.1163
3	2.949	0.1161
4	2.931	0.1154
5	2.948	0.1161
6	2.938	0.1157
7	2.938	0.1157
8	2.945	0.1159
9	2.929	0.1153
10	2.933	0.1155

S/N	FLATNESS	S/N	FLATNESS	S/N	FLATNESS	S/N	FLATNESS
1	0.0011	26	0.0017	51	0.0016	76	0.0015
2	0.0013	27	0.0010	52	0.0020	77	0.0013
3	0.0016	28	0.0019	53	0.0007	78	0.0012
4	0.0013	29	0.0011	54	0.0015	79	0.0012
5	0.0009	30	0.0016	55	0.0026	80	0.0013
6	0.0007	31	0.0015	56	0.0008	81	0.0016
7	0.0018	32	0.0017	57	0.0009	82	0.0018
8	0.0015	33	0.0018	58	0.0020	83	0.0012
9	0.0024	34	0.0010	59	0.0009	84	0.0027
10	0.0020	35	0.0013	60	0.0018	85	0.0007
11	0.0010	36	0.0016	61	0.0016	86	0.0006
12	0.0016	37	0.0014	62	0.0014	87	0.0015
13	0.0022	38	0.0014	63	0.0008	88	0.0010
14	0.0015	39	0.0014	64	0.0016	89	0.0020
15	0.0009	40	0.0016	65	0.0008	90	0.0013
16	0.0012	41	0.0019	66	0.0010	91	0.0013
17	0.0016	42	0.0013	67	0.0011	92	0.0007
18	0.0009	43	0.0018	68	0.0018	93	0.0011
19	0.0006	44	0.0009	69	0.0010	94	0.0016
20	0.0011	45	0.0018	70	0.0011	95	0.0023
21	0.0013	46	0.0012	71	0.0015	96	0.0008
22	0.0005	47	0.0022	72	0.0026	97	0.0023
23	0.0018	48	0.0013	73	0.0008	98	0.0012
24	0.0016	49	0.0022	74	0.0007	99	0.0018
25	0.0012	50	0.0014	75	0.0016	100	0.0011
	0.0014						
	0.0005						

MIN	0.0005
MAX	0.0027
RANGE	0.0021
AVG	0.0014
3STDEV	0.0014

MCM Cross Section

Nominal vs. Measured

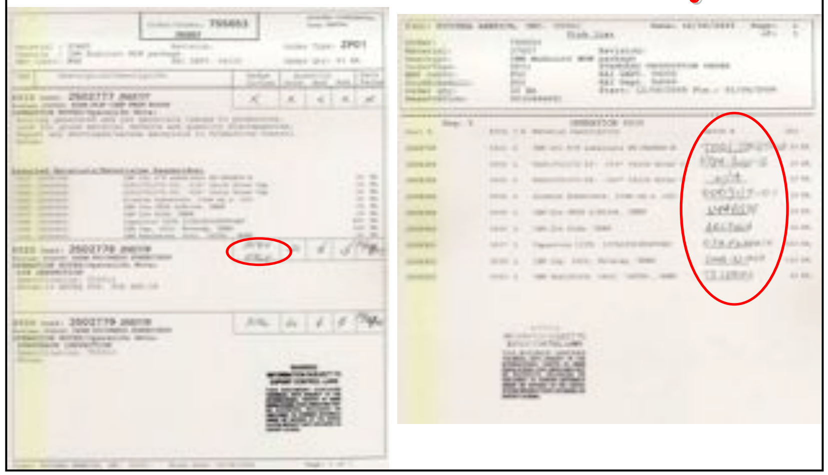


Measurements reflect dielectric thickness

Assembly Process Flow

Process	Conditions	Quality Monitor/Data
Characterize substrates	Measure Flatness	Serialize package
Components Attach, (6 Resistors, 2 Caps) Reflow	Manual Print, place Solder paste	Visual Inspection Reflow Profile
Die placement (2) LICA placement (26) Reflow	ESEC Micron 2 Belt Furnace	Flux Height , Die pull Edge bump inspection Reflow Profile
Underfill Cure	Asymtek Dispenser Oven	Underfill weight, Visual Inspection Profile
Thermal Mtl, lid attach Cure	Asymtek Dispenser Oven	Paste weight Profile
Seam Seal (Outsourced)	AuSn Reflow N_2 w/ tracer He	Program/Profile Visual Inspection Leak Check
Marking, Serialization Cure	Printex Pad marking Oven	Visual Inspection Temp. Profile
Fine Leak Test Gross Leak Test	He Bomb, Fine leak Test FLU Bomb, Gross Leak Test	Per MIL STD 883 1014
Stand-off Attach Cure	Manual epoxy disp, Place in an oven	Visual inspect Temp Profile
Final Inspect, QA, Packing	1X	Visual inspect

Lot Traveler/Traceability



Qualification

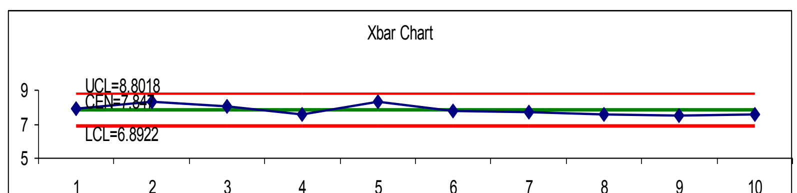
- Development & Qualification Plan (AP5011)
  - Phase 1. Underfill materials
  - Phase 2. Thermal interface/Lid seal evaluation
  - Phase 3. Material set qualification

Example of Qualification test

Test	Conditions		Sample Size
J-STD-020B L3 Preconditioning	30°C / 60% RH	192 Hours	151
Temperature Cycle	-55°C – 125°C	1000 Cycles	112
High Temperature / Humidity (HAST)	130°C / 85% RH	192 Hours	39

Inline Process Control

- Reflow Profile
- Flux height
- Paste weight
- Die pull
- Leak test

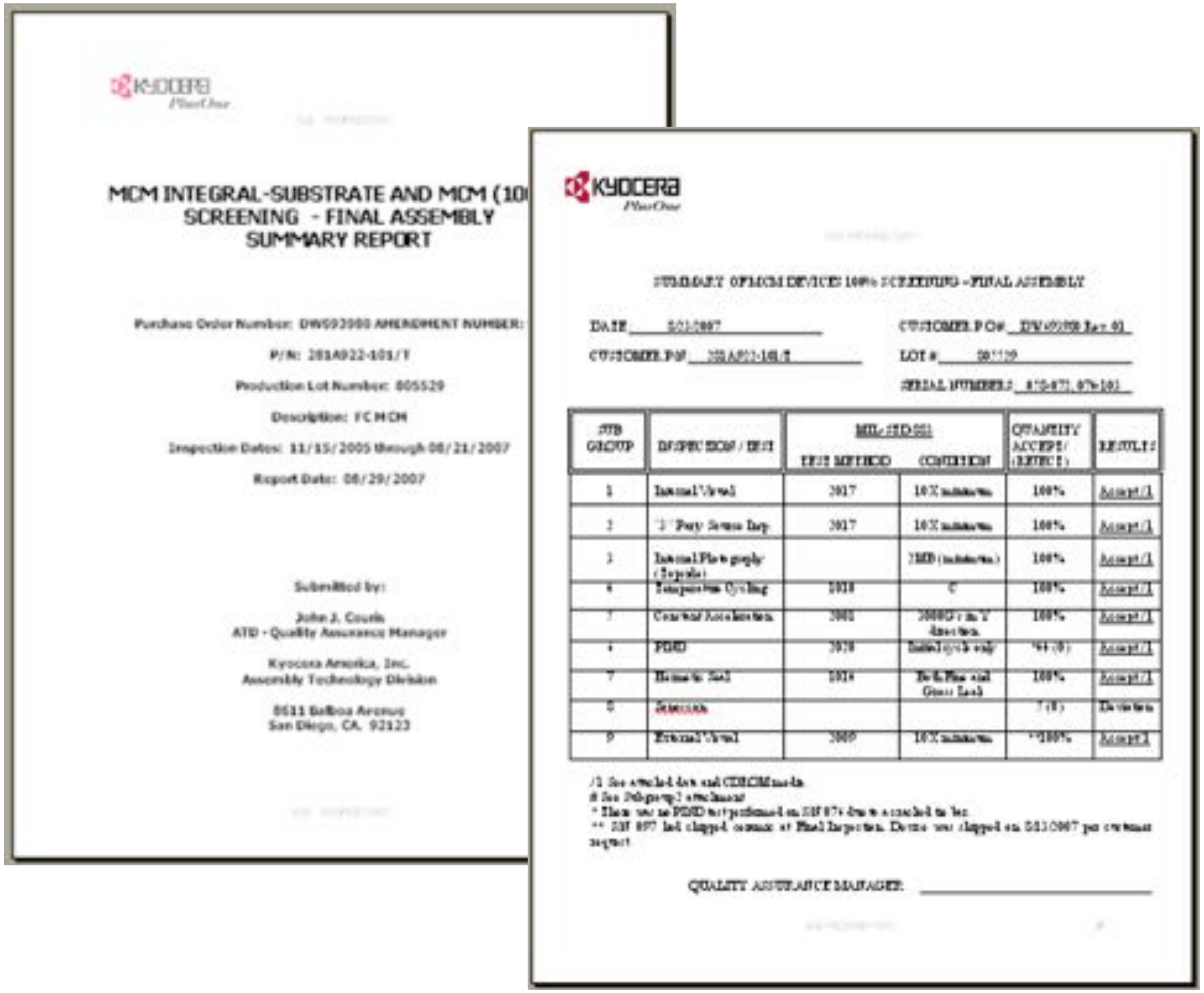


Paste height example

7. Assembly

8. Testing / Inspection / Shipping

9. Design validation



MCM INTEGRAL-SUBSTRATE AND MCM (10
SCREENING - FINAL ASSEMBLY
SUMMARY REPORT

Purchase Order Number: DW693980 AMENDMENT NUMBER:

P/N: 281A022-101/T

Production Lot Number: 805529

Description: FC MCM

Inspection Dates: 11/15/2005 through 08/21/2007

Report Date: 08/29/2007

Submitted by:

John J. Cours
ATD - Quality Assurance Manager

Kyocera America, Inc.
Assembly Technology Division

8611 Balboa Avenue
San Diego, CA 92123

SUMMARY OF MCM DEVICES 100% SCREENING - FINAL ASSEMBLY

DATE: [illegible] CUSTOMER P.O#: [illegible]

CUSTOMER P/N: [illegible] LOT #: [illegible]

SERIAL NUMBERS: [illegible]

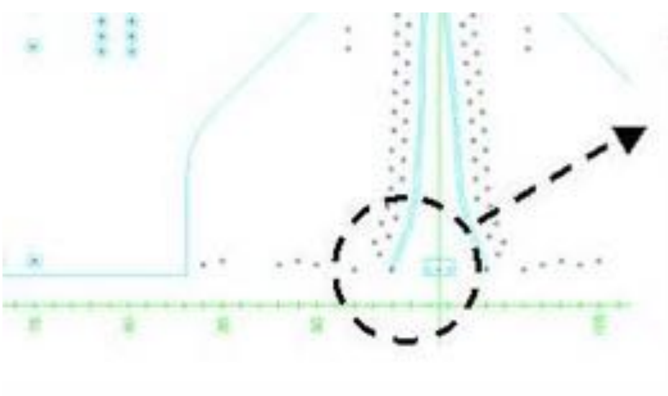
SUB GROUP	INSPECTION / TEST	MIL-STD-883 TEST METHOD	CONDITION	QUANTITY ACCEPT / (REJECT)	RESULTS
1	Internal Visual	2017	10X minimum	100%	Accept/1
2	3rd Party Source Insp	2017	10X minimum	100%	Accept/1
3	Internal Photography (Topside)		[illegible]	100%	Accept/1
4	Temperature Cycling	1010	C	100%	Accept/1
5	Constant Acceleration	2001	[illegible] direction	100%	Accept/1
6	PIND	[illegible]	[illegible]	[illegible]	Accept/1
7	Hermetic Seal	1014	Both Fine and Gross Leak	100%	Accept/1
8	[illegible]			[illegible]	Deviation
9	External Visual	2009	10X minimum	**100%	Accept/1

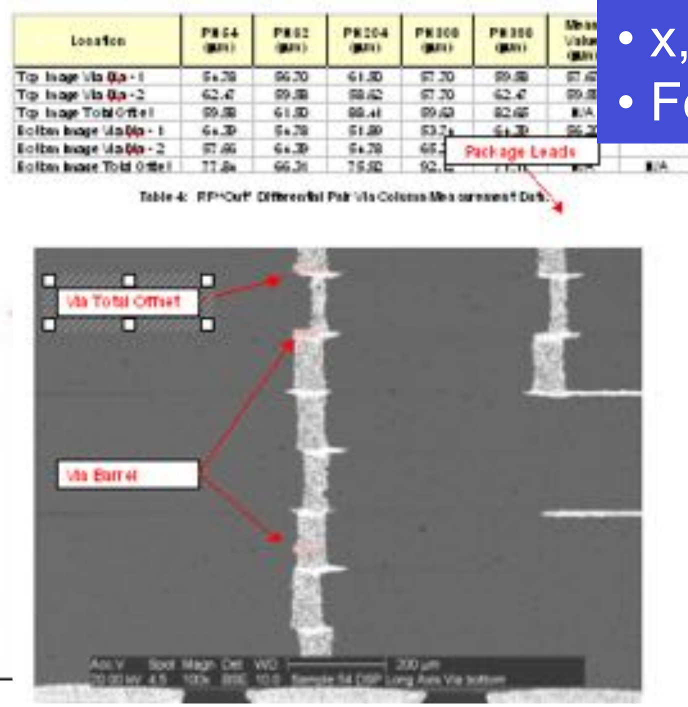
QUALITY ASSURANCE MANAGER: ______

- Standard pkg
- Environmental
- Shock/Vibe
- Thermal

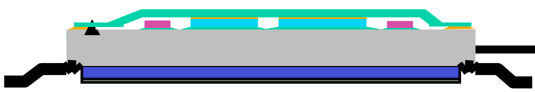
9. Design validation

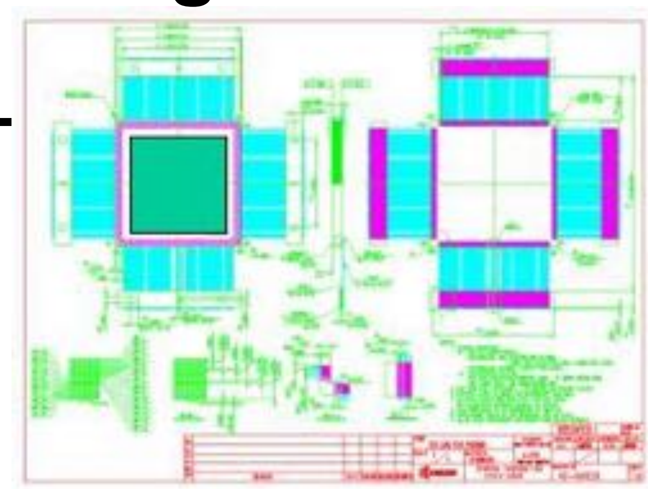
- SEM
- Manual
- x, y, z measurements
- Feedback to design

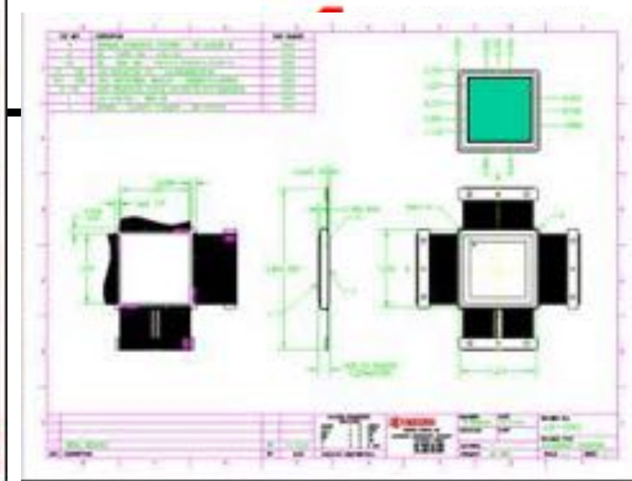


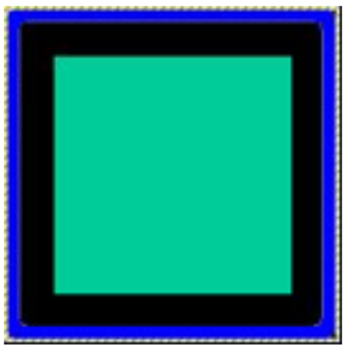


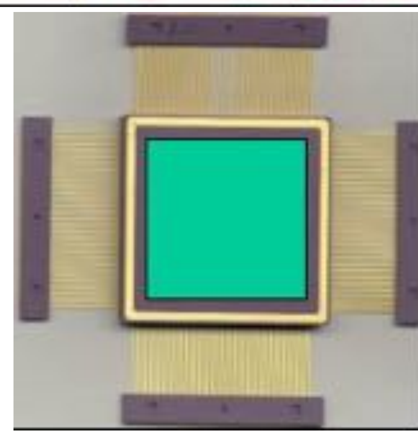
Complete Package Solution

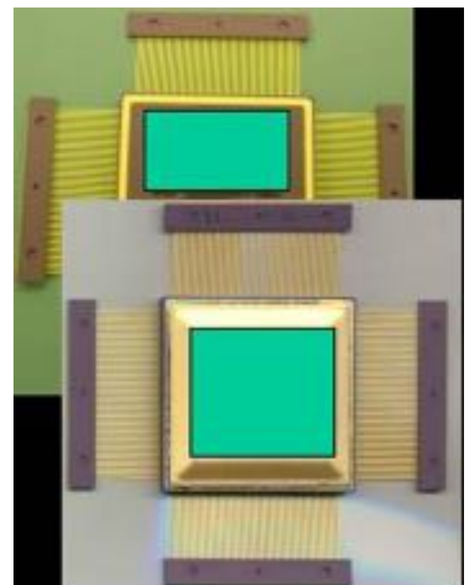


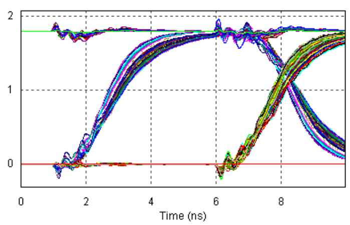












Concept

Package

Assembly

Conclusions

- Space applications require "extreme reliability"
- At the same time, the choice of design and materials may be informed by:
  - Size, Weight
  - Performance
  - Cost
  - Other program requirements