Wafer-level Packaging (WLP) Reliability and Stress Driven Failure Modes

Kaysar Rahim
Northrop Grumman Corporation
md.rahim@ngc.com

Abstract:

Wafer-Level Packages (WLP) offers an excellent solution to meet the growing demand for small, thin, and fast electronic products. Due to its low cost and high performance, WLP has a strong position in the handheld and mobile electronic system applications. However, the Fan-in/Fan-out WLP technologies shows a growing interest in the aerospace and defense applications. Thermo-mechanic reliability of WLP remains a major challenge for higher I/O and larger die in the support of Defense and Aerospace electronic systems. In this work, we provide a comprehensive overview of WLP based on stress test's driven reliability, associate's failure modes, detailed physics of failures, and fundamentals of board level failure mechanism.

Outlines:

- Overview of Wafer-level Packaging (WLP)
- Physics of Failures and Board-level Interconnects Stress Fundamentals
- Stress Test’s Drive Failure Modes
- Board Level Reliability Improvements
- Summary