Electronics Packaging: Fundamentals and Opportunities

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Class time (0800-1600 hrs)

COURSE SUMMARY

This course is intended to provide an overview to the many disciplines within electronics packaging. It will describe all aspects of interconnects starting with the silicon device down to the final product as well as the needs for environmental testing and reliability assessments. An overview on the current state of the industry will be included.

The topics included in this course will be selected from the following:

1. Introduction to packaging
   - Introduces the attendees to packaging and provides an overview of how the lectures are related to familiar applications such as a smart-phones, tablets, wearable devices, etc.
2. Semiconductor technologies and packaging
   - Reviews silicon packaging, describes the structure of a silicon device, materials used and various backend of line features that provide different interconnect options
   - Basic fabrication techniques for silicon-based packaging including lithographic patterning, thin film metal deposition, electro-plating, dielectric materials, and more
3. Packaging materials
   - Reviews the various materials used in packaging, including polymers, ceramics, metals, and solders
4. Chip carrier level packaging
   - Covers wirebond packages, flip chip packages and advances in packages including fan-out and wafer level packages
5. Mechanical analysis and test for package reliability
   - Understand the need for mechanical analysis, need for FEA, mechanical stress on interconnect reliability and the interaction of CTE in packaging materials
6. PCB design fundamentals and fabrication processes
   - Describes the design fundamentals of a PCB, including the layup of a PCB cross section, copper roughness, spread weave cloth for high data rate transmission. Covers what can go wrong in a PCB, the dangers of thin dielectric for power planes, contamination, process defects including fiber fracture, copper wicking and others as they relate to product failures
7. Card and board assembly
   - Reviews the different steps of an SMT process, discusses the need for different solder composition and solder processes and includes smart manufacturing and industry 4.0 with respect to electronics assembly
8. Flexible and hybrid electronics
   - Design, materials, processing, additive manufacturing approaches and assembly of flexible hybrid electronics along with an overview of applications to medical and industrial

devices

9. Reliability of electronics packages
   - What can go wrong, how do we catch defects, how does the environment affect electronic assemblies. How do we test and what does the data mean?
10. Recent advances in electronic packaging
    - Describes the drivers for the industry, including challenges and opportunities

INSTRUCTOR BIOS

Mark D. Poliks, Ph.D. Ph.D. is a SUNY Distinguished Professor and Empire Innovation Professor in Systems Science and Industrial Engineering and Materials Science and Engineering at the State University of New York at Binghamton. He is the director of the Center for Advanced Microelectronics Manufacturing (CAMM), a New York State Center of Advanced Technology and home to the New York Node of NextFlex. He serves as Chair of the Smart Energy Transdisciplinary Area of Excellence at the Binghamton campus. His research is in the areas of industry relevant topics that include high performance electronics packaging, flexible hybrid electronics, medical and industrial sensors, printed RF components, materials, processing, aerosol jet printing, roll-to-roll manufacturing, in-line quality control and reliability of electronics. He is the recipient of the SUNY Chancellor's Award for Excellence in Research. He received FLEXI awards for leadership in Technology and Education from the FlexTech Alliance in 2009 and 2019, he is Fellow of NextFlex Manufacturing USA. Poliks has had significant experience working in the electronics industry, he was a senior technical manager at the IBM Corporation and at Endicott Interconnect Technologies, Inc. He is an active member of IEEE, serves on the board of governors and as a distinguished lecturer of the IEEE Electronics Packaging Society, he was General Chair of the 69th ECTC. He has authored over one hundred fifty technical papers and holds forty-eight US patents.

Benson Chan is the Associate Director for the Integrated Electronics Engineering Center (IEEC), a New York State Center for Advanced Technology at Binghamton University, with a mission to work with companies to understand their use of electronics to improve their business by understanding the design, reliability, and failure analysis of their products. He received his B.S. in Mechanical Engineering in 1981 and M.S. in Engineering Science in 1987 from Rensselaer Polytechnic Institute. Mr. Chan has solid background in electronics packaging, with emphasis in high-speed applications and Electrical Connector design. He had a diverse career with IBM for 22 years in the areas of process and design engineering. His work experience provides the perspective on the history of packaging from PCB manufacturing to assembly to supercomputer design and fabrication. He is an iMAPS Fellow, IEEE Senior Member, IEEE EPS Board of Governors, IEEE EPS Emerging Technology TC Chair, IEEE EPS Binghamton Chair and iMAPS Empire Chapter President.