AN INTEGRATED WORKFLOW FOR SEMICONDUCTOR PACKAGE DESIGN

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CMSE

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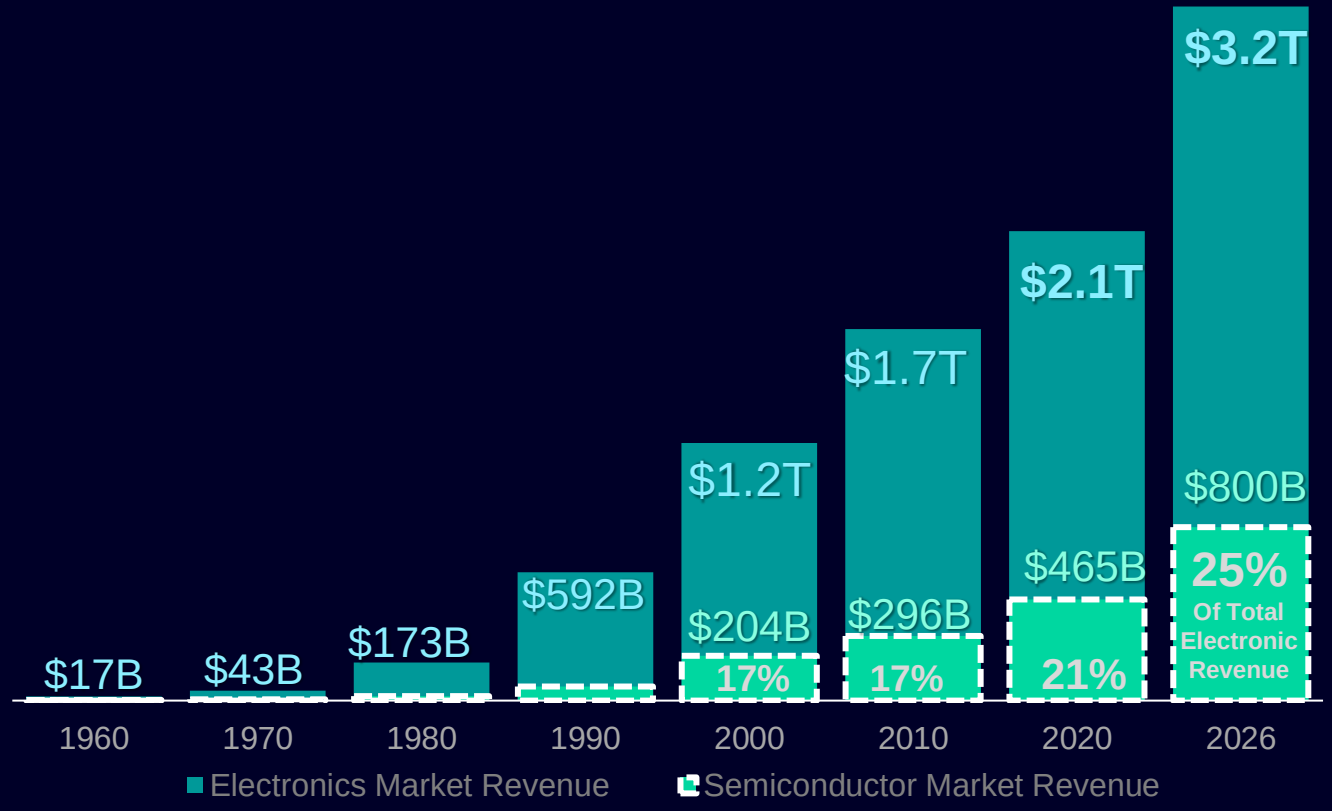
Increasing Semiconductor Content in Electronics Systems

Tightly linked to future Electronics growth areas



Source: VLSI Research, September 2021

The increasing amount of semiconductor content in electronic systems is enabling innovation and driving system value growth

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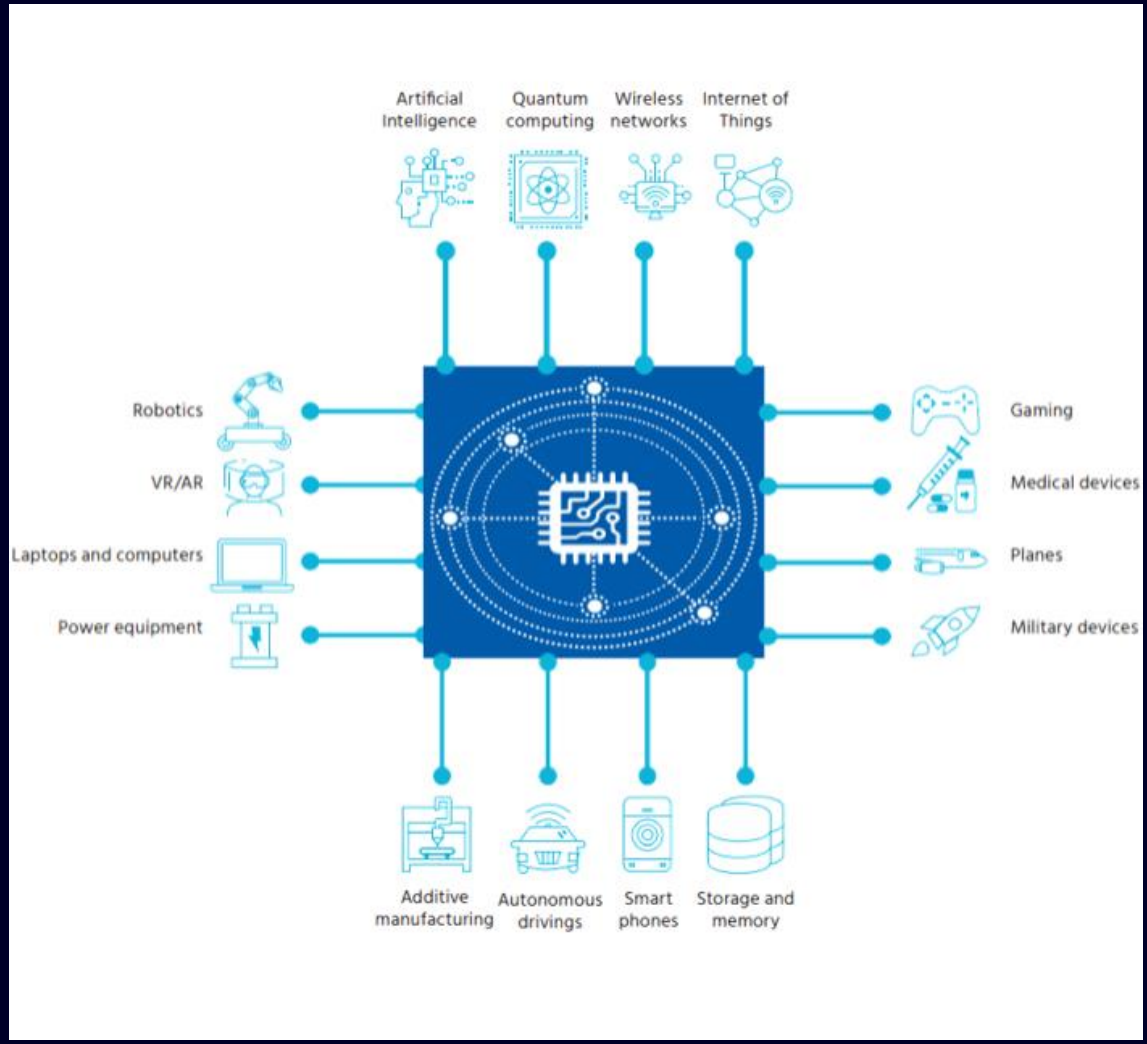
Current Market Drivers in Electronics

- 5G wireless network deployment will see major footprint in cars´ connectivity
- Renewables faces governments´ focus with the new climate agreements
- The slow adoption of electric vehicles is facing a turnaround
- Businesses using IoT technologies from 13 % in 2014 to 25 % in 2020
- AI/ML applications are increasing needs for HPC



Consumption of semiconductors per person in China:
$16.72 per person in 2010
$85.22 in 2020 (+5.10X) (IBS)

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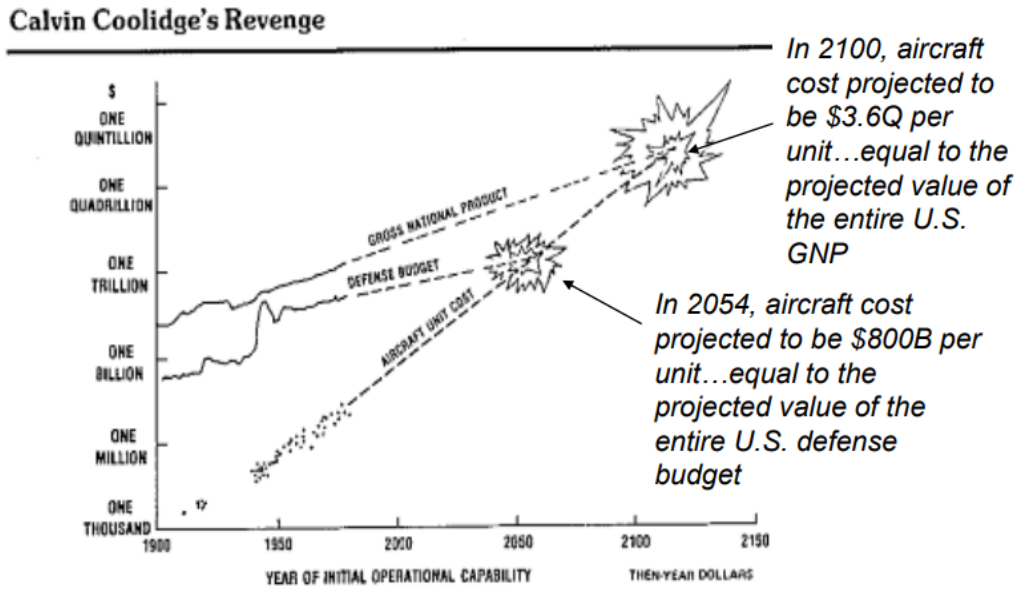
Learning from other industries

"In the year 2054, the entire defence budget will purchase just one aircraft."

- If the U.S. defense budget grows by 2.5% per year…
- If nominal gross national product grows by 5.5% per year….



Integrate, then build!

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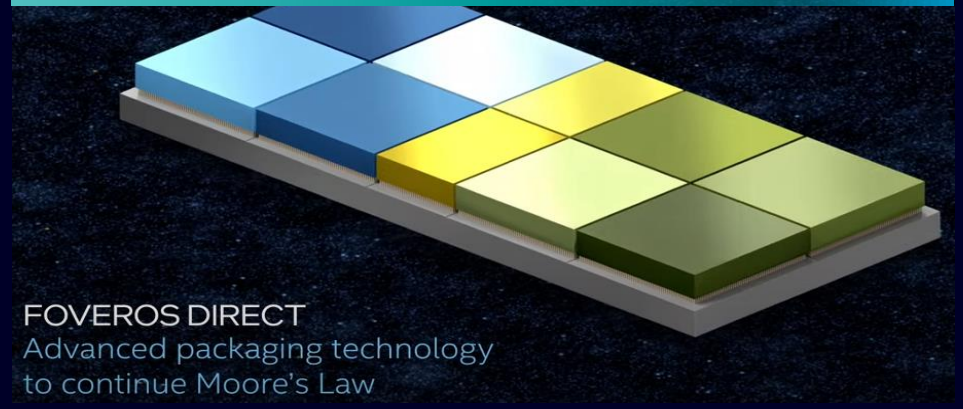
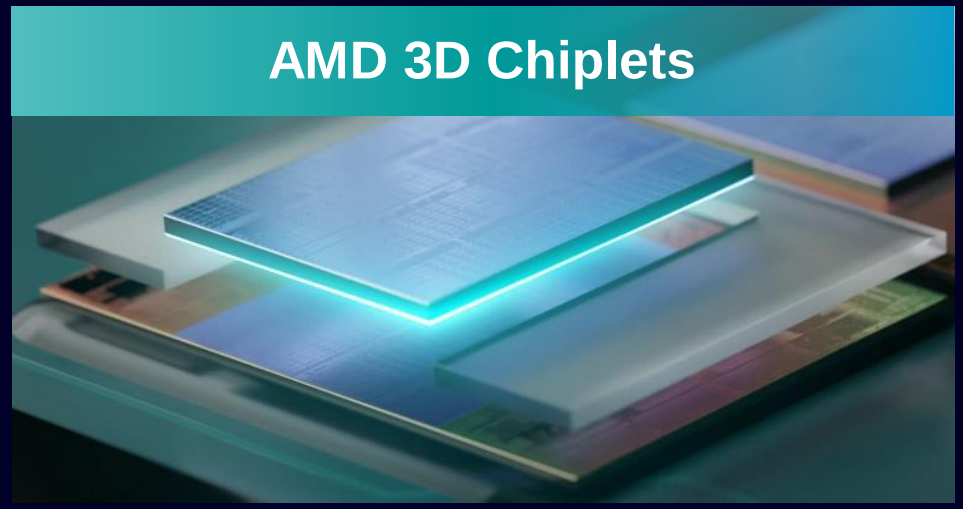
Getting More out of Moore's Law
with High Density Advanced Packaging

Intel Foveros Direct



TSMC 3D Fabric

AMD 3D Chiplets



New Protocols

Universal Chiplet Interconnect Express

Building an open ecosystem of chiplets for on-package innovations

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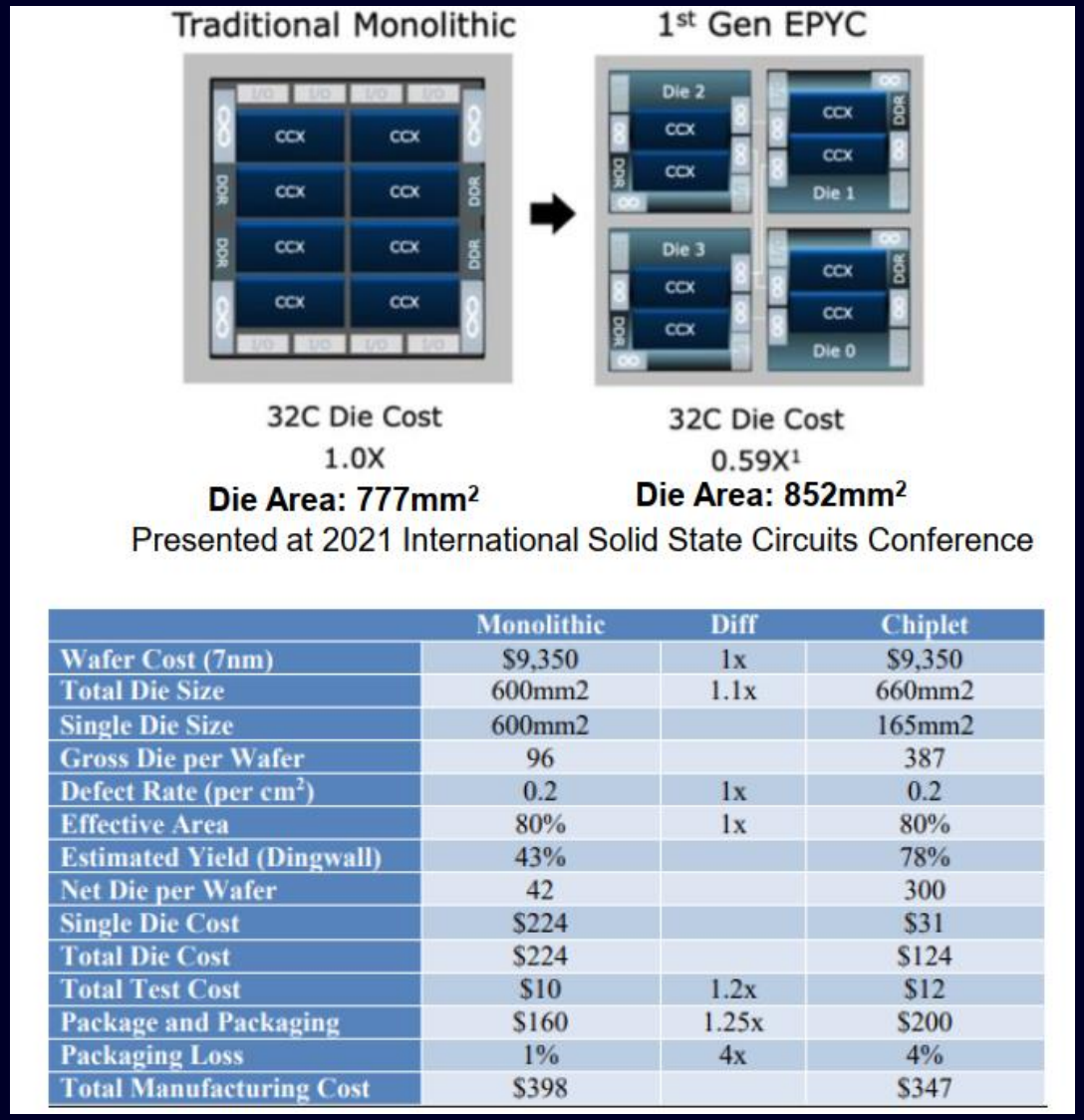
Why Disaggregation?

AMD Case Study:

- 41% reduction in die cost with 10% area increase
- Higher Yield by using smaller die
- Increases peak compute performance
- Optimize process to IP Blocks
  - No benefit from scaling IO, analog
- Maximize platform value – product configurability from single tape out

Expanding/evolving eco-system increasing availability of technology:

- UCIe – Universal Chiplet Interconnect Express
- Intel IDM 2.0
- Turn-key design/build resources – Chipletz, Wavious



	Monolithic	Diff	Chiplet
Wafer Cost (7nm)	$9,350	1x	$9,350
Total Die Size	600mm2	1.1x	660mm2
Single Die Size	600mm2		165mm2
Gross Die per Wafer	96		387
Defect Rate (per cm²)	0.2	1x	0.2
Effective Area	80%	1x	80%
Estimated Yield (Dingwall)	43%		78%
Net Die per Wafer	42		300
Single Die Cost	$224		$31
Total Die Cost	$224		$124
Total Test Cost	$10	1.2x	$12
Package and Packaging	$160	1.25x	$200
Packaging Loss	1%	4x	4%
Total Manufacturing Cost	$398		$347

Source: Linley Report

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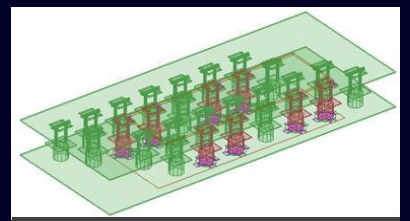
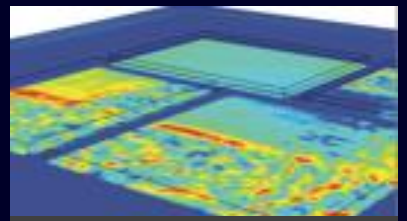
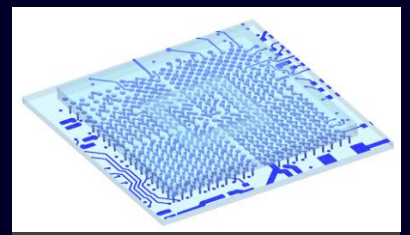
New Challenges Presented by New Frontiers



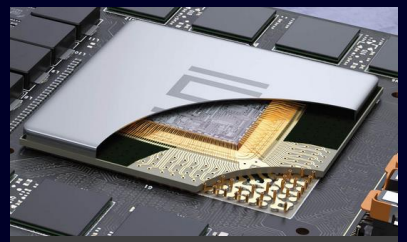
Power Delivery



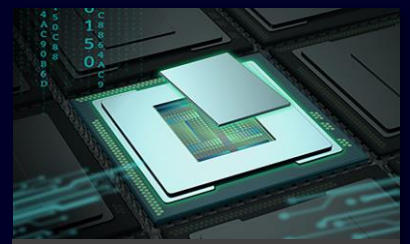
Thermals



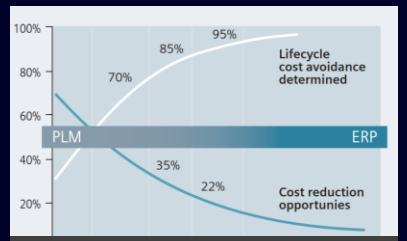
Mechanical Stress



Material Characterization

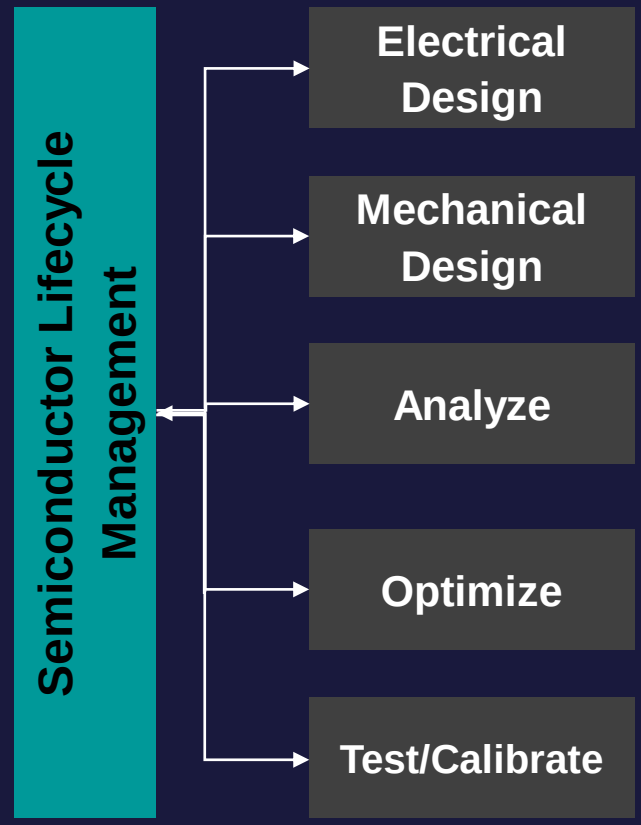


System Integration



Lifecycle Management

Siemens High Density Advanced Packaging Workflow



End to end toolchain

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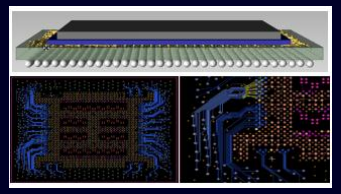
Integrated Electronics and Semiconductor Design Workflow providing end-to-end integration

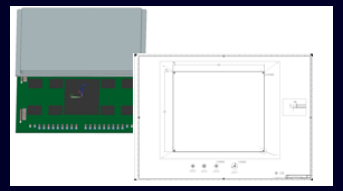
Semiconductor Lifecycle Management

Electrical Design



- Rapid Development of ‘what-if’ prototypes
- Enables system connectivity viewing and management without error-prone spreadsheets
- Flexible multi-direction flow for die, package or PCB- driven optimization

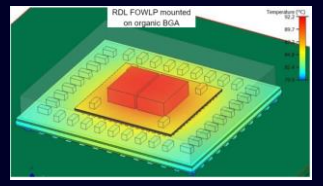
Mechanical Design



- MCAD/ECAD Collaboration workflow
- 2D/3D clearance checking
- Characterize materials for simulation
- Advanced modeling, surfacing, and drafting capabilities

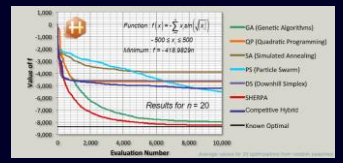
Analyze

Electrical, Thermal, & Mechanical Analysis



- Comprehensive die and package level extraction
- Detailed thermal modeling from die to system level
- Stress analysis to identify unexpected stressors impacting performance

Optimize



- SHERPA, proprietary design optimization algorithm
- Explore the multimodal design space at unparalleled efficiency
- Continuous product improvement

Test/Calibrate

- Non-Destructive test
- Ability to predict infant mortality and future failures
- Integrated into original thermal model to update assumptions
- Assure Quality

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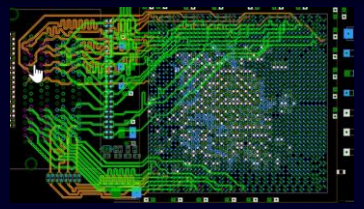
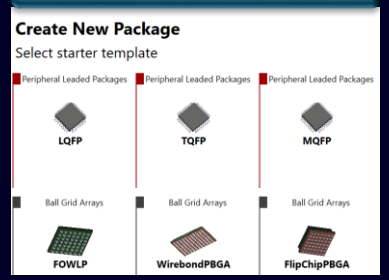
Thermal – Mechanical Workflow

ECAD

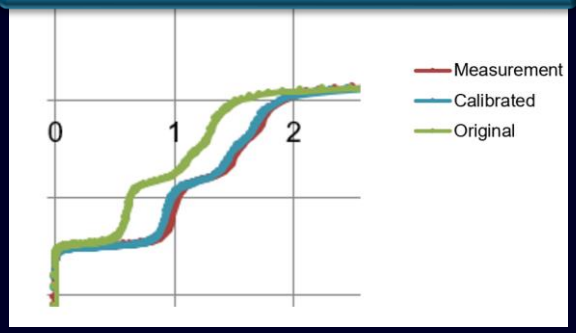


EDA Bridge

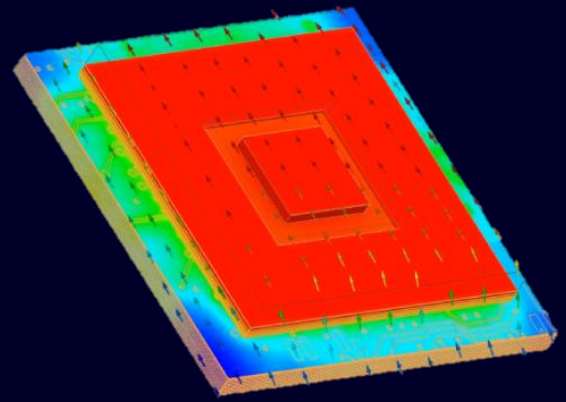
Package Creator



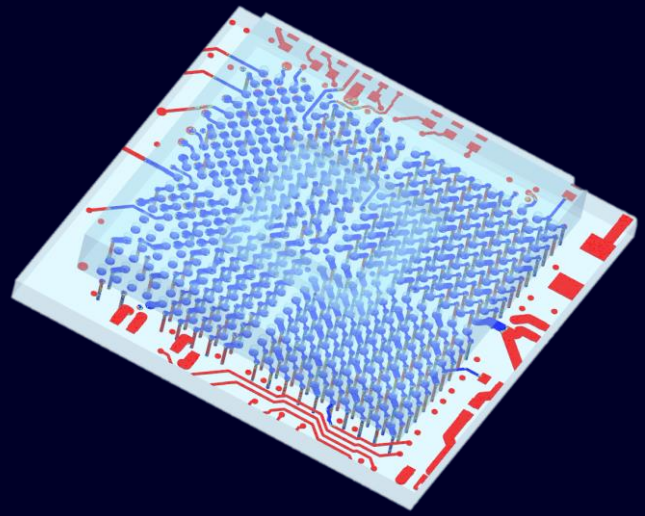
Structure Function Calibration



Thermal Simulation



Creep and Fatigue



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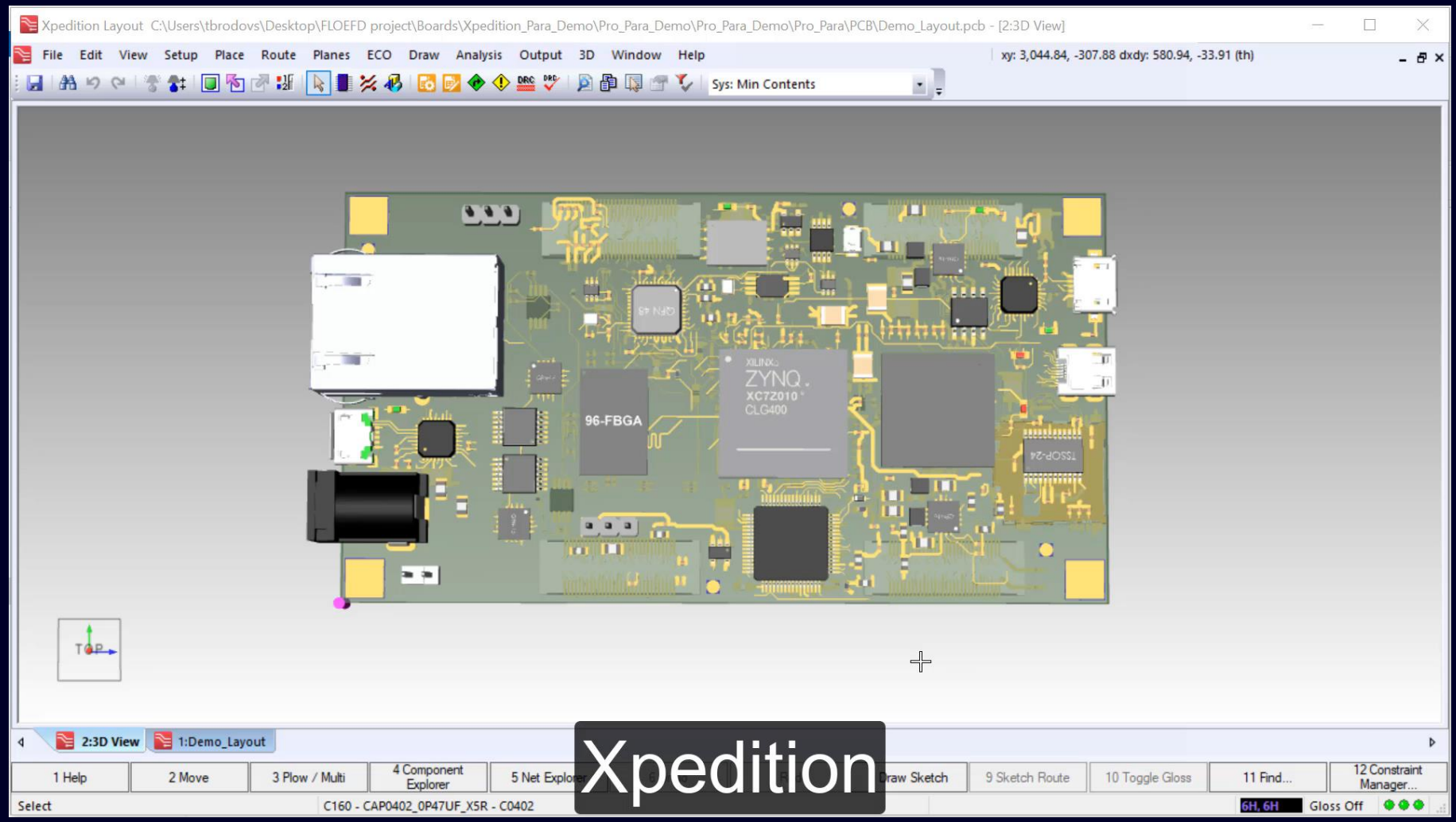
ECAD to MCAD



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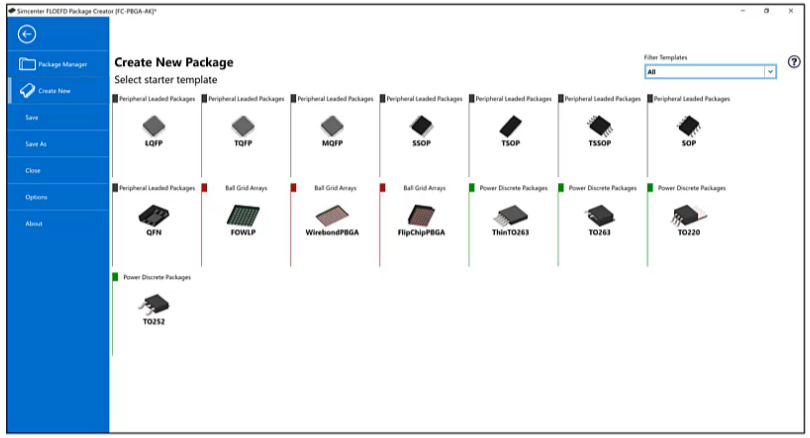
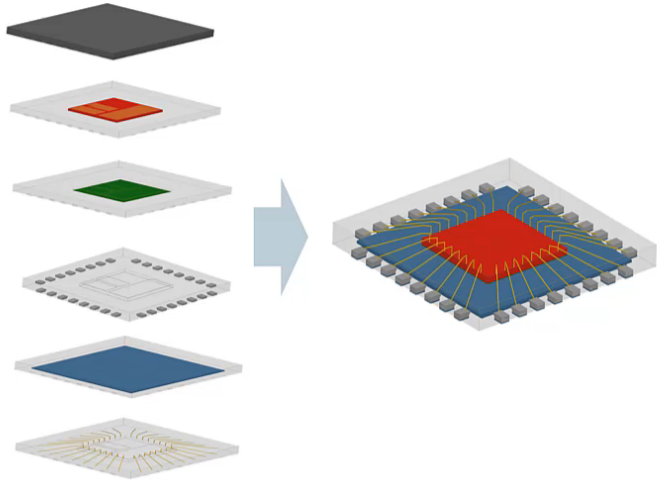
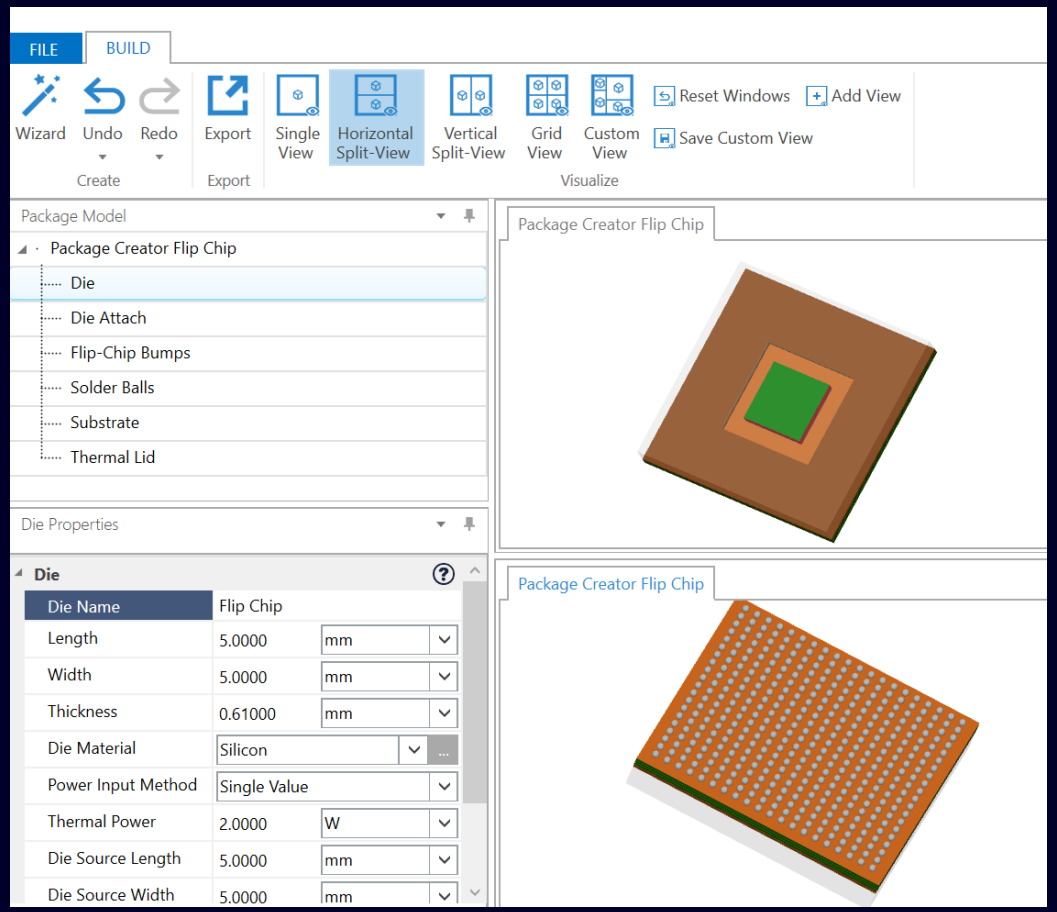
Package Creator

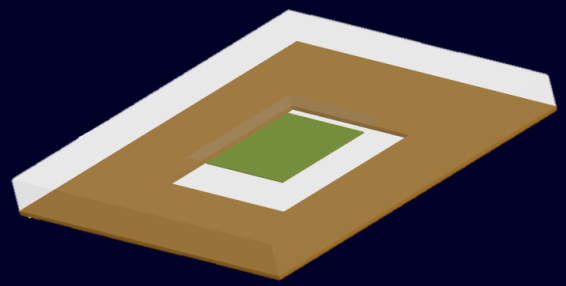
A tool that specializes in the rapid creation of thermal models of electronic packages for use in Simcenter FLOEFD.



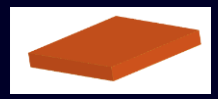


Package Creator – Flip Chip

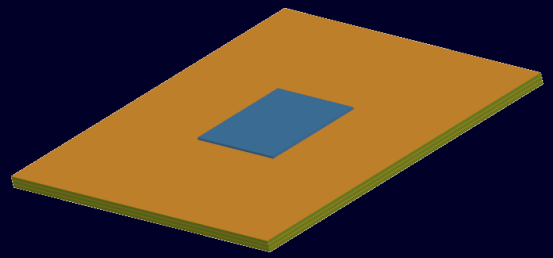




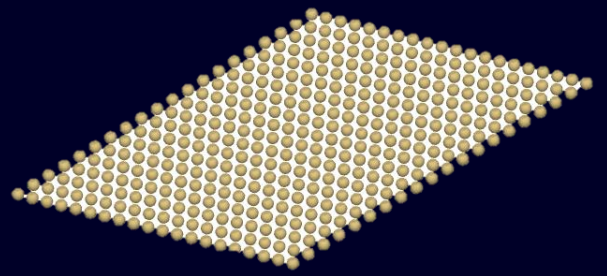
Lid and Die Attach



Die



FC Bumps and Substrate



400 Solder Balls

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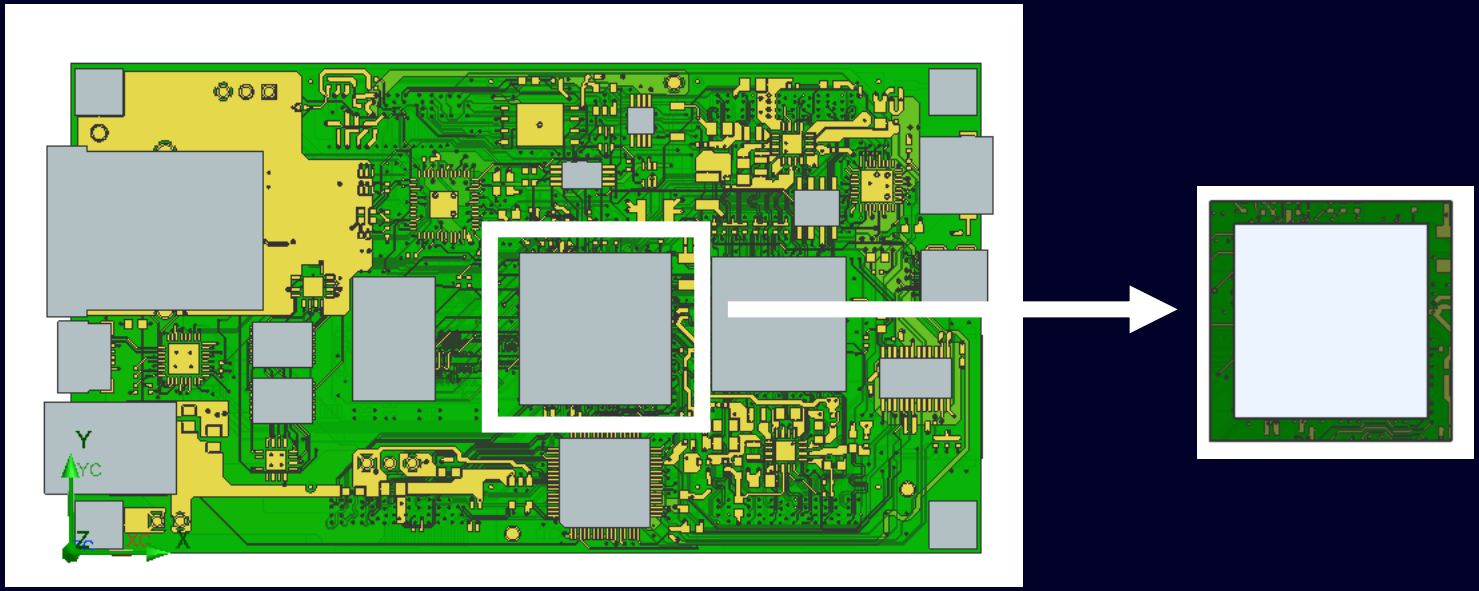
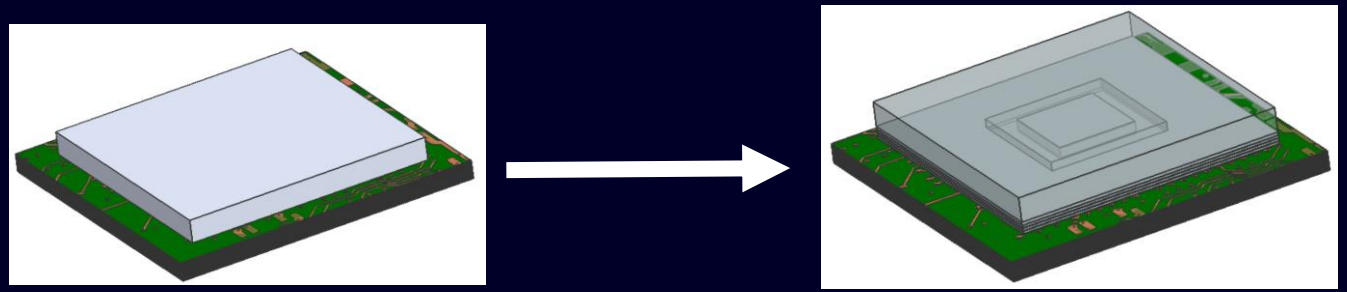
Cutting PCB



Swapping package with Flip Chip from Package Creator



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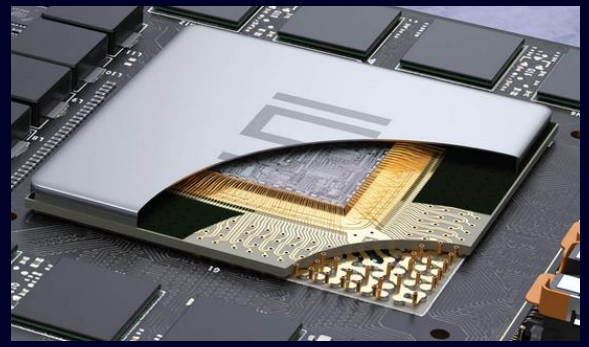
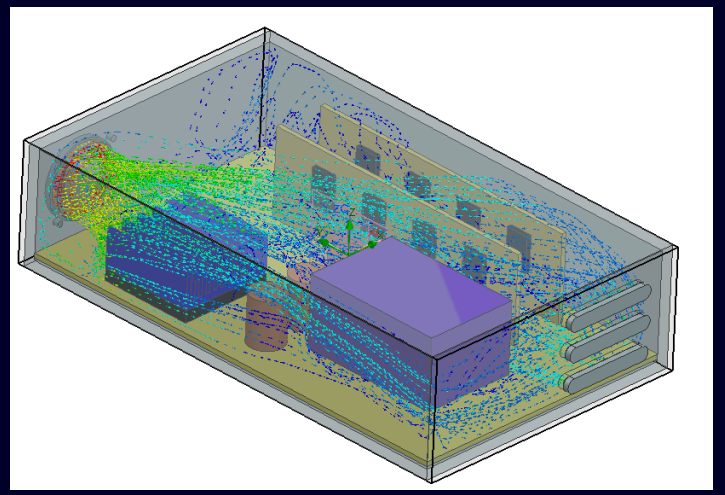
Simulation properties accurate?

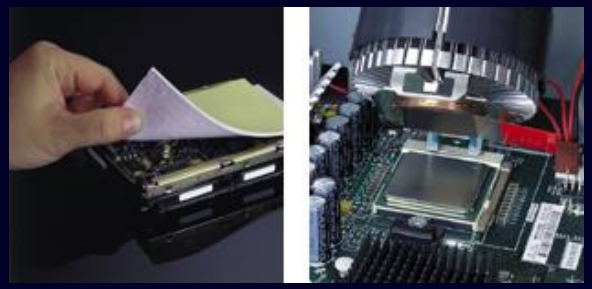
- Thermal resistances
- Material Thermal Conductivity
- Material Specific Heat
- Die Size
- Etc.



Confirm with hardware test data

Confidence in results





Testing thermal interface material. Is the expensive stuff worth the extra $? Is enough applied?

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Measuring the thermal performance

Static test method (JEDEC JESD 51-1 standard)

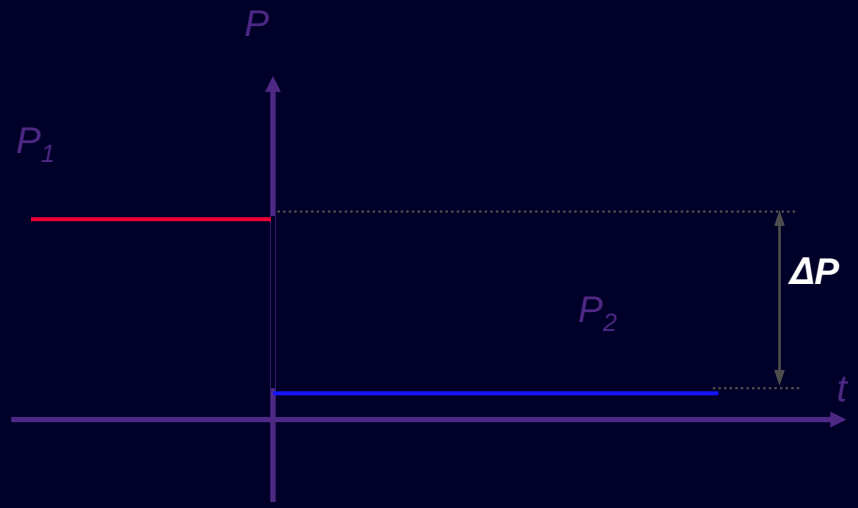
Measurement of P-N junction thermal response using forward Voltage

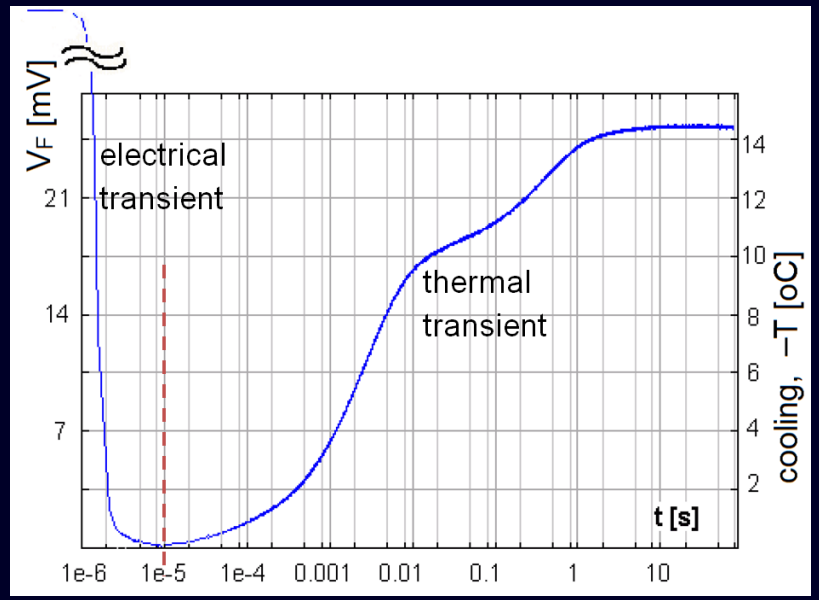
Very fast switching between heating and sensing states

Fast measurement at “junction” (~1µs)

Resolution: 0.01ºC in practice

Uses 4-wire setup (Kelvin setup)





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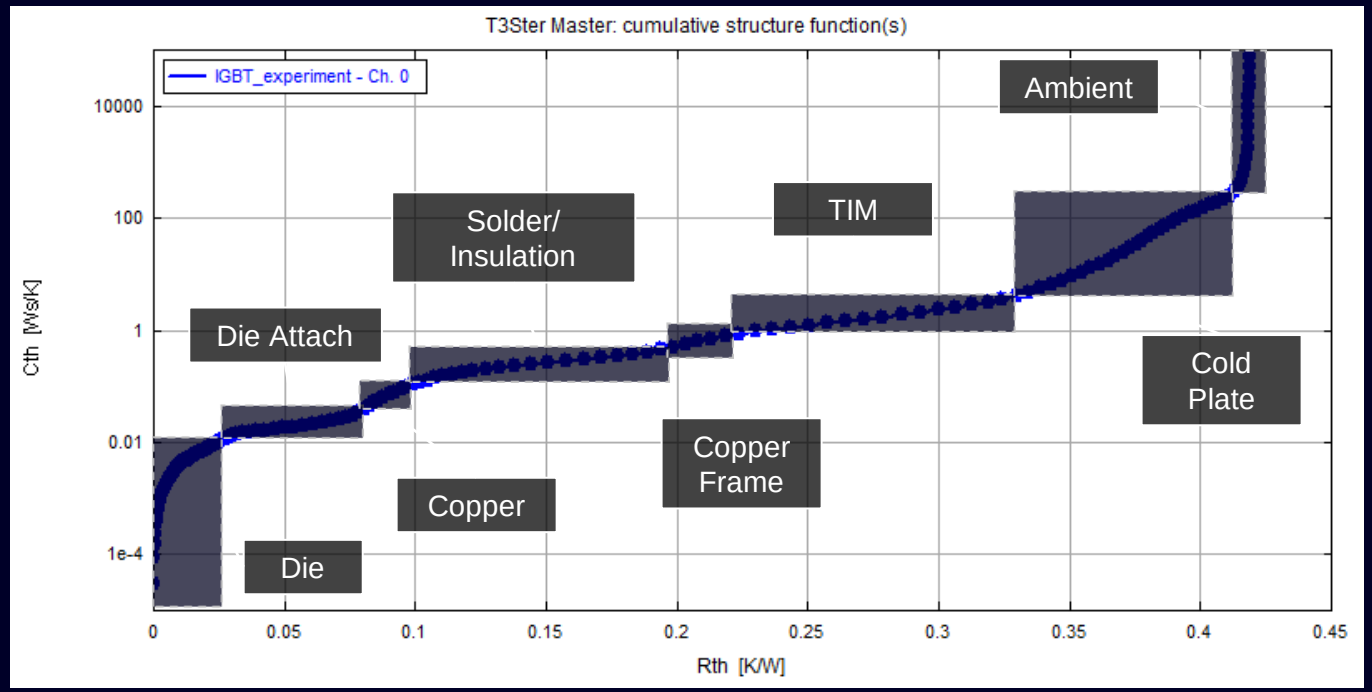
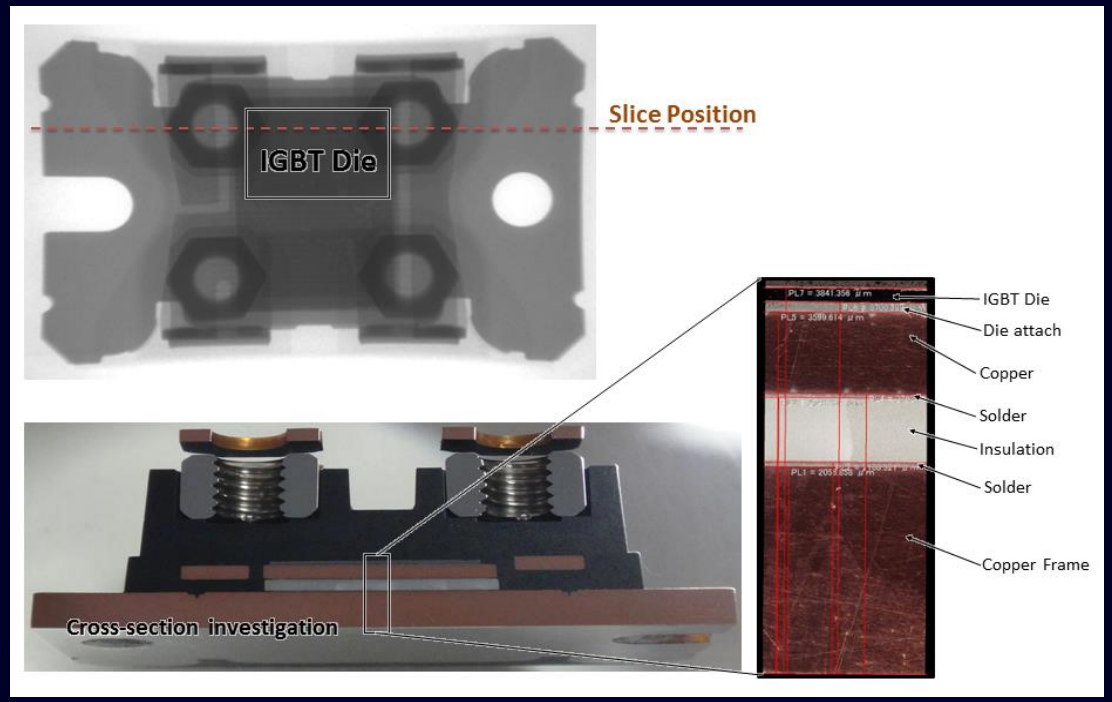
Cumulative Structure Function

- Each section of the Structure Function path represents physical objects the heat encounters. There is a correlation between physical objects and sections of the RC path.





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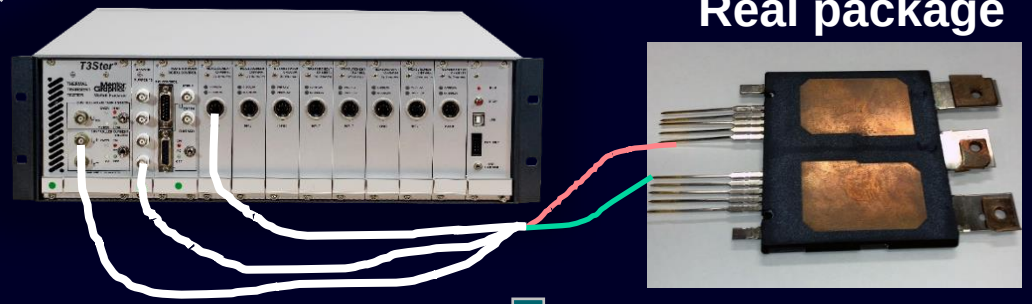
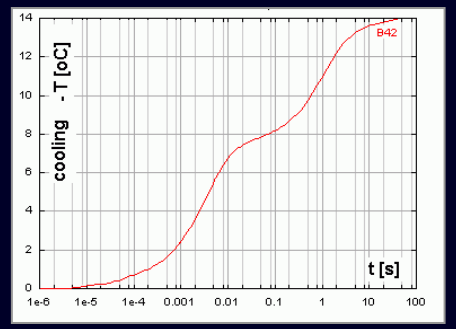
How Simulation and Test Support Each Other

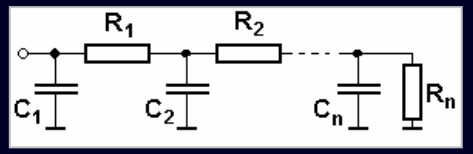
Real package



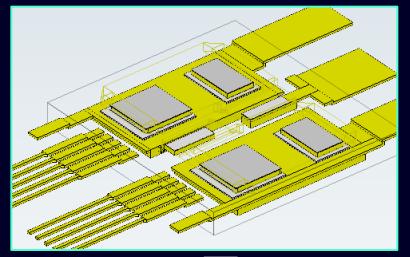
Thermal transient measurement



Test based compact model (for single die components only)

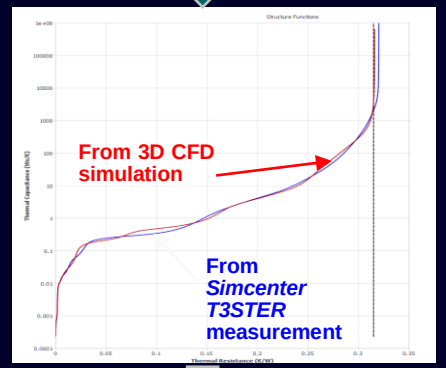


Model to validate



CFD

Simulated thermal transient



Structure functions for structural analysis and validation of detailed models

Validated detailed model
Possibility to create Reduced Order Model
Functional Mock-Up

System Simulation

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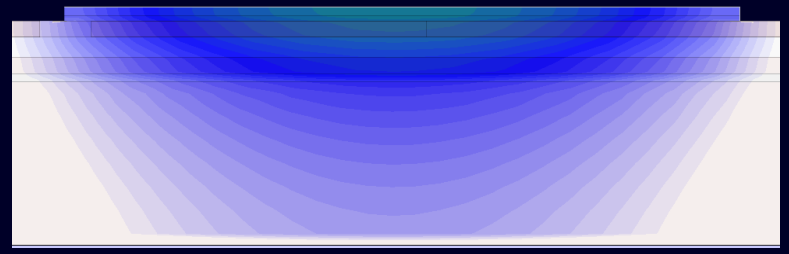
Calibrated Simulation Models based on Simcenter T3STER Measurement Motivation

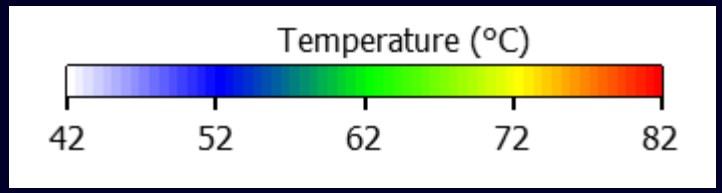
Using thermal design models calibrated against transient measurement leads to shorter design cycles

An un-calibrated model leads to:

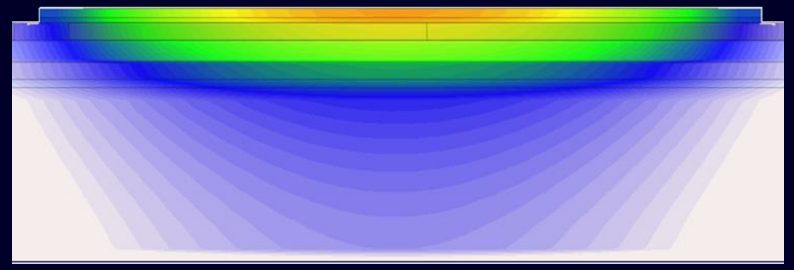
- **Overdesign**
  - where the model's inaccuracy is recognized
- **Underdesign**
  - where it is not, resulting in more field failures
- **Longer design cycles**
  - due to first physical prototypes performing differently to expectation

Uncalibrated





Calibrated



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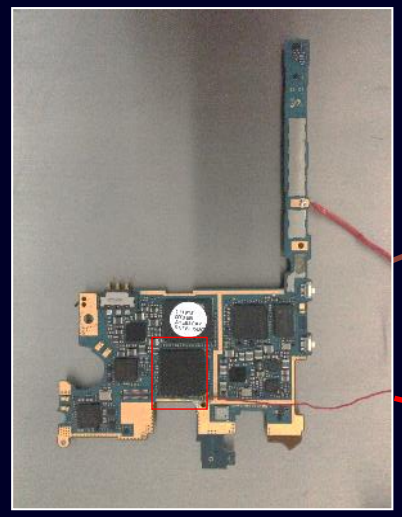
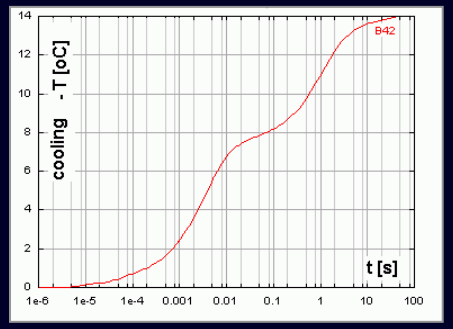
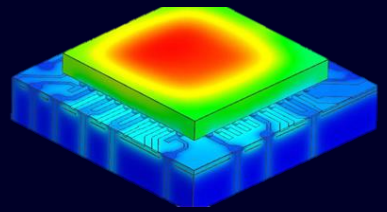
Calibration and BCI ROM workflow



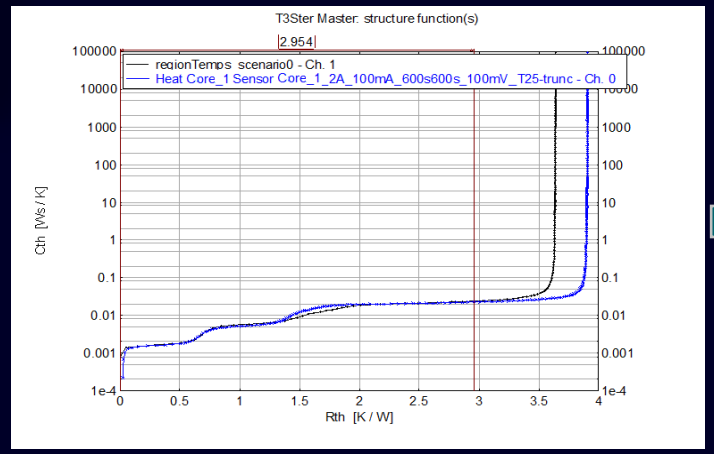
Real package



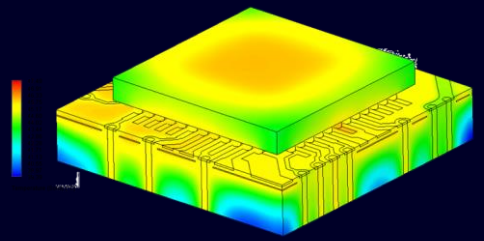
Structure Function



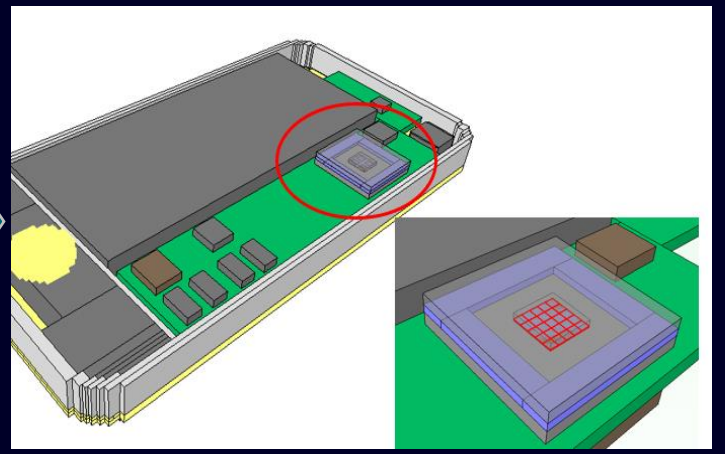
Package model from Vendor



Match structure functions during calibration



Calibrated model



System level model with die power map

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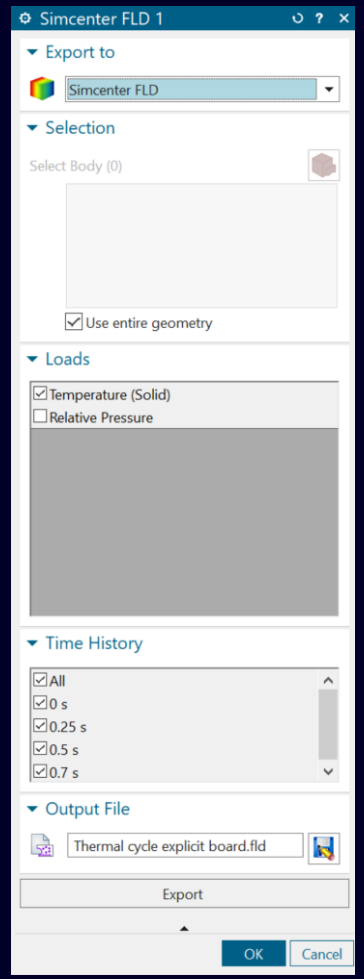
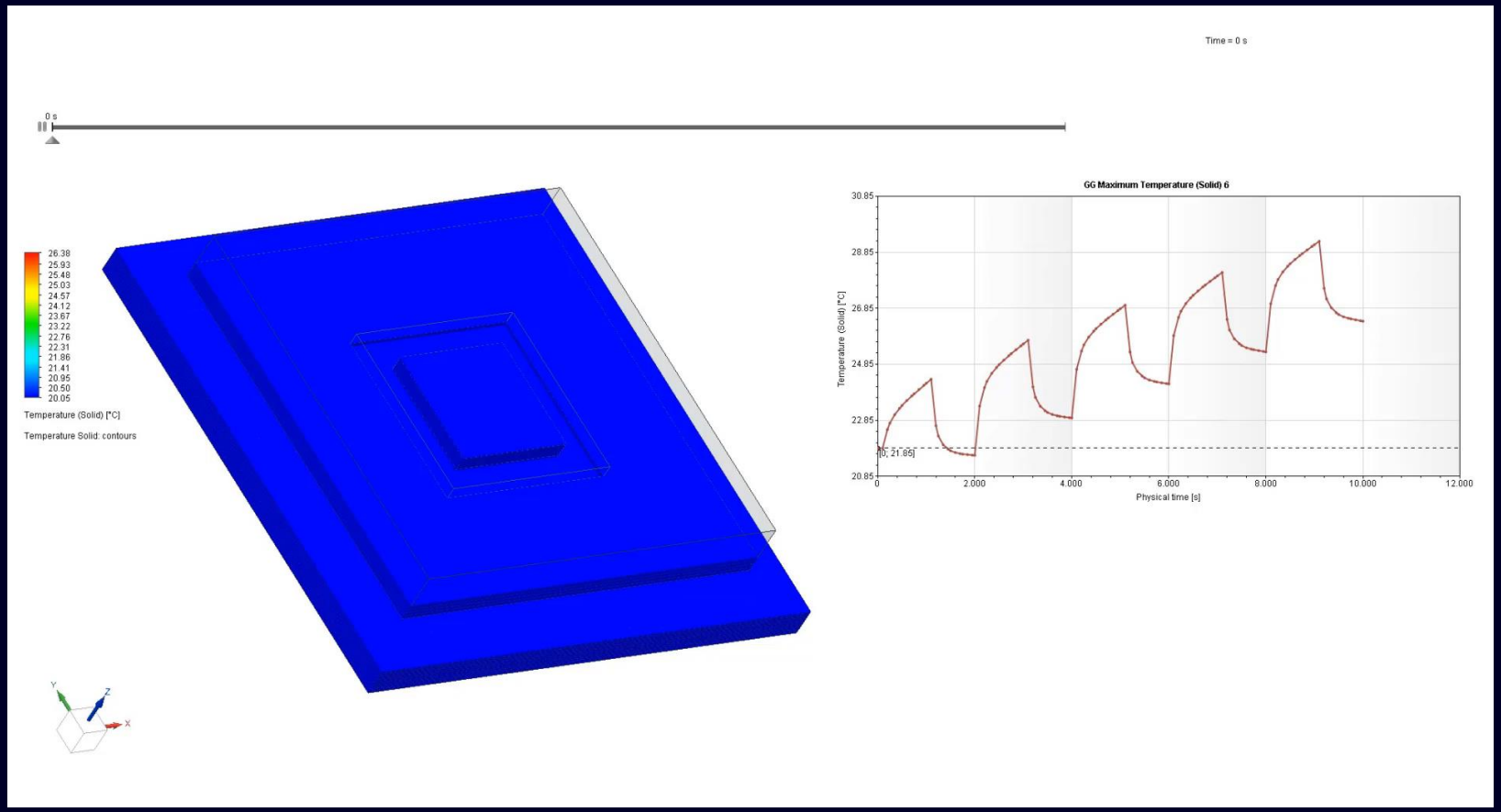
Export Temperature from Simcenter FLOEFD to Field Text Format (FLD)





- Simcenter FLOEFD can export time dependent temperature data to Simcenter 3D as a data field using the field (FLD) format to store steady state or transient temperature fields.

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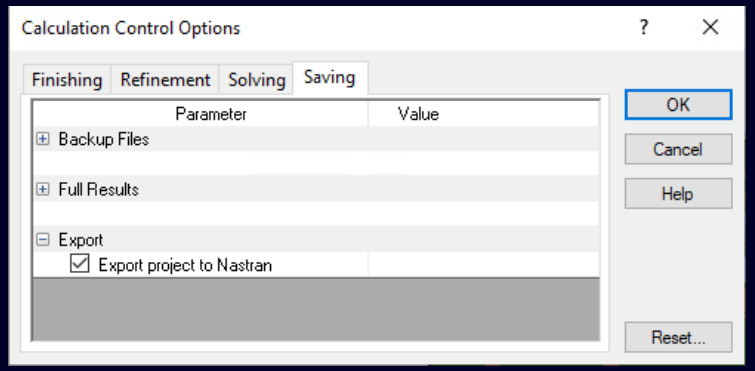
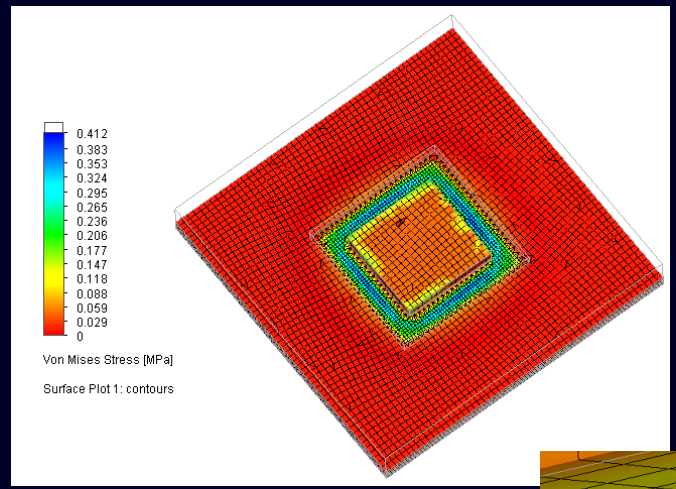
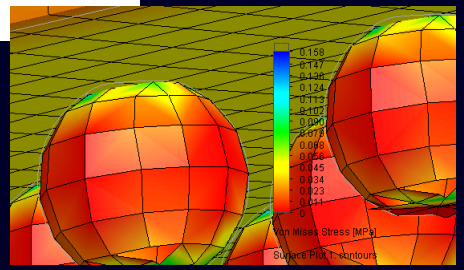
Structural Simulation in Simcenter FLOEFD

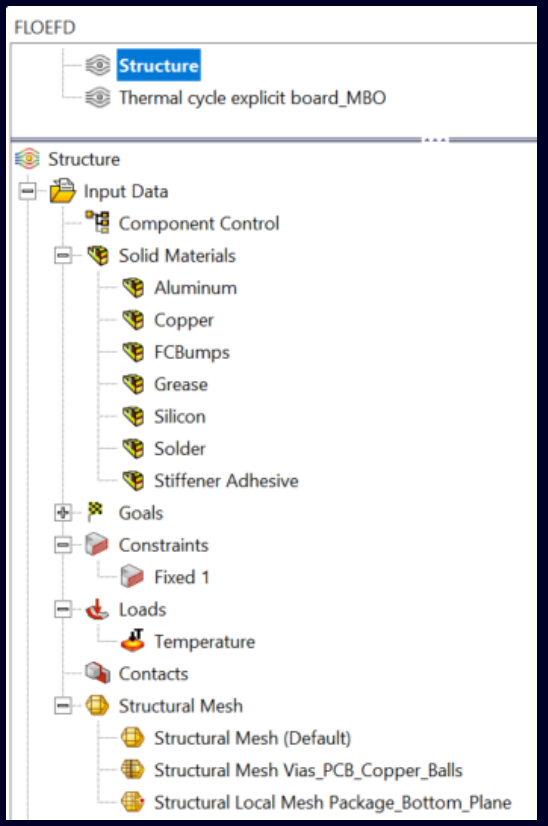
- A structural analysis project can be exported to a **Nastran file**. **Automatically created hex-dominant mesh**, materials, glue contacts, constraints and loads (constant values or transferred from another calculation) can be exported. Export to Nastran option requires a calculation to be run. *dat file is created as an addition result.

- Mesh settings - 3 min
- Mesh generation - 8 min









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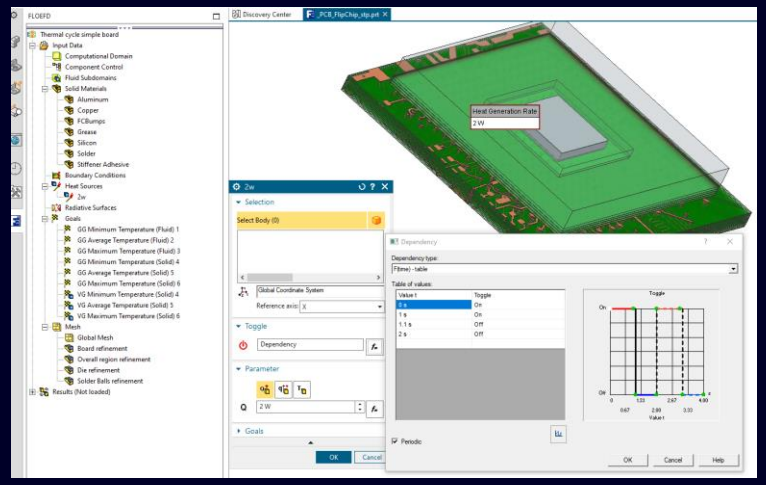
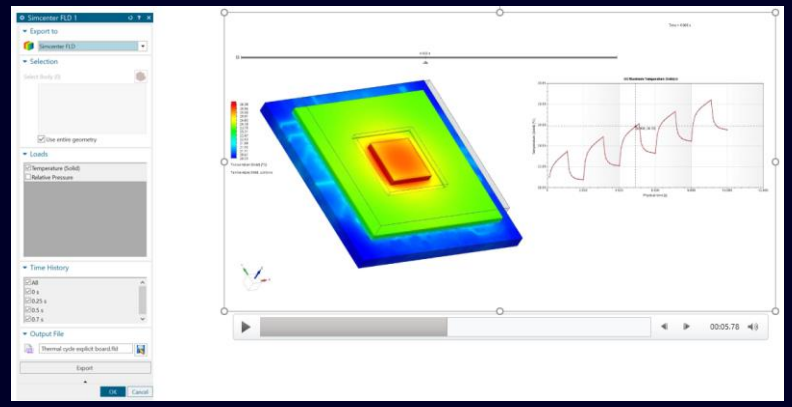
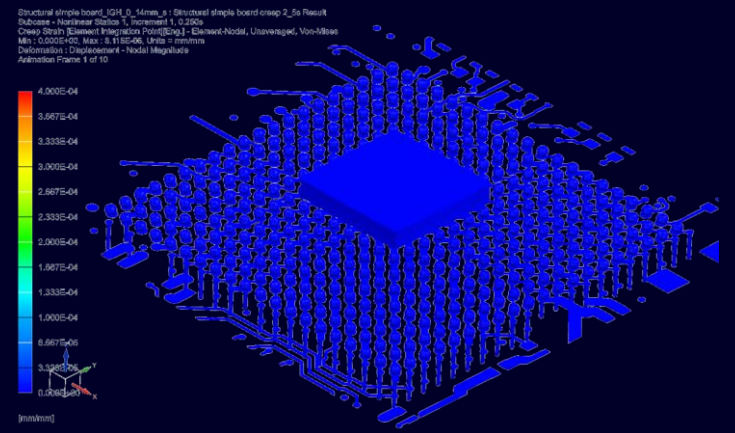
Thermal – Mechanical Workflow for Flip Chip

Thermal Simulation



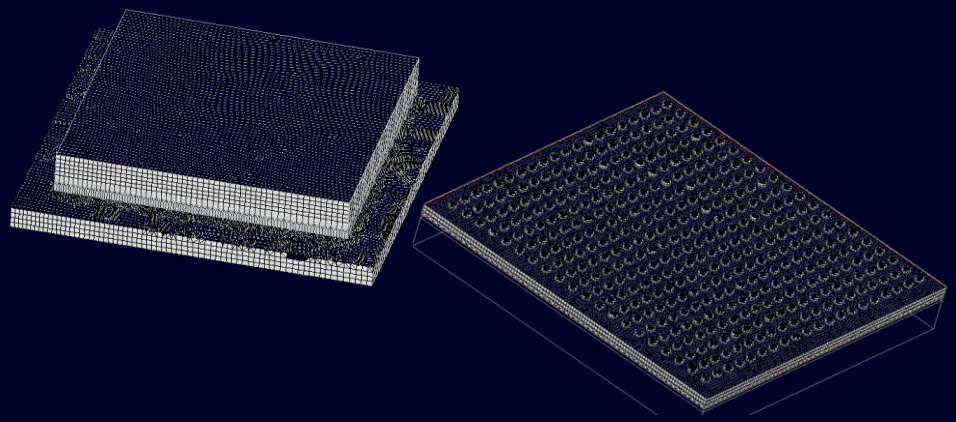
Temperature over Time
***.fld file**



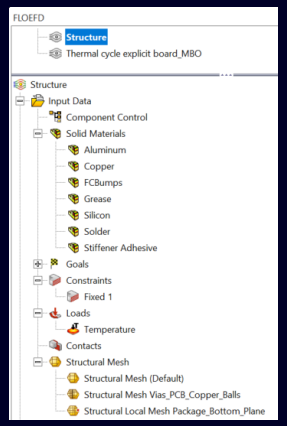


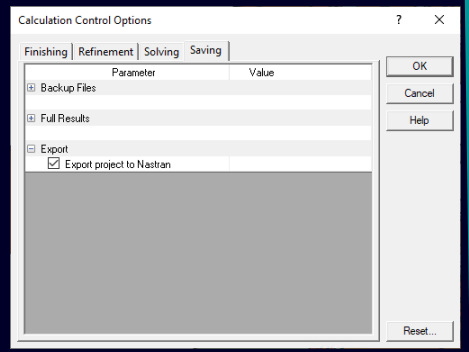
Creep Analysis

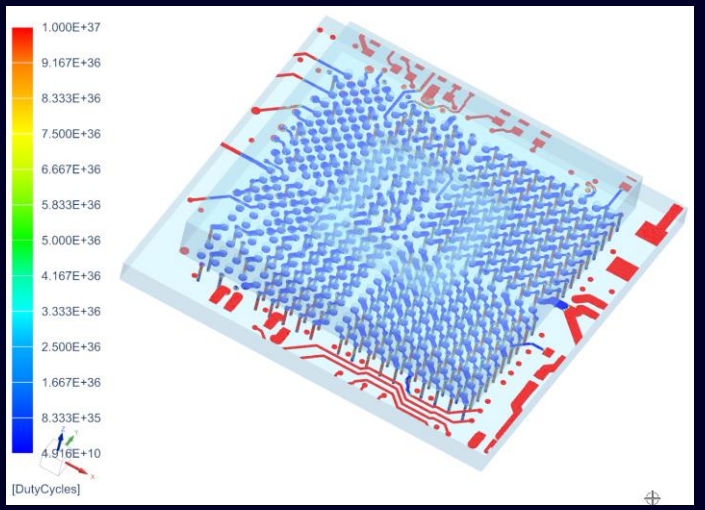
FEM meshe generation



Export mesh







Fatigue Analysis

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Open for discussion

Design Space Exploration

How do you navigate complexity?

Signal Integrity & Power Delivery

How are high power and baud rate designs challenging current workflows?

Model Accuracy

Do you always have access to accurate model parameters?

Disconnected ECAD - MCAD

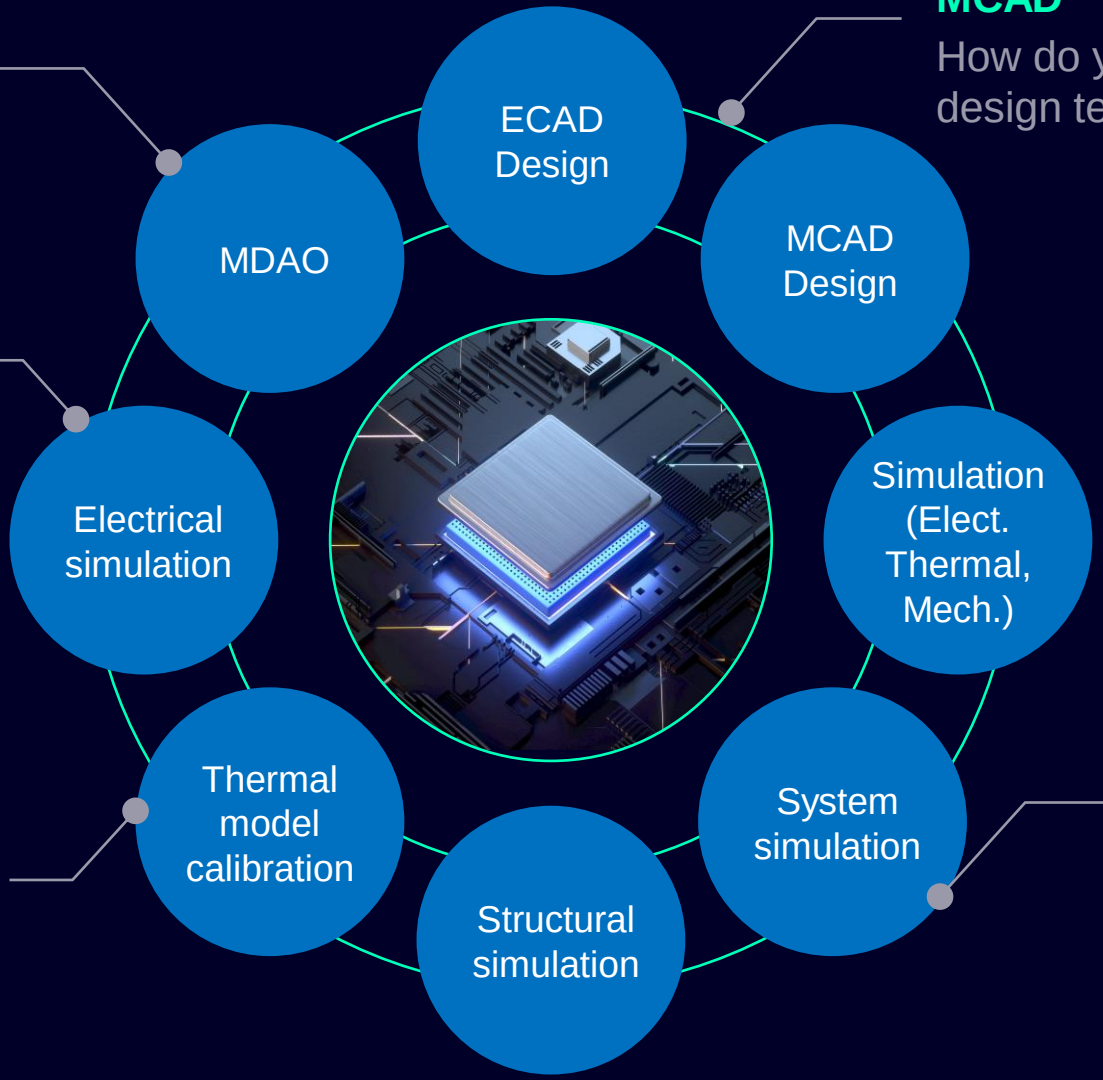
How do you connect your design teams?

Data Management

How do you synchronize data?

System to technology co-optimization

Do you consider component to system design flows?



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