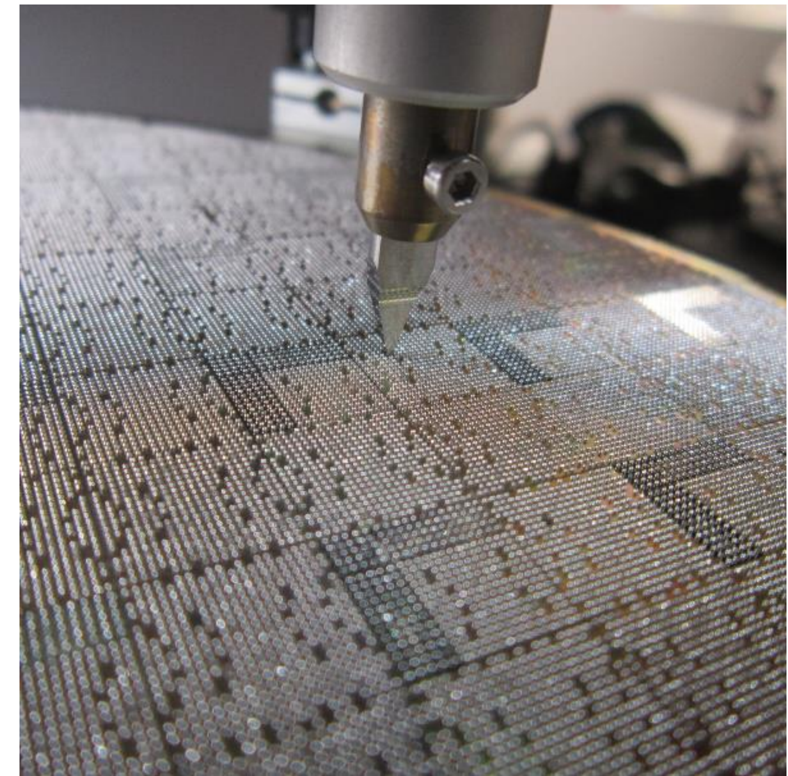
Advanced Packaging: Critical Ecosystem and Reliability Considerations



Kaysar Rahim, Ph.D.
Northrop Grumman Mission Systems

26th Annual Components for Military and Space Electronics Conference and Exhibition

Los Angeles, CA

April 25 - 27, 2023

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Outlines

Advanced Packaging (AP) Overview

Important Stages & Considerations in the AP Value Stream

- Wafer Post-Processing and Interconnects
- Substrates: Boards & Interposers
- Package Assembly

Reliability in 2D+ Flip-Chip Packaging

- Key Processes and Variables
- Common Failure Modes – Electromigration, Electro-Chemical Migration, Solder Fatigue, and Passivation Failures

Summary

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Advanced Microelectronics Packaging

From Wafers to Assembled Packages

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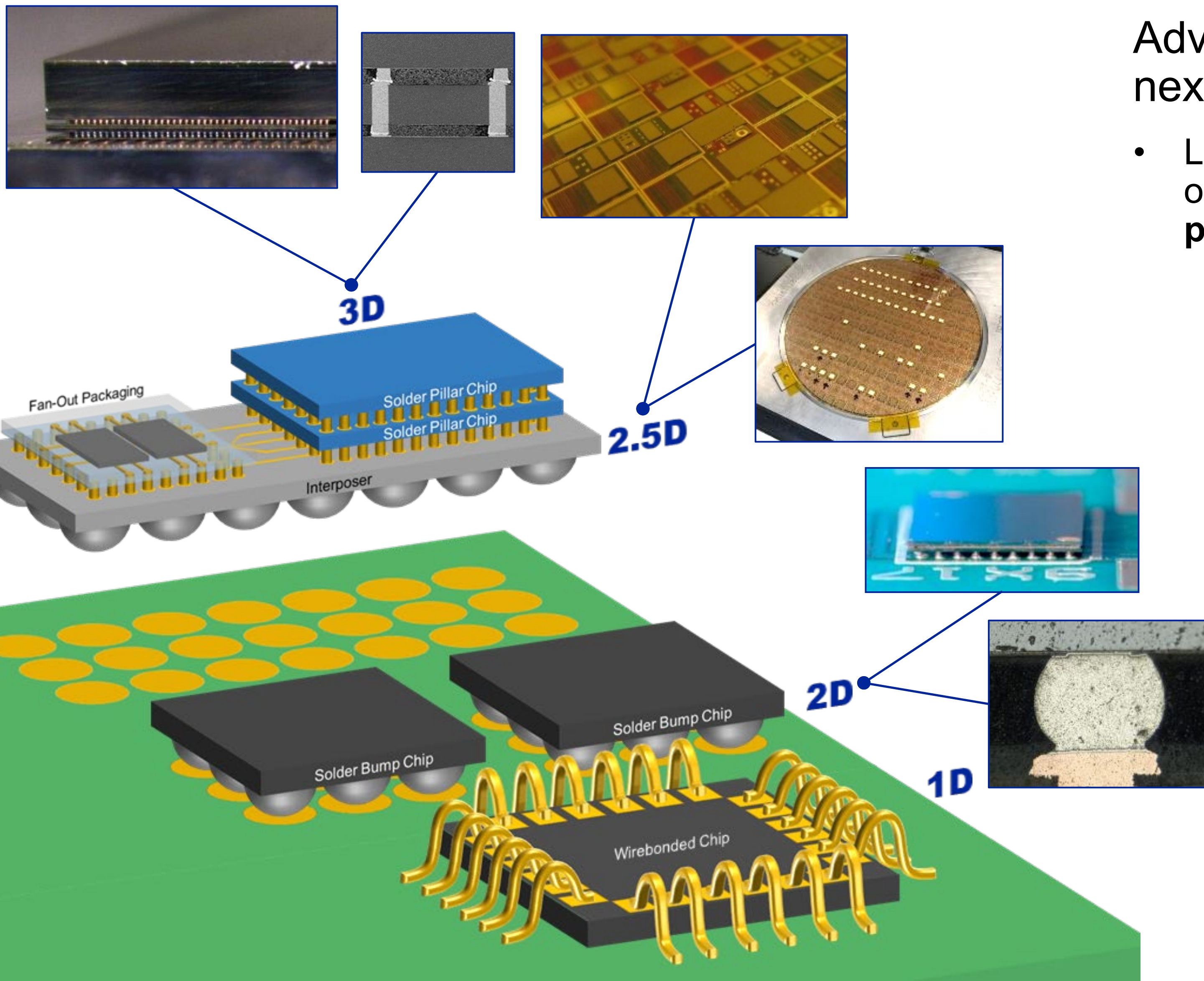

Advanced packaging is a critical enabler for next-gen electronics

- Legacy ceramic, chip/wire packages being phased out in favor of **2D flip-chip** and **2.5/3D advanced packaging**

Priorities for aerospace & defense versus commercial:

- **Truly heterogeneous** integration – much more than just silicon
- Maximum **performance and SWAP-C** driven from the system level
- **High-mix, low-volume** production
- Stable supply chain over **long production durations** (decades)
- **Reliability, quality, security, and stability** throughout the packaging ecosystem and lifecycle

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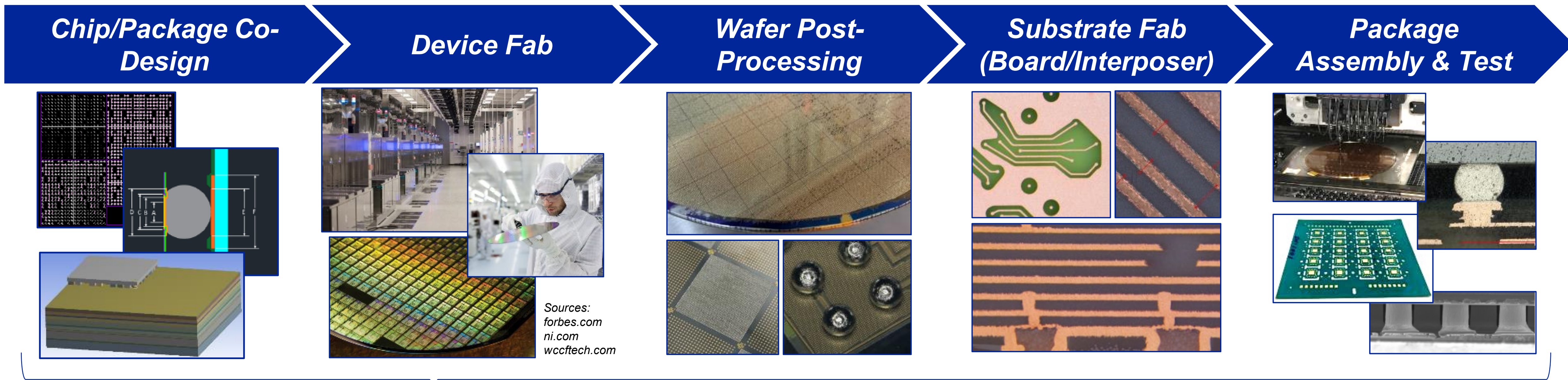
Value Stream for Microelectronics Packaging

Design, Manufacturing, and Test Are Interconnected



USA		Asia
85%	Semiconductor Design	5%
12%	Fab / Manufacturing	**75%**
3%	Packaging	**97%**

IPC Advanced Packaging Ecosystem Report (2021) & U.S. Department of Defense

Congressional Research Service (2020); https://crsreports.congress.gov/product/pdf/R/R46581

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Wafer Post-Processing

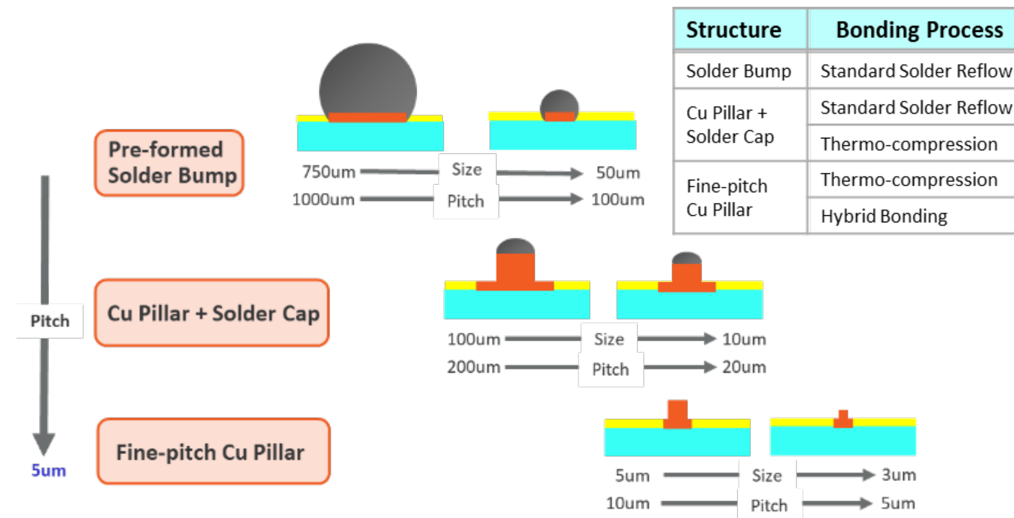
Bumping, Dicing, etc.

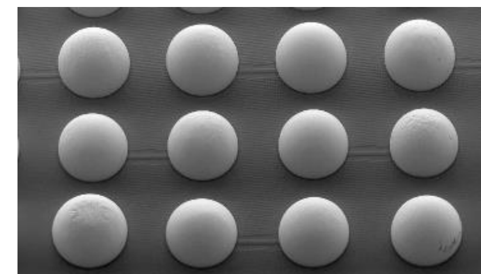
Interconnect fabrication, thinning, dicing, etc.

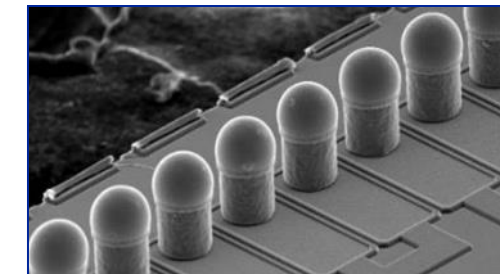
- May also include redistribution layers, TSV insertion, etc.
- May be done at wafer foundry, at packaging house, or separate wafer post-processing vendor

Example considerations for wafer post-processing

- Interconnect type: Solder balls, Cu-pillars, other
  - I/O density, standoff height, etc. drive interconnect type, diameter, pitch
  - Assembly process and interconnect type are closely coupled
- Interconnect materials: Pb-, Pb-free solders, direct bond, etc.
  - Driven by reliability requirements, solder hierarchies in package
  - Material availability (RoHS requirements applicable or not)
- Bump coplanarity across individual die
  - Influenced by bump layout on die, and bump fabrication process
  - Influences wafer probe-ability, assembly process quality & repeatability
- Final thickness and finish of die
  - Influences mechanical reliability, thermal performance, via insertion
- Dicing process compatibility with semiconductor & passivation
  - Influences need for mechanical saw, laser, etc.







Source: asegobal.com

Wafer post-processing is closely interconnected with chip/package design and assembly processes

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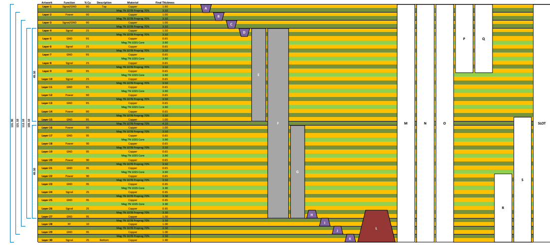
Substrate Materials for Advanced Packaging

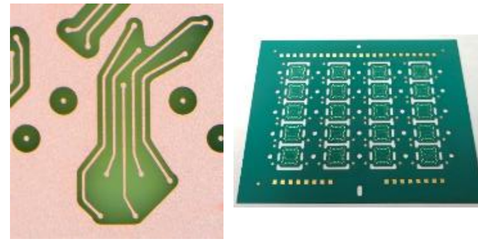
Options Include PWBs, Glass, and Silicon

High Density Interconnect



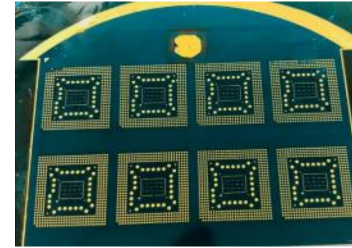
- High density PWBs with glass-weave dielectrics

High Density Build-Up



- Fine line/space organic laminate with Ajinomoto Build-Up Film

Glass



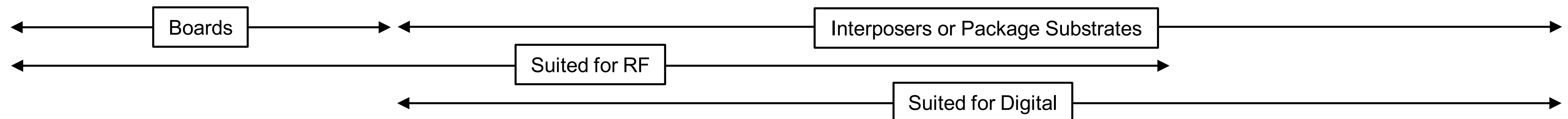
- Emerging glass-core tech with spin-on or laminate dielectrics

Silicon

- Interposer wafers with thru-silicon vias (TSVs) from Si fabs

Format	Panel	Panel	Wafer or Panel	Wafer
Min Line / Space	75 µm	< 25 µm	5 µm	2 µm
Min Pad Dia / Pitch	200 µm / 300 µm	<75 µm / <150 µm	~20 µm / 40 µm	<10 µm / <20 µm
Routing Layers	Many (30+ total)	7+ / side	4 / side	6+ / side
RF Performance	Good	Good	Moderate	Poor
Thermal Conductivity	Low	Low	Low	High
Thermal Expansion	High	High	Moderate	Low
Cost	Low	Low	Moderate → Low	High

Sources: TTM, APCT *Source: Kyocera* *Source: Georgia Tech* *Source: Novati / Skorpios*



Substrate choice determined by performance, cost, and reliability for a given packaging case

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Advanced Packaging Reliability

Factors Affecting Component Reliability

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1. **Level 1 – Package Factors**
    a. Package construction and material
    b. Package size
    c. Die size
    d. Solder ball material composition
    e. Underfill
    f. Process parameters and history (Namely if the package has been stressed)
2. **Level 2 – System Design Factors**
    a) PCB size, thickness/stackup, dielectric materials and metal distribution.
    b) Component locations
    c) Double sided assembly or single sided assembly
    d) Other components on board
    e) Other parts such as PCB stiffener, EM shielding, heat spreader/heat sink, and connector.
    f) Enclosure and how PCB is mounted to enclosure.
3. **Level 3 – Stressing Conditions**
    a. Temperature extremes and cycling rate for TC
    b. Bias / Humidity Tests
    c. EM Tests

Stress > Strength

Always fail at the weakest link

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Advanced Packaging

Fine-Pitch Interconnect and Assembly Readiness

- Key Variables to Consider
  - Ultra-thin Die Warpage
  - Cu Pillar Coplanarity
  - Interposer Pad Surface
    - Paste Printing (> 100 ump)
    - Solder on Pads (> 60 ump)
    - ENIG
  - Bonding Method
    - Thermo-compression
    - Mass Reflow (>40um)
  - Assembly Level
    - 2D, 2.5D & 3D

Ultra thin die warpage

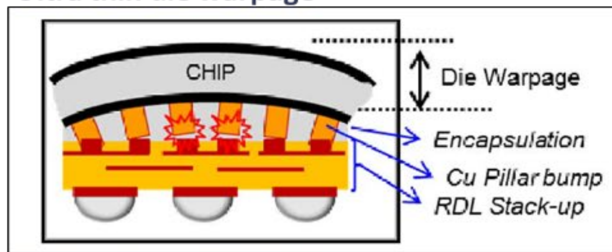

Figure 4: Park, H., Kim, Y., Jang, Y., & Choa, S. (2018).

Copper pillar coplanarity

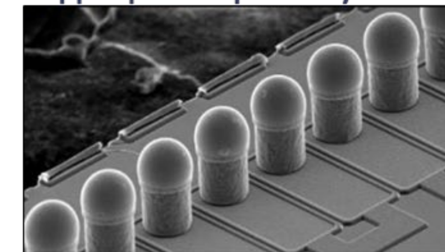

Figure 5: asegobal.com

Interposer Pad surface finish

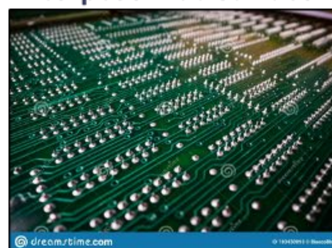

Figure 6: Dreamstime.com

Bonding Method

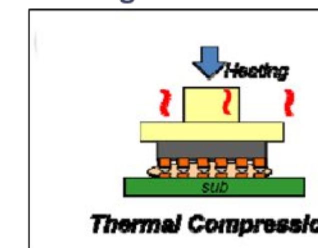

Figure 7: Tsai, M., Lan, A., Yao, Y.H., Wu, M.Y., Chang, C.K., Lo, R., & Chen, E. (2015).

Assembly level

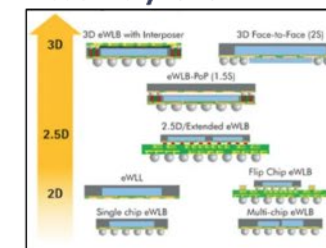

Figure 8: semiengineering.com

Fine-pitch interconnects and 2/2.5D/3D assembly are the keys for high density packaging

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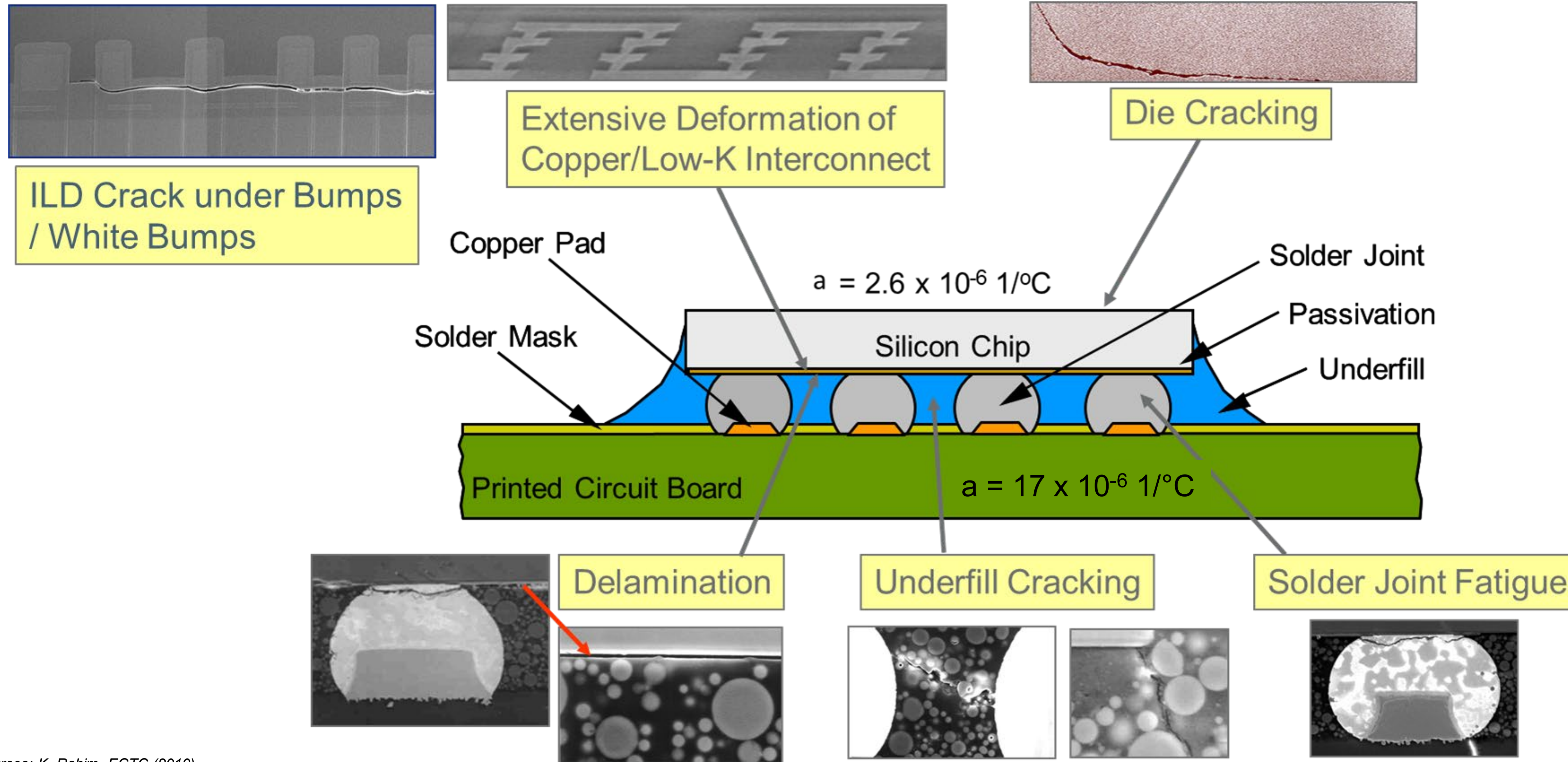
Typical Failure Modes in Flip Chip Packaging

Thermo-Mechanical Stressing



Sources: K. Rahim, ECTC (2010)
IEEE Trans. Comp. Pack. Tech. (2003)

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Typical Failure Modes in Flip Chip Packaging

Electrical, Chemical, Bias Humidity Stressing

Electro-Migration

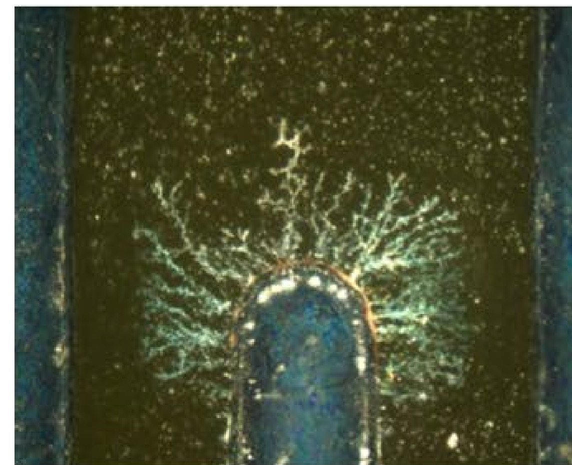
Void growth between solder and UBM/pad interface driven by electron wind, temperature gradient and stress gradient. Results in an open failure.

Figure 9: Failure mode for High Pb bump showing failure on substrate (cathode) side

Syed, Ahmer, Karthikeyan Dhandapani, Robert Moody, Lou Nicholls, and Mike Kelly. "Cu Pillar and μ-bump electromigration reliability and comparison with high pb, SnPb, and SnAg bumps." In *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, pp. 332-339. IEEE, 2011.

Electro-Chemical Migration

Dendritic growth between bumps due to *contamination*, temperature, bias humidity. Results in a short failure.



Bumiller, Elissa, and Craig Hillman. "A review of models for time-to-failure due to metallic migration mechanisms." *DFR Solutions white paper* (2009).

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Chip-Package Interaction Stresses

CTE Mismatch & Warpage between Die and Substrate

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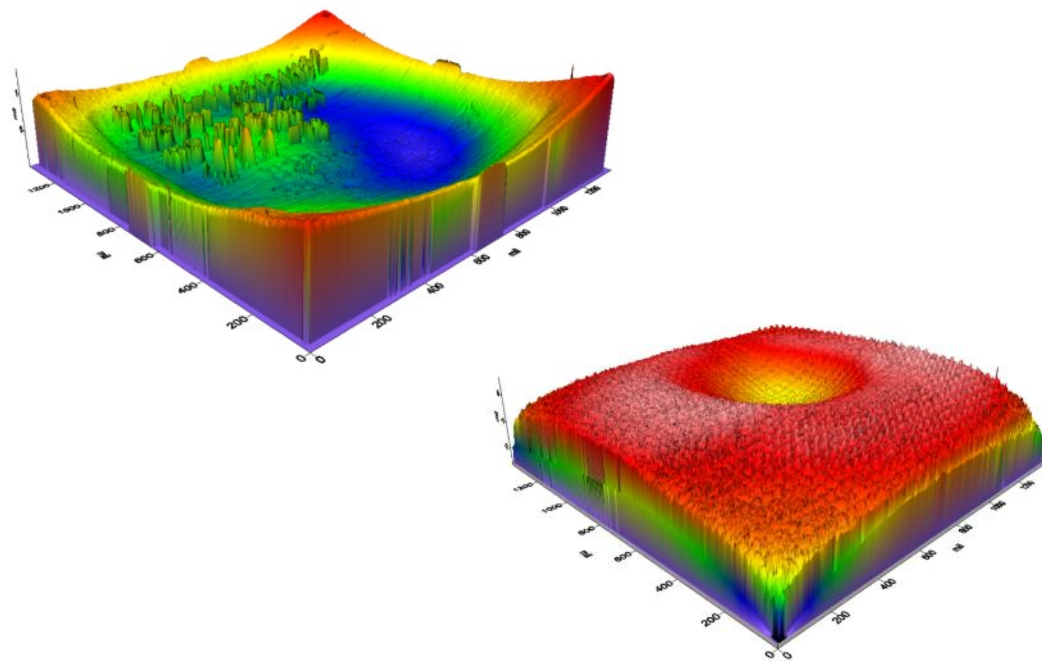
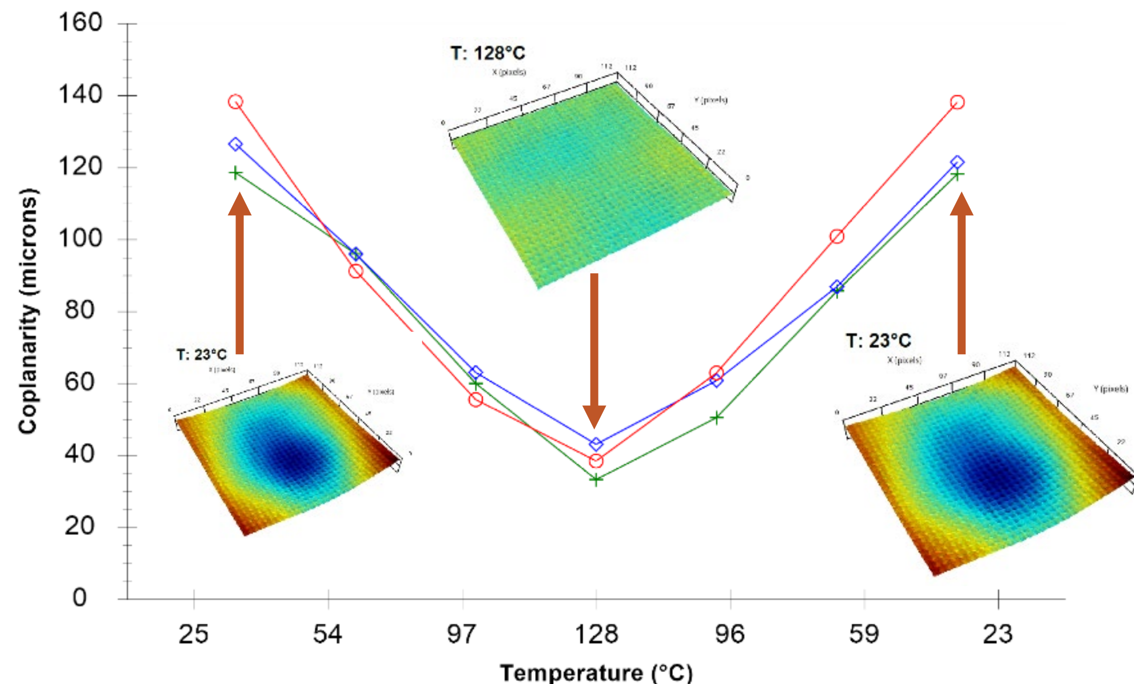
- CTE mismatch between a silicon die and an organic substrate introduces stresses than can impact the overall package reliability through qualification as well as assembly
- Each package will have a unique thermo-mechanical interactions that can be tracked through warpage measurements and correlated to a stress model to determine the impact of materials and processes on the interconnect stresses





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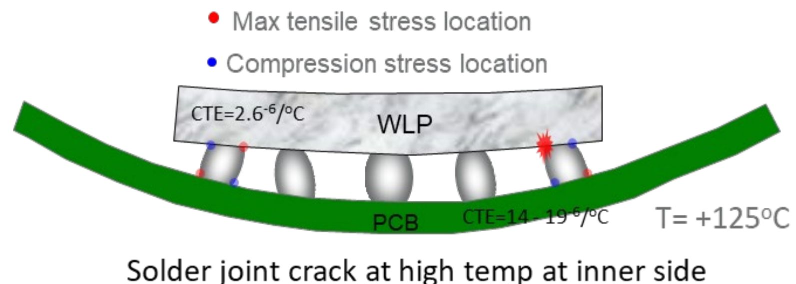
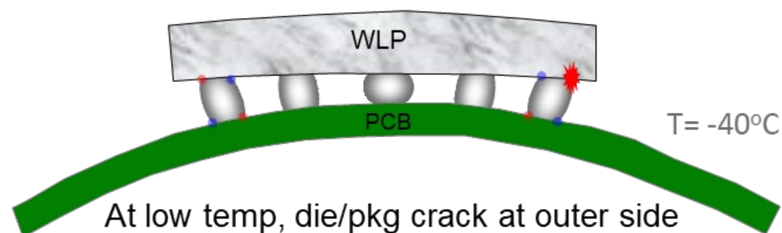
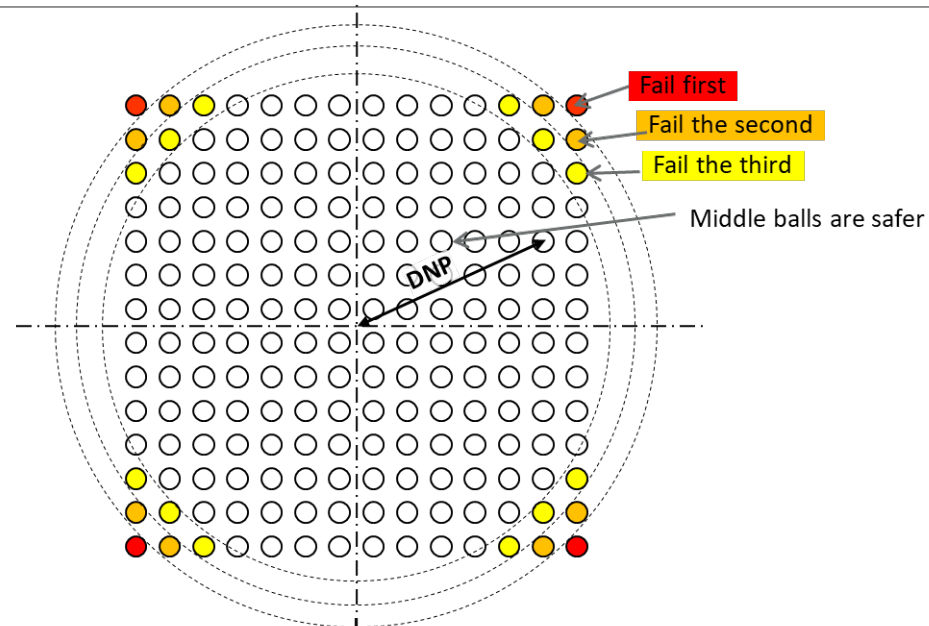
Chip-Package Interaction Stresses

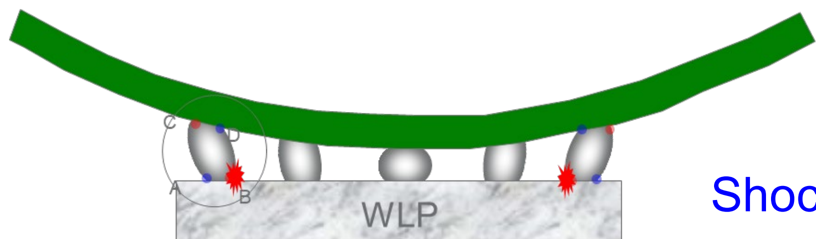
CTE Mismatch & Mechanical Warpage between Die and Substrate



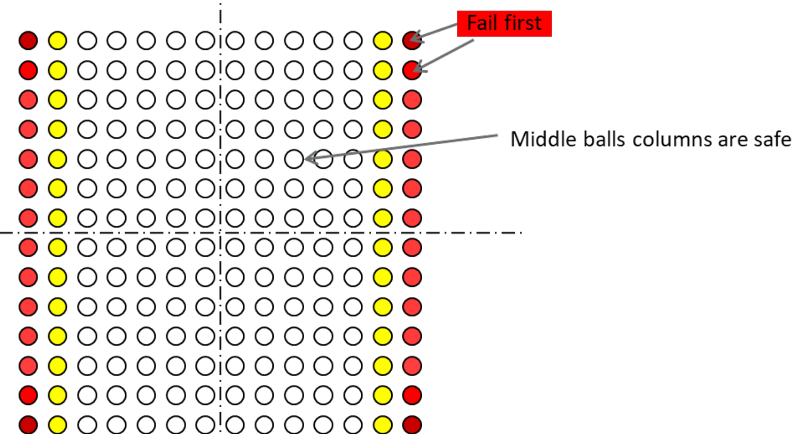


TC Test





Shock / Cyclic Bend Test



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Failure Mechanism in Flip Chip Packaging

Solder Joint Strain Accumulation During Temperature Cycling

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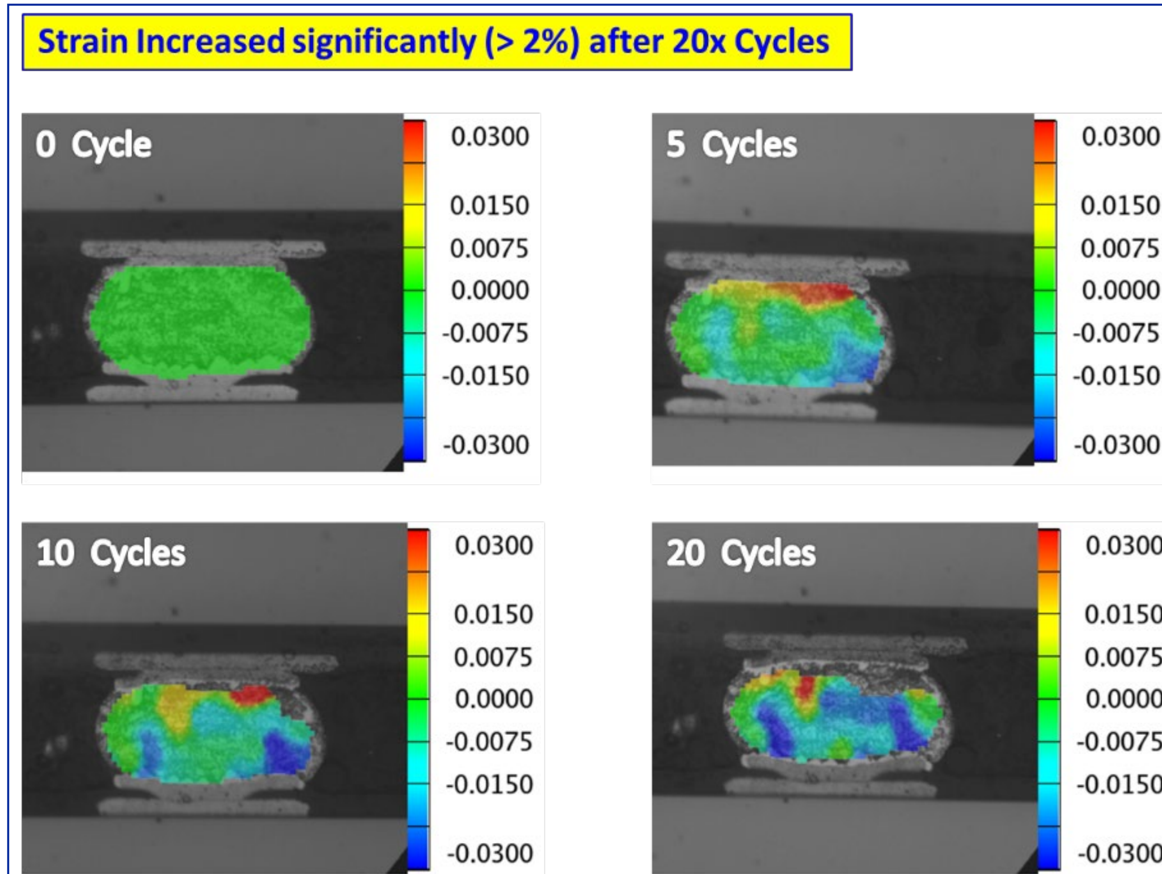
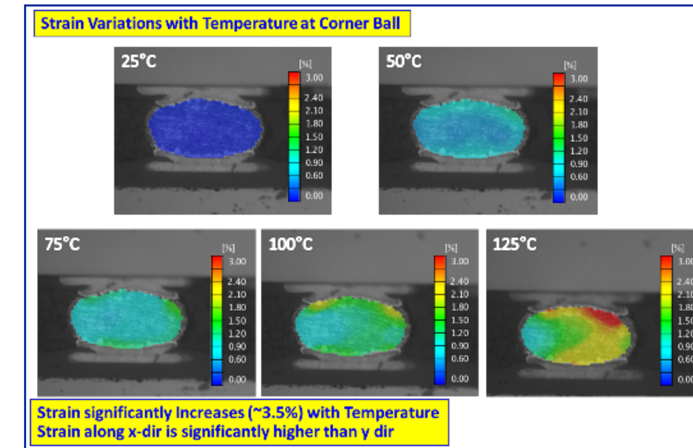
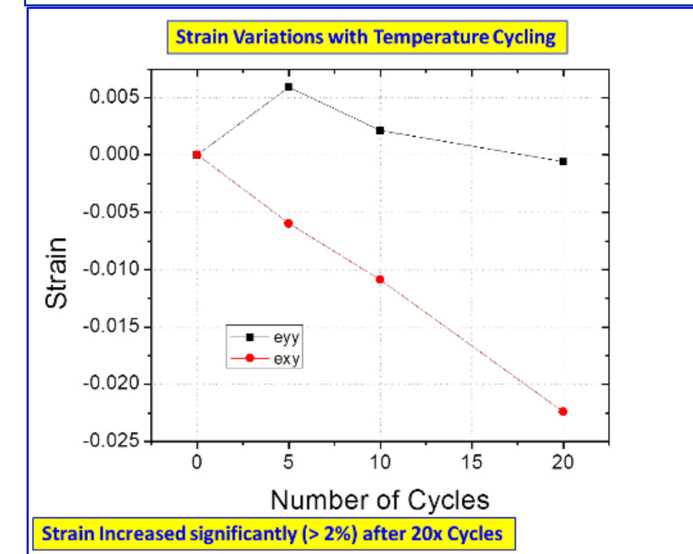
Solder joint strain measured through DIC



Source: K. Rahim, ECTC (2009)





Source: K. Rahim, ECTC (2009)

Solder joints continuously deformed / strained under temperature cycles

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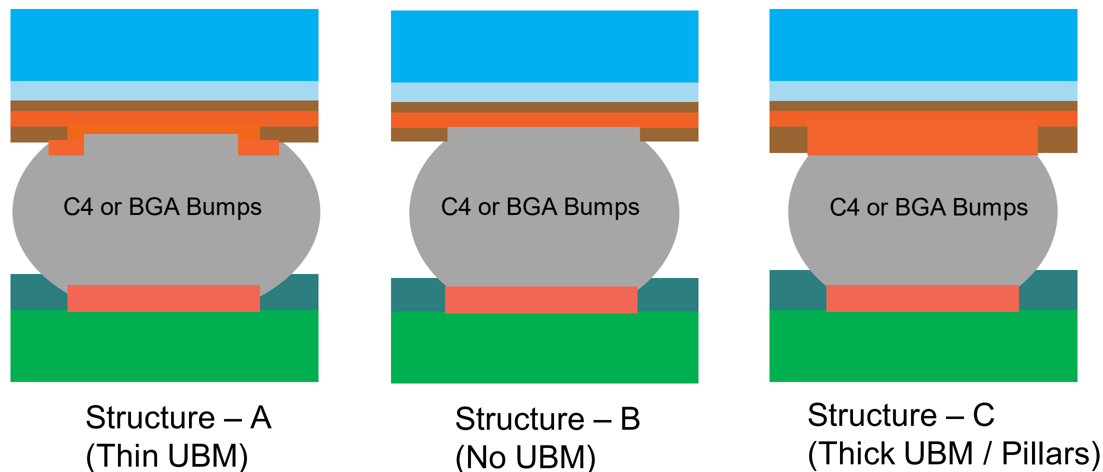
Chip-Package Interaction Stresses

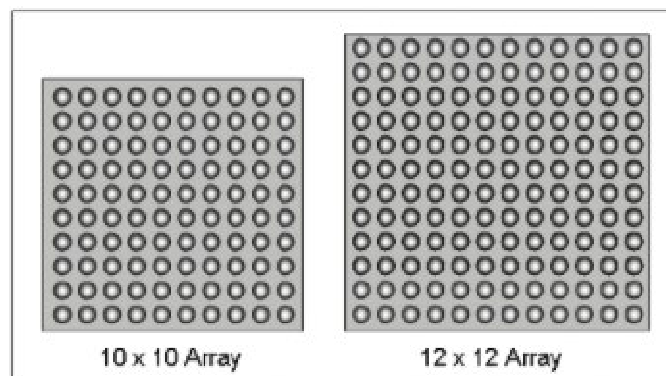
Flip Chip Solder Joint Reliability

Board Level Temperature Cycling Data

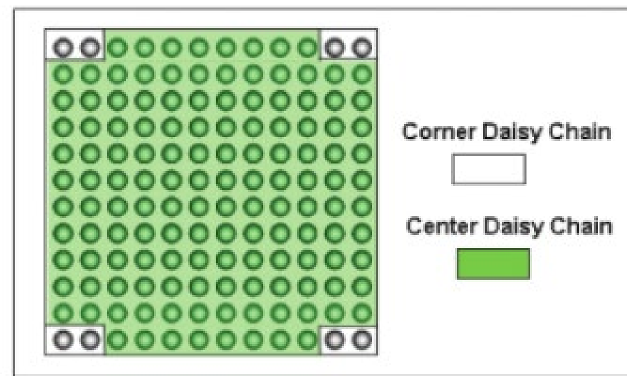


WLP Type	WLP - A	WLP - B	WLP - C
Characteristic Life	1.6	0.8	1

UBM Structure A have higher Solder Joint Reliability Compared to Structures B & C



Array Size	12x12	10x10
Characteristic life	1	1.2



Solder Ball Groups	Corner	Non-corner
Characteristic Life	1	1.3

Reference: Kaysar Rahim, 2009 ECTC Paper

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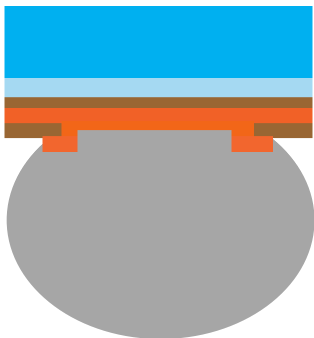
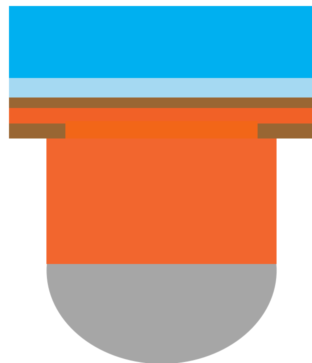
Cu Pillar for High Density 2.5D/3D SiP Module

C4 (Controlled Collapse Chip Connection) Bump vs. Cu Pillar (C2)

C4 Bump and Cu Pillars, both used in high-density packaging





C4 Bump
Size: 75 um – 150 um
Pitch: 150 um – 200 um

Cu Pillar (C2)
Size: 10 um – 100 um
Pitch: 20 um - 150 um

Assembly Variables	Thermo-compression	Mass Reflow
Placement accuracy	Good	Fair
Ability to minimize warpage	Good	Poor
Pitch (>100 um)	Good	Good
Pitch (<100 um)	Good	Fair
Throughput	Poor	Good

Mass reflow is more manufacturable, but thermocompression bonding helped to overcome die warpage from ultra thin die

Cu Pillar Technology and It's Benefits?

- Improved Electromigration Resistance
- Improved Electrical and Thermal Performance
- Simplified Underbump Metallization
- Enables Higher I/O Density
- Enables Fine-pitch Capability that allow Smaller Packaging Footprints

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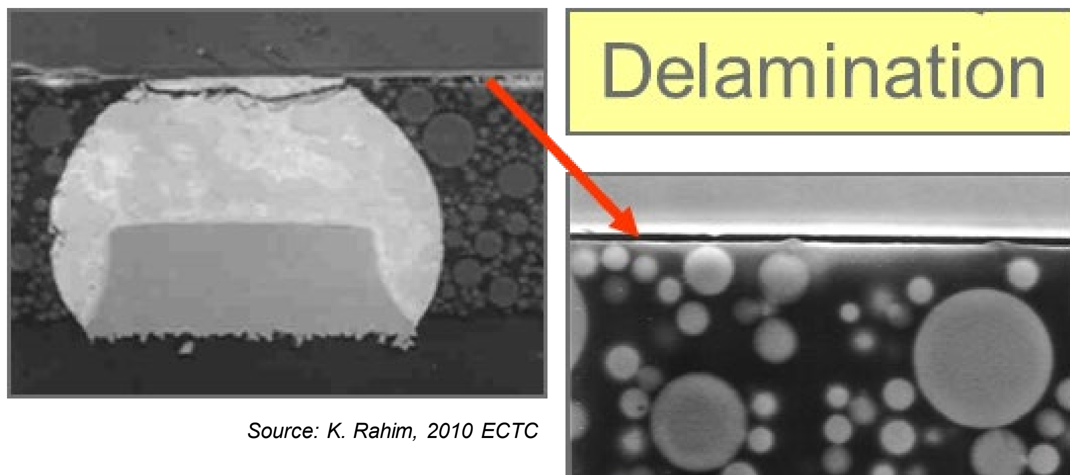
Fine Pitch Flip Chip Underfilling

Factors Affecting Underfilling Process

- **Two Main Processes**
  - Capillary Underfill
  - Pre-applied Underfill
    - *Suitable for < 40um Pitch*
    - *Limited to Thermo-compression Bonding*



Source: K. Rahim, 2010 ECTC

- **Key Variables to Consider for Capillary Underfill**
  - Cleanliness
  - Underfill Epoxy Materials
  - Interconnect Stand-off, Pitch, Type
  - Dispense Pattern
  - Flux / Underfill Compatibility
  - Flux Residue
  - Cleaning method
    - Plasma vs. Wet Clean
  - Underfill Filler Size
  - Underfill Dielectric Constant and Loss Tangent
  - Underfill Cure Conditions
    - Pressure Curing vs. No Pressure
  - Underfill Voids and Delamination

Underfill process control is very critical for fine-pitch interconnect reliability

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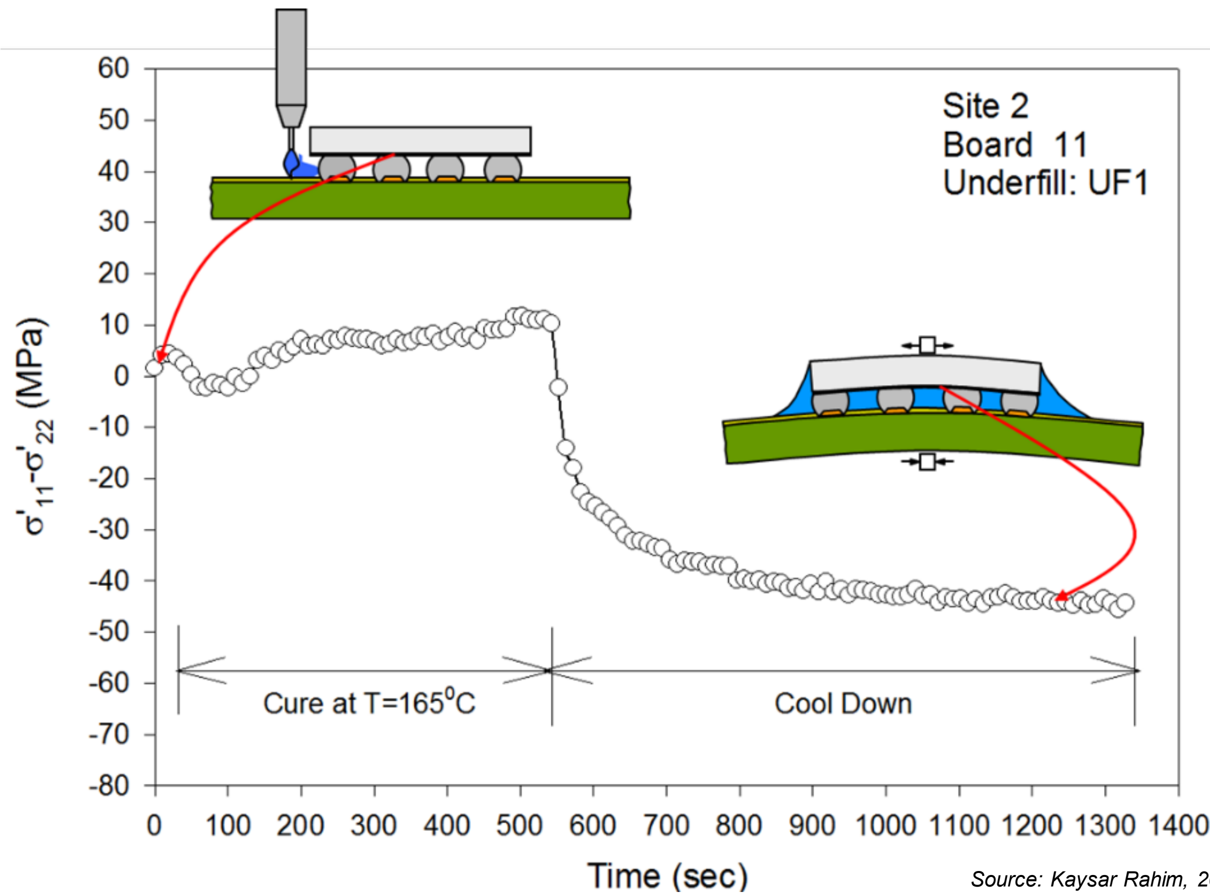
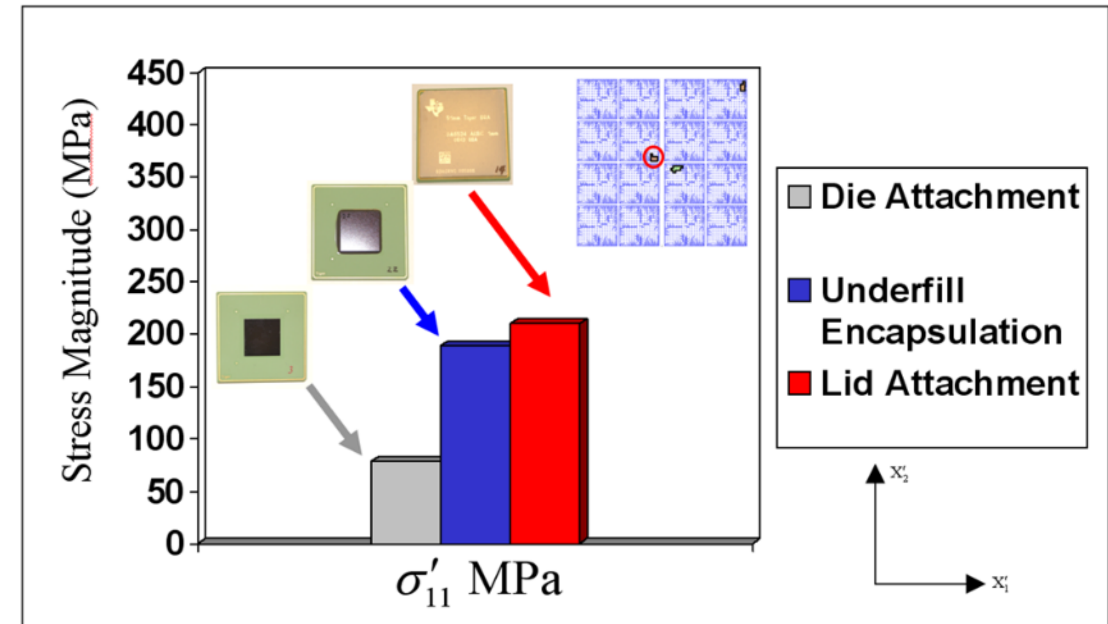
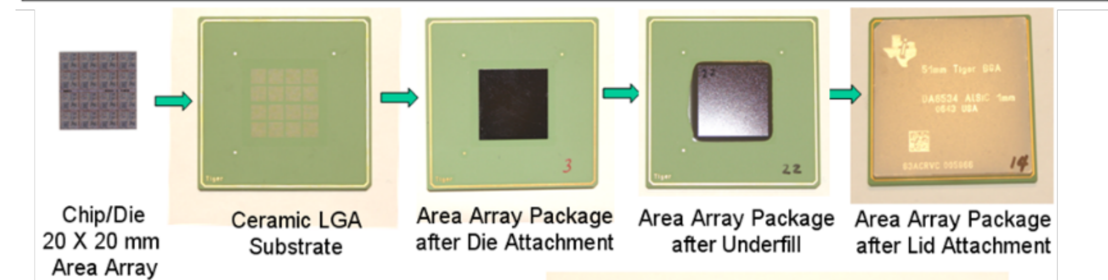
Fine-Pitch Flip Chip Underfilling

Package Stress Due to Underfilling



Source: Kaysar Rahim, 2010 ECTC





Selection of appropriate underfill materials is critical for package reliability – and becomes more complicated with heterogeneous integration, mixed interconnects, etc. on one package

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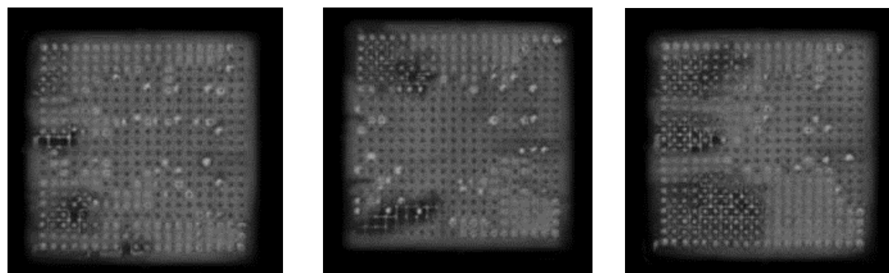
Fine Pitch Flip Chip Underfilling

Flux Residue / FOD Impact on Underfilling Process

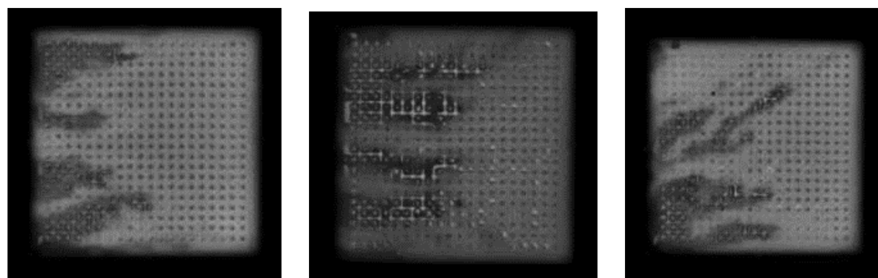
- **Flux residue from flip chip assembly can impact the following:**
  - Voids in underfill
    - Lead solder bridging / extrusion at Time-0 and post TC
  - Poor adhesion with bumps and die
    - Lead delamination both at Time-0 and post TC
    - Cause solder joint Crack

Not Clean



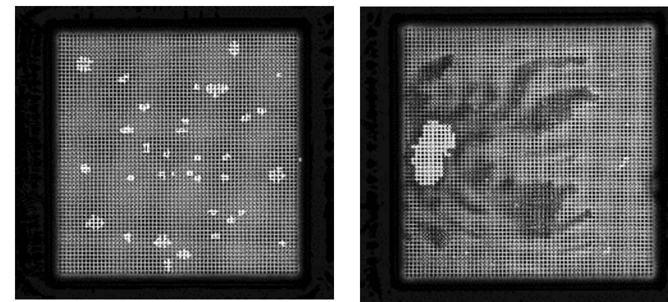
Sample 1 Sample 2 Sample 3

Cleaned



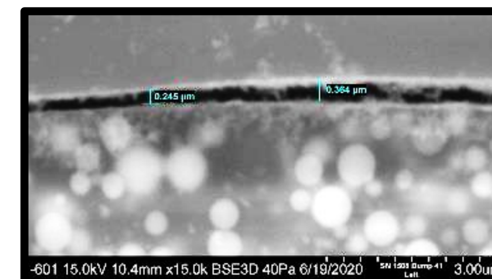
Sample 1 Sample 2 Sample 3

Underfill Voids due to Presence of Flux Residue



Underfill A Underfill B

Underfill Delam due to Presence of Flux Residue



Post-reflow, pre-underfill cleaning reduces voids and improves underfill adhesion

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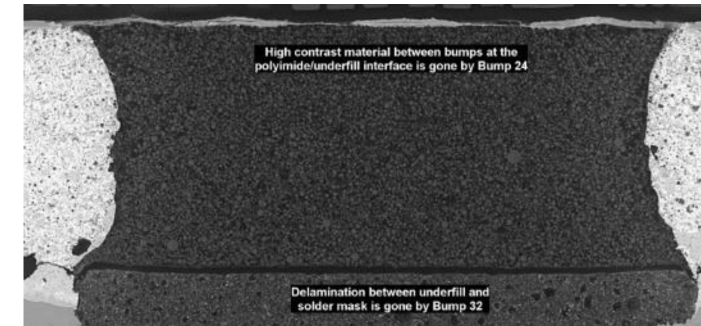
Fine-Pitch Flip Chip Underfilling

Impact of Voids in Solder Joint Reliability

- **Solder extrusion occurs due to thermo mechanical stresses between underfill and solder**
- **Prevalent in high-lead and eutectic solder but can also occur with Pb-free alloys as well**
- **Can result in open and short signals depending on time-temperature environment**



- Electro-chemical migration can span bumps through delaminated or voided underfill
- Can occur in both lead-free and leaded solders in both flip chips and BGAs
- Flip-chips are at higher risk due to smaller spacing between bumps and higher current density

Failure Analysis Flow for Package Failures

Rajen Dias
Intel Corporation, Chandler, Arizona, USA

Source: R. Dias, Microelectronics Failure Analysis Desk Reference (2011).

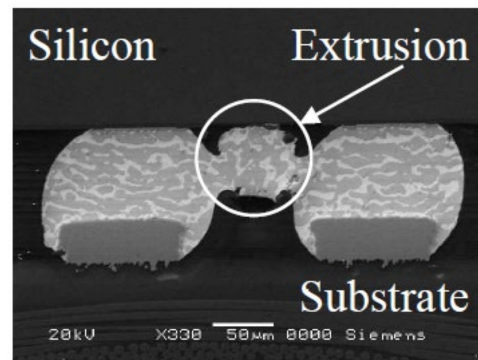


Figure 5-2 SEM image of solder extrusion into underfill void

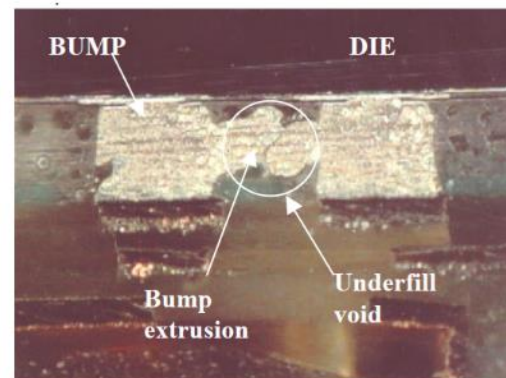


Figure 4. Dark field optical image of x-section of shorted bumps showing that solder extrusion into the underfill void was the mechanism of failure.

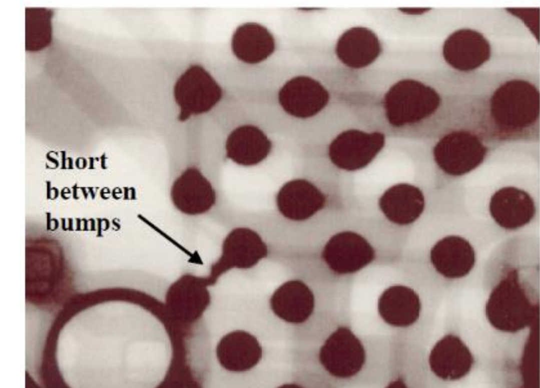


Figure 2. X-ray image of flip chip package showing bridging between bumps that were electrically shorted.

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Challenges in Fine-pitch Large Die Underfilling

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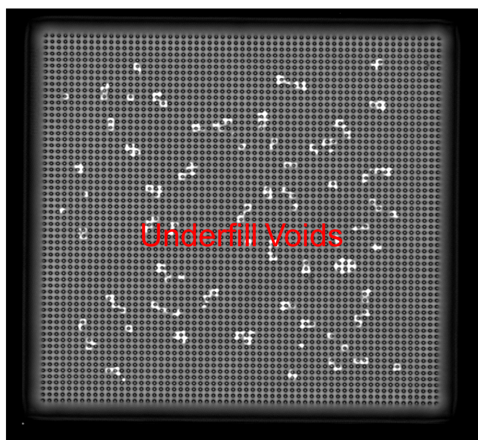
Two Main Issues:

- Fine-pitch Large Dies Cleaning Challenges
- Void-free Underfilling Challenges

150um Pitch Cu Pillar 10 mm x 10mm Die



Vendor Recommended Curing

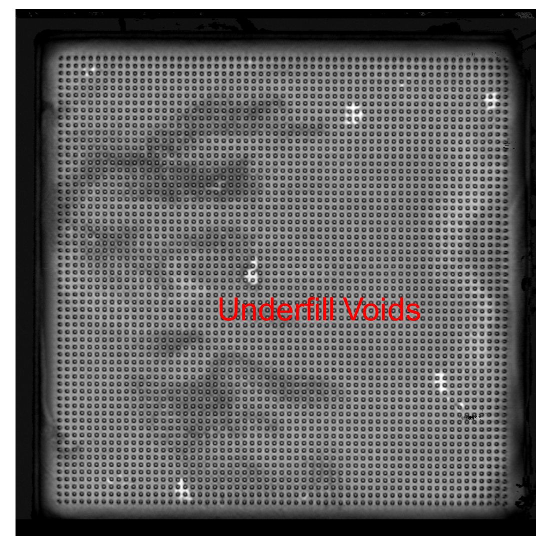
Vacuum Pressure Curing

Pressure Curing helps Reduce Voids
in Fine-pitch Interconnect Large Die

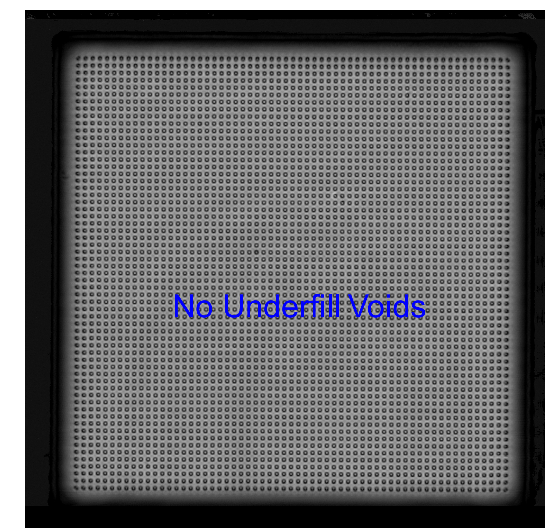
Selection of Underfill Materials is very Critical:

- Good Thermo-mechanical Properties
- % Filler Content → Directly related to CTE, Modulus, Moisture Absorption
- Filler Size → Typically 1/3 of the Die/Substrate Gap
- Good Compatibility with Flux
- Good Adhesion to Die Passivation / Substrate Soldermask
- Higher Creep / Fatigue Resistance

Underfill-A



Underfill-B



Underfill-B Performs better under same Curing Conditions

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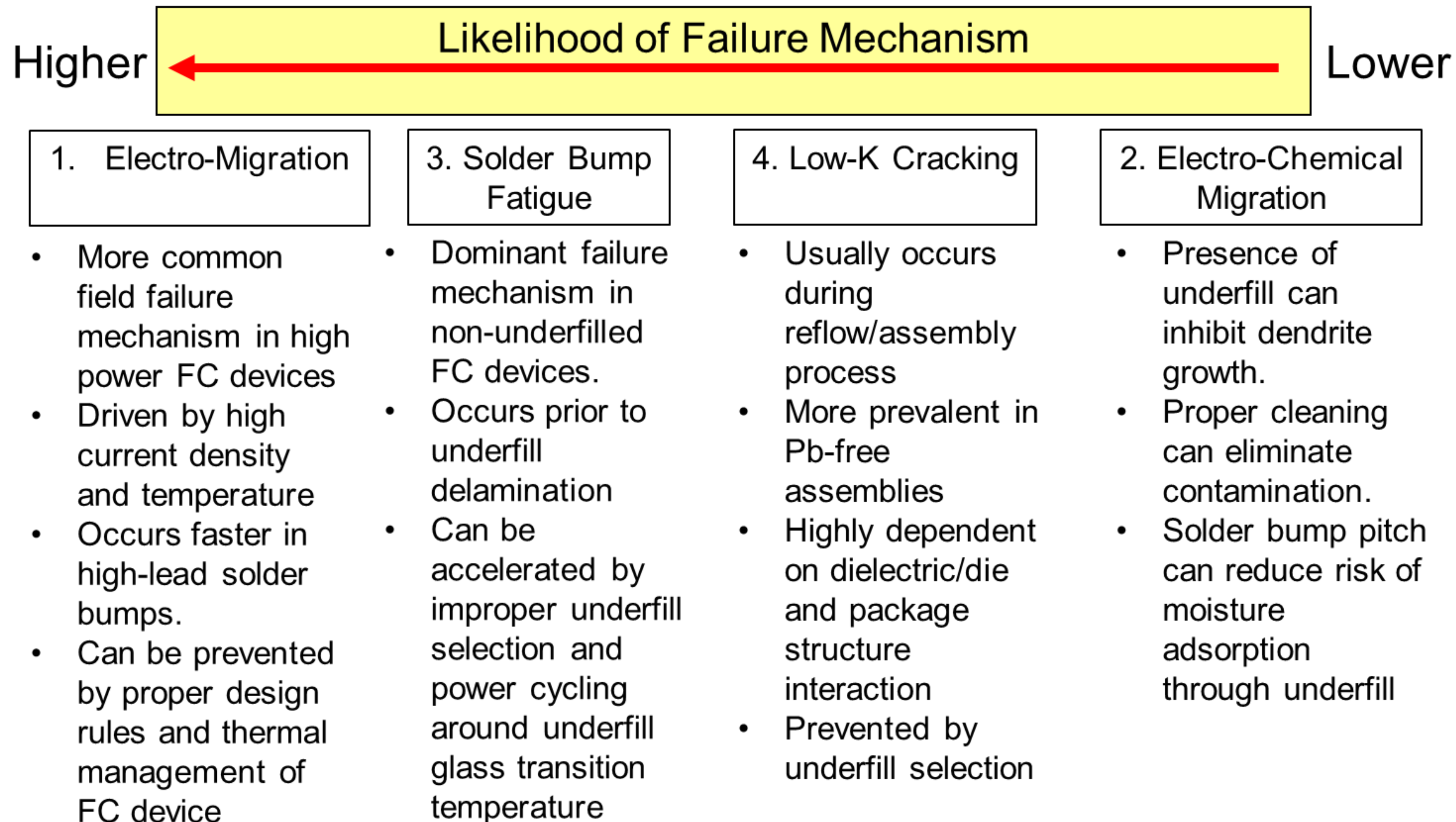
Categorizing Likely Flip-Chip Failure Mechanisms



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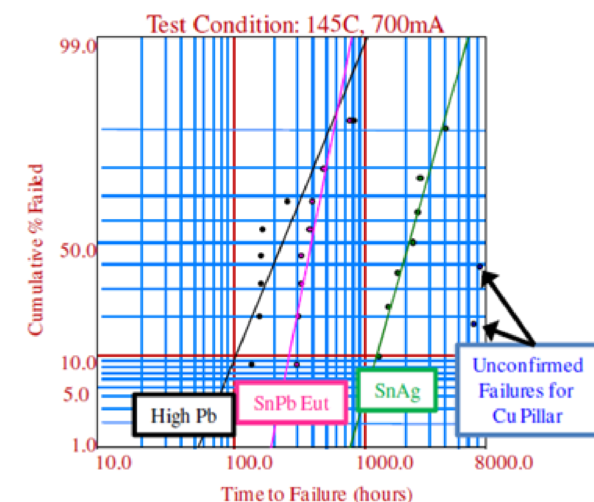
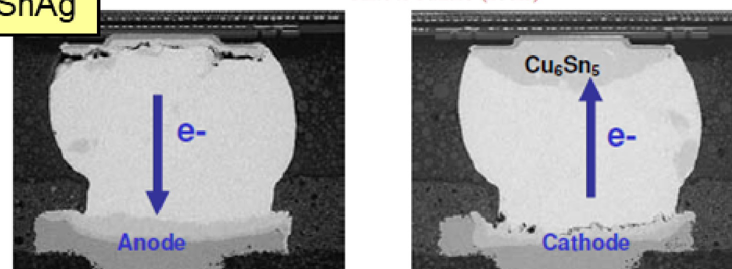
Electromigration

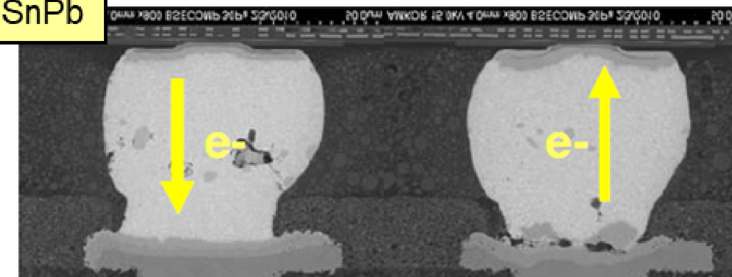
- Study by Syed (Amkor) showed High lead bumps to be less reliable than equivalent SnAg bumps under electromigration.
- Demonstrated increased electromigration resistance of micro-bumps & cu-pillar over flip chip bumps.

FC Bump Test Vehicle 90um UBM, 85um SRO			u-bump Test Vehicle	
Current (Amps)	Current Density - UBM (A/cm^2)	Current Density - SRO (A/cm^2)	Current (Amps)	Current Density (A/cm^2)
0.4	6288	7049	0.1	20372
0.55	8645	9692	0.175	35651
0.7	11003	12336	0.25	50930

Bump Configuration	Stress Current (mA)	Oven Temperature (deg C)	# Samples	# Failed	Test Hours Completed
High Pb	400	130	8	8	5561
High Pb	400	145	8	8	2200
High Pb	550	130	8	8	2267
High Pb	700	130	7	7	714
High Pb	700	145	8	8	799
Eut SnPb	400	130	8	3	7130
Eut SnPb	400	145	8	8	2167
Eut SnPb	400	160	10	10	671
Eut SnPb	700	130	8	8	3274
Eut SnPb	700	145	8	8	742
SnAg	400	130	7	1	7130
SnAg	400	145	8	4	8140
SnAg	700	130	7	4	7130
SnAg	700	145	8	8	4180
Cu Pillar SMD	400	145	8	3	8140
Cu Pillar SMD	550	145	8	6 (4*)	8140
Cu Pillar SMD	700	130	10	2*	7130
Cu Pillar SMD	700	145	8	6 (4*)	8140
Cu Pillar NSMD - 1	700	130	8	3*	7130
Cu Pillar NSMD - 2	700	130	8	4	7130







Source: Syed et al., ECTC (2011)

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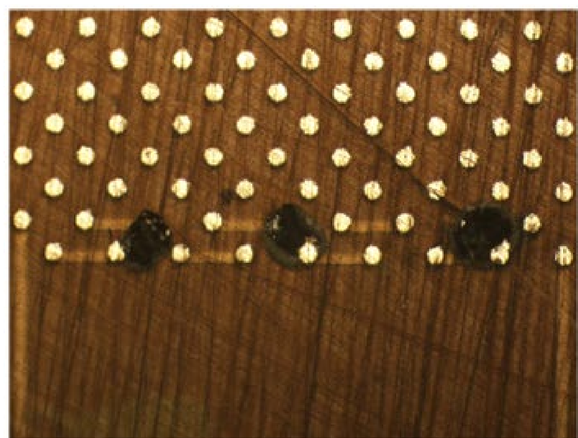
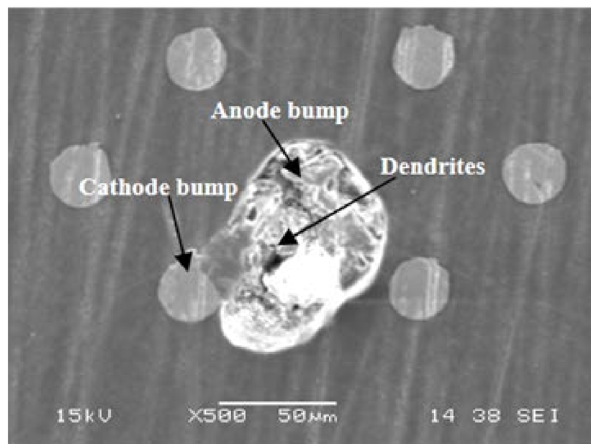
Electro-Chemical Migration

- Dendrites can form in underfilled flip-chip devices with no-clean flux due to the adsorption of water by underfill materials
- Underfill voids bridging two bumps can facilitate risk of dendrite formation
- Solder bump flux residues can facilitate an electrochemical cell and result in Cu dendrite (<1μm thick) formation on die surface





Yu, Da-Quan, Tai Chong Chai, Meei Ling Thew, and Yue Ying Ong. "Electrochemical migration study of fine pitch lead free micro bump interconnect." In *2009 11th Electronics Packaging Technology Conference*, pp. 389-394. IEEE, 2009.

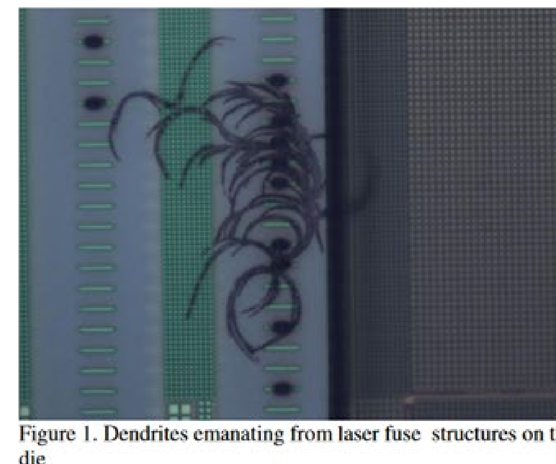


Figure 1. Dendrites emanating from laser fuse structures on the die

Kho, W. F., and Gary HG Chan. "Copper dendrite formation on laser fuse structures of flip chip die." In *2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits*, pp. 565-568. IEEE, 2015.

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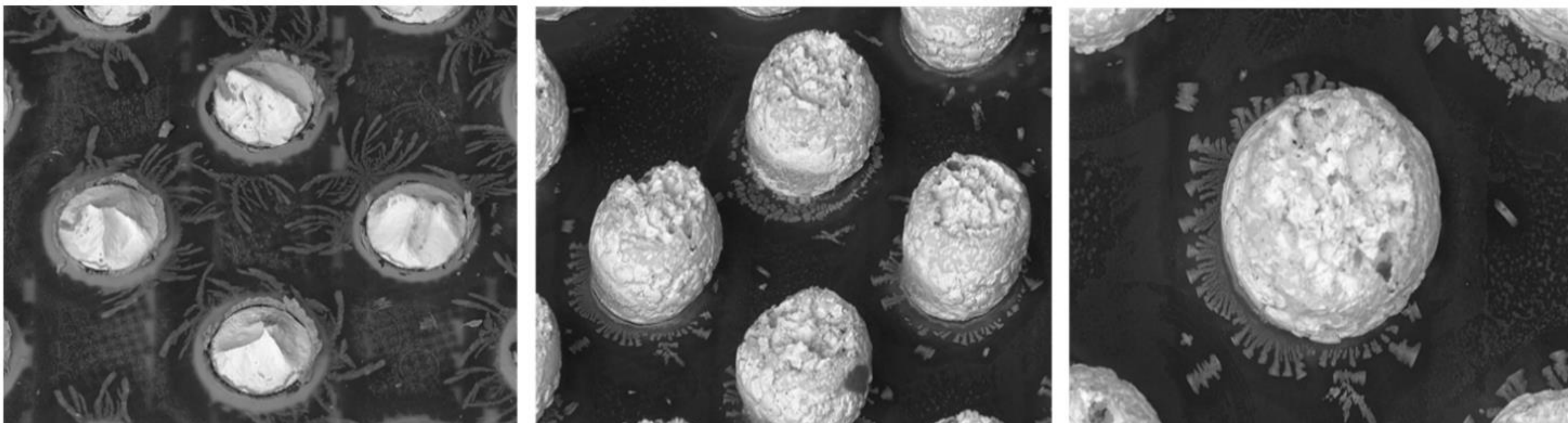
Electro-Chemical Migration

- Cleanliness of incoming bumped die must be monitored to identify contamination/residue from bumping and singulation processes
  - More common in leaded solder plating applications
- Perform die pull pre-underfill to inspect die and substrate surface post clean process
  - Not all flux residues can be cleaned with the same process and chemicals
  - Excessive contamination can lead to dendritic growth as well as poor underfill adhesion



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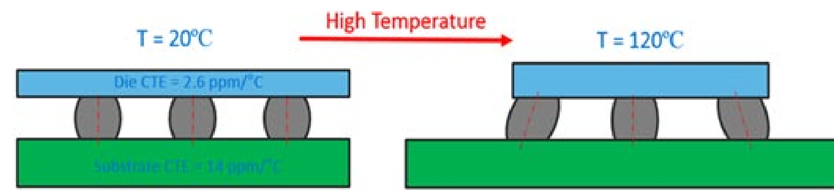
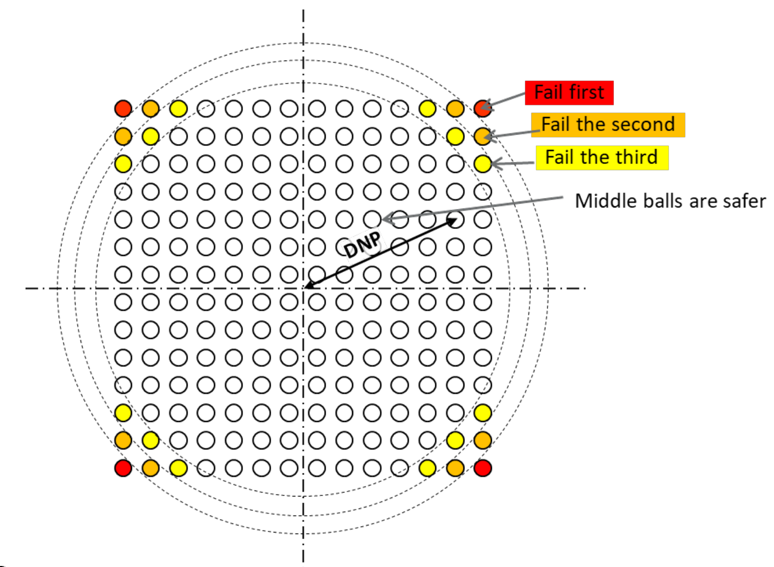
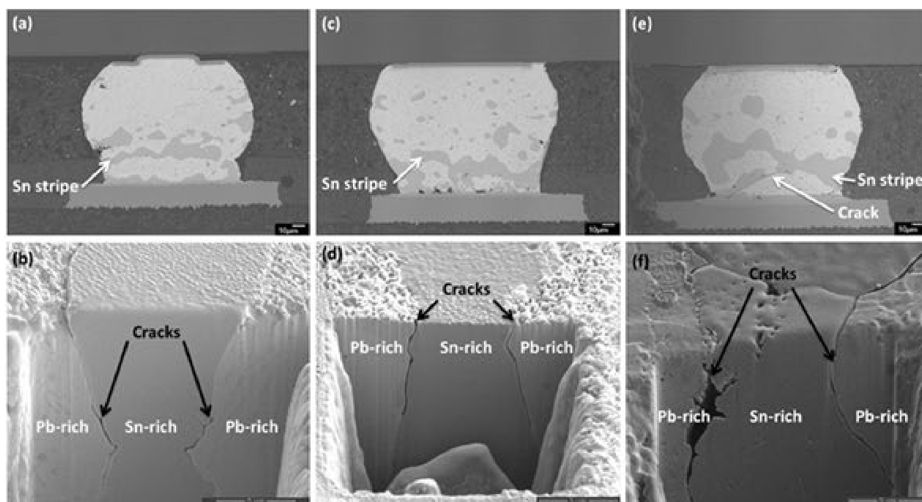
Solder Interconnect Fatigue

- Solder bump fatigue is a direct result of thermal cycling due to internal or diurnal changes in temperature. Due to large CTE mismatch between silicon die and organic substrate bumps can experience repeated creep deformation resulting in fatigue crack propagation across the bump
- Fatigue cracks tends to nucleate at the interface of the Sn and Pb rich phases



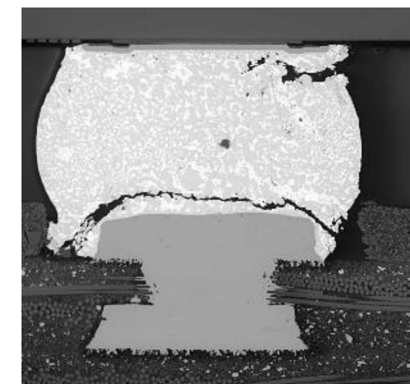




Cross-sectional SEM image showing the FIB-polished second cross-section of the solder bump after TCT for (a and b) 500 cycles, (c and d) 1500 cycles, and (e and f) 14,410 cycles.

Liang, Y. C., H. W. Lin, H. P. Chen, C. Chen, K. N. Tu, and Y. S. Lai. "Anisotropic grain growth and crack propagation in eutectic microstructure under cyclic temperature annealing in flip-chip SnPb composite solder joints." *Scripta Materialia* 69, no. 1 (2013): 25-28.

Solder bump solder fatigue



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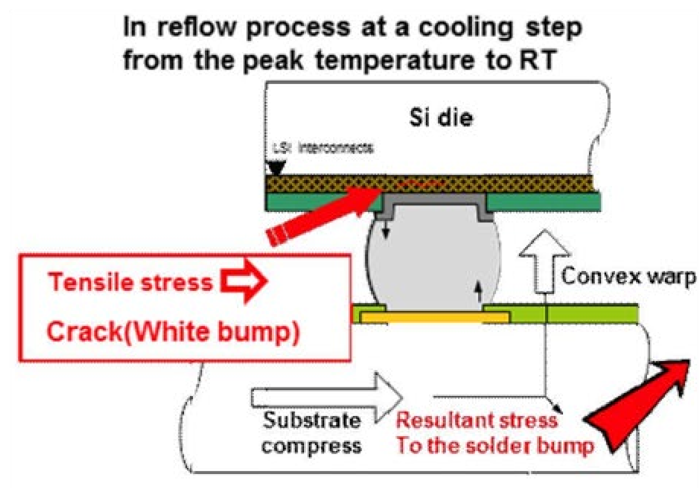
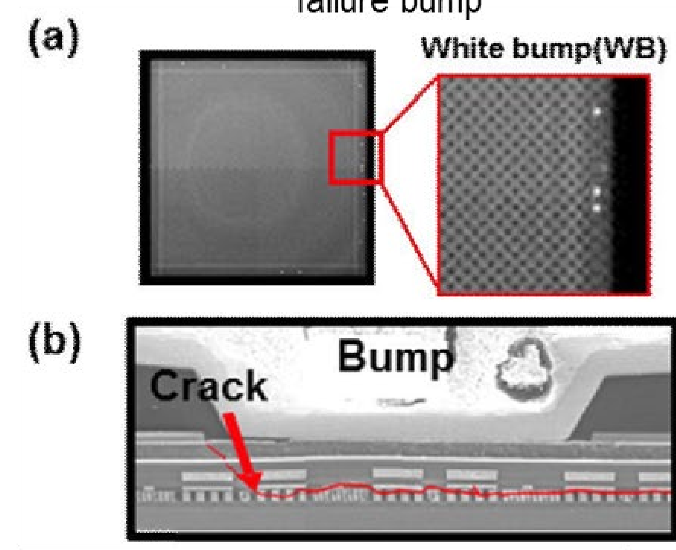
Passivation: Low-K Dielectric Cracking

- Failure of the brittle low-k dielectric layer can form from delamination or cracking under either reflow or thermal cycling (accelerated test or use condition)
- Bump material, underfill and chip structure and dielectric type are governing factors in low-k cracking

Mechanic of "white bump" failure generation



(a) Typical white bump failure image by SAT
(b) Example of cross sectional image of the failure bump



Kawahara, J., I. Kume, H. Honda, Y. Kyogoku, F. Ito, M. Hane, K. Kata, and Y. Hayashi. "A simple model-base prediction method for delamination failures in Low-k/cu interconnects with flip chip packages." In *2013 IEEE International Interconnect Technology Conference-IITC*, pp. 1-3. IEEE, 2013.

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Summary

Advanced packaging is a critical enabler for next-generation systems, both commercial and defense

Successfully creating a complex 2/2.5/3D package requires close coupling between design and manufacturing processes ***across the entire value stream***

Package reliability is closely connected to the chip design(s), package design, manufacturing/process technology, and stress conditions for a given use case

Important parameters in the flip chip assembly process:

- Die/substrate warpage
- Substrate pad surface conditions
- Cleanliness of components and assembly (flux residues, etc.)
- Underfilling process and materials

Primary failure modes in flip chip packages:

- Electro-migration
- Electro-chemical migration
- Solder bump / Cu-pillar joint fatigue
- Dielectric cracking

Implementing Design for Manufacturability (DFM) / Design for Reliability (DFR) across the AP value stream is essential for creating complex, reliable advanced packages

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