

ESA recent challenges in space missions: Cracked capacitors time bomb & Forbidden solderless connectors

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European Space Agency - ESA



In-Orbit
Failures

High Data
Rate

In-Orbit Failures

When a "simple" component causes Satellite in-orbit failures!

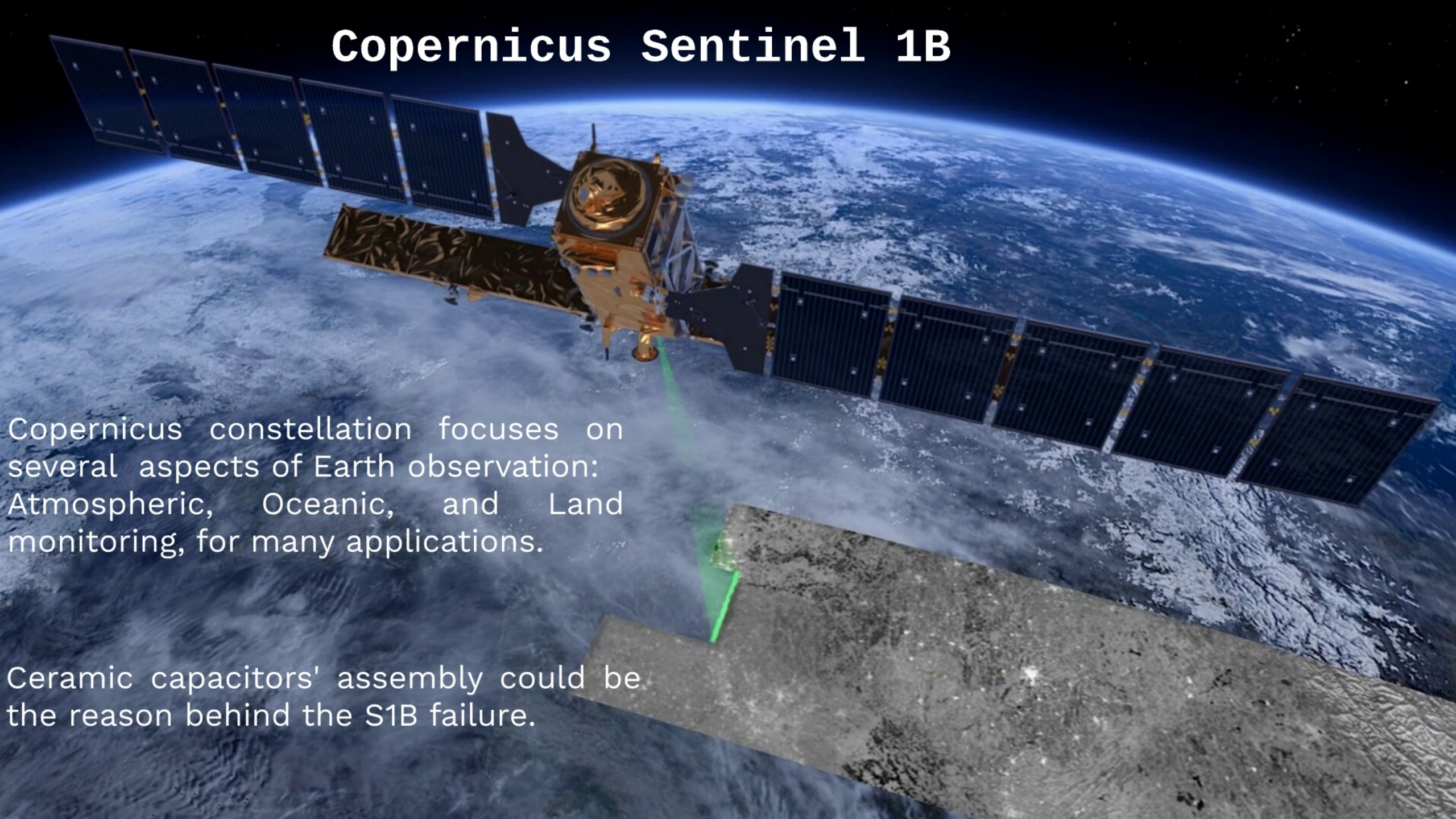


Sentinel 1B

Copernicus Sentinel 1B

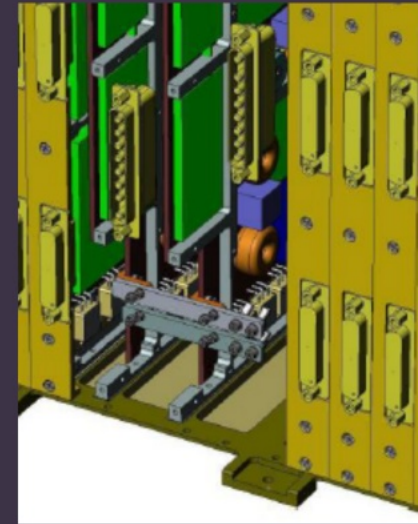
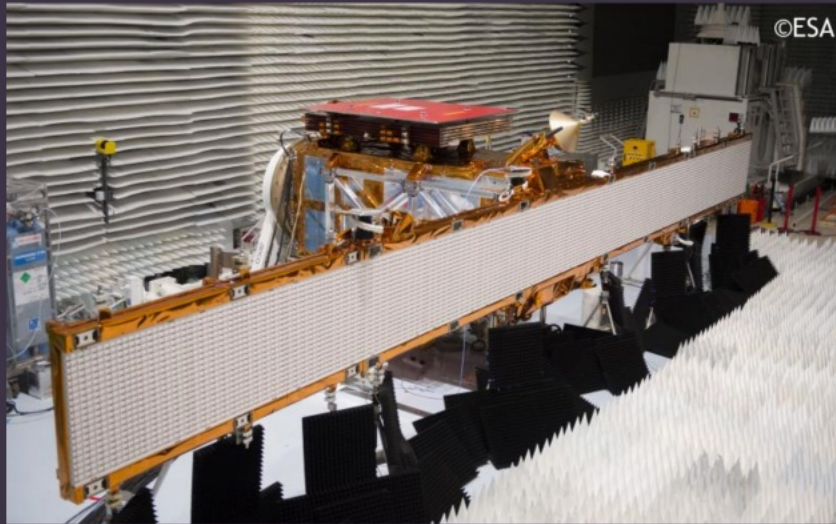
Copernicus constellation focuses on several aspects of Earth observation: Atmospheric, Oceanic, and Land monitoring, for many applications.

Ceramic capacitors' assembly could be the reason behind the S1B failure.



Copernicus Sentinel S1B: The Failure

Sentinel-1B synthetic aperture radar (SAR) payload has malfunctioned and has ended the spacecraft's mission more than six years after its launch!



It was discovered that the main problem is related to the 28V regulated bus of the CAPS (C-SAR Antenna Power Supply), as it was observed that the main & redundant 28V power regulators were both unexpectedly OFF.

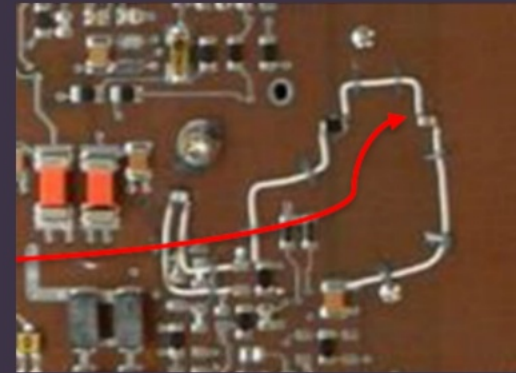
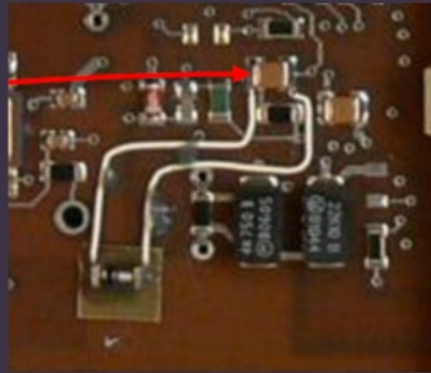
The CAPS is the unit –part of the electrical power sub-system of the platform –that provides power to SAR elements, including the SAR electronics.

Copernicus Sentinel S1B: The Root Cause

Detailed investigations were performed, to understand the root cause of the CAPS anomaly, with the identification of 18 potential failure modes.

The soldering process used on this capacitor is considered the most probable root cause for the failure of the main and redundant regulators.

The possible Root cause is the rework (direct wiring) of ceramic (Type II) capacitors!



This capacitors had to be replaced as a result of a non-compliance detected during the manufacturing and testing phase. For the repair, the capacitors were soldered using a direct wiring soldering process.

Copernicus Sentinel S1B: The Root Cause

At the time of this rework, direct wiring on the capacitor was fulfilling applicable product assurance requirements. This repair process is no longer authorized following revision of applicable ECSS standard in 2017:

Type II chip ceramic capacitors shall not be reworked.

Reprocessing shall not damage the device.

NOTE Reprocessing of ceramic chip capacitors is advised to be avoided due to potential crack formation.

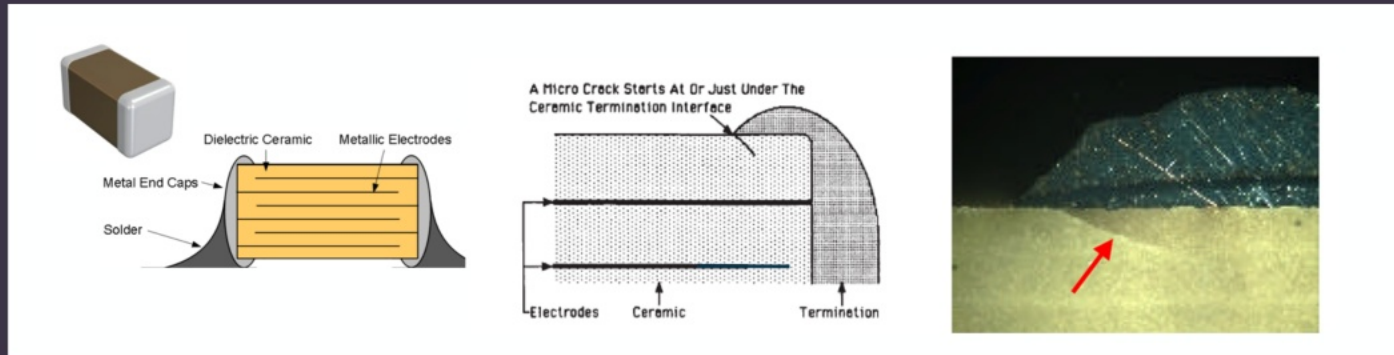
Since 2019, Memo ESA-TECQTM-MO-1143 also forbids direct wiring of ceramic capacitors type II and recommends the use of dedicated patch boards.

Wiring directly on the component termination (eg. Component bonded on PCB and wiring connection made) and wiring made on the same PCB pad than the capacitor (modification after component assembly) shall not be performed due to possible damage within the component such as crack in the ceramic.

It is recommended either to use a patch board with separate pads for the wiring (for addition of a capacitor) or to replace the capacitor during the wiring (modification applied after assembly)

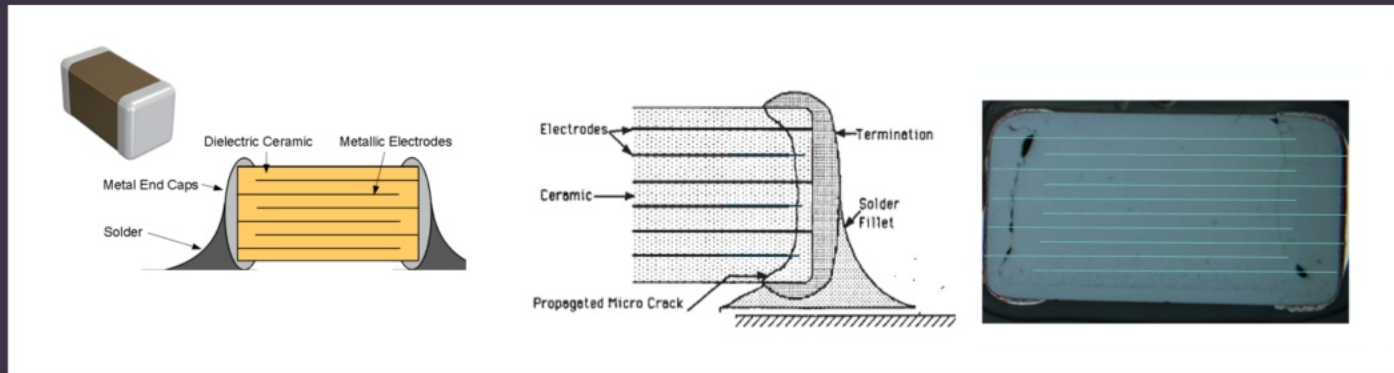
Copernicus Sentinel S1B: The Failure Mechanism

During direct soldering of wire on chip ceramic capacitors, heat distortion occurs inside the chip capacitor.



A crack occur: It starts at the weakest point at the interface between the ceramic and the end point of the termination.

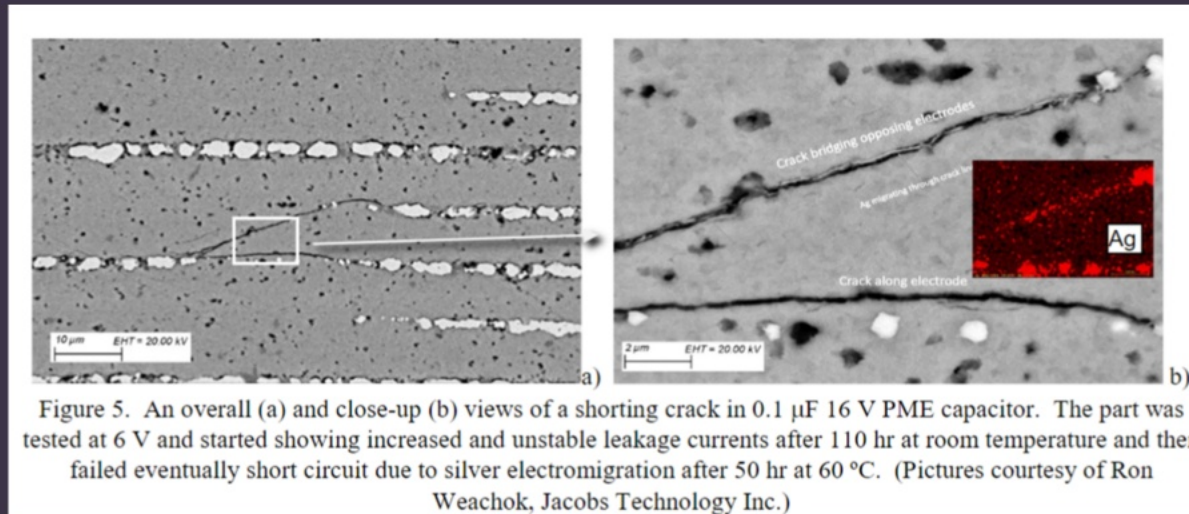
After several thermal cycles, the thermal shock crack propagates:



Copernicus Sentinel S1B: The Failure Mechanism

Diffusion and migration of Ag into dielectric layers from inner Ag or Ag/Pd electrodes might pose a problem for long-term reliability.

Silver is a material that is most susceptible to electromigration in the presence of moisture, and for this reason, cracking of PME (Precious Metal Electrode) capacitors creates a high risk of electrical failures.



This results to excessive current leakage.

As the leakage current gradually increases, the heat generated by the capacitor continues to increase, which will eventually lead to dielectric thermal breakdown failure and a **short circuit**.

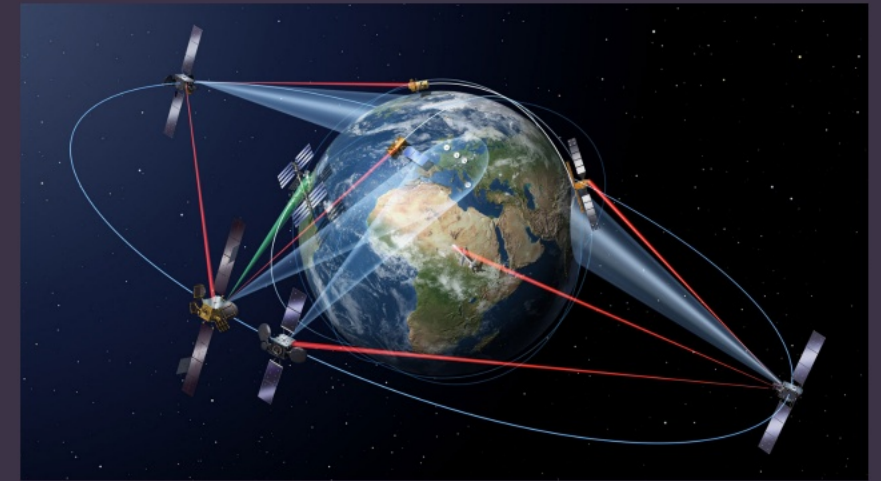
Copernicus Sentinel S1B: Conclusions and LL

Cracks were generated during the direct wiring soldering on the capacitors. Silver Electromigration has then caused a Short-Circuit.

The Satellite S1B has been retired and will be de-orbited according to space de-orbiting rules.

S1A has the same assembly process (Fingers crossed!).

S1C and S1D have been assembled according to the latest ECSS standard, that forbids direct wiring on the capacitors!



Micro-cracks in capacitors generated during assembly can be considered as a **“time bomb”**.

In order to avoid similar issues on Tantalum capacitors and Flexible ceramic capacitors, an internal YGT research is being conducted by Adrià Escoda Marches to perform reliability tests and gather enough data to forbid (or to authorize?) similar processes (direct wiring) on Tantalum SMD capacitors and flexible ceramic capacitors.

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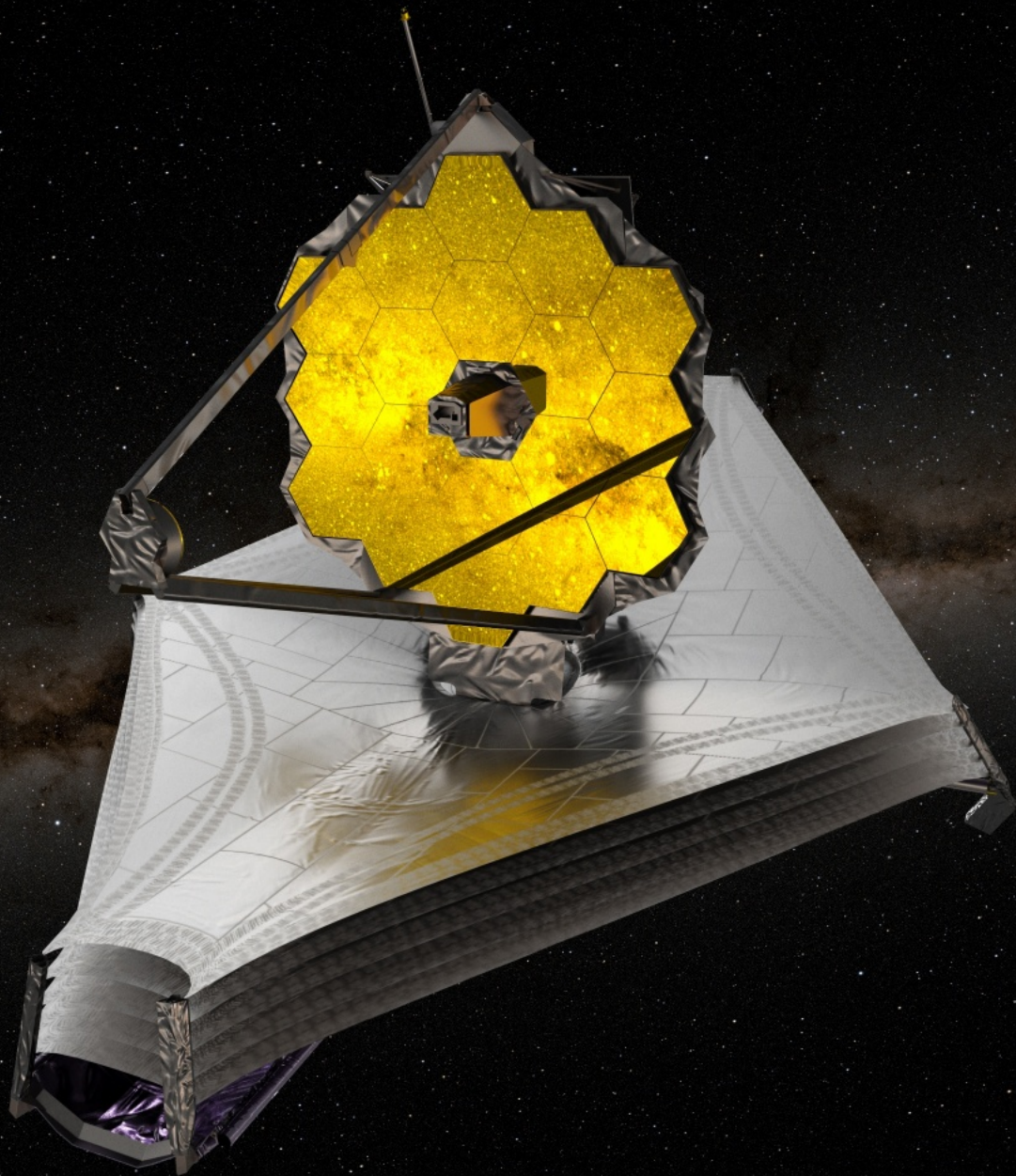
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In-Orbit
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High Data
Rate



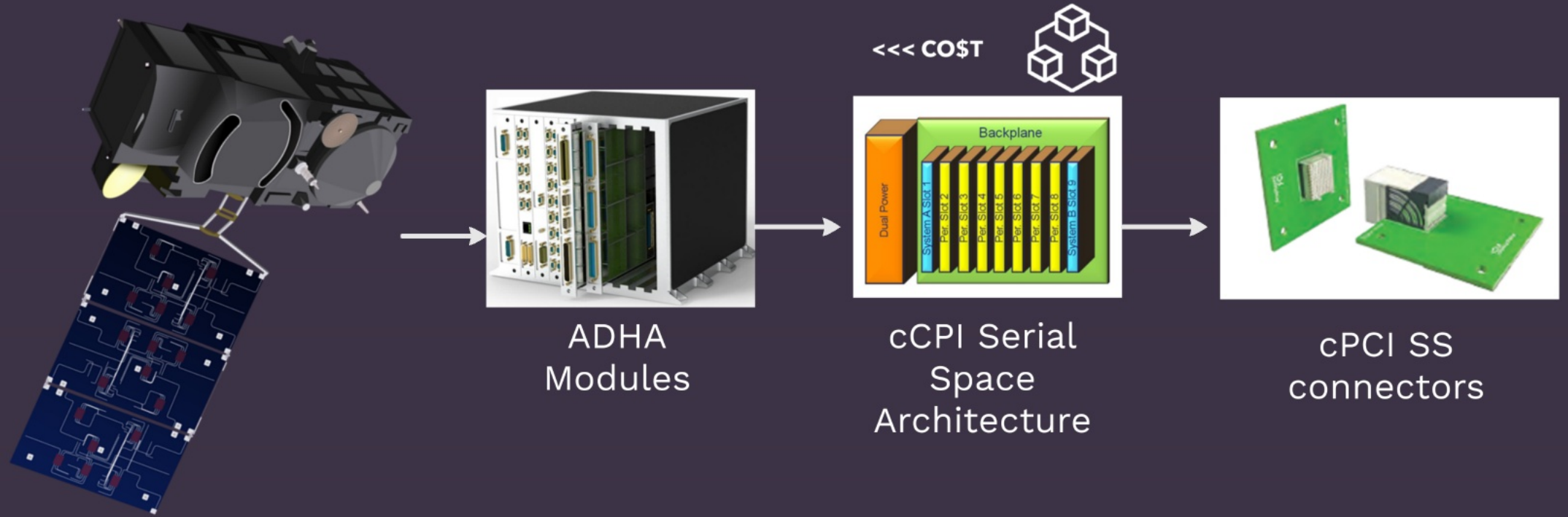
Background



Specification
&
Challenges

On-going
Activities

Background:

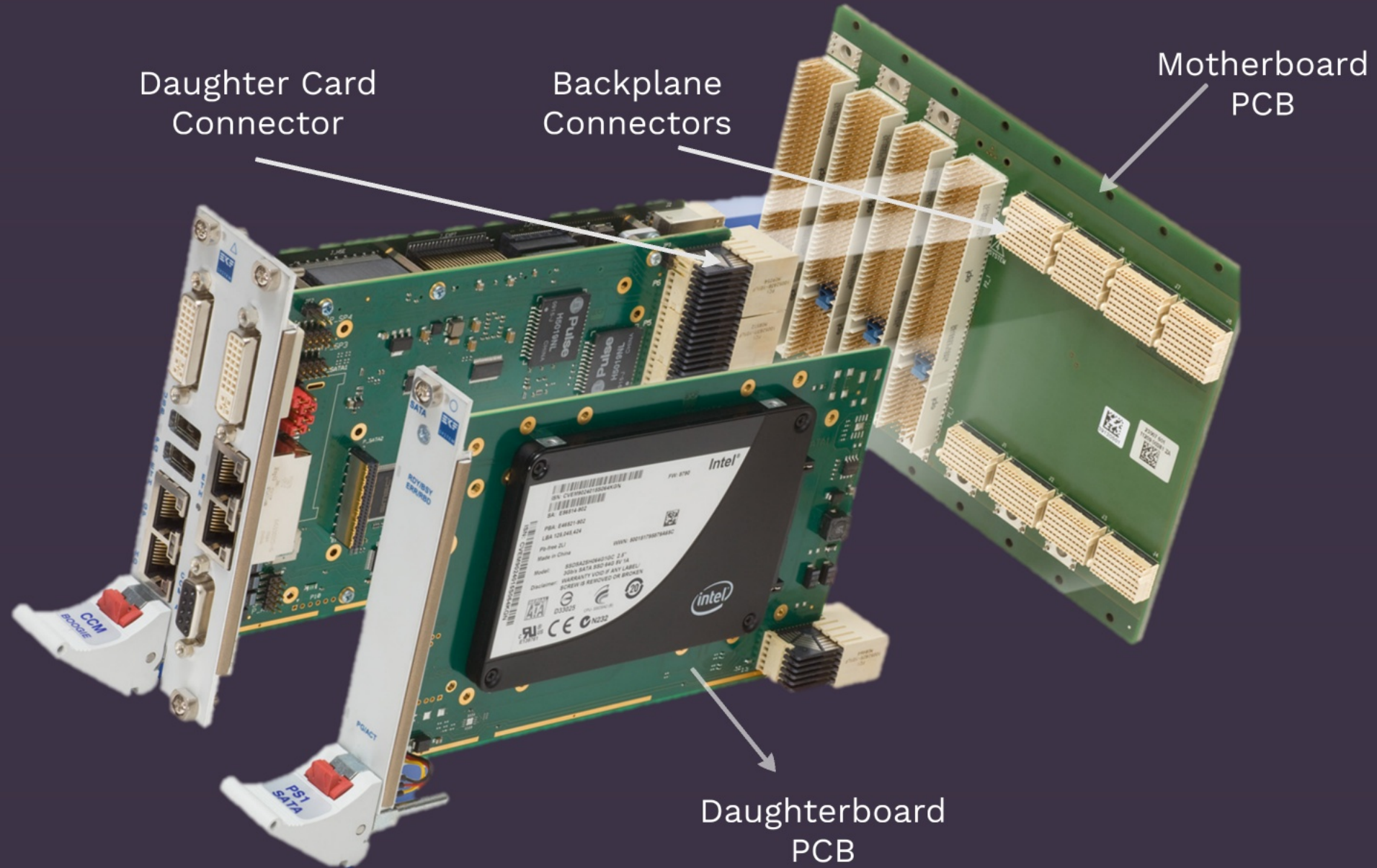


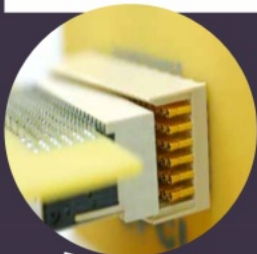
The current large increase of data traffic pushes the space sector to pursue communication standards that allow for higher data rates.

In order to develop the European Advanced Data Handling Architecture (ADHA) units, the compact Peripheral Component Interconnect Serial Space (cPCI SS) standard was selected.

The need is to develop and qualify a backplane solderless connector that reaches 25 Gbits/s (and up to 50 Gbit/s).

Use case of backplane connectors





cPCI

Manufactured by Smiths Interconnect (Hypertac) 

Compatible with cPCI and NASA DLA Qualified

Based on the hyperboloid contact technology

Resistant to Shock & Vibration

Standard soldering reflow, **not solderless!**

High Data Rateup **only up to 3.12 Gb/s**



KVPX

Manufactured by Smiths Interconnect (Hypertac) 

Solderless Solution, based on Press-fit

High Data Rate up to 16Gb/s

Based on the hyperboloid contact technology

Resistant to Shock & Vibration

Compatible with VITA, and **not compatible with cPCI SS**



Airmax

Manufactured by Amphenol  

Compatible with cPCI SS

Solderless Solution, based on Press-fit

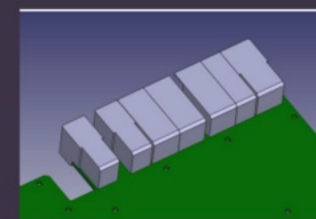
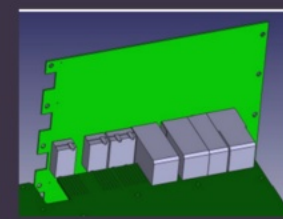
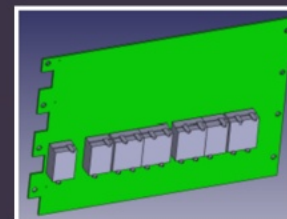
Specified up to 25 Gb/s

Low cost, but **not proven** in harsh environment

No available reliability data!

The available solutions are either not compatible with cPCI-SS or do not reach the required 25 Gb/s
Therefore the need to develop, manufacture and qualify a space-grade High Data Rate connectors compatible with cPCI SS!

Specification and Challenges



ADHA



AIRBUS

beyond gravity

ThalesAlenia
Space
a Thales / Leonardo company

AIRBUS		Ref : DOC-433-0902-0102 Issue : 02 Rev : 00 Date : 15/03/2021 Page : 1	
Specification Document : cPCI Serial Connector for Space			
	Name and Function	Date	Signature
Prepared by	Christian LOPES-GUNTAS Application Engineer		
Verified by	Hassan EL ANDBAKH EEE Manager		
Approved by	Simon RUSSEK Project Manager		
Authorized by	Olivier GUERARD Head of Equipment Support France		
Document type	No WBS	Keywords	
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Main Challenge w.r.t. ADHA Specification:

- High Speed up to **25 Gb/s**
- **Solderless** solutions (i.e. Press-fit)
- Operating Temperature: -55°C to 125°C
- No impedance change or discontinuity of **1ns** or longer duration during mechanical and thermal tests
- Current rating per contact: **2 A**

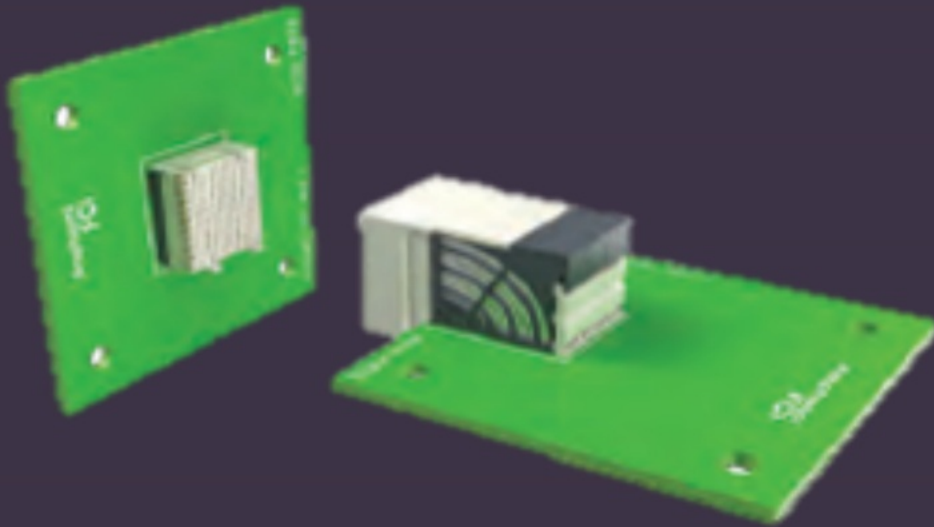
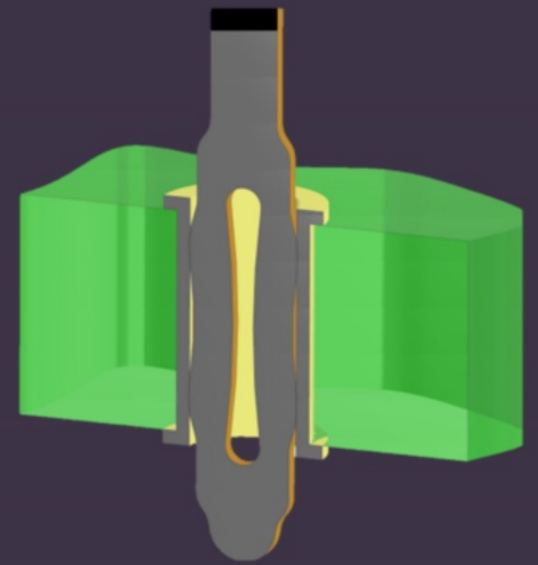
Specification & Challenges

- **Known reliability issues related to the press-fit technologies:**

- 1.- Impedance discontinuities during mechanical tests**

All the mechanical stress goes through the press-fit terminations.
This leads to intermittent loss of connectivity during vibration or shock.

No clamping mechanism (or additional screws) to hold the mated pair together.



Specification & Challenges

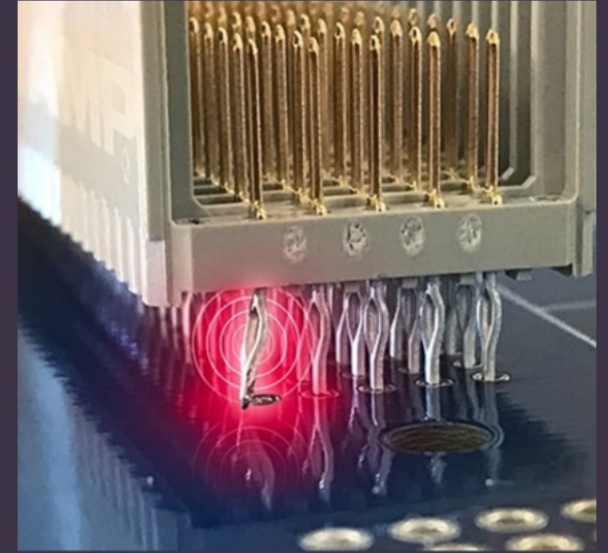
- **Known reliability issues related to the press-fit technologies:**

- 2.- PCB Damage due to fretting of the plating materials**

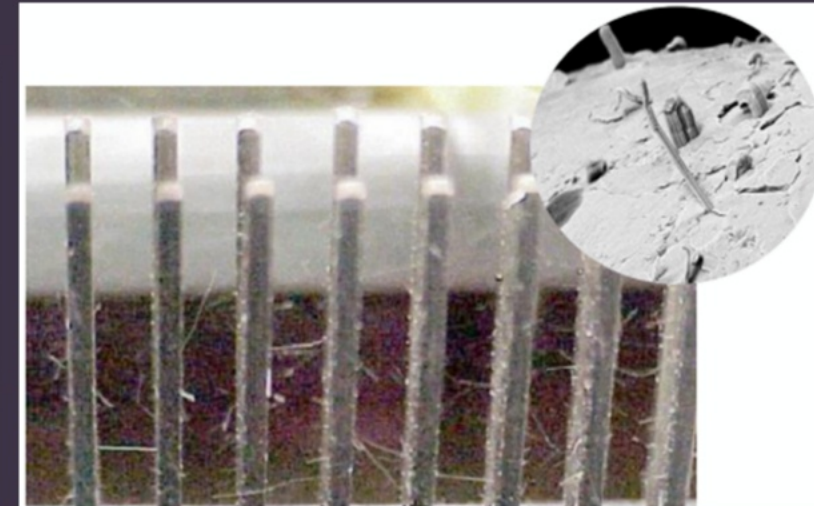
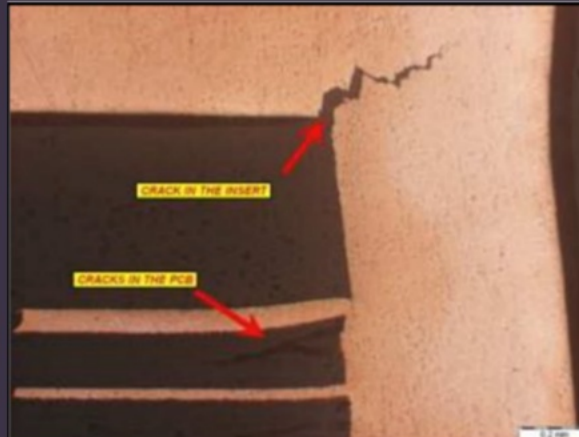
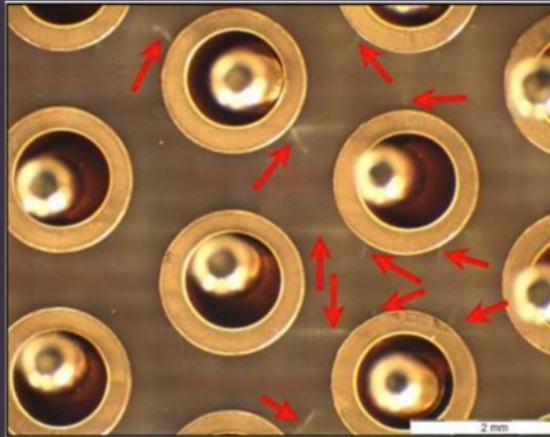
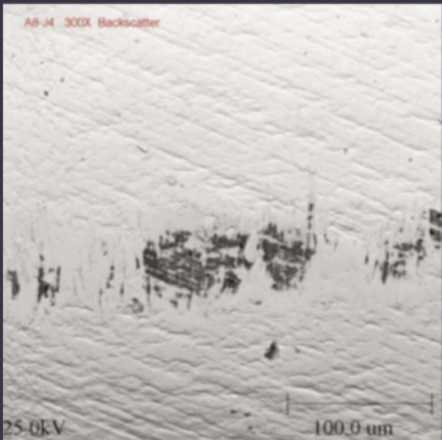
corrosion wear or cracks in PCB and pin materials, due to the relative movement of the press-fit pins inside the PCB.

- 3.- Growth of dendrites**

tin whiskers on pins with pure tin are also considered as delayed failures



This leads to an increase in contact resistance, thus a drastic decrease of the data rate!

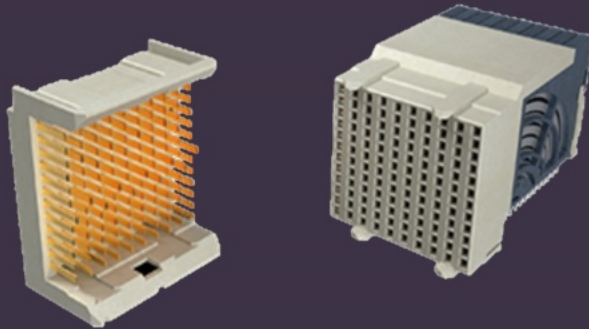


On-going Activities @ESA

"Procurement and reliability assessment of high data rate press-fit cPCI SS connectors"

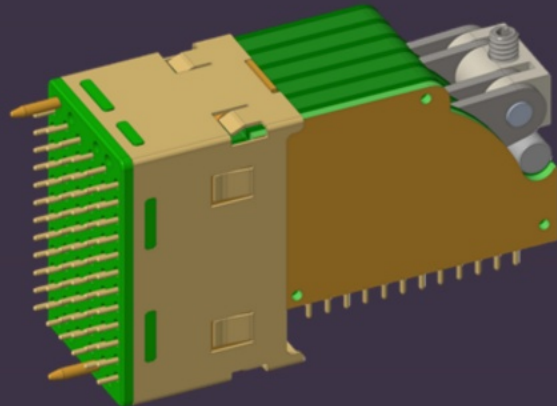
The aim of this activity is double:

1.- To procure and assess the reliability of existing high data rate press-fit connectors compatible with cPCI SS: The commercial AirMax® manufactured by Amphenol, USA/China.

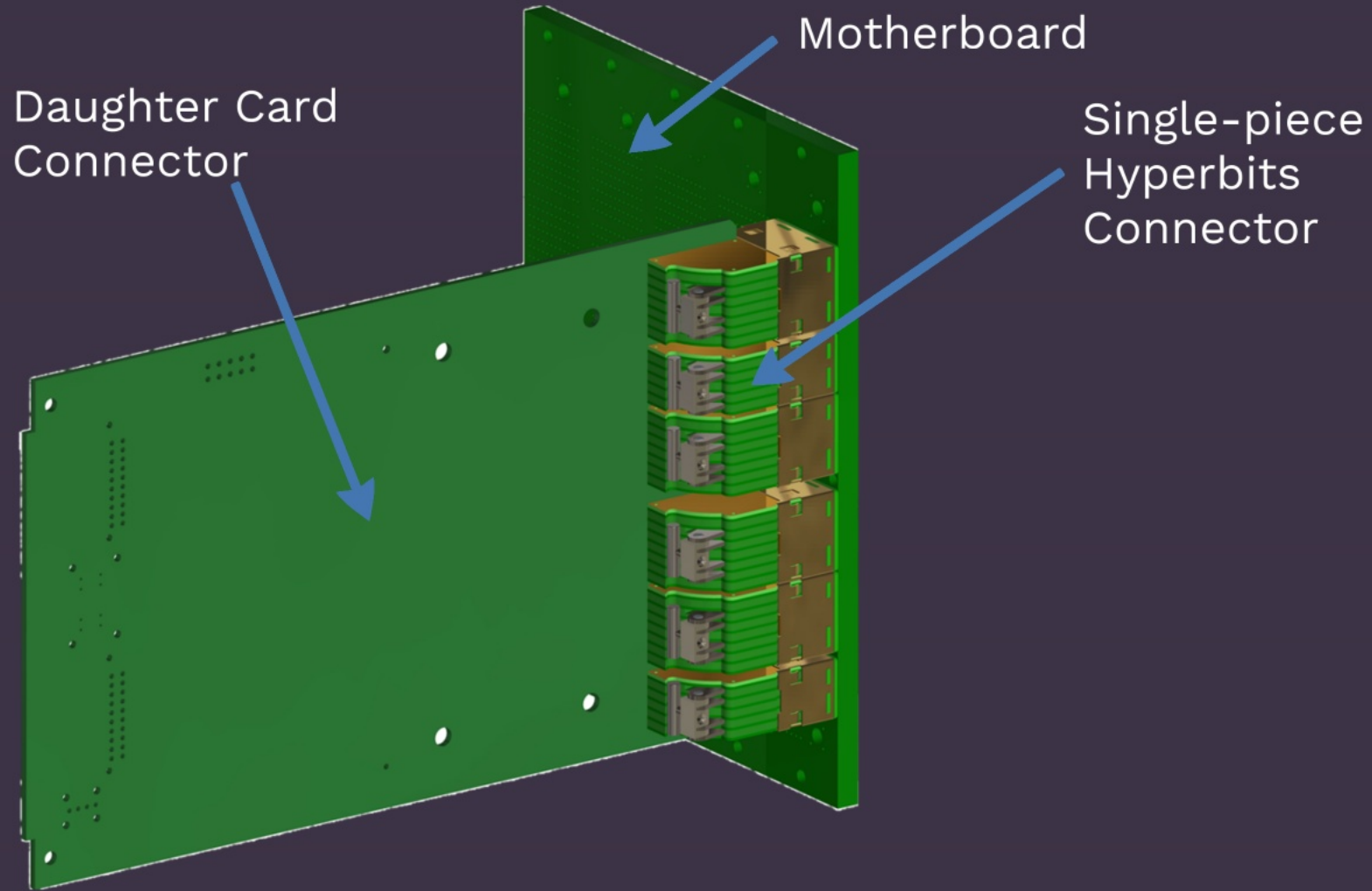


Amphenol

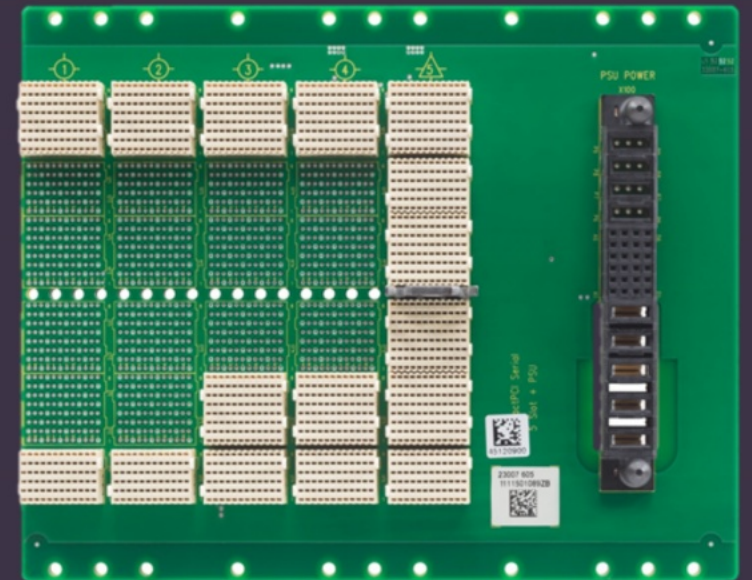
2.- To support the development and assess the reliability of the HyperBits™ S-FECT (Performance Interconnect, FR).



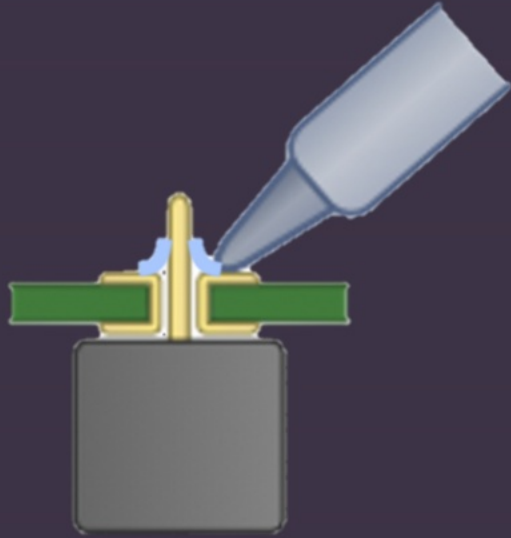
On-going Activities: Hyperbits?



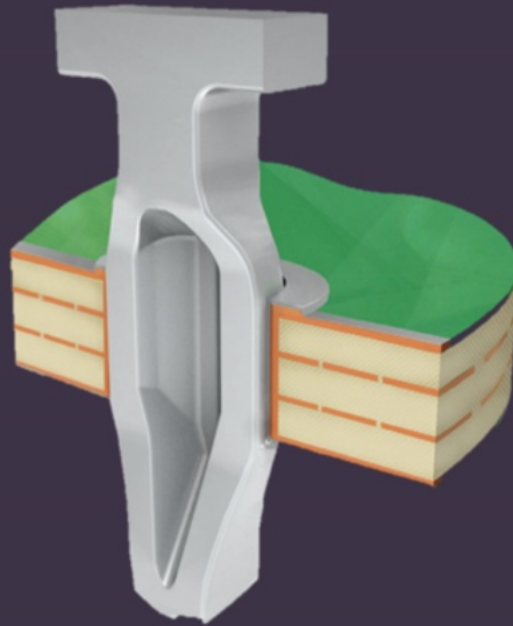
Eliminates the backplane connector



On-going Activities: Hyperbits?



NO hand soldering



NO press-fit

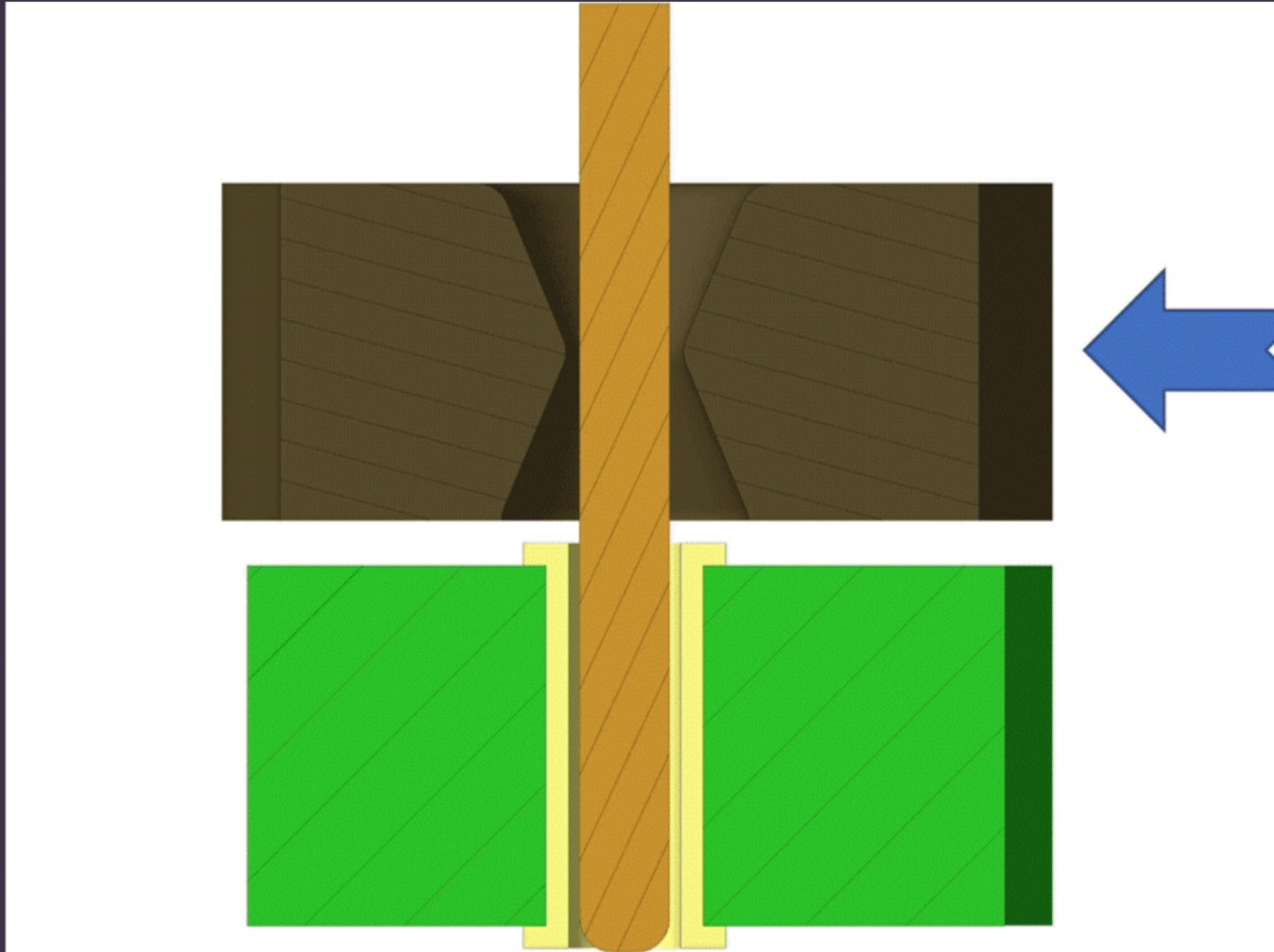


<Higher
normal
Force

>Lower
resistanc

Based on **S-FECT**
Technology
Contacts slide and operate
in elastic deformation

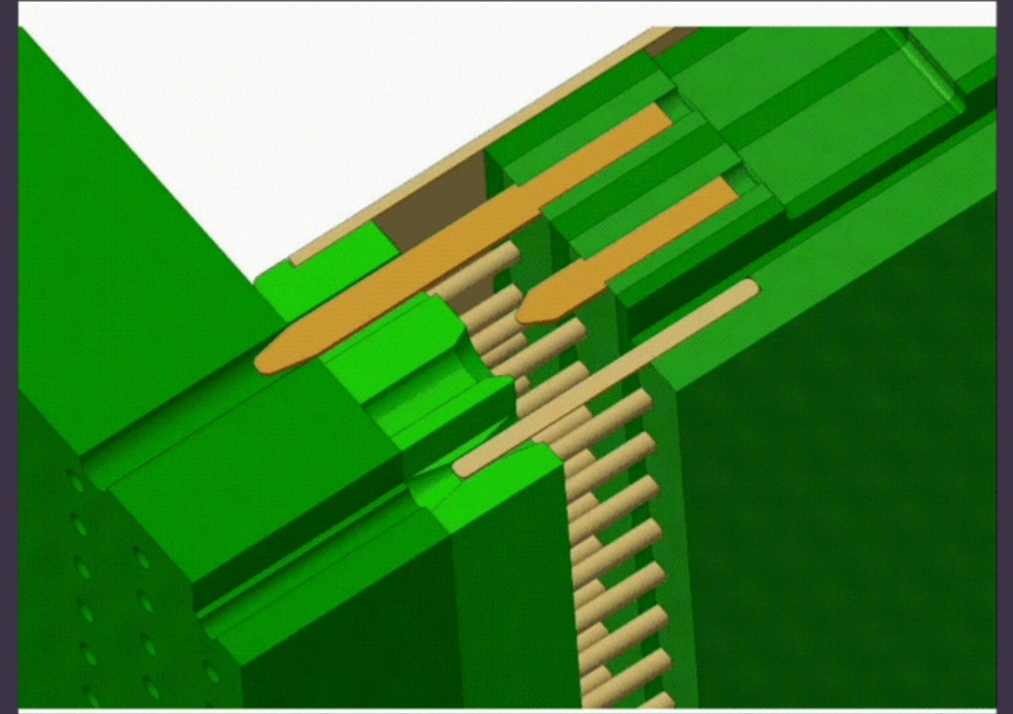
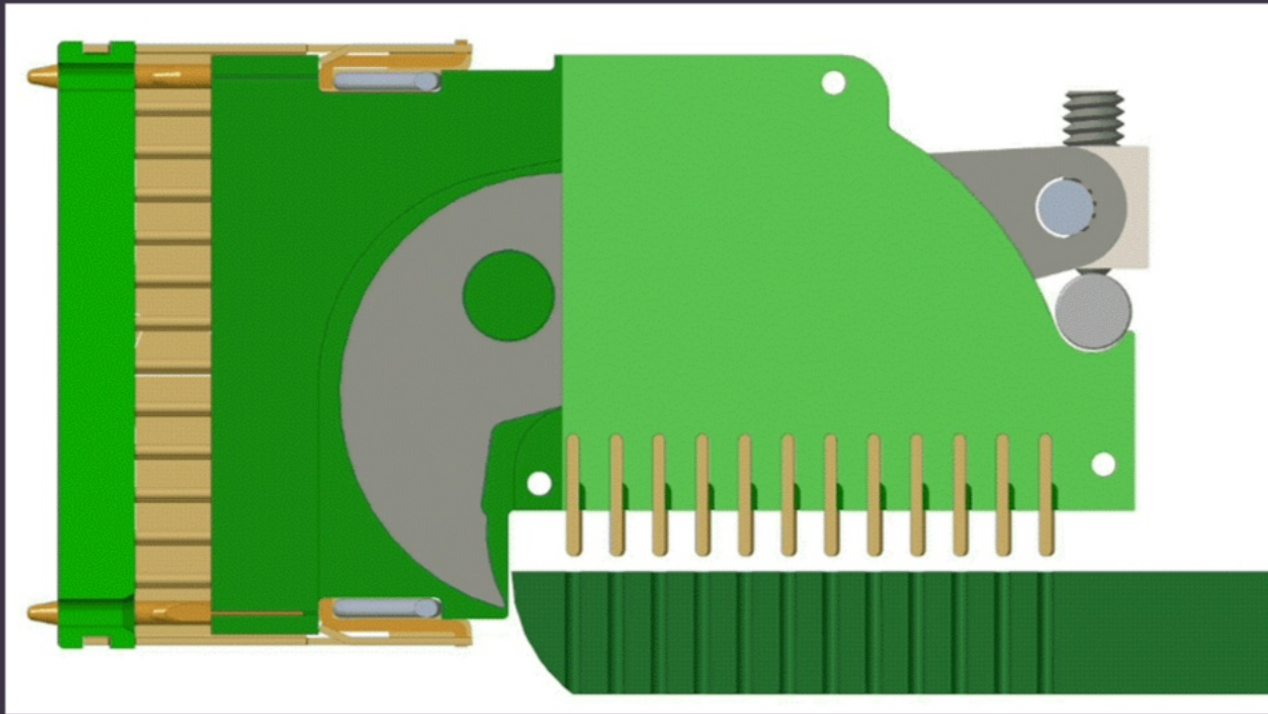
On-going Activities: Hyperbits?



SLIDE-**F**IT
ELECTRICAL
CONTACT
TERMINATION

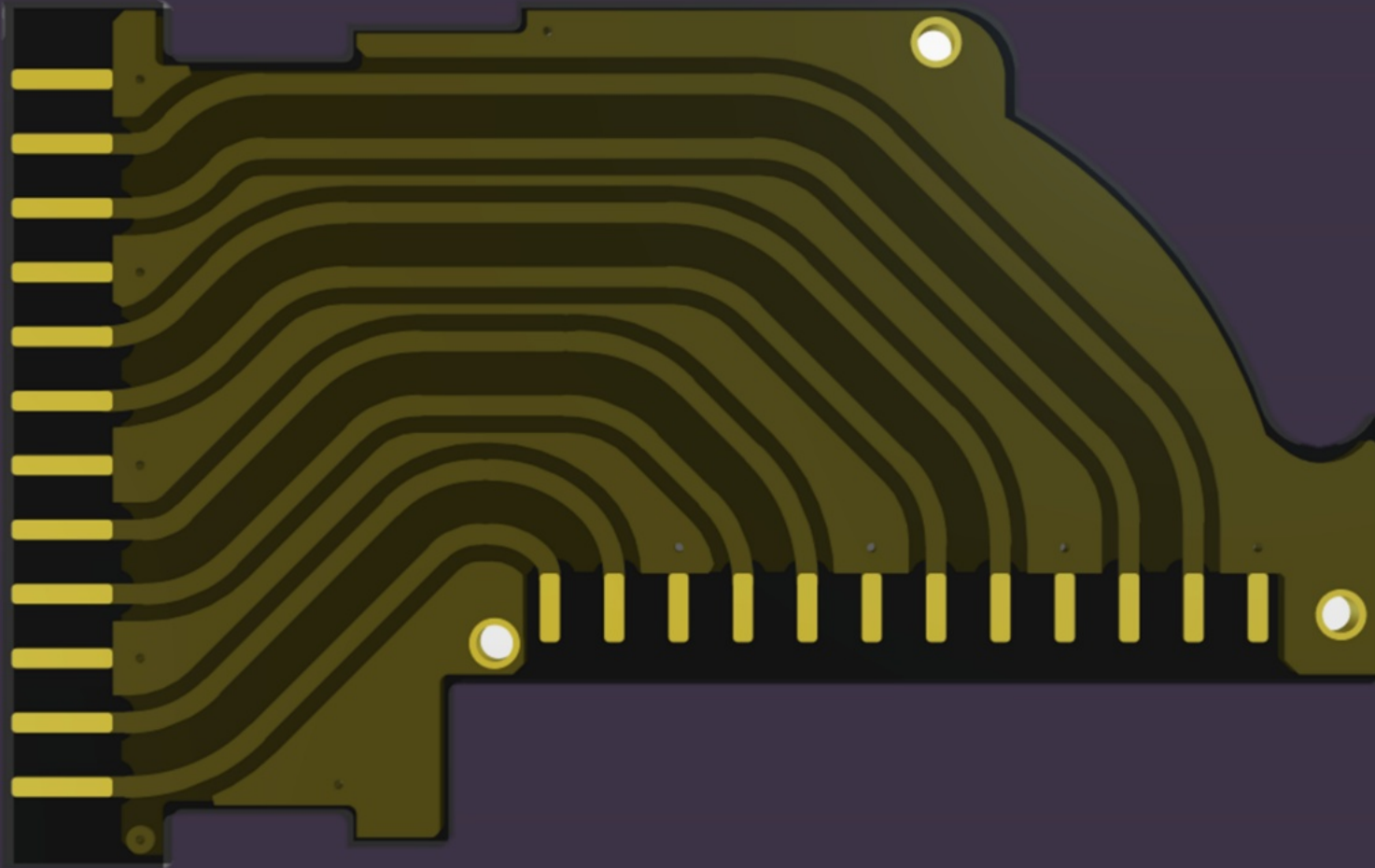
On-going Activities: Hyperbits?

A Single-piece connector which blind-mates directly with the backplane!



The mechanical function is fully separated from the electrical function



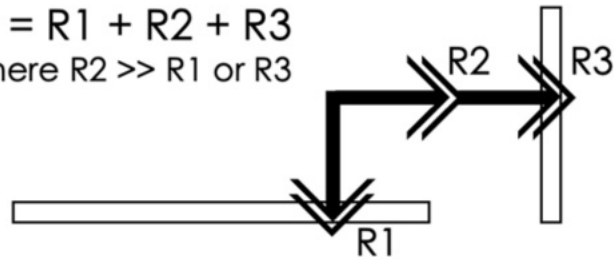
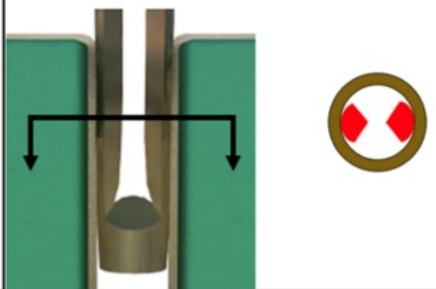
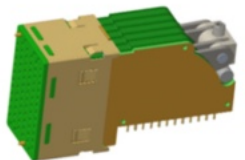

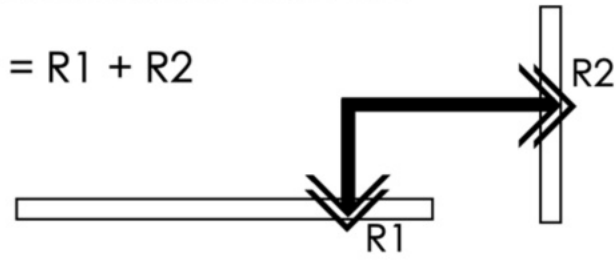
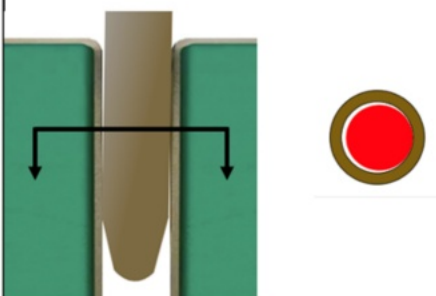
On-going Activities: Hyperbits?



Eliminates the discontinuity between the internal tracks of the connector.

Based on “Tachyon 100G” material of internal PCB, given for high speed up to 100Gb/s.

On-going Activities: Hyperbits vs Airmax ?

Traditional Press-Fit Technology 	Cost of components and total installed cost:  Requires special assembly tooling	Total resistance PCB to PCB: $R_t = R_1 + R_2 + R_3$ where $R_2 \gg R_1$ or R_3 	Increased current density in reduced cross-section: 
S-FECT™ Technology 	Cost of components and total installed cost:  No special assembly tooling required	Total resistance PCB to PCB: $R_t = R_1 + R_2$  Same logic applies to impedance	Constant current density in continuous cross-section: 

Evaluation tests are being performed on both connectors.

Two new Activities are (or will) be initiated in order to further develop, optimise and qualify the cPCI HDR connectors for space applications!

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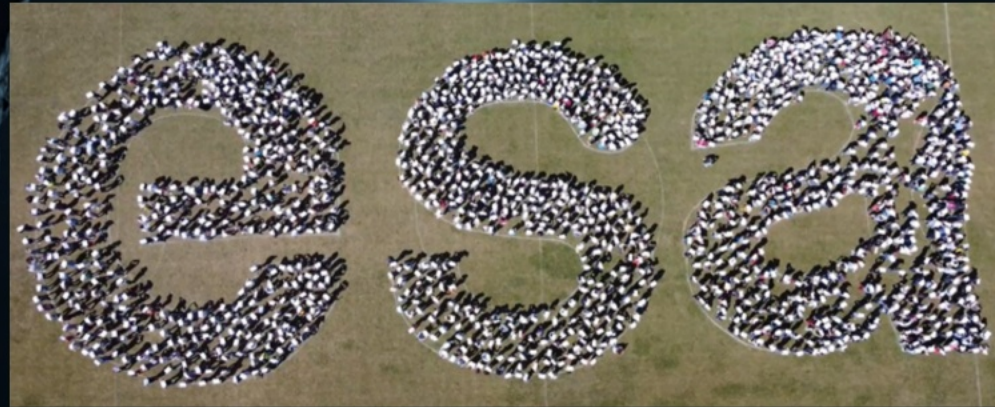
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