







PWB defects on Overhaul & Repair assemblies Analysis and Variances to J-STD-001 & IPC-A-610

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Outline

- ✓ CCA assembly history; Reason for analysis
- ✓ Standards assessment; Definitions of PWB violations
- ✓ PWB assessment; General construction & characterization of the J-STD / IPC defects
- ✓ Detailed Visual & X-Ray analysis
- ✓ Key Findings and Recommendations



CCA History & Analysis Requested

- CCA assembly evaluated and repaired during Overhaul and Repair (O/R) activities, on a mature legacy program
- PWB around connector P2 subjected to excess thermal stress during rework, resulting in the core being discolored / blistered. CCA originally built / inspected to <u>Class 3</u> requirements Violates-

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J-STD-001H 9.1.1 Blistering/Delamination & 9.1.9 Burns IPC-A-610H 10.2.2 Blistering and Delamination 10.2.6 Burns
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- The subject repaired CCA, passed extensive electrical and environmental tests
- Program requested Visual & X-ray analysis to determine if there is evidence of underlying damage / degradation that cannot be detected through inspection
- Provide an assessment of PWB construction and resulting damage, to determine viability
- CCA is a dedicated spare assembly, no longer in production and <u>cannot</u> be replaced

Use case is unique. Requires additional assessment & analysis beyond standard inspection practices



Standards Assessment: J-STD-001H & IPC-A-610H

- J-STD-001: No Visual aid examples provided. Defines defects
- **9.1.1 Blistering/Delamination** [Class 1-3]: Shall not **exceed 25%** of distance between plated through-holes or internal conductors. Shall not reduce space between conductive patterns to less than minimum electrical clearance.
- **9.1.9 Burns** [Class 1-3]: Shall not **physically damage** the surface of the assembly. *Open to interpretation*
- IPC-A-610: Visual aid examples provided. Defines acceptable anomalies and defects
- **10.2.2 Blistering/Delamination** [Class 2-3 defect]: Exceeds 25% distances between plated through-holes or internal conductors. [Class 1-3 defect]: **Reduces space** between conductive patterns **below minimum clearance**.
- **10.2.6 Burns** [Class 1-3 defect]: Burns that **physically damage** the surface or assembly. **Open to interpretation**

J-STD-001 takes a defects approach; IPC-A-610H Provides acceptance / rejection criteria with examples



PWB Assessment- Overall construction

Older RF board design- Includes a rigid center portion (fiberglass epoxy reinforced substrate)

Ground plane features- laminated on front and backside surface layer, no solder mask

RF circuit traces- Also laminated on the front and backside surface layer, no solder mask

Control, Power, Ground- Interconnects completed with plated thru holes & 2 additional layers. Traces go to <u>P1 connector ONLY</u>

Basic 7-layer board design- *NOT* similar to current process FR4 Multilayer copper construction (12-36+ layers)

Induced heat damage defects do not pose the same degradation risk in this configuration, when compared to complex multi-layer board designs

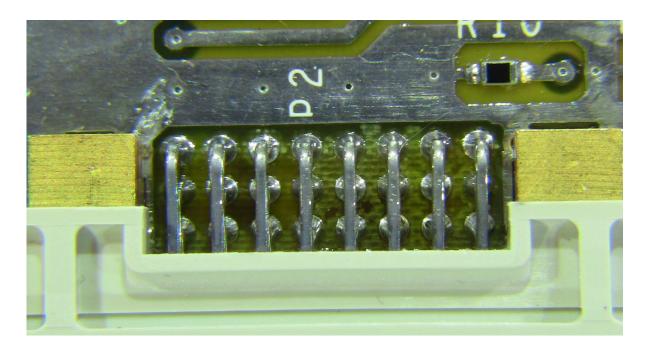
Extent of localized damage requires further review



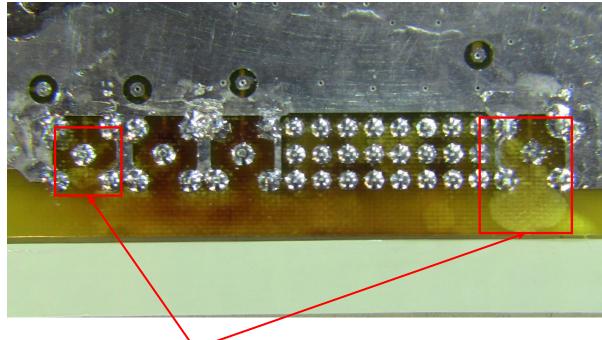
Visual Assessment- Rework Affected P2 Area

Images owned by Raytheon Technologies

P2 Connector Front side- Fiberglass separation



P2 Connector Backside- Discoloration / Blistering



Potential areas of concern

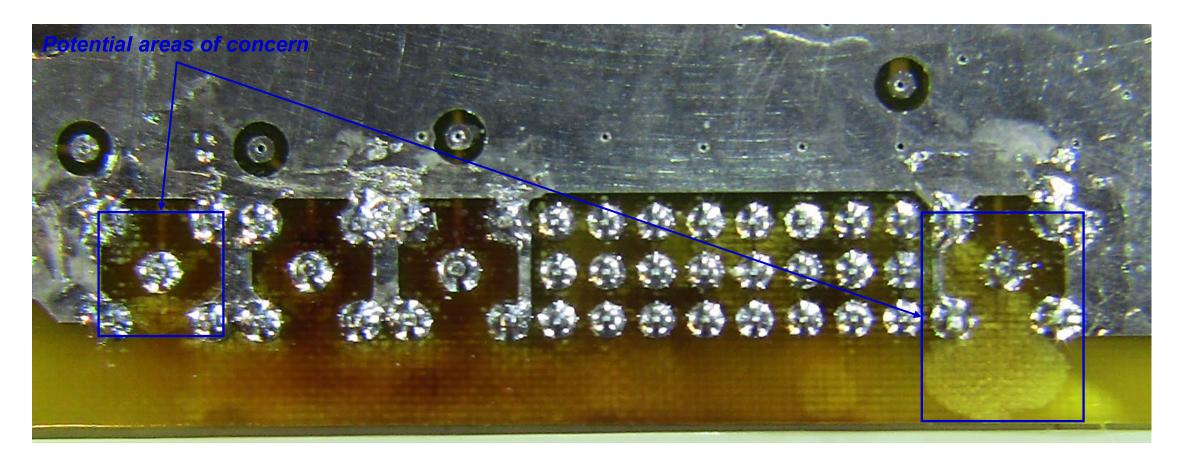
PWB substrate- Signs of heat stress & Internal blistered/separated fiberglass reinforcement from rework



Visual Assessment- Rework Affected P2 Area

Images owned by Raytheon Technologies

P2 Connector Backside- Close up, Discoloration / Blistering



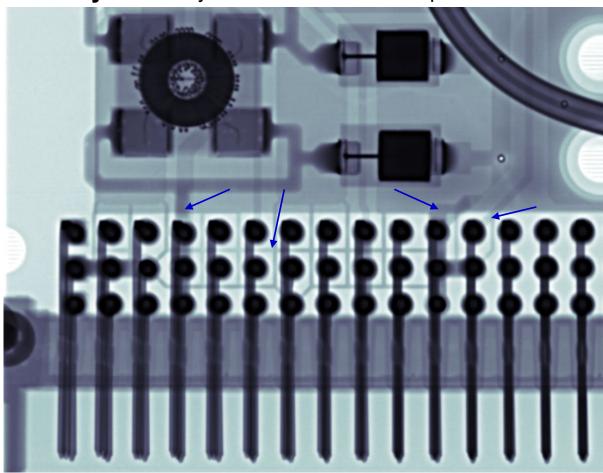
PWB substrate- Signs of heat stress & Internal blistered/separated fiberglass reinforcement from rework



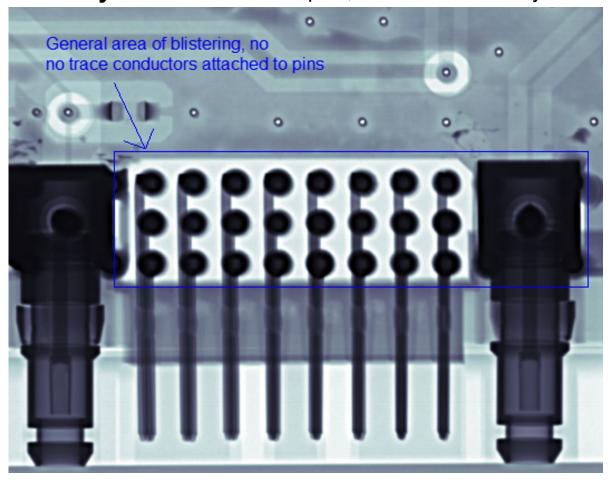
X-Ray Analysis- General Construction

Images owned by Raytheon Technologies

P1 X-ray- Active layer trace connections to pins



P2 X-Ray- No active traces to pins, RF connectors only



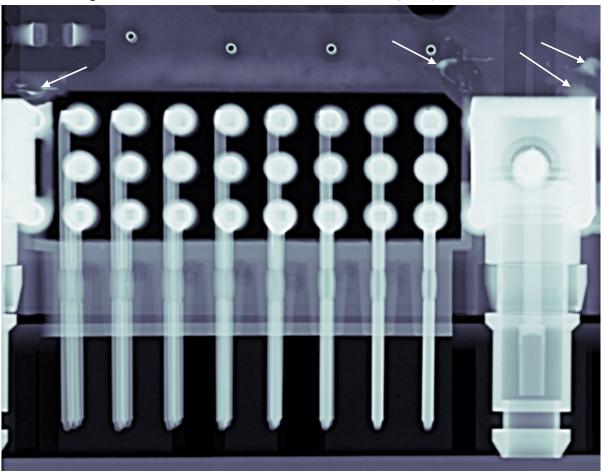
Connectors P1 & P2- Active traces P2 connector is pins ONLY



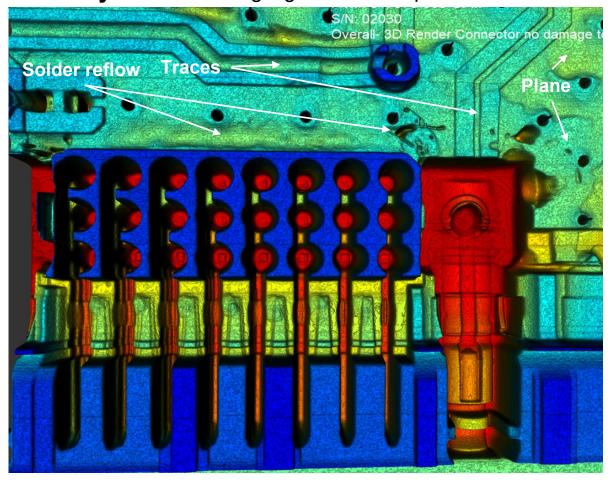
X-Ray Analysis- General Construction

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P2 X-ray- Area of concern, *Negative*. Highlights solder rework



P2 X-Ray- 3D Render highlights traces & planes



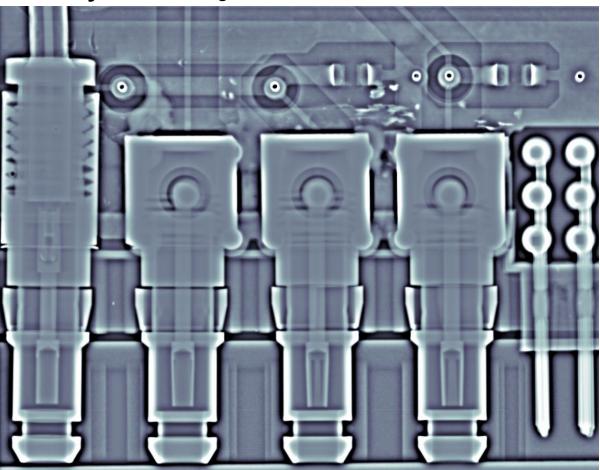
P2 Pins & RF Connector- Surface solder reflow highlighted, NO evidence plane or trace damage



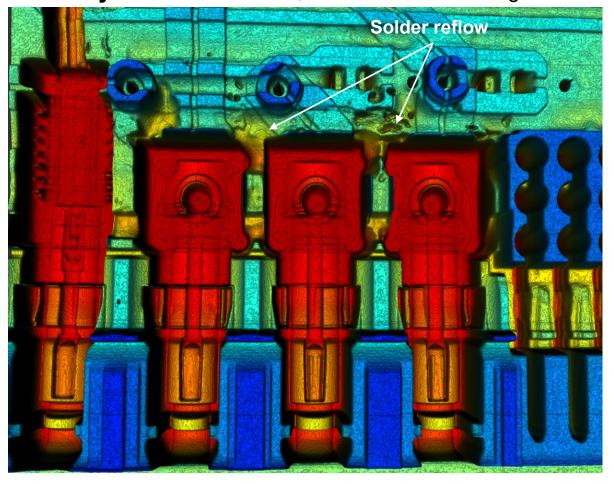
X-Ray Analysis- General Construction

Images owned by Raytheon Technologies

P2 X-ray- RF side edge enhancement, connectors In-tact



P2 X-Ray- RF side 3D render, no evidence of damage



P2 RF Connector Side- Edge Enhancement & 3D render show NO evidence plane or trace damage



Conclusions & Recommendations

Rework defects manifested as fiberglass disruptions / separation due to thermal stress

- ➤ NO copper inter-layer or pre-preg delamination in the P2 affected area
- > Can lead to failure in newer board designs, where there is active circuitry

Damage is located primarily where there are no active traces going to the pins on P2

- ➤ Adjacent RF connectors outside the damage area, are discolored
- > Two RF connectors show delamination / blistering on the PWB backside

X-ray shows there is no degradation of the active RF trace or ground planes

> Negative / Edge & 3D Render tools in R/T X-ray greatly improves assessment capabilities

Mechanical Integrity of the board and connector in this case are not compromised

Recommend: CCA bake out and the addition of an environmental barrier coating to mitigate moisture / contaminant ingress around the affected RF connectors

Review Findings and Recommendations at Customer MRB, use CCA "AS IS"



Thank you!

Questions???

