The Evolution of Moore's Law Through Chipletized Architectures

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Abstract ---As Moore's Law reaches its limits in monolithic applications and semiconductor technology node cycles become much longer, Heterogeneous Integration (HI) will both increase compute density and reduce design cycle times. HI 2.5D SiP technology is a powerful new trend in microelectronics driven by the slow-down of Moore's Law.

Keywords --- Heterogenous Integration, chiplets, Moore's Law, chipletized architecture, 2.5D integration, silicon interposer, RF system-in-package

Staying ahead of America's adversaries requires control of the electromagnetic spectrum and therefore an evolution of the sensor processing chain. Agile, chip-scale solutions at the sensor edge are needed to overcome data bandwidth and latency limitations that are inherent with legacy EW and radar systems. There is also a need to reduce design cycles, size, weight, power, and cost (SWaP-C). Heterogeneous, 2.5D integration is the next phase of Moore's Law, enabling a new approach to microelectronics based on chipletized architectures. The acceleration of deployable, modular, high-performance microelectronics to the tactical edge is achieved by integrating the best silicon offerings for analog, digitization, processing, memory, and AI functionality on to one chip *(Fig. 1)*.

Mercury is partnering with leading semiconductor providers to deliver to defense customers the only trusted, RF system-in-package (RFSiP) devices that utilize an ecosystem of advanced, die-level IP building blocks, called chiplets, purpose-built for each mission. Through assembly of high-density chiplets into a single device, high-speed die-to-die interconnects enable high-performance processing while reducing system complexity, latency, and SWaP-C. The use of open-standard, die-to-die interfaces such as AIB (Advanced Interface Bus) and UCIe (Universal Chiplet Interconnect Express), allow the mix of chiplets to be upgraded or modified more rapidly, to meet the intended use case. In this paper, Mercury explores how HI of state-of-the-art chiplets into a System in Package (SiP) device, coupled with a unique business model, can rapidly deliver next-generation EW and radar system solutions to the sensor edge.

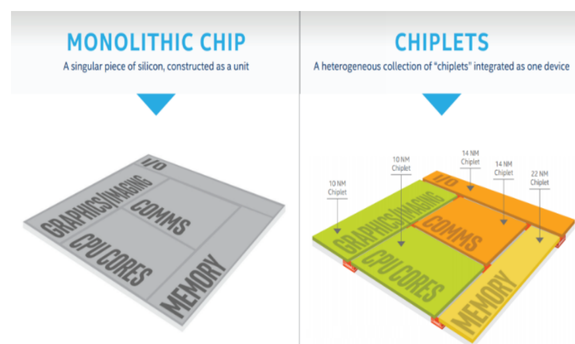

Fig. 1 Monolithic Silicon vs. Chipletized, Heterogeneous Architecture

A Flexible Approach to Semiconductor Design

As Moore's Law reaches its limits in monolithic applications and semiconductor technology node cycles become much longer, HI will both increase compute density and reduce design cycle times.

HI 2.5D SiP technology is a powerful new trend in microelectronics driven by the slow-down of Moore's Law *(Fig. 2)*.

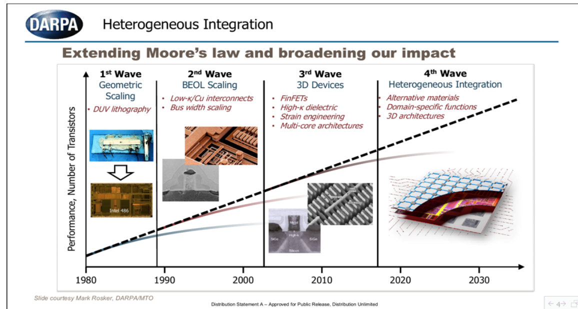

Fig. 2 Extending Moore's Law with Heterogeneous Integration

This design approach integrates individual intellectual property (IP) blocks called chiplets, as opposed to a monolithic solution where all the functionality is contained in a single semiconductor device. The IP in a chiplet performs a specific function, such as RF capture and transmission, ADC/DAC data conversion, digital I/O, FPGA-based digital signal processing, or other tasks needed to implement a mixed-signal solution. Each chiplet is an individual semiconductor device, that is highly optimized for its specific function. HI 2.5D integration allows the designer to select chiplets/die from a broad range of technology. For example, the designer can select a silicon process node for a processing-intensive FPGA and a totally different silicon-germanium process for high-frequency ADC/DAC blocks. The different processing types can be mixed and matched to achieve the optimal solution for the intended use case.

To develop an application-specific solution, the chiplets are integrated into a functioning System-in-Package (SiP) by mounting them onto a custom piece of silicon called a silicon interposer. The interposer includes high-density routing between the chiplets and through-silicon via (TSV) technology for routing the signals to an organic substrate and then out of the package. Each chiplet is a reusable component—designed, developed, and tested to perform its specific function by the chiplet vendor and often by different companies. Within the interposer, a variety of high-frequency signals must be routed between individual chiplets in a very small space, while minimizing cross talk and other Signal Integrity (SI) issues.

Overcoming the complexity challenges of a SiP design requires highly specialized expertise, analysis tools, and fabrication equipment. Because the interposer consists only of interconnects and no active circuitry, an interposer can be designed and fabricated more quickly and at lower cost than a monolithic ASIC. In addition, the development cost for each chiplet can usually be spread across multiple HI 2.5D SiP implementations. Reuse of chiplets and their existing design infrastructure can also reduce cost and schedule. These and other advantages are making HI 2.5D SiP technology the preferred approach for many commercial applications.

2.5D SiP components are proving to be an excellent match for sensor-edge processing requirements. Mixed-signal designs for radar and EW, which combine analog RF and digital circuits, map well into combinations of IP chiplets. 2.5D SiP designs have the flexibility to select the correct mix of CPUs, GPUs, and FPGAs and apply each where it fits best in a specific application's digital processing chain. A single SiP can combine the digital processing chain with transceivers and ADC/DAC components that match the targeted RF band. New high-performance chiplets support direct digitization of wideband RF signals, achieving the high fidelity needed for next-generation radar and EW systems. As the chiplets are in very close proximity and communicating via the high-density interconnects within an interposer, this has several advantages including reduced latency and improved signal integrity.

A final advantage worthy of attention is the outstanding SWaP characteristics possible with a 2.5D SiP technology approach. All the compact chiplets are mounted on a single silicon interposer, with no unnecessary cores or processing overhead. Small size, low weight, and minimal power are all hallmarks of 2.5D SiP solutions.

HI Computing Enabling DoD Modernization

HI processing is foundational to the DoD's ability to modernize. It enables rapid development & deployment, integration of diverse sensors into multifunction systems (e.g. cyber, EW, radar, comms). Partnerships between the development and acquisition communities drive the ability to design, fabricate, integrate, package, and globally deploy these advanced capabilities. The integration of advanced microelectronics into sensors, networks, and weapons is critical to all domains: land, air, sea, space, and cyberspace. Mercury Systems is proud to support a trusted and secure development flow with advanced packaging capability for the most challenging missions: broadband multi-function RF systems, heterogeneous 2.5D SiPs, radiation tolerant processors, and secure processing.

Mercury is advancing and prototyping a new model for heterogeneous, 2.5D microelectronics manufacturing and processes that leverages diverse commercial investment and best practices, and tailors the implementation, scale, and mix for the DoD community. This tailored approach is based upon Mercury Systems' extensive design and microelectronics manufacturing experience with complex, mixed-signal, multi-chip modules. It also includes unique device partnerships with leading semiconductor suppliers, providing Mercury access to chiplets not available to the open market at die-level.

A Novel Approach to Rapid HI Development

Bringing the next generation HI capabilities forward requires an innovative business model. Mercury introduces a Defense Industrial Base (DIB) "storefront" to support multiple customer program needs and ultimately reduce the timeline and cost of HI development efforts. This concept will provide a means for rapid prototyping and quick delivery of both standard and custom solutions for customers. The storefront would offer solutions in three areas: standard parts, derivative parts, and fully custom parts. Standard parts would be off-the-shelf and ready-to-go for multiple users. Derivative parts would be a way for customers to quickly enhance/customize a standard part to fit their needs. Fully custom parts would be for those customers who need a new/different solution.

The storefront will enable the high-mix, low volume development and production needs of the DIB. Mercury brings together multiple, existing capabilities to enable the storefront, including trusted and secure processes and IP libraries. Mercury also has partnerships with leading semiconductor manufacturers to access their cutting-edge, state-of-the-art devices at the chiplet/die level. Mercury can also provide solutions beyond the device-level SiP with integrated sub-system platforms.

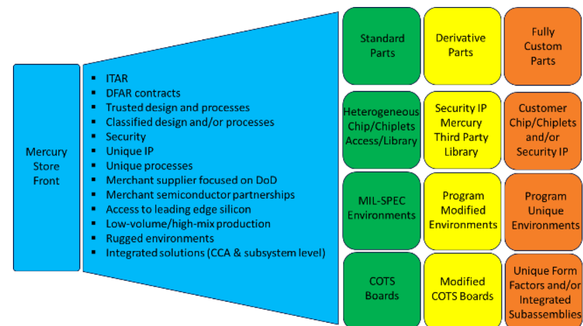

Fig. 3 DIB Storefront Model

The storefront would allow the DIB to choose from a variety of solutions and development paradigms. For rapid solutions, a standard part from Mercury's existing HI portfolio may fit the need. These would already be Defense-grade and ready to integrate on COTS or custom boards. If a change is needed, customers may initiate a derivative part and drive the integration of additional chiplets and/or IP such as security features, environmental requirements, or form factor modifications. If a custom solution is needed, Mercury will assist in the development of a fully custom device, integrating custom chiplets, IP, or other specific requirements.

Rapid Enablement of Customer Designs

As customers seek to engage in the HI 2.5D area, they'll need to understand the design drivers, rules, parameters, and capabilities of vendors like Mercury and their manufacturing partners. To enable customers and reduce risk across the development life cycle, an Assembly Design Kit (ADK) is needed. This ADK will provide customers with the necessary insight and design guidelines to rapidly develop solutions.

Mercury will develop an ADK for customers to use for rapid and low-risk development in the HI 2.5D SiP space. Mercury will investigate and document the necessary design parameters, reference designs, tool flows, design/manufacturing processes, representative test code, and other factors that are necessary for development.

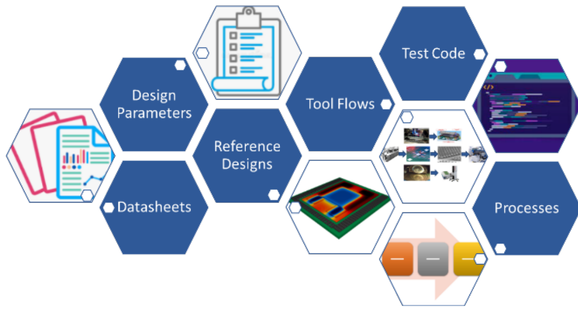

Fig. 4 Mercury Assembly Design Kit Concept

This may include compilations of vendor datasheets, design guidelines, and other important information so that customers can quickly understand best practices. As part of each development effort, new insights and lessons learned will be added to the ADK to enhance it going forward.

The ADK will provide customers, including DoD primes, with the necessary tools to reduce cycle-time and risk during HI development efforts. It will allow them to design solutions within a secure and trusted ecosystem with pre-vetted vendors. Since lessons learned can be integrated after each effort, the ADK will get better and better over time.

Driving the Future of HI

While the advantages of HI are clear, efforts to improve interoperability of chiplet interfaces, system integrity, and rapid prototyping are paramount to DoD modernization. A supporting ecosystem is necessary to develop an open-source development model. These standards will include the physical interfaces as well as the integration software & firmware between chiplets, standardized interposers, and the ability to demonstrate rapid integration of novel chiplets. Together, it becomes possible to upgrade silicon during a platform's lifetime without the expense and program disruption of a major redesign. Additionally, automated verification of the interface through commonly used design tools would improve the ecosystem and enable rapid integration of inline chiplets.

Driving advances in HI 2.5D SiP products, Mercury will support championing the industry effort to define an open systems architecture for chip-scale development. An environment where the IP chiplets can be easily and confidently reused, replaced, or upgraded for rapid prototyping and deployment benefits the entire DIB.

Mercury is pleased to be at the forefront of bringing the exciting advances in HI 2.5D solutions to the DIB. Chipletized architectures offer a way to combine the best commercial devices into custom solutions, tailored to meet the specific needs of Defense customers. These efforts will be enhanced through a "storefront" business model and an ADK to lower the barriers to entry and assist customers in their adoption and development of these solutions. Mercury strives to be the preferred partner to deliver uncompromised, low-SWaP, and trusted microelectronic solutions to the aerospace, defense, and semiconductor markets.