MILSPEC Training

Basic Review of:

MIL-PRF-19500 - Semiconductor Devices

MIL-PRF-38534 - Hybrid Microcircuits

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing

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To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

Acronyms

Abbreviation	Definition
AF	Air Force
BGA	Ball Grid Array
BN	Bayesian Network
BoK	Body of Knowledge
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off the Shelf
CPU	Central Processing Unit
DDR	Double Data Rate
DLA	Defense Logistics Agency
DMEA	Defense Microelectronics Activity
DoD	Department of Defense
DoE	Department of Energy
EEE	Electrical, Electronic, and Electromechanical
ETW	Electronics Technology Workshop
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
GIDEP	Government Industry Data Exchange Program
GPU	Graphics Processing Unit
GRC	Glenn Research Center
GSFC	Goddard Space Flight Center
GSN	Goal Structuring Notation
HQ	Headquarters
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
JPL	Jet Propulsion Laboratory
JSC	Johnson Space Center
LaRC	Langley Research Center
LGA	Land Grid Array
MAPLD	Military and Aerospace Programmable Logic Devices (Workshop)
MBMA	Model-Based Mission Assurance
MRAM	Magnetic Random Access Memory
MSFC	Marshall Space Flight Center

Abbreviation	Definition
NASA	National Aeronautics and Space Administration
NEPAG	NASA Electronic Parts Assurance Group
NEPP	NASA Electronic Parts and Packaging (Program)
NESC	NASA Engineering and Safety Center
NODIS	NASA Online Directives Information System
NPR	NASA Procedural Requirement
NRO	National Reconnaissance Office
NSREC	Nuclear and Space Radiation Effects Conference
OCE	Office of the Chief Engineer
OGA	Other Government Agency
PIC	Photonic Integrated Circuit
POC	Point of Contact
PoF	Physics of Failure
RF	Radio Frequency
RH	Radiation Hardened
RHA	Radiation Hardness Assurance
SAPP	Space Asset Protection Program
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single-Event Effects
SiC	Silicon Carbide
SMA	Safety and Mission Assurance
SMC	Space and Missile Systems Center
SOA	Safe Operating Area
SoC	System on a Chip
SRAM	Static Random Access Memory
SSAI	Science Systems and Applications, Inc.
STMD	Space Technology Mission Directorate
STT	Spin Transfer Torque
SysML	System Modeling Language
TID	Total Ionizing Dose
TSV	Thru-Silicon Via

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Special Thanks

MIL-PRF-19500

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Overview

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- General / Common Points
- RHA Designators
- 19500
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- 38535
  - Screening
  - Qualification

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Where are they?

The Mil Specs and Drawings system is managed by the Defense Logistics Agency, Lands and Maritime

https://landandmaritimeapps.dla.mil/programs/milspec/

Document & Drawing Search
https://landandmaritimeapps.dla.mil/programs/milspec/DocSearch.aspx

MIL-PRF-19500
Semiconductor Devices, General Specification for (w/Amendment 4)
FSC: 5961, Revision: P, Dated: 18 May 2018

MIL-PRF-38534
Hybrid Microcircuits, General Specification for
FSC: 5962, Revision: L, Dated: 03 December 2019

MIL-PRF-38535
Integrated Circuits (Microcircuits) Manufacturing, General Specification for
FSC: 5962, Revision: L, Dated: 06 December 2018

These documents are evolving!

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General / Common Points

A Performance Spec

19500….The main body specifies the **performance requirements** and requires the manufacturer to verify that their devices are capable of meeting those performance requirements.

38534…..This document is a **performance specification**. It is intended to provide the device manufacturers an acceptable established **baseline…** These appendices **provide guidance** to manufacturers on demonstrated **successful approaches to meeting defense performance requirements**.

38535…allow the device manufacturer the **flexibility to implement best commercial practices** to the maximum extent possible while still providing product that **meets military performance needs**.

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General / Common Points

- DLA certified manufacturers have to comply with the following requirements:
  - Has to sign up to be part of the military components standardization program in order to manufacture products to the required quality levels.
  - Successfully audited and certified by Defense Logistics Agency (DLA) Land & Maritime for their manufacturing facility. Multiple audits may be required if more than 1 facility is involved.
  - Successfully pass periodic DLA re-audits to remain in the MIL-PRF-19500 standardization program.

General / Common Points

- Document control encompasses various areas:
  - Design control requires that DLA (and user community) have to review and approve any proposed military specification sheet product design changes.
  - Procedures for each manufacturing and testing process step
- Traceability of a specific production lot back to the original wafer lot and other internal elements.
- Participate in the GIDEP alert system
- Changes IAW specification requirements
- Failures reported to DLA

RHA Designator & Levels

RHA level designator	Radiation total ionizing dose level (krad(Si))
- (dash)	No RHA
M	3
D	10
P	30
L	50
R	100
F	300
G	500
H	1000

19500 – Table E-II 38534 – Table G-I 38535 - Section 3.4.3

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MIL-PRF-19500 - Semiconductor Devices

MIL-PRF-19500
Semiconductor Devices, General Specification for (w/Amendment 4)
FSC: 5961, Revision: P, Dated: 18 May 2018

JANS – Joint Army Navy Space parts are the highest quality level parts manufactured and supplied to military and space programs.
JANTXV – highest military quality level with additional screening
JANTX – standard military quality level with standard screening.
JAN – lowest quality level with minimal screening to verify parts are functional. Cost is slightly more expensive than commercial grade parts; however, JAN parts have a pedigree and reliability built in.
JANKC – Joint Army Navy Space qualified QML die
JANHC – Joint Army Navy military qualified QML die

Military and space grade parts are identified with the JAN, JANTX, JANTXV, and JANS in the part number, e.g. JAN2N2222AUB, JANTX2N2222AUB, JANTXV2N2222AUB, and JANS2N2222AUB.

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19500 - Screening tests comparison

TABLE E-IV. Screening requirements

Screen	MIL-STD-750, method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
1a. Die visual for glass diodes	2073	Condition B, die form prior to assembly	100-percent	Not applicable	Not applicable
1b. Internal visual (pre-cap) inspection			100-percent	100-percent	Not applicable
For diodes	2074 1/				
For power FETs	2069				
For microwave transistors	2070				
For transistors	2072				
2. High temperature life Nonoperating life (stabilization bake)	1032	T_{STG} ≤ maximum rated storage temperature t = as specified	Optional	Optional	Optional
3a. Temperature cycling	1051	20 cycles. No dwell time is required at +25°C. Test condition C or maximum storage temperature, whichever is less.	100-percent	100-percent	100-percent
3b. Surge (as specified) 2/	4066	Condition A or B, as specified	100-percent	100-percent	100-percent
3c. Thermal impedance (as specified) 2/		As specified	100-percent	100-percent	100-percent
Transistors,					
Power FETs	3161				
Bipolar	3131				
Diodes	3101				
IGBT	3103				
GaAs FET	3104				
4. Constant acceleration. Not required for stud devices and metallurgically bonded diodes.	2006	Y_1 direction at 20,000 G minimum, except at 10,000 G minimum for devices with power rating of ≥10 watts at T_C = +25°C. The 1 minute hold time requirement shall not apply.	100-percent	Optional 3/	Optional 3/
5. PIND 4/	2052	Condition A	100-percent See E.5.4.1	Not applicable	Not applicable

See footnotes at end of table.

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19500 - Screening tests comparison

TABLE E-IV. Screening requirements - Continued.

Screen	MIL-STD-750, method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
6. Instability shock test (axial lead diodes only) 5/				Not applicable	Not applicable
a. FIST	2081		100-percent		
b. BIST	2082		100-percent		
7. Hermetic seal 6/					
a. Fine	1071		Optional	Optional	Optional
b. Gross 7/ 8/			Optional	Optional	Optional
8. Serialization		See 3.10.9.	100-percent	Not applicable	Not applicable
9. Interim electrical parameters		As specified	100-percent (read and record)	For case mounted rectifiers as specified.	For case mounted rectifiers as specified.
10. High temperature reverse bias (HTRB)					
a. For transistors	1039	Test condition A. 80 percent (minimum) of rated V_{CB} (bipolar), V_{GS}(FET) or V_{DS}(FET), as applicable.	100-percent	100-percent	100-percent
b. For power FETs	1042	Test condition B. 80 percent (minimum) of rated V_{GS}	100-percent	100-percent	100-percent
c. For diodes and rectifiers	1038	Test condition A. Diodes (not required for LEDs, Zeners, and case mounted rectifiers) 80 percent minimum of rated V_R or V_{RWM} when dc conditions are specified. 95 - 100 percent of V_{RWM}, when half sine condition is specified.	100-percent 9/	100-percent	100-percent

See footnotes at end of table.

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19500 - Screening tests comparison

TABLE E-IV. Screening requirements - Continued.

Screen	MIL-STD-750, method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
11. Interim electrical and delta parameter for PDA (see E.5.2)		As specified but including all delta parameters as a minimum. When HTRB is performed leakage current shall be measured on each device before any other specified parametric test is made.	100-percent (Measure all specified parameters. Measure leakage current within 16 hours after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 13 of table E-IV.)	100-percent (Measure all specified parameters. Measure leakage current within 24 hours after removal of applied voltage in HTRB. Record those Parameters which have a delta limit.) (See screen 13 of table E-IV.)	100-percent (Measure all specified parameters. Measure leakage current within 24 hours after removal of applied voltage in HTRB. Record those Parameters which have a delta limit.) (See screen 13 of table E-IV.)
12. Burn-in a. For bipolar transistors	1039	As specified. Test condition B.	100-percent 240 hours (minimum)	100-percent 160 hours (minimum)	100-percent 160 hours (minimum)
b. For power FETs	1042	Test condition A.	240 hours (minimum)	160 hours (minimum) 10/	160 hours (minimum) 10/
c. For diodes, Zeners, and rectifiers	1038	Test condition B.	240 hours (minimum)	96 hours (minimum)	96 hours (minimum)
For case mount rectifiers		Condition A (HTRB), JANTX and JANTXV only.	Not applicable	48 hours (minimum)	48 hours (minimum)
		Condition B , for JANS	240 hours (minimum)	Not applicable	Not applicable
d. For thyristors 11/	1040		240 hours (minimum)	96 hours (minimum)	96 hours (minimum)
e. For bipolar small die transistors	1039	Condition B	240 hours (minimum)	160 hours (minimum)	160 hours (minimum)
f. For bipolar power transistors	1039	Condition B	240 hours (minimum)	160 hours (minimum)	160 hours (minimum)

See footnotes at end of table.

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19500 - Screening tests comparison

TABLE E-IV. Screening requirements - Continued.

Screen	MIL-STD-750, method	Condition	JANS requirements	JANTXV requirements	JANTX requirements
13. Final electrical test (see E.5.2 For PDA) 12/		As specified.	100-percent	100-percent	100-percent
a. Interim electrical and delta parameters for PDA			Group A, subgroup 2, interim electrical and delta parameters. (read and record)	Group A, subgroup 2. Read and record interim electrical and delta parameters (see E.5.3.2).	Group A, subgroup 2. Read and record interim electrical and delta parameters (see E.5.3.2).
b. Other electrical parameters 13/			Group A, subgroup 3	Not applicable	Not applicable
14. Hermetic seal 6/	1071		100-percent	100-percent	100-percent
a. Fine		Omit for double plug diodes.			
b. Gross 7/ 8/					
15. Radiography	2076		100-percent 14/ 15/	Not applicable	Not applicable
16. External visual examination	2071	To be performed after complete marking and prior to lot acceptance	100-percent	Not applicable	Not applicable
17. Case Isolation 16/	1081	To be performed on all case isolated packages, as specified.	100-percent	100-percent	100-percent

See footnotes at end of table.

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19500 - Screening tests comparison

TABLE E-IV. Screening requirements - Continued.

1/ Visual inspection (test method 2074 of MIL-STD-750) on clear glass diodes shall be performed any time prior to marking. Diodes assembled in packages other than glass shall be inspected to test method 2072.
2/ Shall be performed any time before completion of screen 13. Surge shall precede thermal impedance. Surge and thermal impedance are applicable only when specified in the screening table of the specification sheet.
3/ Constant acceleration shall be performed on gold ball bond devices and gold wire for germanium.
4/ PIND is not applicable to any device with external and internal pressure contacts (die to electrical contacts), optical coupled isolators, and double plug diodes. PIND screening may be performed any time after screen 4 when imposed by contract or order (see E.5.4.1).
5/ Omit BIST and FIST tests for double plug or case-mounted diodes. Omit FIST test for temperature compensated referenced diodes.
6/ Non-transparent glass encased double plug, noncavity axial lead diodes only may use test method 2068 of MIL-STD-750 in lieu of test method 1071 of MIL-STD-750.
7/ Conditions C is prohibited for MIL-PRF-19500 product. Condition D, fluorocarbon tests, are prohibited as a standalone test, but may be used as a supplemental test as applicable after dry gas hermeticity tests. When Condition D is utilized as a supplement it must be followed by a bake at 150°C for one hour to remove residual fluorocarbon. If helium is used after fluorocarbon the failure criteria must be tightened by one order of magnitude. Glass diodes shall not be painted until after seal tests. For clear glass diodes, utilize condition E for gross leak seal test.
8/ When condition E, or method 2068 of MIL-STD-750, is the required gross leak seal test, then it may be performed anytime after temperature cycle (screen 3a).
9/ For JANS only, Zener diodes shall be subjected to high temperature reverse bias at 80 - 85 percent of nominal V_Z for $V_Z > 10$ V. Omit test for devices with $V_Z \leq 10$ V. For JANS case mounted rectifiers condition A is required.
10/ Optional accelerated HTRB for power FETs in accordance with test method 1042 of MIL-STD-750, condition A, shall be 48 hours minimum at T_A = +175°C minimum. Initial use of this option is contingent upon subsequent completion of a one time 1,000 hour qualification in accordance with test method 1042 condition A, at T_A = +175°C minimum, and as specified on group E of the individual specification sheet; to be submitted with the initial qualification report. Alternate flow options shall not be used to qualify this accelerated HTRB option.
11/ For JANTX and JANTXV levels, full wave-blocking test shall replace power burn-in for all thyristors.
12/ For JANTX and JANTXV levels, tests previously performed 100-percent (surge, thermal impedance) need not be repeated in screen 13. For JANS, read and record thermal impedance shall be performed in screen 13 or anytime after serialization. Thermal impedance is not part of the PDA.
13/ Ninety-six hours post burn-in measurement time not applicable.
14/ The radiographic screen for JANS may be performed in any sequence after screen 8. The radiographic screen for packages whose construction contains materials such as: tungsten, molybdenum, copper tungsten etc.; where the package material interferes with the radiographic view of the die, including, but not limited to: Die, die mounting areas, die attach region, and lid seals shall use real time radiography in lieu of film, or equivalent, with the approval of the qualifying activity. An additional alternate view, as described in MIL-STD-750, Test Method 2076, Real Time Radiography paragraph specifying additional views shall be added when an initial view produces a completely black image.
15/ Conformance inspection may be initiated immediately prior to screen 15.
16/ May be performed anytime after plating. Test conditions not specified in the test method shall be provided by the supplier unless specified in the specification sheet.

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Qualification Inspection Group A

TABLE E-V. Group A inspection.

Subgroups	MIL-STD-750, method	JANS sample plan 1/	JAN, JANTX, JANTXV sample plan 1/
Subgroup 1 (all devices except small die flow)		15 devices c = 0	116 devices, c = 0 (JANTXV)
Visual and mechanical inspection (test method 2071 of MIL-STD-750)	2071		45 devices, c = 0 (JAN, JANTX)
Subgroup 1 (for small die flow only 2/ 3/)			
Visual and mechanical examination 4/	2071		116 devices, c = 0 (JANTXV)
			45 devices, c = 0 (JAN, JANTX)
Solderability 4/	2026		15 leads, c = 0
Resistance to solvents 4/ 5/	1022		15 devices, c = 0
Salt atmosphere (corrosion), (Laser marked devices only. Not required for non-corrosive base metals.)	1041		6 devices, c = 0
Temperature cycling (air to air) 4/	1051		Test condition C, or maximum storage temperature, whichever is less, 25 cycles. 22 devices, c = 0
Electrical measurements (group A, subgroup 2)			
Hermetic seal 6/	1071		22 devices, c = 0
Fine leak Gross leak			
Bond strength 4/	2037		Precondition T_A = +250°C at t = 24 hrs or T_A = +300°C at t = 2 hrs 11 wires, c = 0
Decap internal visual (design verification)	2075		4 devices, c = 0

See footnotes at end of table.

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Qualification Inspection Group A

TABLE E-V. Group A inspection – Continued.

Subgroups	MIL-STD-750, method	JANS sample plan 1/	JAN, JANTX, JANTXV sample plan 1/
Subgroup 2 DC (static) test at +25°C ±3 degrees C		116 devices c = 0 7/ 9/	116 devices 7/ c = 0
Subgroup 3 DC (static) tests at high (-0C, +10C) and low (+0C, -10C) specified temperatures.			116 devices 7/ 8/ c = 0
Subgroup 4 Dynamic tests at +25°C ±3 degrees C			116 devices 7/ 8/ c = 0
Subgroup 5 Safe operating area test (for transistors only): a. DC b. Clamped inductive (only when applicable) c. Unclamped inductive (only when applicable) End-point electrical measurements		45 devices c = 0 10/	45 devices c = 0
Subgroup 6 Surge current (for diodes/rectifiers only) End-point electrical measurements			22 devices c = 0
Subgroup 7 Selected static and dynamic tests			22 devices c = 0

See footnotes at end of table.

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Qualification Inspection Group A

TABLE E-V. Group A inspection – Continued.

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable specification sheet. Where no parameters have been specified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements. A single sample may be used for all subgroup testing. These tests are considered nondestructive and devices may be shipped.

2/ For resubmission of failed table E-V, subgroup 1, double the sample size of the failed test or sequence of tests. A failure in table E-V, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Not required for JANS devices.

4/ Separate samples may be used.

5/ Not required for laser marked devices.

6/ This hermetic seal test is an end-point to temperature cycling in addition to electrical measurements.

7/ If a device in the sample fails one or more test(s) in the subgroup(s) being sampled, each device in the (sub)lot represented by the sample shall be screened for the test(s) for which the sample failed. An alternate test method to remove the failure mode may be used after an engineering evaluation is performed. After the rescreening, a second sample (first resubmittal) using double the large lot sample size shall be tested to the original failed parameter. If the second sample fails, the lot shall be rejected. When processing devices using the small die flow, (TABLE E-VIC), A4 may be performed once per wafer lot.

8/ For small lot sampling plan, n = 45.

9/ All devices required by the specified sample plan shall be subjected to subgroups 2, 3, and 4 combined.

10/ All devices required by the specified sample plan shall be randomly selected from the devices subjected to subgroups 2, 3, and 4, and shall be subjected to subgroups 5, 6, and 7 combined.

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Qualification Inspection comparison Group B JANS

TABLE E-VIA. Group B inspections for JANS devices.

Inspections	MIL-STD-750, method	MIL-STD-750, condition	Qualification and large lot conformance inspection sample plan	Small lot conformance inspection
Subgroup 1 1/				
Physical dimensions	2066	Dimensions in accordance with case outline specified in specification sheets. Unless otherwise specified, lead dimensions are pre-solder dip or pre-secondary finish.	22 devices, c = 0	8 devices c = 0
Subgroup 2 1/		Separate samples may be used for each test.		
Solderability	2026	The sample plan applies to the number of leads inspected. A minimum of three devices shall be tested.	15 leads, c = 0	6 leads c = 0
Resistance to solvents	1022	Ink marked devices only. Not required if marking is etched into the device.	15 devices, c = 0	6 devices c = 0
Salt atmosphere (corrosion)	1041	Laser marked devices only Not required for non-corrosive base metals.	6 devices, c = 0	6 devices, c = 0
Subgroup 3				
Thermal shock (liquid-to-liquid)	1056	25 cycles, condition B (glass diodes only).	22 devices, c = 0	6 devices c = 0
Temperature cycling (air-to-air)	1051	Test condition C, or maximum storage temperature, whichever is less. (100 cycles).		
Surge	4066	As specified.		
Hermetic seal 2/	1071			
a. Fine		Fine leak not required for double plug diodes.		
b. Gross				
Electrical measurements		Group A, subgroup 2.		
Decap-internal visual (design verification) 3/	2075	Visual criteria in accordance with qualified design and internal visual precap criteria.	6 devices, c = 0	6 devices c = 0

See footnotes at end of table.

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Qualification Inspection comparison Group B JANS

TABLE E-VIA. Group B inspections for JANS devices - Continued.

Inspections	MIL-STD-750, method	MIL-STD-750, condition	Qualification and large lot conformance inspection sample plan	Small lot conformance inspection
Subgroup 3 - Continued				
Bond strength (wire or clip bonded devices only)	2037	Condition D.	22 wires or 11 devices, c = 0, (whichever requires the smaller number of devices.)	12 wires or 6 devices c=0 (whichever requires the smaller number of devices.)
SEM (for applicable designs) 4/	2077	See test method for sample size information.		
Die shear (excluding axial leaded devices)	2017		The same number of devices used for bond strength will also be used for die shear (minimum of six die).	
Subgroup 4				
Intermittent operation life	1037 or 1042	2,000 cycles, Devices with .008 inch or larger bond wires, 6,000 cycles. (Condition D is required when using TM1042)	22 devices, c = 0	12 devices c = 0
Hermetic seal 2/	1071			
a. Fine		Fine leak not required for double plug diodes.		
b. Gross				
Electrical measurements		Group A, subgroup 2 and as specified.		
Bond strength (wire or clip bonded devices only) 5/	2037	Condition D. The sample shall include a minimum of three devices and shall include all wire sizes.	11 wires, c = 0	11 wires, c = 0
Subgroup 5				
Accelerated steady-state operation life	1027	Bias conditions as specified. T_J = +275°C minimum (for 96 hours minimum) or T_J = +225°C minimum (for 216 hours minimum) or T_J = rated °C minimum (for 1,000 hours minimum).	22 devices, c = 0	12 devices c = 0
Electrical measurements		Group A, subgroup 2 and 3. 6/		

See footnotes at end of table.

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Qualification Inspection comparison Group B JANS

TABLE E-VIA. Group B inspections for JANS devices - Continued.

Inspections	MIL-STD-750, method	MIL-STD-750, condition	Qualification and large lot conformance inspection sample plan	Small lot conformance inspection
Subgroup 5 - Continued				
Schottky diodes, Case mount rectifiers	1038	T_J = rated T_J maximum (for 1,000 hours minimum).		
Electrical measurements		Group A, subgroup 2 and 3. 6/		
Accelerated steady-state gate stress power MOSFETS	1042	Condition B, V_{GS} = rated, T_A = +175°C, t = 24 hours or T_A = 150°C, t = 48 hours.		
Electrical measurements		Group A, subgroup 2 and 3. 6/		
Accelerated steady-state reverse bias power MOSFETS	1042	Condition A, V_{DS} = rated, T_A = +175°C, t = 120 hours or T_A = 150°C, t = 240 hours and as specified.		
Electrical measurements		Group A, subgroup 2 and 3. 6/		
Bond strength (wire or clip bonded devices only)	2037	As specified. Bond strength samples shall have passed accelerated steady-state operation life.	20 wires, c = 0	20 wires c = 0
Subgroup 6 7/				
Thermal resistance		As specified. Thermal resistance may be performed on a group C frequency whenever 100 percent thermal impedance is performed, except for power and case mounted devices.	22 devices, c = 0	8 devices c = 0
Diodes	3101 or 4081			
Transistors (bipolar)	3131			
Transistors (POWER FETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs FET	3104			

See footnotes at end of table.

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Qualification Inspection comparison Group B JANS

TABLE E-VIA. Group B inspections for JANS devices - Continued.

Inspections	MIL-STD-750, method	MIL-STD-750, condition	Qualification and large lot conformance inspection sample plan	Small lot conformance inspection
Subgroup 7 8/ High-temperature life (nonoperating) Electrical measurements	1032	340 hours minimum, $T_{STG(max)} = T_A$ Group A, subgroup 2	32 devices, c = 0	12 devices c = 0

1/ Electrical reject devices, from the same inspection lot, may be used for all subgroups, when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table E-IV through screen 13.
2/ Non-transparent glass encased double plug noncavity diodes only may use test method 2068 in lieu of 1071 of MIL-STD-750. This test may be performed after electrical measurements.
3/ Verification of metallurgical bond as defined in appendix A in its entirety shall be documented. (Photos are required with a scale or magnification identifier).
4/ This test may be performed at any time prior to lot formation. When performing SEM as part of a qualification or requalification, it shall include a cross section analysis. See E.3.1.2.1 for applicable designs.
5/ If sample is continued to satisfy the C6 requirement then bond strength may be performed after C6.
6/ Ninety-six hours post burn-in measurement time not applicable for A3.
7/ Thermal resistance may be performed on a group C frequency whenever 100-percent thermal impedance is performed, except for power and case mounted devices.
8/ Not required for power MOSFETs.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

Qualification Inspection Group B JAN, JANTX, JANTXV

TABLE E-VIB. Group B inspections for JAN, JANTX, and JANTXV devices.

Inspections 1/	MIL-STD-750		Sample plan	Small lot conformance inspection
	Method	Condition		
Subgroup 1 2/		Separate samples may be used for each test		
Solderability	2026	The sample plan applies to the number of leads inspected. A minimum of 3 devices shall be tested.	15 leads c = 0	4 leads c = 0
Resistance to solvents	1022	Not required if marking is etched into the device.	15 devices c = 0	3 devices c = 0
Salt atmosphere (corrosion)	1041	Laser marked devices only	6 devices, c = 0	6 devices, c = 0
Subgroup 2			22 devices c = 0	6 devices c = 0
Thermal shock (liquid-to-liquid)	1056	10 cycles, condition B, (glass diodes only).		
Temperature cycling (air-to-air)	1051	Test condition C, or maximum storage temperature, whichever is less. (45 cycles including screening)		
Surge	4066	As specified.		
Hermetic seal 3/	1071			
a. Fine leak		Fine leak not required for double plug diode.		
b. Gross leak				
Electrical measurements 4/		Group A, subgroup 2		
Subgroup 3 5/			45 devices c = 0	12 devices c = 0
Steady-state operation life 6/	1027	Bias conditions as specified, 340 hours (minimum)		
Electrical measurements		Group A, subgroup 2		
or				
Intermittent operation life 7/	1037	2,000 cycles (minimum)		
	1042	Condition D, 2,000 cycles (minimum)		
Hermetic seal 3/	1071			
a. Fine		Fine leak not required for double plug diodes.		
b. Gross				
Electrical measurements		Group A, subgroup 2		
Bond strength (wire or clip bonded devices only)	2037	Condition D. The sample shall include a minimum of three devices and shall include all wire sizes.	11 wires c = 0	11 wires c = 0

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Qualification Inspection Group B JAN, JANTX, JANTXV

TABLE E-VIB. Group B inspections for JAN, JANTX, and JANTXV devices – Continued.

Inspections 1/	MIL-STD-750		Sample plan	Small lot conformance inspection
	Method	Condition		
Subgroup 4			1 device c = 0	1 device c = 0
Decap internal visual (design verification)	2075	Visual criteria in accordance with qualified design.		
Subgroup 5			15 devices c = 0	6 devices c = 0
Thermal resistance		As specified. Thermal resistance maybe performed on group C frequency whenever 100-percent thermal impedance is performed except for power and case mounted devices.		
Diodes	4081			
Transistors (bipolar)	3131			
Transistors (power FETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs FET	3104			
Subgroup 6 8/			32 devices c = 0	12 devices c = 0
High-temperature life (non-operating)	1032	340 hours minimum, $T_{STG(max)} = T_A$		
Electrical measurements		Group A, subgroup 2		

1/ An engineering evaluation shall be performed if there is a device failure. Corrective action shall be taken as necessary.
2/ Electrical reject devices from the same inspection lot, may be used for all subgroups when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table E-IV through screen 13.
3/ Non-transparent glass encased double plug non-cavity diodes only may use test method 2068 in lieu of 1071 of MIL-STD-750. This test may be performed after electrical measurements.
4/ Unless otherwise specified, omit delta parameters limits for low current gain (h_{fe}) and leakage measurements included in end-point measurements.
5/ If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, the 340-hour or 2,000 cycle life tests may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements; and bond pull may be performed after group C life test. End-point measurements shall be performed at either group B, subgroup 3 (340 hours or 2,000 cycles, as applicable) to satisfy group B lot acceptance or group C, subgroup 6 (1,000 hours or 6,000 cycles, as applicable) to satisfy group B and C lot acceptance. Bond strength may be performed after C6.
6/ T_J = 150°C (min) or rated T_J, whichever is less (except Schottky and power MOSFETs) for operation life.
7/ Intermittent operation life shall be performed on all case mounted devices.
8/ Not required for power MOSFETs.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

Qualification Inspection Group B Small Die Flow

TABLE E-VIC. Group B inspections (small die flow only) for JAN, JANTX, and JANTXV devices.

Inspections 1/ 2/	MIL-STD-750		Sample plan
	Method	Condition	
Step 1			n = 45, c = 0
Steady-state operation life 3/	1026	1,000 hours minimum 4/ 5/	
Electrical measurements		Group A, subgroup 2	
or			
intermittent operation life	1037	Intermittent life 6,000 cycles	
Hermetic seal 6/	1071		
a. Fine		Fine leak not required for double plug diodes.	
b. Gross			
Electrical measurements		Group A, subgroup 2	
Step 2			n = 45, c = 0
HTRB	1048	48 hours minimum.	
Electrical measurements		Group A, subgroup 2	
Step 3			n = 22, c = 0
High-temperature life (non-operating),	1032	t = 340 hours, T_A = +200°C.	
Electrical measurements		Group A, subgroup 2	

1/ For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot.
2/ Small die shall be device types identified by the manufacturer based on the manufacturer's internal process capabilities and the expected business model for the product. Classification of devices as small die shall be approved by the procuring activity. Once a device type is approved a small die, it shall be processed in accordance with the conformance inspection small die flow identified herein and shall not be changed without qualifying activity approval.
3/ Test method 1026 of MIL-STD-750 is required for eutectic die attach and test method 1037 of MIL-STD-750 is required for solder die attach.
4/ T_J = 150 degrees C (min) or rated T_J, whichever is less (except Schottky and power MOSFETs) for operation life.
5/ The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
6/ Non-transparent glass encased double plug noncavity diodes only may use test method 2068 of MIL-STD-750, in lieu of 1071.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

Qualification Inspection Group C

TABLE E-VII. Group C periodic inspections (all quality levels) .

Inspections	MIL-STD-750		Sample plan	Small lot conformance inspection
	Method	Condition		
Subgroup 1			15 devices c = 0	6 devices c = 0
Physical dimensions 1/ (not required for JANS)	2066	Dimensions in accordance with case outline specified in specification sheets. Unless otherwise specified, lead dimensions are pre-solder dip or pre-secondary finish.		
Subgroup 2			22 devices c = 0	6 devices c = 0
Thermal shock (liquid to liquid)	1056	25 cycles, condition B.		
Temperature cycling (air-to-air)	1051	Test condition C, or maximum storage temperature, whichever is less. (45 cycles including screening).		
Terminal strength	2036	As specified.		
Surface mount end cap bond integrity	2038	As specified (Condition B for US devices)		
Hermetic seal 2/	1071			
a. Fine leak		Fine leak not required for double plug diodes.		
b. Gross leak				
Moisture resistance	1021	Omit initial conditioning.		
Electrical measurements		Group A, subgroup 2.		
Subgroup 3		Not required for disc packages or metallurgically bonded double plug devices or stud packaged devices.	22 devices c = 0	6 devices c = 0
Shock	2016	Nonoperating, 1,500 G's, 0.5 ms, 5 blows in each orientation, X1, Y1, and Z1 (Y1 only for axial glass diodes.)		
Vibration, variable frequency	2056			
Constant acceleration 3/	2006	1 minute minimum in each orientation. X1, Y1, and Z1 at 20,000 G's minimum, except at 10,000 G's minimum for devices with power rating of ≥ 10 watts. T_C = +25°C.		
Electrical measurements		Group A, subgroup 2.		

See footnotes at end of table.

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Qualification inspection Group C

TABLE E-VII. Group C periodic inspections (all quality levels) – Continued.

Inspections	MIL-STD-750		Sample plan	Small lot conformance inspection
	Method	Condition		
Subgroup 4			15 devices c = 0	6 devices c = 0
Salt atmosphere (corrosion) 1/	1041			
Subgroup 5			15 devices c = 0	6 devices c = 0
Thermal resistance 4/		As specified.		
Diodes	4081			
Transistors (bipolar)	3131			
Transistors (power FETs)	3161			
Thyristors	3181			
IGBT	3103			
GaAs FET	3104			
Subgroup 6 5/ 6/		Not required for disc packages.	22 devices c = 0	12 devices c = 0
Steady-state operation life	1026	1,000 hours minimum, bias conditions as specified. 7/ 8/		
Electrical measurements		Group A, subgroup 2.		
or				
Intermittent operation life	1037	6,000 cycles minimum.		
	1042	Condition D, 6,000 cycles minimum.		
Hermetic seal 2/	1071			
a. Fine		Fine leak not required for double plug diodes.		
b. Gross				
Electrical measurements		Group A, subgroup 2.		
Bond strength 9/	2037	Condition D, .008 inch or larger wire or clip bonded devices only. The sample shall include a minimum of three devices and shall include all wire sizes.	11 wires, c = 0	11 wires, c = 0
or				
Blocking life 8/	1048			
Electrical measurements		Group A, subgroup 2.		
Subgroup 7 10/			3 devices c = 0	3 devices c = 0
Internal gas analysis	1018	To be performed on each structurally identical package family.		

See footnotes at end of table.

Qualification Inspection Group C

TABLE E-VII. Group C periodic inspections (all quality levels) – Continued.

1/ Electrical reject devices, from the same inspection lot, may be used for all subgroups when electrical end-point measurements are not required. Other non-catastrophic rejected devices (i.e., PIND, X-ray) may be utilized for all subgroups. For subgroups with end-point measurements, the devices shall be screened to table E-IV through screen 13. Salt atmosphere not required for Laser marked devices when devices from group B, or from group A for small die flow, salt atmosphere have been selected to satisfy group C inspection requirements.

2/ Non-transparent glass encased double plug noncavity diodes only may use test method 2068 of MIL-STD-750, in lieu of 1071. This test may be performed after electrical measurements.

3/ Not applicable to any devices with external and internal pressure contacts (die to electrical contacts), optical coupled isolators, and double plug diodes.

4/ Not required when performed in group B.

5/ If a given inspection lot undergoing group B inspection has been selected to satisfy group C inspection requirements, then the life test samples may be continued on test to 1,000 hours or 6,000 cycles, as applicable, in order to satisfy the group C life test requirements. End-point measurements shall be performed on either table E-VIA, group B, subgroup 4, or table E-VIB group B, subgroup 3 (340 hours or 2,000 cycles, as applicable) to satisfy group B (table E-VIA or table E-VIB) lot acceptance or group C, subgroup 6 (1,000 hours or 6,000 cycles, as applicable) to satisfy group B and C lot acceptance.

6/ Intermittent operation life shall be performed on all case mounted devices.

7/ T_J = 150°C (min) or rated T_J whichever is less (except schottky and power mosfets) for operation life.

8/ The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 22,000 device hours minimum, and the actual time of test is at least 340 hours.

9/ Required for JANS devices with .008 inch or larger bond wires only. Not required when JANS devices from group B bond pull inspection have been selected to satisfy group C inspection requirements.

10/ Internal gas analysis shall be performed on hermetic devices. An engineering evaluation shall be performed if there is a device failure to determine the moisture source (e.g. sealing environment, non hermetic device). The entire lot shall be rescreened in accordance with screen 14 herein (and resubmitted at 6/0.) Corrective action shall be taken as necessary. Subgroup 7 is not required for noncavity double plug devices.

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Qualification Inspection Group D

TABLE E-VIII. Group D inspection (RHA inspections). 1/

Test	MIL-STD-750		JANS		JANTXV	
	Method	Condition	Quantity/ (accept number)	Notes	Quantity (accept number)	Notes
Subgroup 1 2/						
Neutron irradiation	1017	+25°C				
Qualification and conformance inspection			11(0)	3/	(a) 11(0)	4/
End-point electrical parameters		As specified in accordance with specification sheet				
Subgroup 2 5/						
Steady-state total dose irradiation	1019	+25°C				
Qualification and conformance inspection			4(0) 2(0) 1(0)	6/ 8/ 9/	11(0)	7/
End-point electrical parameters		As specified in accordance with specification sheet				
Subgroup 3 10/						
Power transistor electrical dose rate test	3478	+25°C	11(0)	3/	11(0)	4/
End-point electrical parameters		As specified in accordance with specification sheet				

See footnotes at end of table.

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Qualification Inspection Group D

TABLE E-VIII. Group D inspection (RHA inspections) – Continued. 1/

1/ Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Unless testing is performed within the time limits of the test method, total exposure shall not be considered cumulative. Group D tests may be performed prior to device screening (see E.6.5).
2/ Unless by design, waive neutron tests for MOS devices, bipolar elements are an integral part of the device function.
3/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18 devices, c = 1.
4/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18 devices, c = 1.
5/ JANTXV devices shall be inspected using either the JANTXV quantity/accept number criteria as specified, or by using the JANS criteria on each wafer.
6/ For device types with greater than or equal to 4,000 die per wafer, selected from a random locations on the wafers.
7/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 27 devices, c = 1. For devices which require more than one bias, the sample size shall be 11(0) for each bias.
8/ For device types with greater than 500 and less than 4,000 die per wafer, selected from random locations on each wafer.
9/ For device types with less than or equal to 500 die per wafer, selected from random locations on each wafer.
10/ Upset testing during qualification on first conformance inspection shall be conducted when specified in contract or order when specified, the same devices may be tested in more than one subgroup.

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Qualification Inspection Group E

TABLE E-IX. Group E inspections (all quality levels).

Inspections	MIL-STD-750		Sample plan
	Method	Condition	
Subgroup 1			45 devices, c = 0 or as specified.
Thermal shock or Temperature cycling	1056 1051	100 cycles or as specified. 500 cycles minimum or as specified. Test condition C or max storage temp, whichever is less.	
Hermetic seal 3/ a. Fine leak b. Gross leak	1071	As applicable. Fine leak not required for double plug diodes.	
Electrical measurements		Group A, subgroup 2.	
Subgroup 2			45 devices, c = 0 or as specified.
Intermittent operating life Electrical measurements or	1037	As specified. Group A, subgroup 2.	
Life test Electrical measurements or	1042	Condition A, B, C, or D. Group A, subgroup 2.	
Steady-state operating life Electrical measurements or	1026	As specified. Group A, subgroup 2.	
Blocking life Electrical measurements	1048	As specified. Group A, subgroup 2.	
Subgroup 3 Not applicable			
Subgroup 4			
Thermal impedance curves (as applicable)	N/A	Each supplier shall submit a thermal impedance ($Z_{\theta JX}$) histogram of the entire qualification lot. The histogram data shall be taken prior to the removal of devices that are atypical for thermal impedance. Thermal impedance curves (from $Z_{\theta JX}$ test pulse time to $R_{\theta JX}$ minimum steady-state time) of the best device in the qual lot and the worst device in the qual lot (that meets the supplier proposed screening limit), or from the thermal grouping, shall be submitted. The optimal test conditions and proposed initial thermal impedance screening limit shall be provided in the qualification report. Data indicating how the optimal test conditions were derived for $Z_{\theta JX}$ shall also be submitted. The proposed specification maximum thermal impedance curve shall be submitted. The qualifying activity may approve a different $Z_{\theta JX}$ limit not to exceed the specification's thermal curve for conformance inspection end-point measurements as applicable. The supplier shall support (with applicable data) their $Z_{\theta JX}$ end-point limit proposal when it exceeds the screening $Z_{\theta JX}$ limit. A delta (read and record) $Z_{\theta JX}$ shall be determined by the manufacturer and approved by the qualifying activity for all case mounted devices for conformance inspection (intermittent life test and temperature cycling) end-point measurements. Any exceptions shall be justified to, and approved by, the qualifying activity. Equivalent data, procedures, or SPC plans may be used for part, or all, of the above requirements.	N/A

See footnotes at end of table.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

Qualification Inspection Group E

TABLE E-IX. Group E inspections (all quality levels) - Continued.

Inspections	MIL-STD-750		Sample plan
	Method	Condition	
Subgroup 4 - continued		The approved thermal impedance conditions and limit for Z_{aux} shall be used by the supplier in screening, and group A subgroup 2. The approved thermal resistance conditions for R_{aux} shall be used by the supplier for conformance inspection. For product families with similar thermal characteristics based on the same physical and thermal die, package, and construction combination (thermal grouping), the supplier may use the same thermal impedance curves.	
Subgroup 5 Barometric pressure (reduced) (required only on all devices with rated voltage > 200 V)	1001	As specified.	3 devices, c = 0 or as specified.
Subgroup 6 ESD	1020	As required by E.4.2.1.	11 devices.
Subgroup 7 Resistance to soldering heat 1/ Visual inspection Hermetic seal 3/ a. Fine leak b. Gross leak Electrical measurements	2031 1071	See test method 2031 of MIL-STD-750 and H.6 for package family and test conditions. 2/ As applicable. Fine leak not required for double plug diodes. Group A, subgroup 2.	3 devices, c = 0 or as specified.
Subgroup 8 Reverse stability (for bipolar transistors only)	1033	When specified. Condition A for devices > 400 V. Condition B for devices < 400 V.	45 devices, c = 0 or as specified.
Subgroup 9 Resistance to glass cracking (glass diodes only)	1057	Condition B. Step stress to destruction by increasing cycles or up to a maximum of 25 cycles. The results shall be available upon request.	45 devices.

1/ As an option, the manufacturer may submit data (alternate testing) to the qualifying activity for approval in lieu of performing specific soldering heat test conditions.
2/ After subjection to the test, failure of one or more specified end-point measurements or examinations, evidence of defects or damage to the case, leads, or seals shall be considered a failure. Damage to the marking caused by fixturing or handling during tests shall not be cause for device rejection.
3/ Non-transparent glass encased double plug noncavity diodes only may use test method 2068 of MIL-STD-750, in lieu of 1071. This test may be performed after electrical measurements.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

MIL-PRF-19500 – QML Die

MIL-PRF-19500
Semiconductor Devices, General Specification for (w/Amendment 4)
FSC: 5961, Revision: P, Dated: 18 May 2018

JANKC – Joint Army Navy Space qualified QML die
JANHC – Joint Army Navy military qualified QML die

MIL-PRF-19500 Appendix G provides users and hybrid manufacturers access to DLA certified and qualified military and space level die.

- MIL-PRF-19500 Appendix G table G-II is equivalent to MIL-PRF-38534 table C-II-1 semiconductor dice evaluation
- Element evaluation already completed for JANKC/JANHC die.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

JANKC/JANHC Die Qualification

TABLE G-II. Die element evaluation requirements.

Subgroup	Class		Test	MIL-STD-750		Quantity	Reference paragraph
	K	H		Method	Condition	(Accept no.)	
1	X	X	Electrical test			100-percent	G.5.2.1
2	X	X	Visual inspection	2069 2070 2072 2073		100-percent	G.5.2.2
3A	X	X	Internal/die visual inspection	2069 2070 2072 2073		10 (0) For class H 22 (0) For class K	G.5.2.3.1
3B	X	X	Sample assembly			10 pieces min for class H, 22 pieces min for class K	G.5.2.3.2 G.5.2.3.3
4						10 (0) For class H 22 (0) For class K	
	X	X	Temperature cycling	1051	C		
	X		Mechanical shock or	2016	Y1 axis direction		
			Constant acceleration	2006	Y1 axis direction		
	X	X	Electrical test (read/record)		Group A, subgroups 2, 3, 4		1/
	X	X	HTRB		Screen 10		2/
	X	X	Electrical test (read/record)		Group A, subgroup 2		1/ 3/
	X	X	Burn-in		Screen 12		2/
	X	X	Electrical test (read/record)		Group A, subgroup 2		1/ 3/
	X		Steady-state life				4/
			Transistors Power FETS Diodes/rectifiers	1039 1042 1038	B A A or B		

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

JANKC/JANHC Die Qualification

TABLE G-II. Die element evaluation requirements – Continued.

Subgroup	Class K	Class H	Test	MIL-STD-750 Method	MIL-STD-750 Condition	Quantity (Accept no.)	Reference paragraph
4 (Continued)	X		Electrical test (read/record)		Group A, subgroup 2, 3, 4		1/
5A	X	X	Wire bond evaluation	2037	As applicable	10 (0) wires or 20 (1) wires	G.5.2.5.1
5B	X	X	Die shear evaluation	2017		5 (0) or 10 (1)	G.5.2.5.2
6	X		SEM	2077	As applicable	See test method 2077	G.5.2.6 5/
7			RHA			6/	G.5.2.7 5/
	X		Total dose	1019			
	X		Neutron irradiation	1017			

1/ Thermal impedance shall not apply.
2/ HTRB and burn-in shall be performed when specified on the applicable specification sheet.
3/ For JANHC only, if one device fails during any of the subgroup 4 tests following "electrical tests" (table E-V, group A, subgroups 2, 3, or 4), then 20 additional devices may be added to the element evaluation with no additional failures allowed, 30 devices, c = 1.
4/ Time and temperature requirements in accordance with table G-I.
5/ May be performed at any time.
6/ Sample size shall be in accordance with the specification sheet.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

MIL-PRF-38534 - Hybrid Microcircuits

MIL-PRF-38534
Hybrid Microcircuits, General Specification for
FSC: 5962, Revision: L, Dated: 03 December 2019

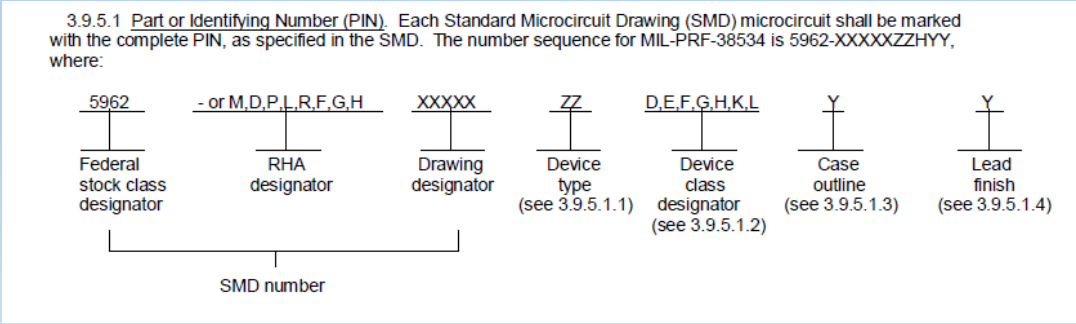
6.4.22 **Hybrid microcircuit**. A microcircuit that contains two or more of a single type, or a combination of the following types of elements with at least one of the elements being active.
a. Film microcircuit (6.4.19).
b. Monolithic microcircuit (6.4.30).
c. Semiconductor element (6.4.42).
d. Passive chip or printed or deposited substrate elements (6.4.35).

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

Classification & Part Identifying Number (PIN)

1.3 Classification. Seven quality assurance levels are provided for in this specification. Four of these classes, in highest to lowest order, are K, H, G and D, as defined below. The fifth class is Class E, the quality level associated with a Class E device is defined by the acquisition document.

1.3.1 **Class K**. - the **highest reliability level** provided for in this specification. It is intended for **space** applications.
1.3.2 **Class H**. - the standard **military** quality level.
1.3.5 **Class E**. - designates devices which are based upon one of the other classes (L, K, H, G, or F) with **exceptions** taken to the requirements of that class.
1.3.6 **Class L**. - the highest quality class for **non-hermetic** devices.
1.3.7 **Class F**. - the standard quality class for **non-hermetic** devices.



Same format for 38535

Element Evaluation Summary

TABLE C-I. Element evaluation summary.

Element	Paragraph	Table or MIL-STD-883 method
Microcircuit dice	C.3.3	Table C-II
Semiconductor dice	C.3.3	Table C-II-1
Wire Bondable and Surface Mount Resistors.	C.3.4	Table C-III
Capacitors, Ceramic	C.3.4	Table C III-1
Chip Capacitors, Solid Tantalum	C.3.4	Table C III-2
Capacitors, MOS – NMOS	C.3.4	Table C III-3
Coils, Transformers	C.3.4	Table C III-4
Surface acoustic wave (SAW) elements	C.3.5	Table C-IV
Alternate evaluation	C.3.6	N/A
Substrate evaluation	C.3.7	Table C-V
Package evaluation	C.3.8	Table C-VI
Integral substrate/package evaluation	C.3.9	Table C-VII
Polymeric material evaluation	C.3.10	Method 5011
Sub-assembly evaluation	C.3.11	Table C-VII-1

Microcircuit Dice Evaluation Requirements

*

TABLE C-II. Microcircuit dice evaluation requirements.

Subgroup	Class K	Class H	Test	Specification or Standard	Method	Condition	Comments	Quantity (accept number)	Reference paragraph MIL-PRF-38534
1	X	X	Element Electrical	Per Acquisition Document			25°C	100%	C.3.3.1
2		X	Element Visual	MIL-STD-883	2010	B		100%	C.3.3.2
	X		Element Visual	MIL-STD-883	2010	A			
3		X	Internal Visual	MIL-STD-883	2010	B		10(0)	C.3.3.3
	X		Internal Visual	MIL-STD-883	2010	A			C.3.3.4.2
4	X		Initial Electrical	Per Acquisition Document			25°C Record Data	10(0)	
	X		Temperature Cycle	MIL-STD-883	1010	C	20 Cycles		C.3.3.3
	X		Mechanical Stress 1/	MIL-STD-883 - Constant Acceleration	2001	A	Y1 Direction		
				MIL-STD-883 - Mechanical Shock	2002	B	Y1 Direction		
	X		Interim Electrical	Per Acquisition Document			25°C Record Data		C.3.3.4.3
	X		Burn-In 2/	MIL-STD-883	1015		240hrs Min. at Tc or Ta = 125ºC Min.		
	X		Post-BI Electrical 3/	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
	X		Steady State Life 2/	MIL-STD-883	1005		1000hrs at Tc or Ta =125°C Min. or 500hrs at Tc=150°C Min.		
	X	X	Final Electrical 3/	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
5	X	X	Wirebond Evaluation 4/	MIL-STD-883	2011		Bake for 1 hour minimum @ +300ºC (Bimetallic bonds only)	10(0) or 20(1) wires	C.3.3.3 C.3.3.5
6	X		SEM 5/	MIL-STD-883	2018			See 5/	C.3.3.6

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Semiconductor Dice Evaluation Requirements Pg 1

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TABLE C-II-1. Semiconductor dice evaluation requirements.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode - Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
1	X	X	Element Electrical	X	X	X	X	X	X	Per Acquisition Document			25°C	100%	C.3.3.1
2	X	X	Element Visual					X		MIL-STD-750	2069			100%	C.3.3.2
	X	X		X							2070				
	X	X		X	X				X		2072				
	X	X				X	X				2073				
3	X	X	Internal Visual					X		MIL-STD-750	2069			10(0)	C.3.3.3
	X	X		X							2070				C.3.3.4.2
	X	X		X	X				X		2072				
	X	X				X	X				2073				
4	X		Initial Electrical 1/	X	X	X	X	X	X	Per Acquisition Document			25°C Record Data	10(0)	
	X		Temperature Cycle 2/	X	X	X	X	X	X	MIL-STD-883	1010	C	20 Cycles		C.3.3.3
	X			X	X	X	X	X	X	MIL-STD-750	1051	C	20 Cycles		
	X		Surge			X				MIL-STD-750	4066	B			
	X						X					A			

See footnotes at end of table.

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Semiconductor Dice Evaluation Requirements Pg 2

TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode – Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
4	X		Mechanical Stress 2/	X	X	X	X	X	X	MIL-STD-883 - Constant Acceleration	2001	A	Y1 Direction 5000g	10(0)	
										MIL-STD-750 - Constant Acceleration	2006				
	X			X	X	X	X	X	X	MIL-STD-883 - Mechanical Shock	2002	B	Y1 Direction		
										MIL-STD-750 - Mechanical Shock	2016		Y1 Direction 1500g		
	X		Interim Electrical 1/	X	X	X	X	X		Per Acquisition Document			25°C Record Data		C.3.3.4.3
	X		High Temperature Reverse Bias (HTRB) 3/	X	X					MIL-STD-750	1039	A	80% Min. of rated VCB (bipolar), as applicable.		C.3.3.3
	X							X		MIL-STD-750 - Burn-in (Power MOSFET) MIL-STD-750 - Gate Bias (IGBT)	1042	B	80% Min. of rated VGS.		
	X					X	X			MIL-STD-750 - Burn-in (Power) MIL-STD-750 - Reverse Bias (Zener, Rectifier)	1038	A	80% Min. of rated VR or VRWM when DC conditions are specified. 95-100% of VRWM, when half sine condition is specified.		

See footnotes at end of table.

Semiconductor Dice Evaluation Requirements Pg 3

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TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode - Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
4	X		Interim Electrical 1/ 3/	X	X	X	X	X	X	Per Acquisition Document			25°C Record Data	10(0)	C.3.3.4.3
	X		Burn-In	X	X					MIL-STD-750	1039	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X							X		MIL-STD-750	1042	A	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X					X	X			MIL-STD-750	1038	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X								X	MIL-STD-750	1040	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X		Post BI Electrical 1/ 4/	X	X	X	X	X	X	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3

See footnotes at end of table.

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Semiconductor Dice Evaluation Requirements Pg 4

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TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode - Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
4	X		Steady State Life	X	X					MIL-STD-750	1039	B	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C	10(0)	
	X							X		MIL-STD-750	1042	A	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C 80% Vds Min.		
	X					X	X			MIL-STD-750	1038	B	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C		
	X								X	MIL-STD-750	1040	B	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C		
	X	X	Final Electrical 1/ 4/	X	X	X	X	X	X	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
5	X	X	Wirebond Evaluation 2/ 5/	X	X	X	X	X	X	MIL-STD-883	2011		Bake for 1 hour minimum @ +300ºC (Bimetallic bonds only)	10(0) or 20(1) wires	C.3.3.3 C.3.3.5
	X	X		X	X	X	X	X	X	MIL-STD-750	2037				
6	X		SEM 2/ 6/ 7/	X	X			X	X	MIL-STD-883	2018			See 7/	C.3.3.6
										MIL-STD-750	2077				

See footnotes at end of table.

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Device Screening

TABLE C-IX. Device screening.

Test or inspection	MIL-STD-883		Requirement		Reference paragraph
	Method	Condition	Class K	Class H	
Preseal burn-in	1030		Optional	Optional	C.5.3
Non-destructive bond pull	2023		100 percent	Optional	C.5.4
Internal visual	2017		100 percent	100 percent	C.5.5
Temperature cycling	1010	C, 10 cycles	100 percent	100 percent	C.5.6
Mechanical shock or constant acceleration	2002 2001	B, (Y1 direction only) 3,000 g's, Y1 direction only	100 percent	100 percent	C.5.6
PIND	2020	Condition A shall be used for Class K, unless otherwise specified	100 percent	Optional	C.5.7
Pre-burn-in electrical test	In accordance with applicable device specification		100 percent	Optional	C.5.8
Burn-in	1015		100 percent	100 percent	C.5.9
Final electrical test	In accordance with applicable device specification		100 percent	100 percent	C.5.10
Seal (fine and gross)	1014		100 percent	100 percent	C.5.11
Radiographic	2012		100 percent	Optional	C.5.12
External visual screen	2009		100 percent	100 percent	C.5.13

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Qual - Group A Electrical Test

APPENDIX C

TABLE C-Xa. Group A electrical test.

Subgroup	Parameters	Quantity (accept number)
1	Static test at +25°C	116 (0)
2	Static tests at maximum rated operating temperature	76 (0)
3	Static tests at minimum rated operating temperature	45 (0)
4	Dynamic tests at +25°C	116 (0)
5	Dynamic tests at maximum rated operating temperature	76 (0)
6	Dynamic tests at minimum rated operating temperature	45 (0)
7	Functional tests at +25°C	116 (0)
8	Functional tests at maximum and minimum rated operating temperatures	76 (0)
9	Switching tests at +25°C	116 (0)
10	Switching tests at maximum rated operating temperature	76 (0)
11	Switching tests at minimum rated operating temperature	45 (0)

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Qual - Group B In-line Tests

TABLE C-Xb. Group B testing (option 2 only).

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	K	H		Method	Condition		
1	X	X	Physical dimension	2016		2(0)	
2			Not used				
3	X	X	Resistance to solvents	2015		3(0)	
4	X	X	Internal visual and mechanical	2014		1(0)	C.6.4.2.1
5	X	X	Bond strength: a. Thermocompression b. Ultrasonic or wedge c. Flip-chip d. Beam lead	2011	 C or D C or D F H	2(0)	C.6.4.2.2
6	X	X	Die shear strength	2019		2(0)	C.6.4.2.3
7	X	X	Solderability	2003	Solder temperature +245°C ± 5°C	1(0)	C.6.4.2.4
8		X	Seal: a. Fine b. Gross	1014	 A or B C or D	15(0)	C.6.4.2.5

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Qual - Group C In-line Tests

APPENDIX C

TABLE C-Xc. Group C testing.

Subgroup	Class		Test	MIL-STD-883			Quantity (accept number)	Reference paragraph
				Method	Conditions			
	K	H			PI	QML		
1	X	X	Resistance to Soldering Heat	2036	1/	N/A	5 (0)	C.6.3.3.5
	X	X	External visual	2009				
	X	X	PIND 2/	2020	N/A	A 3/		C.7.5.4.1
	X		Temperature cycling	1010	C, 20 cycles	C, 100 cycles		C.7.5.4.2
		X	Temperature cycling	1010	C, 10 cycles	C, 100 cycles		C.7.5.4.2
	X	X	Mechanical shock	2002	B, Y1 direction 4/	B, Y1 direction		C.7.5.4.3
	X	X	Constant acceleration	2001	3,000 g's, Y1 direction 4/	5,000 g's, Y1 direction		C.7.5.4.4
	X	X	Random vibration 5/	2026	N/A	F		C.7.5.4.5
	X	X	Seal (fine and gross) 6/	1014				
	X	X	PIND	2020	N/A	A, 1 pass 3/		C.7.5.4.1
	X	X	Visual examination	1010				C.7.5.4.6
	X	X	End-point electrical	7/				C.7.5.4.7
2	X	X	Steady-state life test	1005	1,000 hours at +125°C or equivalent in accordance with method 1005	1,000 hours at +125°C or equivalent in accordance with method 1005	8/ 22 (0) or 5 (0)	C.7.5.4.8
	X	X	End-point electrical	7/				C.7.5.4.7
3	X	X	Internal gas analysis	1018			9/ 3 (0)	C.7.5.4.9
4	X	X	Internal visual	2017	Option 1 only		9/ 2 (0)	C.7.5.4.10
	X	X	Wire bond strength	2011	Option 1 only			C.7.5.4.11, C.6.3.3.2
	X	X	Element shear	2019 or 2027	Option 1 only			C.7.5.4.12, C.6.3.3.3
5 10/	X	X	ESD a. End point electrical b. ESDS c. End point electrical	3015	Group A-1 Group A-1	N/A	3 (0)	C.6.3.3.4

See footnotes at end of table.

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Qual - Group D Package Related Tests

TABLE C-Xd. Group D package related tests.

Subgroup	Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
		Method	Condition		
1	Thermal shock	1011	C	5(0)	
	Stabilization bake	1008	+150°C, 1 hour	5(0)	
	Lead integrity	2004 2028	B2 (lead fatigue) D (leadless chip carrier) B1 for rigid leads (pin grid array leads)	1(0)	C.6.4.4.3
	Seal: a. Fine b. Gross	1014	 A or B C or D	5(0)	
2	Not used				
3	Salt atmosphere	1009	A	5(0)	C.6.4.4.4
4	Metal package isolation	1003	600 V dc, 100 nA maximum	3(0)	C.6.4.4.5

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

Appendix D – Non-Hermetic Devices

- Definitions
  - **Non-hermetic device** - A device which has all or some of the elements not hermetically sealed and is categorized as follows:
    - a. **Cavity non-hermetic device** - A cavity device having construction utilizing non-hermetic (polymeric) seals.
    - b. **Non-cavity non-hermetic device** – A non-cavity device having construction utilizing molding compounds or other materials encapsulation the internal elements.
    - c. **Open non-hermetic device** – A open device having construction with minimal or no protection of the internal elements.
    - d. **Open architecture device (OA)** – A single substrate with hermetically sealed hybrid or multichip cavity(s) in which all bare die, chip and wire, or flip chip are mounted in the hermetically sealed area. Non-hermetic packaged components integral to the substrate (resistors, capacitors, coils, tranformers, and transistors) which are typically mounted on printed circuit boards are not hermetically sealed.

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.

MIL-PRF-38535 - Integrated Circuits

MIL-PRF-38535

Integrated Circuits (Microcircuits) Manufacturing, General Specification for
FSC: 5962, Revision: L, Dated: 06 December 2018

The basic section of this specification has been structured as a performance specification, which is supplemented with detailed appendices.

Appendix A is mandatory for manufacturers of device types supplied in compliance with MIL-STD-883 and forms the basis for QML classes Q, V and Y.

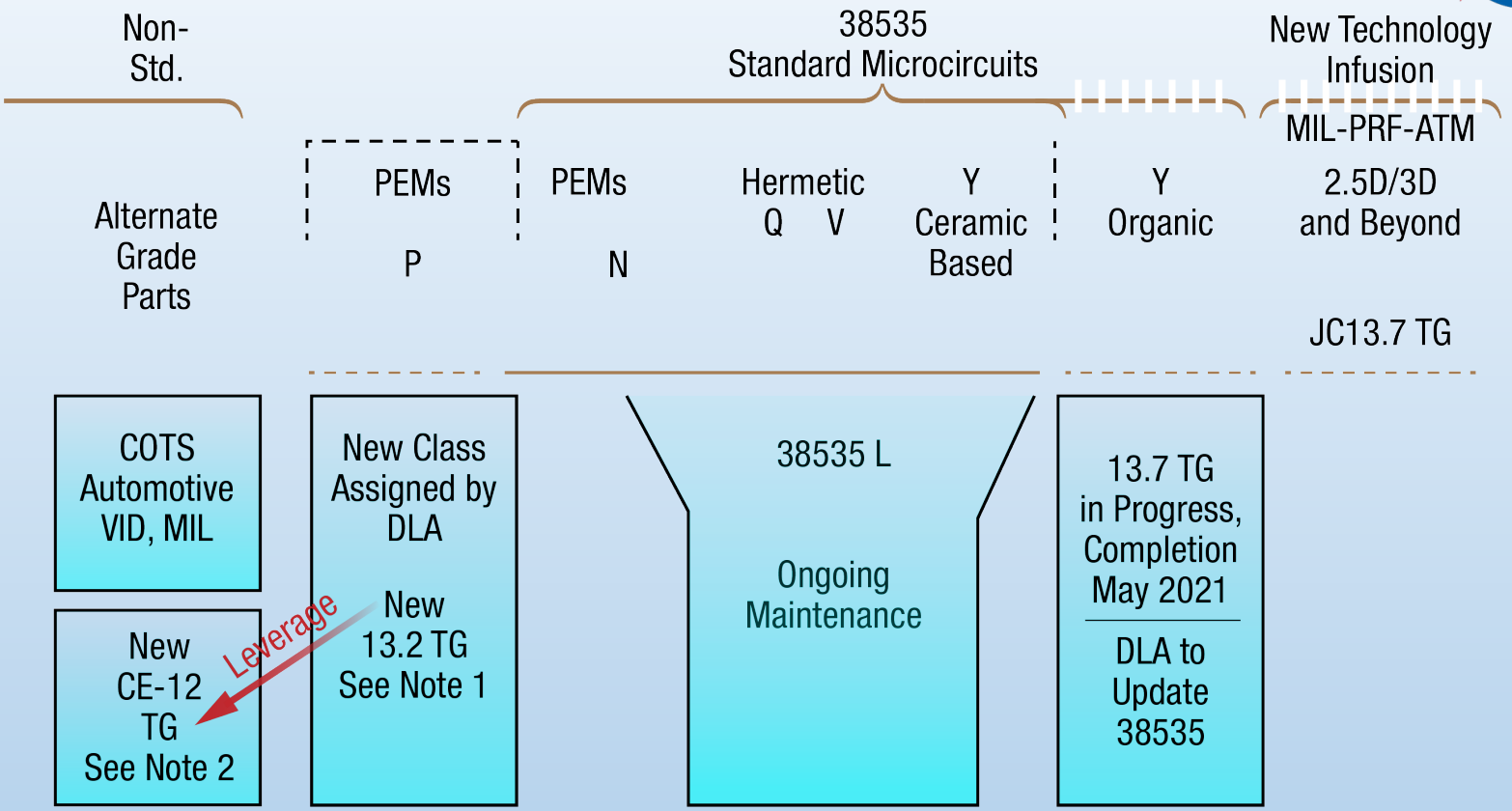
Appendix B is intended for **space application** and is required for class V and class Y (class level S) devices.

Appendix C is mandatory for devices requiring **radiation hardness assurance** (RHA).

Appendix D is mandatory for statistical sampling, life test, and qualification procedures used with microcircuits.

Options for Microcircuits

Rev. B 3-16-21



- Note 1: Standard PEMs for Space (QMLP) initiative using SAE AS6294 as baseline.
- Note 2: For alternate grade microcircuits, follow the activity in 13.2 TG to avoid any duplication of effort.
- Note 3: VID = Vendor Item Drawing; ATM = Advanced Technology Microcircuits

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits.

Screening Tests	MIL-STD-883, test method (TM) and conditions		
	Class Q (class level B)	Class V (class level S)	Class Y (class level S)
1. Wafer lot acceptance test	QM plan (see H.3.2.1.4) 1/	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)
2. Nondestructive bond pull (NDBP) test 2/		TM 2023	TM 2023
3. Internal visual inspection 3/	TM 2010, condition B	TM 2010, condition A	TM 2010, condition A
4. Temperature cycling 4/	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum
5. Constant acceleration 5/	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only
6. Visual inspection 6/	100%	100%	100%
7. Particle Impact Noise Detection (PIND) test 7/ 8/		TM 2020, test condition A on each device	TM 2020, test condition A on each device
8. Serialization 9/	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)
9. Pre burn-in (Interim) electrical parameters test 10/	In accordance with device specification 11/	In accordance with device specification 12/	In accordance with device specification 12/
10. Burn-in test: 10/ 13/ 14/	TM 1015 160 hours at +125°C minimum	TM 1015 240 hours at 125°C, condition D 15/	TM 1015 240 hours at 125°C , condition D 15/
11. Post burn-in (Interim) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/
12. Reverse bias burn-in test (Static burn-in) 13/ 14/ 16/		TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum
13. Post burn-in (Interim-reverse bias) electrical parameters test 10/		In accordance with device specification 12/	In accordance with device specification 12/

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

Screening Tests	MIL-STD-883, test method (TM) and conditions		
	Class Q (class level B)	Class V (class level S)	Class Y (class level S)
14. Percent defective allowable (PDA) calculation 17/	5 percent PDA (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)
15. Final electrical tests 18/ (see table III) a. Static test : (1) at 25°C (2) Maximum and Minimum operating temperature b. Dynamic or functional test : 19/ (1) at 25°C (2) Maximum and Minimum operating temperature c. Switching test : (1) at 25°C (2) Maximum and Minimum operated temperature	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test)
16. Seal test 20/ a. Fine leak b. Gross leak	TM 1014	TM 1014	Not applicable
17. Radiographic (X-ray) and/or SAM test 21/		X-ray: TM 2012, Two views; SAM TM 2030	X-ray: TM 2012, Two views; SAM TM 2030
18. External visual inspection 22/ 23/	TM 2009	TM 2009	TM 2009
19. Qualification or quality conformance inspection/TCI test sample selection	24/	24/	24/
20. Radiation dose rate induced latch-up test 25/	TM 1020	TM 1020	TM 1020

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

1/ Testing per manufacturer's QM plan. See paragraph H.3.2.1.4 of MIL-PRF-38535 or TM 5007 of MIL-STD-883.

2/ For flip chip packages Nondestructive bond pull (NDBP) test is not required.

3/ Unless otherwise specified, at the manufacturer's option for test samples selection of group B, bond strength test (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam), and unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controlled environment until sealed. Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3 method 5004 of MIL-STD-883). For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 should be used. For flip chip devices, both internal visual and SAM inspection (such as prior to bump attach to die and after bump attach to substrate and underfill cured etc.) shall be performed in accordance with TM 2010 and TM 2030.

4/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of PIDTP and QM plan.

5/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.

6/ At the manufacturer's option, external visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

7/ See paragraph A.4.6.3 of appendix A and paragraph B.4.1 of appendix B of MIL-PRF-38535. The PIND test may be performed in any sequence after temperature cycling test and prior to post burn-in (interim) electrical parameters test.

8/ For device without a cavity or for flip chip devices with underfill, PIND test is not applicable.

9/ Class V or class Y (class level S) devices shall be serialized prior to the first recorded electrical measurement in screening. Class Q (class level B) microcircuits shall be serialized if delta calculations or matching characteristics are a requirement of the device specification. Each microcircuit shall be assigned a unique serial number in order to trace the data back to an individual device within the inspection lot which shall, in turn, be traceable to the wafer lot from which the device originated.

10/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when PDA is specified (Ref. test step 14: PDA calculation, and footnote 17 herein). If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or standard microcircuit drawing (SMD). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to the time and temperature effects of burn-in and the most effective in removing electrically defective devices.

11/ When specified in the applicable device specification, 100 percent of the devices shall be tested and the results recorded for those parameters requiring delta calculations.

12/ For class V and class Y (class level S) microcircuit devices, delta measurements shall be performed. The specific delta parameters shall be as defined in the applicable device specification. Pre burn-in and post burn-in interim electrical parameters shall be read and recorded when delta measurements have been specified as part of post burn-in electrical measurements, 100 percent of the devices shall be tested and the results shall be recorded for those parameters requiring delta calculations.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

13/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with SMD section 4.2, or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the wafer lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request. For devices with solder terminations, burn-in test may be performed before solder balls/columns have been attached to the packages.

14/ When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in , it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (e.g, to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

15/ Where applicable(for new product families or new technology devices use JEDEC publication JEP163) , dynamic burn-in test shall be performed, and test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class V or class Y (class level S), burn-in test shall be performed in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the qualifying activities for dealing with lot failures.

16/ The reverse bias burn-in is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be a concern. When reverse bias burn-in is not required, interim post burn-in electrical parameter measurements shall be omitted. The order of performing the burn-in test and the reverse bias burn-in test may be inverted. Static burn-in may be substituted for high temperature reverse bias burn-in based on device technology and must be approved by the QA. Moreover, burn-in time-temperature regression table I of TM 1015 of MIL-STD-883 can be used for determination of reverse bias burn-in time and temperature.

17/ The percent defective allowable (PDA) shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class V or class Y (class level S) the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater (see A.4.6.1.1 and A.4.6.1.2 of MIL-PRF-38535). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices.

TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic class Y microcircuits - Continued.

18/ Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of table III, group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification. For solder termination devices, ball grid array (BGA) packages electrical test shall be performed across the full military temperature range after attachment of the solder balls on the package, and for column grid array (CGA) packages, electrical test shall be performed across the full military temperature range before attachment of the solder columns on the package. After column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.

19/ Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH}(min) +20$ percent, -0 percent; $V_{IL} = V_{IL}(max) +0$ percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH}(min)$ and $V_{IL}(max)$ requirements are not violated at the device terminals.

20/ The fine and gross leak seal tests shall be performed separately or together, between constant acceleration and external visual inspection test. For class level S and class level B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal or external visual inspection shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method TM 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (method TM 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class level S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal, but before external visual, if the devices are installed in individual carriers during electrical test.

21/ The radiographic and/or SAM screening test may be performed in any sequence after serialization. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides. For flip chip technology, only SAM inspection is required. SAM inspection may be performed in any sequence after underfill cure for flip chip technology. For additional requirements for this test, see appendix B paragraph B.4.1 of MIL-PRF-38535.

22/ External visual inspection shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

23/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

24/ Samples shall be randomly selected from the assembled inspection lot for testing in accordance with the specific device class and lot requirements of Group A, B, C, D, E and applicable appendices of MIL-PRF-38535 or TM 5005 of MIL-STD-883; after the specified screen requirements herein table IA or TM 5004 have been satisfactorily completed.

25/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, it may be performed at any screening operation step after seal test, at the manufacturer's option. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the device specification. The PDA for each inspection lot for class V or class Y (class level S) sublot submitted for radiation latch-up test shall be 5 percent or one device, whichever is greater.

TABLE III. Group A (electrical tests) . 1/

Subgroups	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.) 2/ 3/ 4/ 5/		
		Class Q (class level B)	Class V 6/ (class level S)	Class Y 6/ (class level S)
1 2 3	Static tests at +25°C Static tests at maximum rated operating temperature Static tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
4 5 6	Dynamic tests at +25°C Dynamic tests at maximum rated operating temperature Dynamic tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
7 8A 8B	Functional tests at +25°C Functional tests at maximum rated operating temperature Functional tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
9 10 11	Switching tests at +25°C Switching tests at maximum rated operating temperature Switching tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/ herein) may be conducted individually or combined into sets of tests, subgroups (as defined in table III), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in 2/ herein, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For those lots having a quantity of less than 116 devices, the test shall be imposed on a 100 percent basis with zero failure.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For device class V or class Y (class level S), if the testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

6/ For class V and class Y, group A electrical tests additional requirements see paragraph B.4.3 appendix B of MIL-PRF-38535.

TABLE II. Group B tests (Mechanical and environmental test)

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 1	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)		a. Physical dimensions 3/ TM 2016 2(0) b. Internal gas analysis (IGA) test TM 1018 3(0) 3/ 4/ 5/ (5,000 ppm maximum water content at 100°C)
Subgroup 2 6/	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	a. Resistance to solvents 2/ TM 2015 3(0)	a. Resistance to solvents 2/ TM 2015 3(0) b. Internal visual and mechanical TM 2013, TM 2014 2(0) c. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H d. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) e. Flip chip pull off test TM 2031 or TM 2011 2(0) f. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)

TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 3 sample size 22(0) (22 leads from 3 devices) 8/	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C
Subgroup 4 sample size 45(0) 3/		For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)	For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package - TM 2038 (45 columns from 2 devices minimum)		a. Lead integrity TM 2004 9/ (Test condition B2, lead fatigue) b. Seal test TM 1014 as applicable (1) Fine leak (2) Gross leak c. Lid torque TM 2024 10/ as applicable d. For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)

TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)			Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Class Q	Class V	Class Y	Class level B	Class level S
Subgroup 5				a. Bond strength TM 2011 15(0) 11/ (1) Thermo compression - Test condition C or D (2) Ultrasonic - condition C or D (4) Beam lead - condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0) c. Flip chip pull off test TM 2031 or TM 2011 2(0) d. Flip chip die shear strength test or substrate attach strength test (test perform post underfill cure) TM 2019 or TM 2027 3(0)	sample size 45(0) a. End-point electrical parameters 12/ - As specified in the applicable device specification b. Steady state life test 13/ TM 1005 Test condition C, D or E c. End-point electrical parameters 12/ - As specified in the applicable device specification
Subgroup 6 Sample size 15(0) 14/					a. Temperature cycling TM 1010, condition C, 100 cycles minimum b. Constant acceleration TM 2001, condition E, Y_1 orientation only c. Seal test TM 1014 (1) Fine leak (2) Gross leak d. End-point electrical parameters - As specified in the applicable device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.

2/ Resistance to solvents testing required only on devices using inks or paints as a marking medium.

3/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot. For devices with solder terminations, Physical dimension test shall be performed with balls/columns.

4/ This test is required only, if it is a glass-frit-sealed package. Unless handling precautions for beryllium packages are available and followed TM 1018, procedure 3 shall be used (see group D, subgroup 6 of table V). For class Y non-hermetic microcircuits devices Internal gas analysis (IGA) test is not applicable.

5/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturer's option, if the initial test sample fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the test data from both submissions is submitted to the qualifying activity.

6/ For all devices, except flip chip, the die shear test or substrate attach strength or stud pull test including passive elements shall be performed per TM 2019 or TM 2027, as applicable. For flip chip devices, flip chip pull off test shall be performed per TM 2031 or TM 2011. Flip chip die shear test or substrate attach strength test shall be performed after underfill is cured per TM 2019 or TM 2027. If the flip chip device uses passive elements the substrate attach strength or stud pull test shall also be performed per TM 2019 or TM 2027. For solder termination devices, subgroup 2 test may be performed without balls and columns attached.

7/ Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition H is the number of dice (not bonds) (see TM 2011).

8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003.

9/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 10/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use TM 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need to be performed only on packages having leads exiting through a glass seal. For LGA/BGA/CGA packages, TM 2004 does not apply.

10/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

11/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in table IA herein or TM 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see TM 2011).

12/ Read and record group A subgroups 1, 2 and 3.

13/ The alternate removal-of-bias provisions of 3.3.1 of TM 1005 shall not apply for test temperature above 125°C.

14/ For devices with solder terminations, Temperature cycling and Constant acceleration test may be performed without balls/columns attachment.

TABLE IV. Group C life tests .

Subgroup	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B) 1/	Class V (class level S) 1/ 2/	Class Y (class level S) 1/ 2/
Subgroup 1	a. Steady-state life test	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C
	b. End-point electrical parameters	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification

1/ Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-months period.

2/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with table IV herein. Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

(a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

(b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

(c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

TABLE V. Group D tests (Package related test) .

Subgroups test	Tests 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 1 sample size 15(0) 2/	Physical dimensions	TM 2016	TM 2016	TM 2016
Subgroup 2 sample size 45(0) 2/ 3/	a. Lead/terminal integrity test	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style
	b. Seal test 4/ (1) Fine leak (2) Gross leak	b. TM 1014 Test condition as applicable	b. TM 1014 Test condition as applicable	b. 5/
	c. For BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages
	(i) Ball shear test for BGA package	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)
	(ii) Solder column pull test for CGA package	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)
Subgroup 3 sample size 15(0) 6/ 7/	a. Thermal shock	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum
	b. Temperature cycling	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum
	c. Moisture resistance	c. TM 1004 8/	c. TM 1004 8/	c. HAST in accordance with JESD22-A118, condition B
	d. Visual examination	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010
	e. Seal test 9/ (1) Fine leak (2) Gross leak	e. TM 1014 test condition as applicable	e. TM 1014 test condition as applicable	e. 5/
	f. End-point electrical parameters 10/	f. As specified in the applicable device	f. As specified in the applicable device	f. As specified in the applicable device

TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 4 sample size 15(0) 6/ 7/	a. Mechanical shock	a. TM 2002 condition B minimum	a. TM 2002 condition B minimum	a.TM 2002 condition B minimum
	b. Vibration, variable frequency	b. TM 2007 condition A minimum	b. TM 2007 condition A minimum	b.TM 2007 condition A minimum
	c. Constant acceleration 11/	c. TM 2001 Test condition E, Y1 orientation only	c. TM 2001 Test condition E, Y1 orientation only	c.TM 2001 Test condition E, Y1 orientation only
	d. Seal test (1) Fine leak (2) Gross leak	d. TM 1014 condition as applicable	d. TM 1014 condition as applicable	d. 5/
	e. Visual examination	e. In accordance with visual criteria of TM 2007	e. In accordance with visual criteria of TM 2007	e. In accordance with visual criteria of TM 2007
	f. End-point electrical parameters	f. As specified in the applicable device specification	f. As specified in the applicable device specification	f. As specified in the applicable device specification
Subgroup 5 sample size 15(0) 2/	a. Salt atmosphere	a. TM 1009 Test condition A minimum	a. TM 1009 Test condition A minimum	a. TM 1009 Test condition A minimum
	b. Visual examination	b. In accordance with visual criteria of TM 1009	b. In accordance with visual criteria of TM 1009	b. In accordance with visual criteria of TM 1009
	c. Seal 9/ (1) Fine leak (2) Gross leak	c. TM 1014 condition as applicable	c. TM 1014 condition as applicable	c. 5/
Subgroup 6 2/ 12/	Internal gas analysis (IGA) test (cavity packages)	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	5/
Subgroup 7 sample size 15(0) 2/ 13/ 14/	Adhesion of lead finish	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025

TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 8 sample size 5(0) 2/	Lid torque 15/	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024
Subgroup 9 sample size 3(0) (3 leads minimum) 16/	a. Soldering heat	Where applicable a. TM 2036	Where applicable a. TM 2036	Where applicable a. TM 2036
	b. Seal (1) Fine leak (2) Gross leak	b. TM 1014 condition as applicable	b. TM 1014 condition as applicable	b. 5/
	c. External Visual examination	c. TM 2009	c. TM 2009	c. TM 2009
	d. End-point electrical	d. As specified in the applicable device specification	d. As specified in the applicable device specification	d. As specified in the applicable device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

1/ In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.

2/ Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5 and 8 tests shall be performed with balls and columns.

3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use TM 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum. For LGA/BGA/CGA packages, TM 2004 does not apply.

4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

5/ This test is not applicable for class Y non-hermetic microcircuits devices.

6/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

TABLE V. Group D tests (Package related test). - Continued.

7/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns.

8/ Lead bend stress initial conditioning is not required for leadless chip carrier packages or BGA/CGA packages. For fine pitch packages (25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.

9/ After completion of the required visual examinations and prior to submittal to TM 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

10/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

11/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.

12/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes, the lot shall be accepted provided the test data from both submissions is submitted to the qualifying activity.

13/ The adhesion of lead finish test shall not apply for leadless chip carrier, land grid array (LGA), ball grid array (BGA), and column grid array (CGA) packages.

14/ Sample size number 15 leads from 3 devices minimum are based on number of leads with zero failure.

15/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

16/ This test is performed at qualification/re-qualification of design changes which may affect this test. The manufacturer shall determine, for each package, the applicable conditions from TM 2036 that are appropriate for the mounting conditions, and assure by testing, or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

Questions?

To be presented by P. Majewicz at the Components for Military & Space Electronics Virtual Conference (CMSE), April 19-23, 2021.