all around you

Qualification Activities at Qorvo for GaN Space Applications

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Agenda

- Introduction
- GaN HEMT DC and RF reliability tests
- Passive component reliability tests
- Environmental testing
- Other wafer, die, and product-level tests and qualifications
- Summary

Introduction

- Several Qorvo lead customers have designed circuits using our GaN foundry services for their space programs
- Qorvo has conducted comprehensive testing to qualify our GaN devices for use in space
- Some of the test results are summarized in this presentation

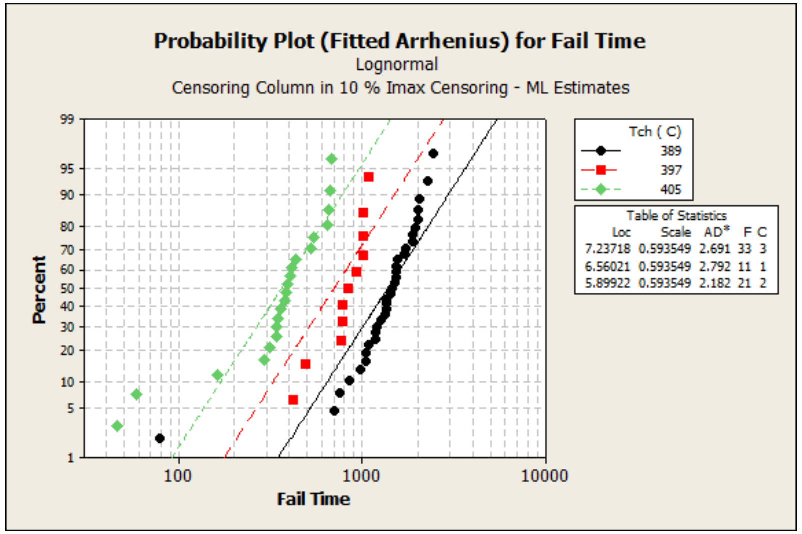
GaN HEMT Accelerated DC Life Test

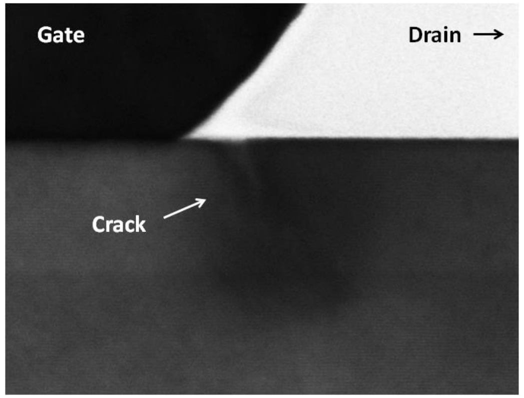
GaN HEMT Accelerated DC Life Test

- **Objectives**
  - Study GaN HEMT degradation mechanisms under DC bias and elevated temperature
  - Establish maximum operating conditions for reliable transistor operation with median life tm > 10^6 h
- **Results**
  - Qorvo has extensive DCLT GaN HEMT data collected over more than 15-year span
  - Qorvo GaN HEMT degradation under DC bias is temperature (but not voltage) driven
  - Operating at temperatures of Tch = 200 °C guarantees tm > 10^7 h for all Qorvo GaN technologies
- **Test Methods**
  - A number of multi-temperature and multi-voltage tests performed
  - Some tests performed at Vd up to ~2x technology Vdmax
  - Continually adjust Vg to maintain constant Id = 250-350 mA/mm
  - Tb chosen to achieve Tch = 355-415 °C based on detailed thermal models
  - Monitor in-situ Imax, Ig
  - Some tests performed with additional room-temperature transfer, IV, and BV sweeps

DCLT Activities for Technology Qualification

- For each GaN technology qualification, DC life tests performed on multiple lots/wafers on over 100 die and for durations in excess of 1000 h per test in some cases[1]
- Multiple three-temperature tests show all Qorvo GaN technologies (GaN15, GaN25, GaN25HV) have the same activation energy Ea = 2.1 eV (1.7 eV 90 % SS LB)
- Failure mechanism is well understood and shown to be pitting/cracking at drain edge of the gate (inverse piezo-electric effect)[2]





[1]Gergana I. Drandova, Jose L. Jimenez, Peter T. Goeller, and Aaron P. Ferreira, TriQuint's 2nd Generation TQGaN25 Technology Reliability Assessment, Reliability of Compound Semiconductors Workshop, 2013

[2]U. Chowdhury, J. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri; S. Y. Park, T. Lee, J. Wang, and M. J. Kim; J. Joh, and J. A. del Alamo, Electron Device Letters, 2008

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RF Operational Life Test

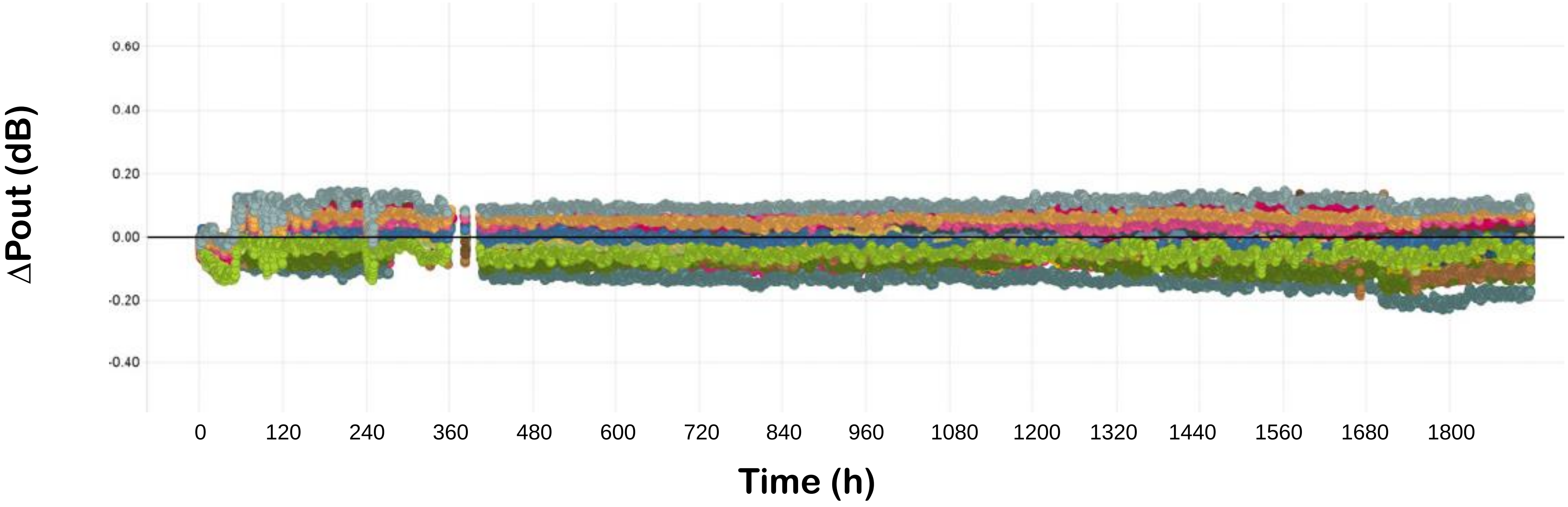
Qorvo GaN RFOLT Results

Summary

- Testing performed under RF drive on variety of GaN products (15 W to 100 W) up to a 4000-hour duration, both under CW and pulsed conditions
- Test methodology
  - Devices tested at the maximum allowed bias and temperature for the product
  - Constant Vg
  - No DC or RF burn-in performed prior to test
- Small changes (avg. -0.2 dB over all DUTs) observed soon after start of test followed by saturation
  - Consistent with charge trapping causing ~ 3 % Vp increase and respective Idq decrease impacting small signal gain
  - Heavily saturated amplifiers show negligible Pout change
  - Lightly compressed amplifiers show more Pout change
  - Shorter gate lengths suffer from higher charge trapping

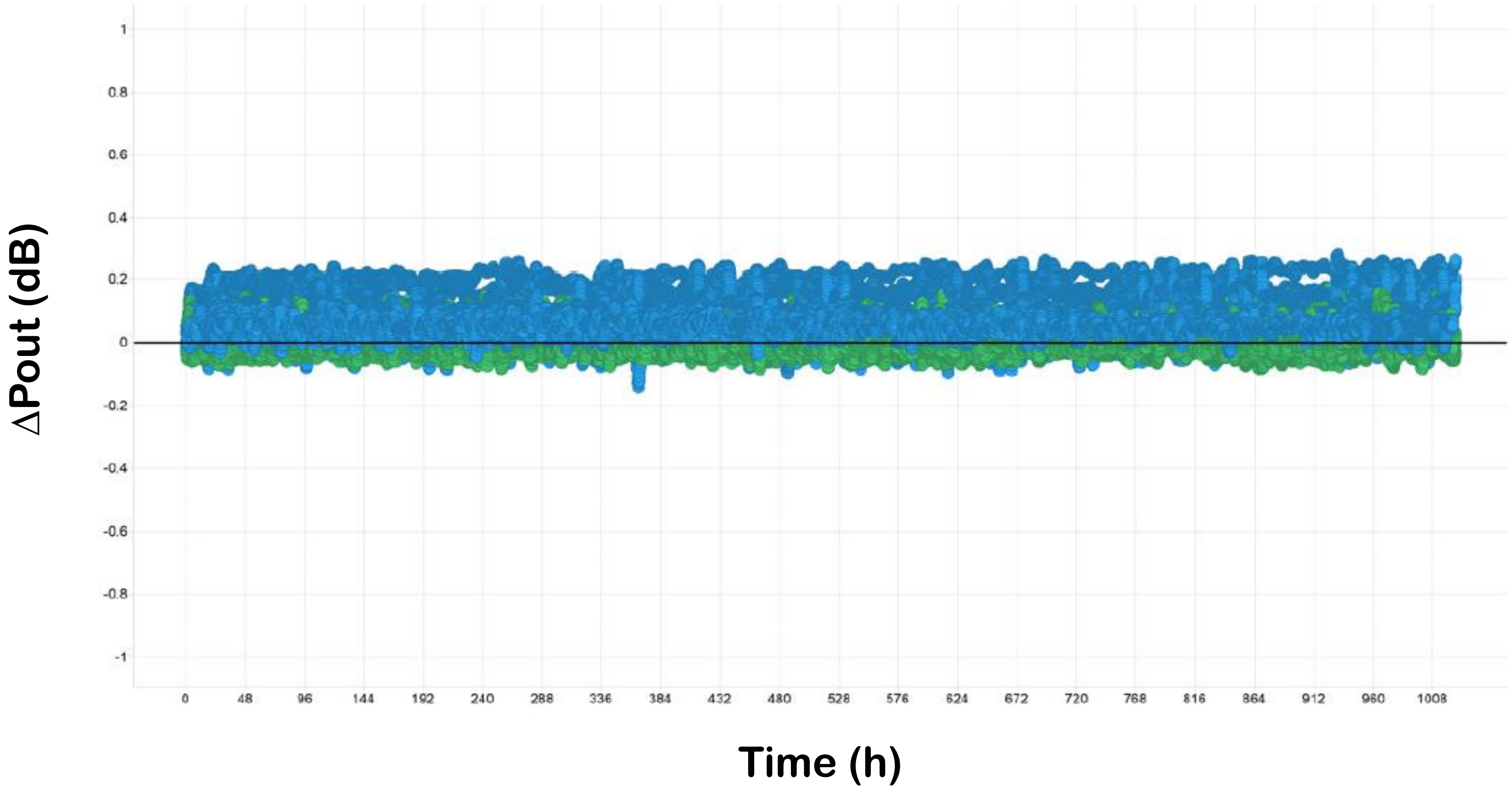
GaN25 HPA RFOLT Example

- Highly-compressed GaN25 HPAs (24 devices) showing no appreciable change in Pout over 2000 h



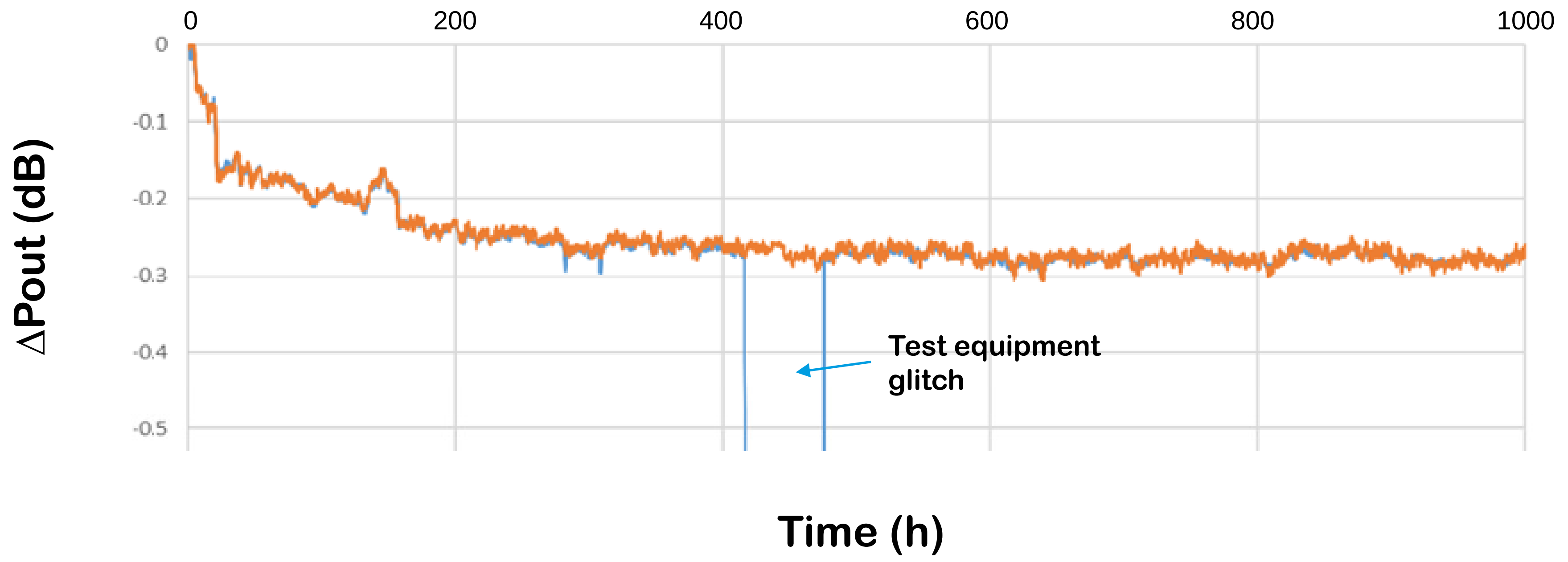
GaN25HV High Power Transistor Example

- **Highly-compressed GaN25HV high-power transistors showing no appreciable change in Pout over 1000 h**



Multi-Stage GaN HPA at Lower Compression Level

- Example of HPA operated at a lower compression level
- Reduction in small-signal gain from charge trapping and Vp shift results in Pout reduction, most of which occurs rapidly after start and then saturates
- Majority of Pout recoverable after baking



HTRB Test

High-Temperature Reverse-Bias (HTRB) Test Summary

- GaN15 devices (count 24) stressed under pinched conditions
  - Bias: Vg = -5 V, Vd = 35 V (higher than Vd_{max} = 28 V for technology)
  - Temperatures: 30 °C & 125 °C
  - Test duration: 2000 hours
- DUTs periodically taken off stress and measured on test bench
  - Bench test – transfer sweeps at room temperature
- Results
  - No catastrophic failures
  - Idmax shift < 5 % and Vp shift ~ 10 % observed at 125 °C (half of this at 30 °C). Shifts occur soon after start of test, similar to RFOLT
  - No in-situ Ig increase at 30 °C, some increase at 125 °C with final current < 0.5 mA/mm

HTRB Test Results Summary

30 °C

Parameter	Min	Average	Max
(% change from 0 to 2000 hours)			
Vp (Pinch Off)	2.5	4.7	5.9
Gm0 (Gm at Vg=0)	-1.09	2.18	5.49
Gm Max	-2.23	10.05	23.2
Idss	-3.75	-4.88	-5.47
Idmax	-2.25	-2.95	-3.89

125 °C

Parameter	Min	Average	Max
(% change from 0 to 2000 hours)			
Vp (Pinch Off)	6.64	10.5	18.21
Gm0 (Gm at Vg=0)	1.12	5.23	7.83
Gm Max	-2. 32	10.4	22.9
Idss	-7.32	-7.84	-8.29
Idmax	-4.12	-4.68	--5.35

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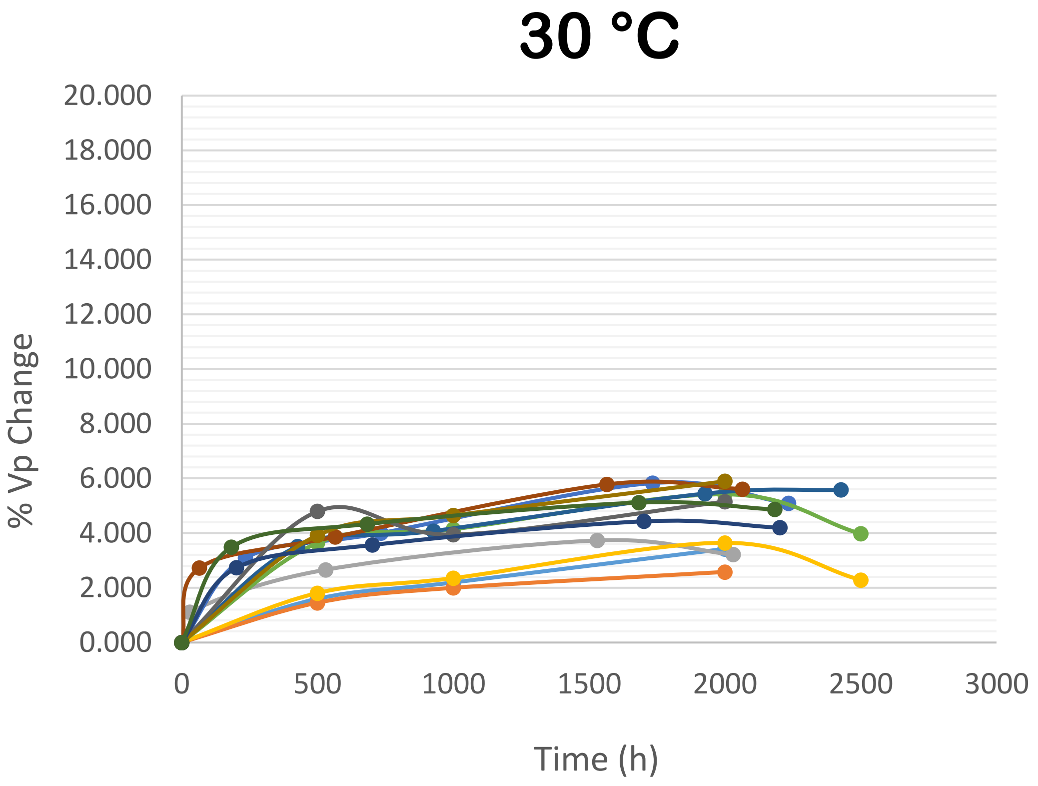
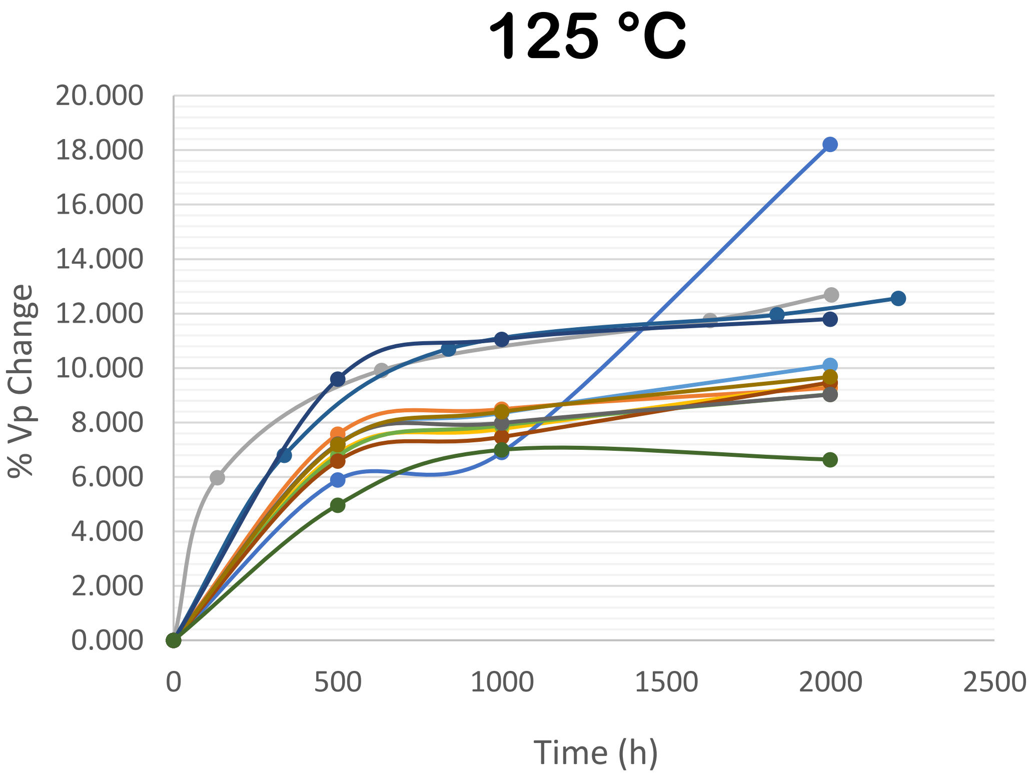
HTRB Test Vp Plots

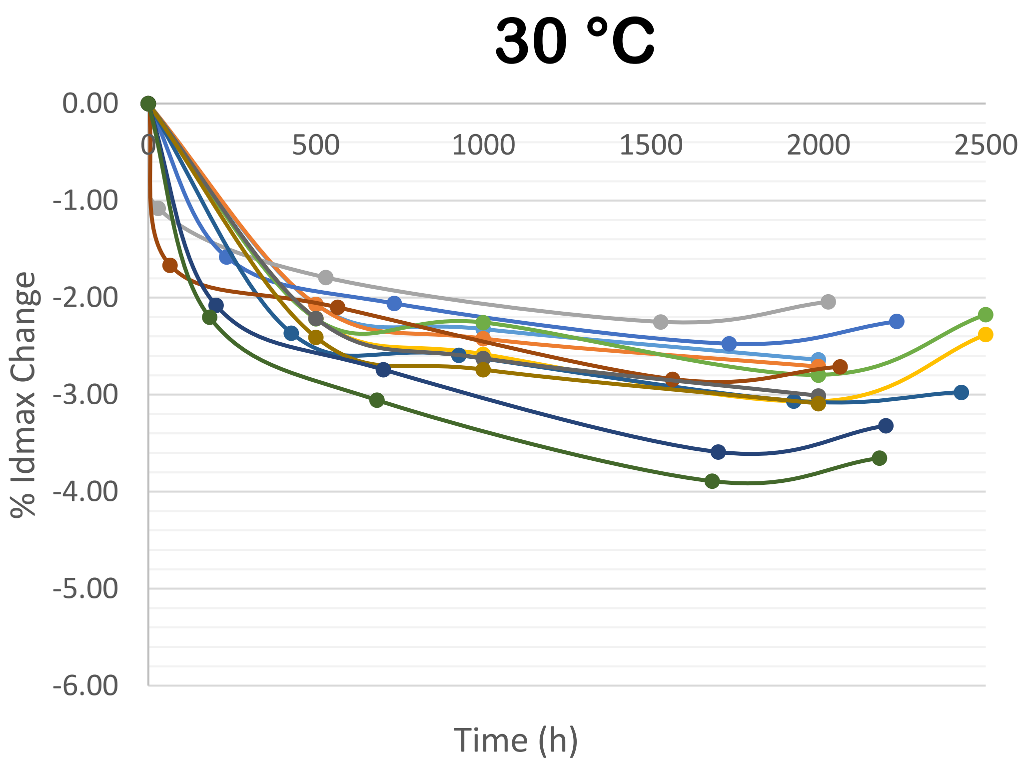
- No catastrophic failures under 2000+ h HTRB stress at Vg = - 5 V, Vd = 35 V (Vd max for technology = 28 V)
- Approx. 5 % Vp shift at 30 °C, 10 % shift at 125 °C

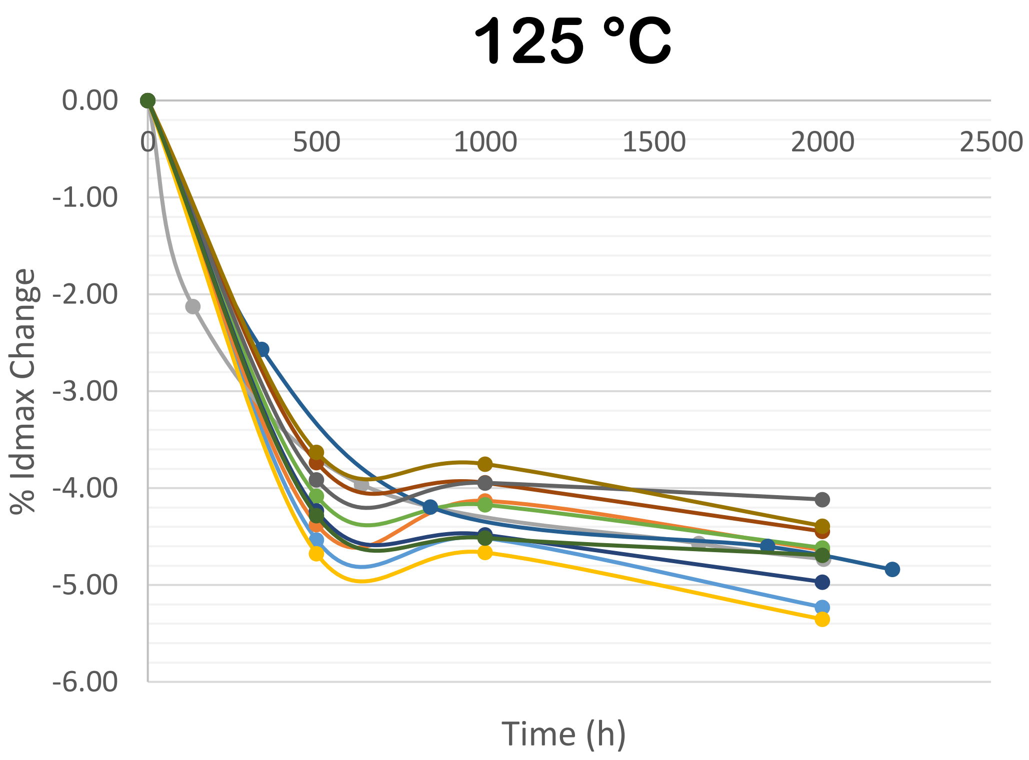




HTRB Test Idmax Plots

- **Approx. 3 % Imax shift at 30 °C, 5 % shift at 125 °C under 2000+ h HTRB stress at Vg = - 5 V, Vd = 35 V (Vd max for technology = 28 V)**





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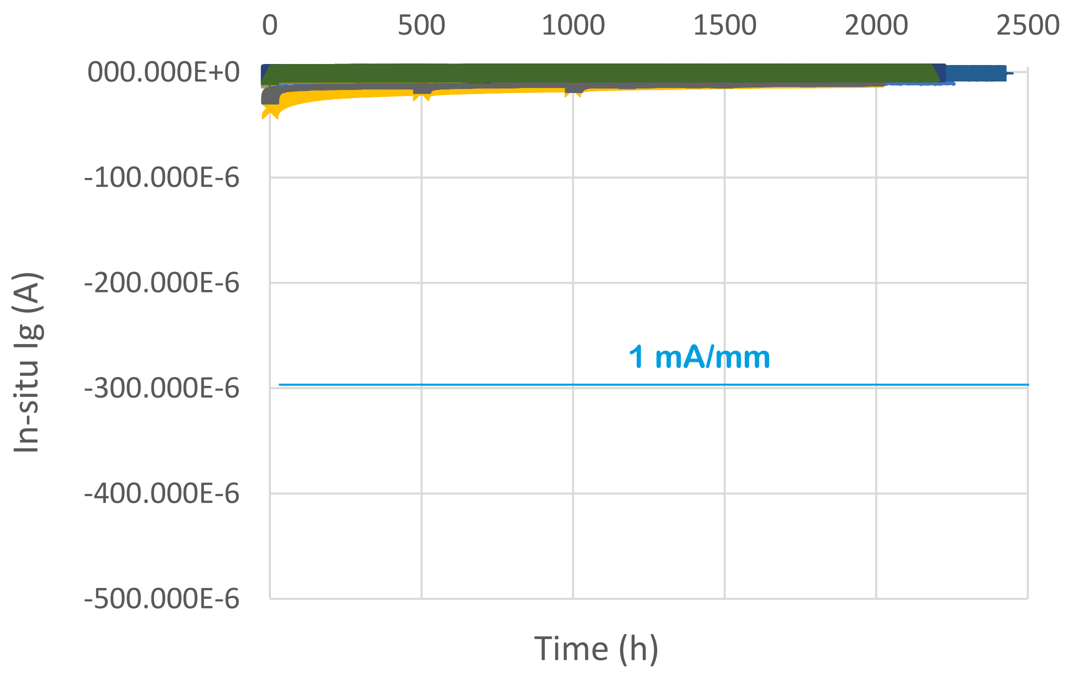
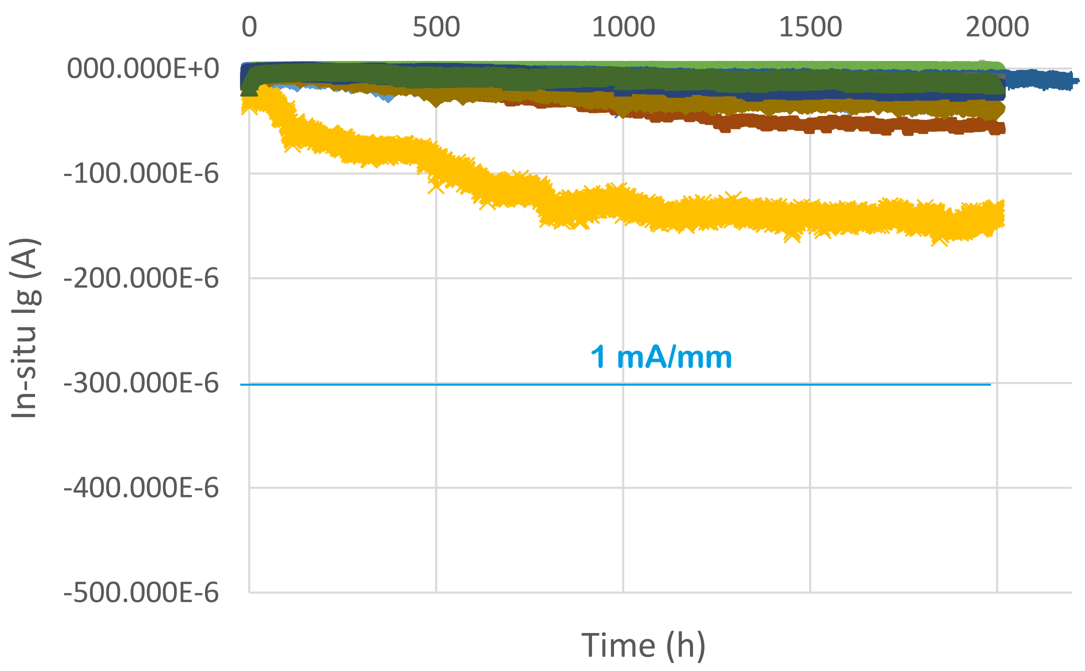
HTRB Test In-Situ Ig Plots

- Decrease in in-situ Ig leakage at 30 °C, slight increase in in-situ Ig leakage at 125 °C up to 0.5 mA/mm

30 °C



125 °C



MIM Capacitor Qualification

GaN MIM Capacitor Qualification Summary

- Qorvo GaN technology provides 3 types of capacitors supporting high capacitance density and high voltage operation
  - CTG: voltage rating 8.5 V (high capacitance density)
  - CT7: voltage rating 65 V (high voltage)
  - CT9: voltage rating 65 V (high voltage)
- GaN MIM cap reliability assessment consists of
  - Leakage testing (reduced leakage suggests improved reliability)
  - Ramped-voltage breakdown testing (provides information for weak population and lower bound on lifetimes)
  - Fixed-voltage life tests (allows more accurate median lifetime predictions)

GaN MIM Cap Reliability Assessment

- Ramped-voltage test (fast)
  - On-wafer ramp test to failure at two ramp rates and both voltage polarities
    - Assess wafer-to-wafer and lot-to-lot variation
    - Check for weak population
    - Fast estimate of median life (t_{50}) and time to 1st % failure (t_1) using linear-field model (conservative predictions)
- Fixed-voltage life test (slow) at multiple voltages and both voltage polarities
  - Predict lifetimes using more precise methods

MIM Cap Reliability Concepts

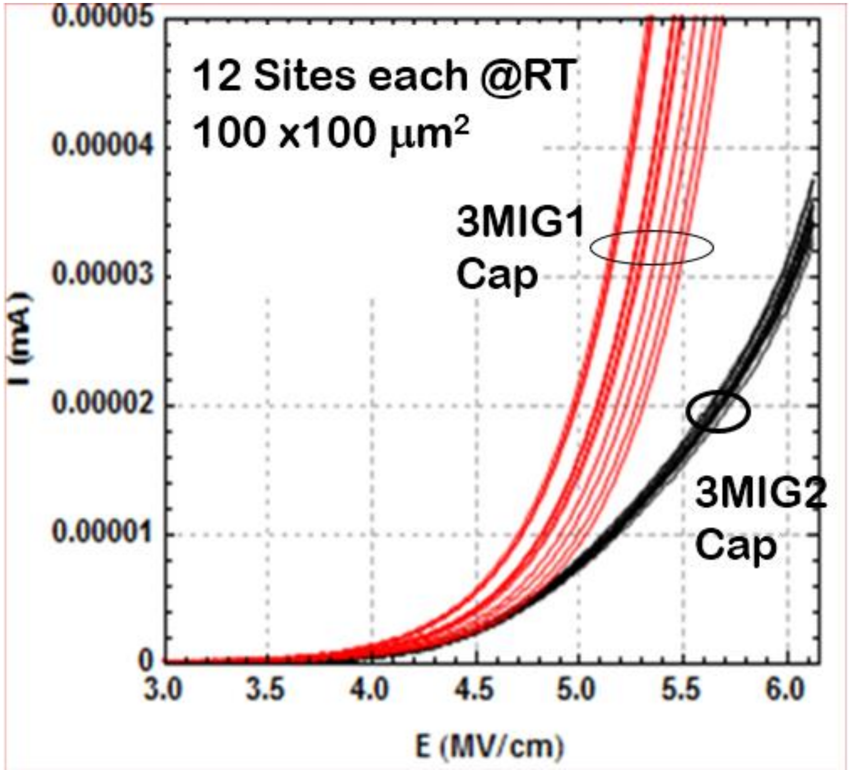
- Time-Dependent Dielectric Breakdown (TDDB)
  - Wear-out through
    - Dielectric leakage
    - Charge-trapping
  - Catastrophic failure when

$$E_{Applied} + E_{Qtrap} > E_{Breakdown}$$

  - Cap lifetimes can be improved by slowing E_{Qtrap} build-up (equivalent to reducing dielectric leakage)

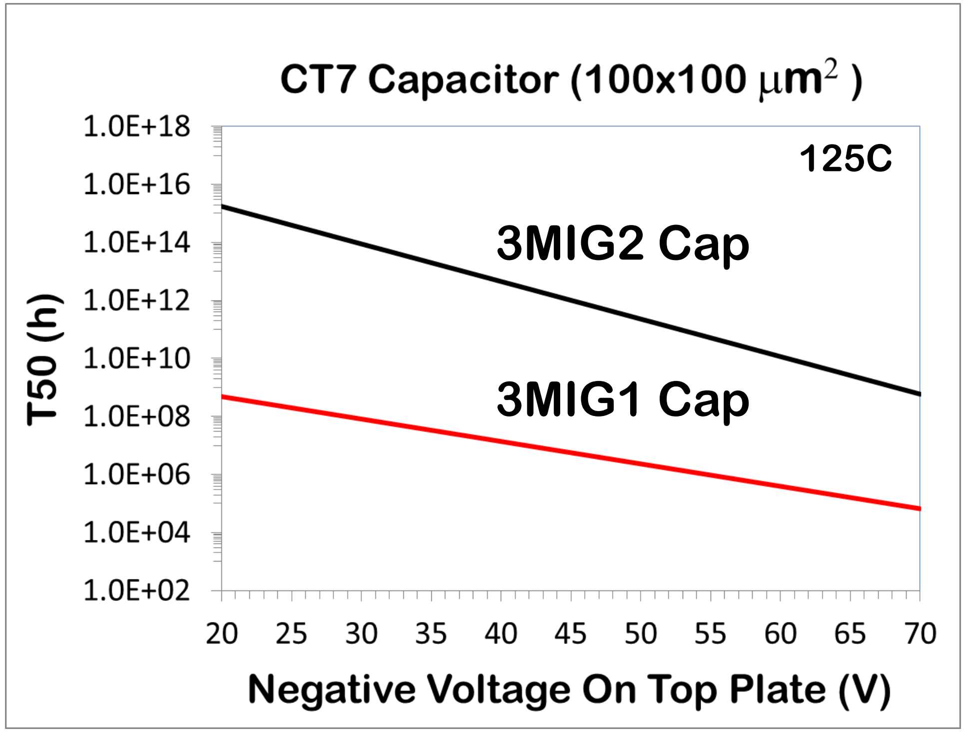
GaN Cap Dielectric Leakage Reduction

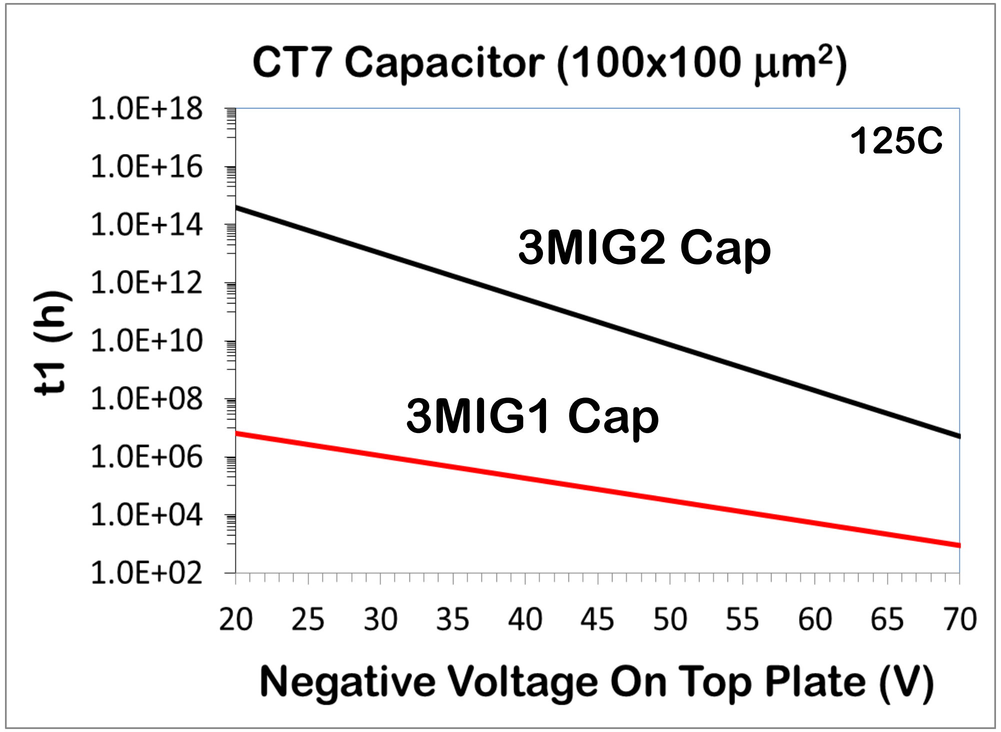
- **Significantly lower leakage for new GaN caps**
  - Slower increase of E_{Qtrap}
  - Major positive impact on cap reliability



GaN Cap Ramped-Voltage Test Results

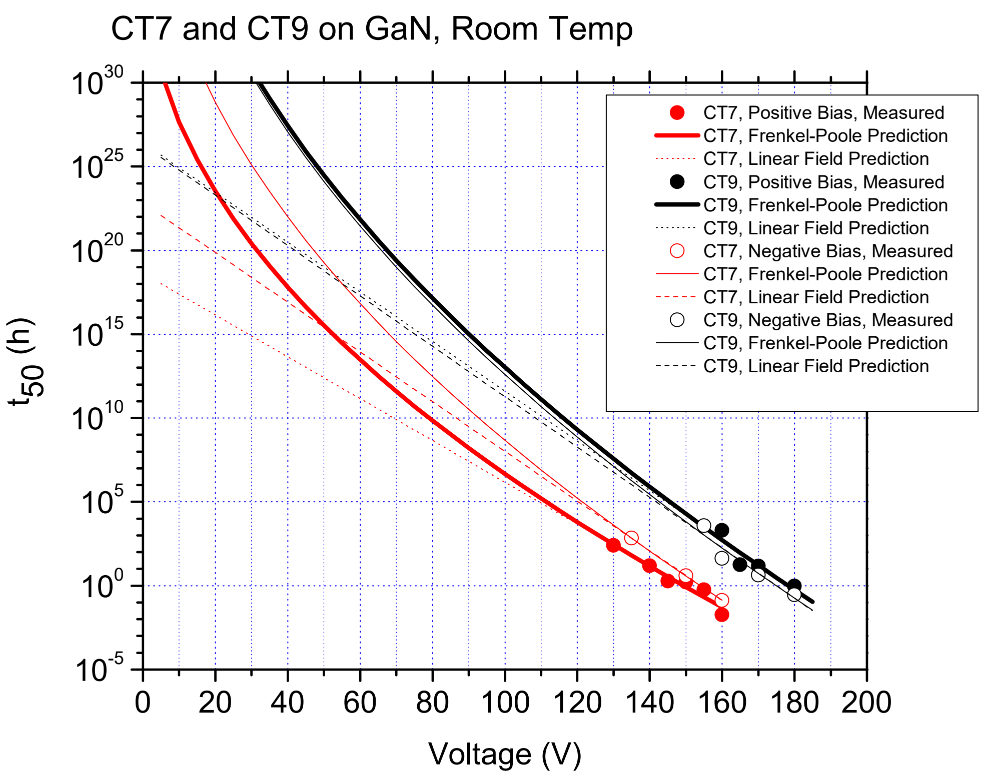
- Superior t_1 and t_{50} for new 3MIG2 GaN caps compared to older caps at the same applied voltage, due to much lower leakage predicted by ramp-voltage testing and linear field model





GaN Cap Fixed Voltage Life Test

- CT7 and CT9 GaN cap life testing at multiple voltages (both voltage polarities) performed with test duration > 4000 h at lowest voltages
- Used two models for lifetime extraction, Frenkel-Poole (more accurate at low voltages) and Linear Field model (conservative estimation) [1]
- New GaN CT7 and CT9 capacitors median life t_{50} > 1 x 10^6 h at voltages in excess of 100 V (based on single-wafer test)
- New GaN CT7 and CT9 qualified up to 65 V

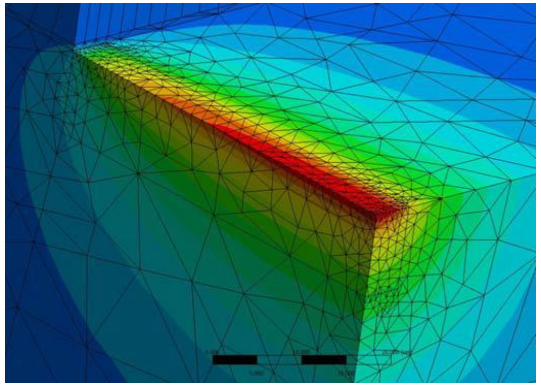


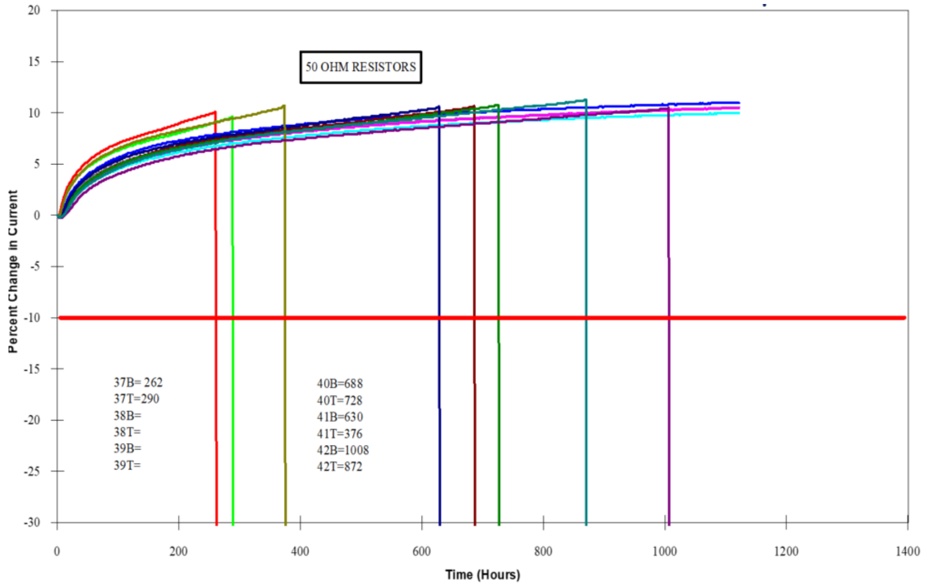
[1] G. I. Drandova, J. M. Beall, and K. D. Decker, SiN Conductivity and Capacitor Reliability, ECS Dielectrics Symposium, 2007

TaN Resistor Qualification

TaN Resistor Accelerated DC Life Tests

- **Qorvo GaN and GaAs technologies share use of on-chip TaN thin-film resistors**
- **Numerous TaN resistor life tests were conducted on different GaAs lots and wafers and on different resistor physical sizes**
- **Significant self-heating in the TaN resistors due to relatively high sheet resistance of 50 Ω/☐ → proper thermal modeling is key**
- **TaN accelerated DC life tests at high current densities and temperatures show gradual resistance decrease, followed by catastrophic burnout**





TaN Resistor Life Tests

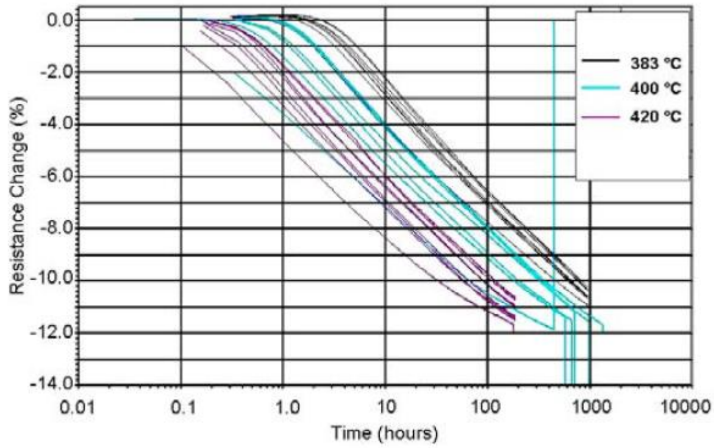
- **Extracted median lifetime model has dependence of current and temperature**

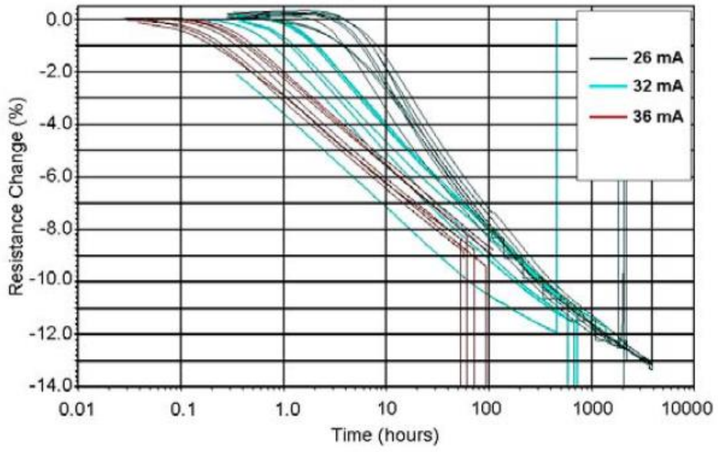
$$t_m = A(I)\, e^{\left(\frac{1}{B(I)}\left|\frac{\Delta R}{R}\right| + \frac{Ea}{kT}\right)}$$

- **High activation energy obtained from several different life tests**

  Ea = 2.3 eV

- **Based on Qorvo TaN maximum current limit we predict t1 > 10^6 h at 240 °C for TaN on GaAs. TaN resistors should be cooler on GaN on SiC at the same current density and so should have longer life**





Gergana I. Drandova, Kenneth D. Decker, TaN Resistor Reliability Studies, CS Mantech Technical Digest, 2010

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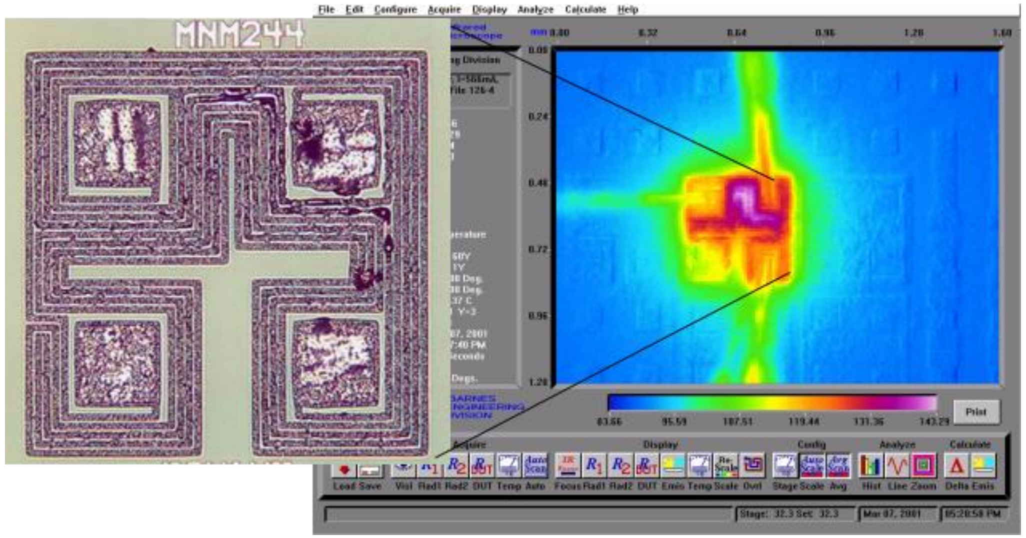
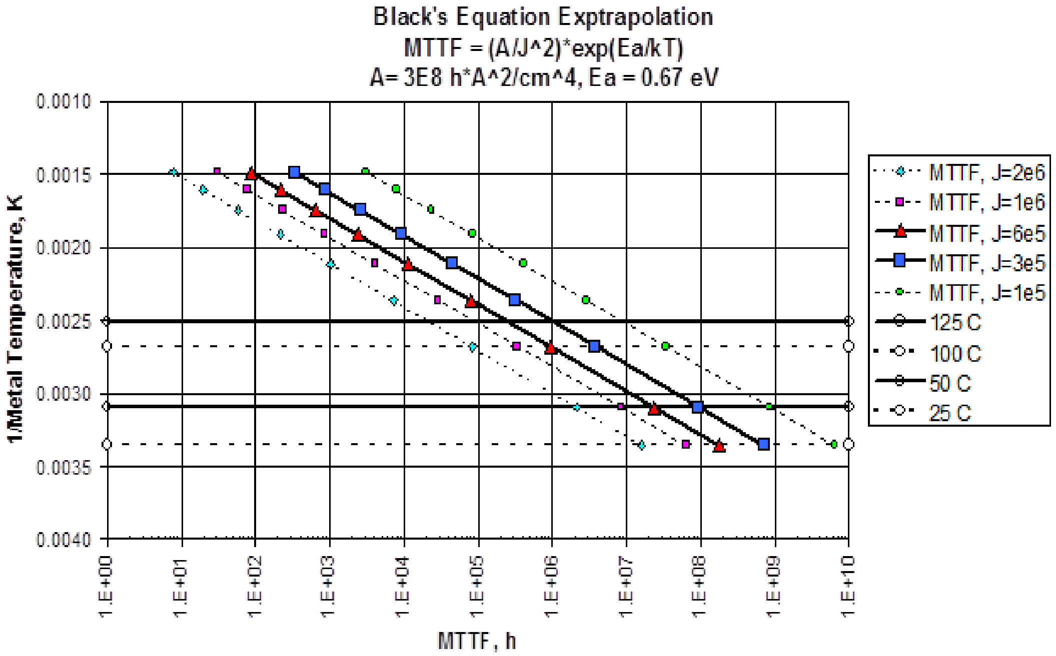
Reliability Specifications for Interconnect and Gates

Qorvo Interconnect Reliability Studies

- **Electro-migration life tests conducted on meandering structures of various Au interconnect layers at different current densities and temperatures**
- **Black's equation tm = A . $e^{Ea/kT}/J^n$ confirmed with Ea = 0.67 eV and n = 2**



Life-tested meandering structure showing signs of electro-migration. Infrared Image shows hottest area coincides with location of largest electro-migration damage



Interconnect Maximum Current Limits

- Qorvo Au interconnect maximum current design limit is 3×10^5 A/cm^2 for temperatures up to 125 °C (1/2 of MIL-PRF-38535 requirement to allow for scratches causing line-width reduction)
- Since gates can become very hot due to proximity to the FET channel, current limits for gates are scaled based on gate metal cross-sectional area and expected device channel temperature (see GaN15 example below) using extracted Black's equation parameters from our electro-migration studies

Technology	Max Gate Current at 125 °C (mA/finger)	Max Gate Current at 150 °C (mA/finger)	Max Gate Current at 175 °C (mA/finger)	Max Gate Current at 200 °C (mA/finger)	Max Gate Current at 225 °C (mA/finger)	Max Gate Current at 250 °C (mA/finger)
GaN15	1.21	0.72	0.45	0.30	0.21	0.15

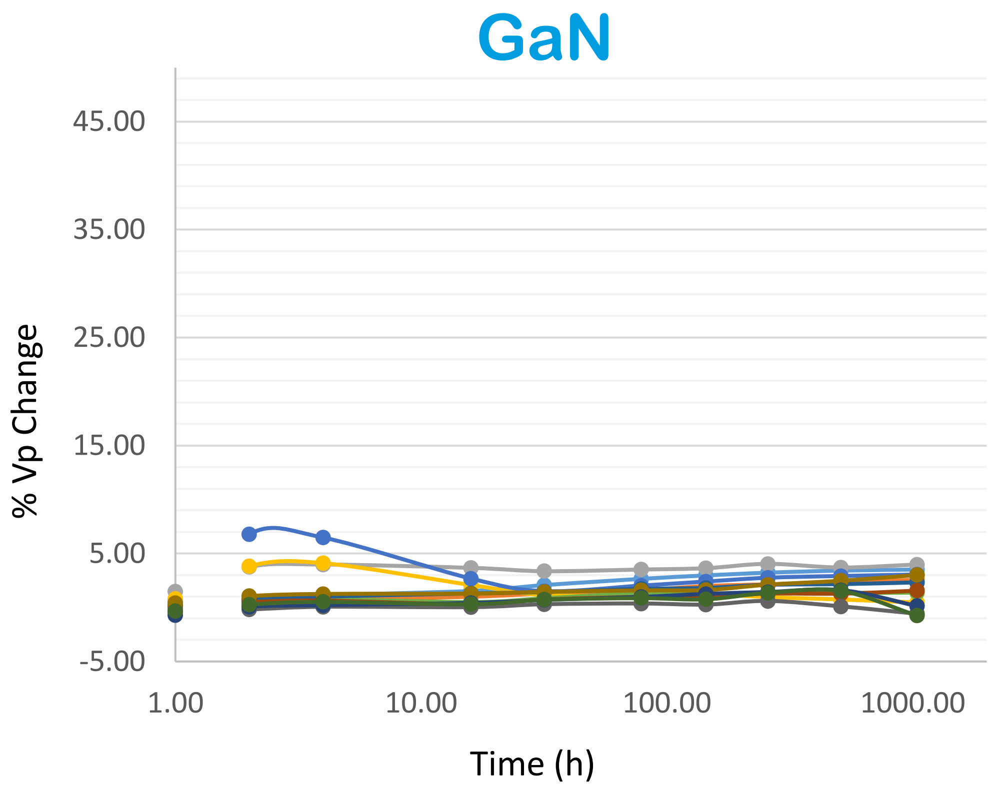
Hydrogen Sensitivity Test

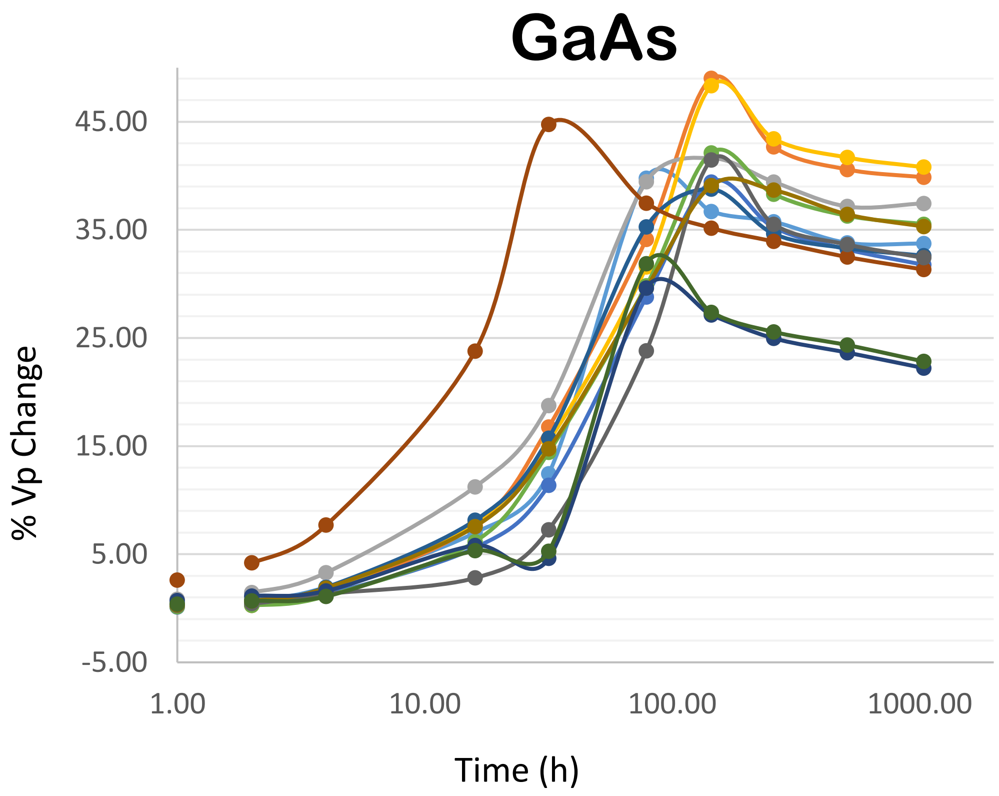
Hydrogen Sensitivity Test Summary

- GaN15 devices exposed to H_2 together with known hydrogen-sensitive GaAs devices (for comparison)
  - Stress conditions: 10% H_2, 150 °C
  - Test duration: 1000 hours
- DUTs periodically taken out and measured on test bench
  - Bench test – transfer sweeps at room temperature
- Results
  - No appreciable key parameter shifts seen for GaN under 10% H_2 exposure
  - Significant shifts confirmed for the hydrogen-sensitive GaAs process as expected

Hydrogen Sensitivity Test Vp Plots

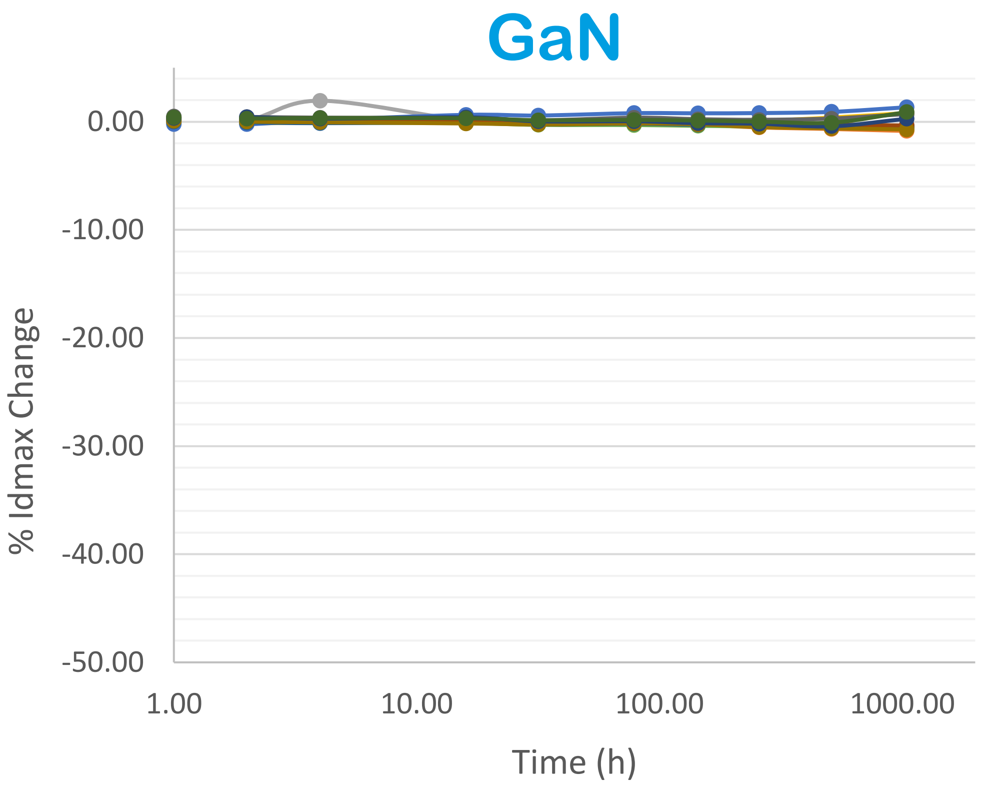
- **GaN shows 2-3 % pinch-off voltage shift under 1000 h 10% H_2 exposure in comparison to ~ 40 % shift for a hydrogen-sensitive GaAs process**

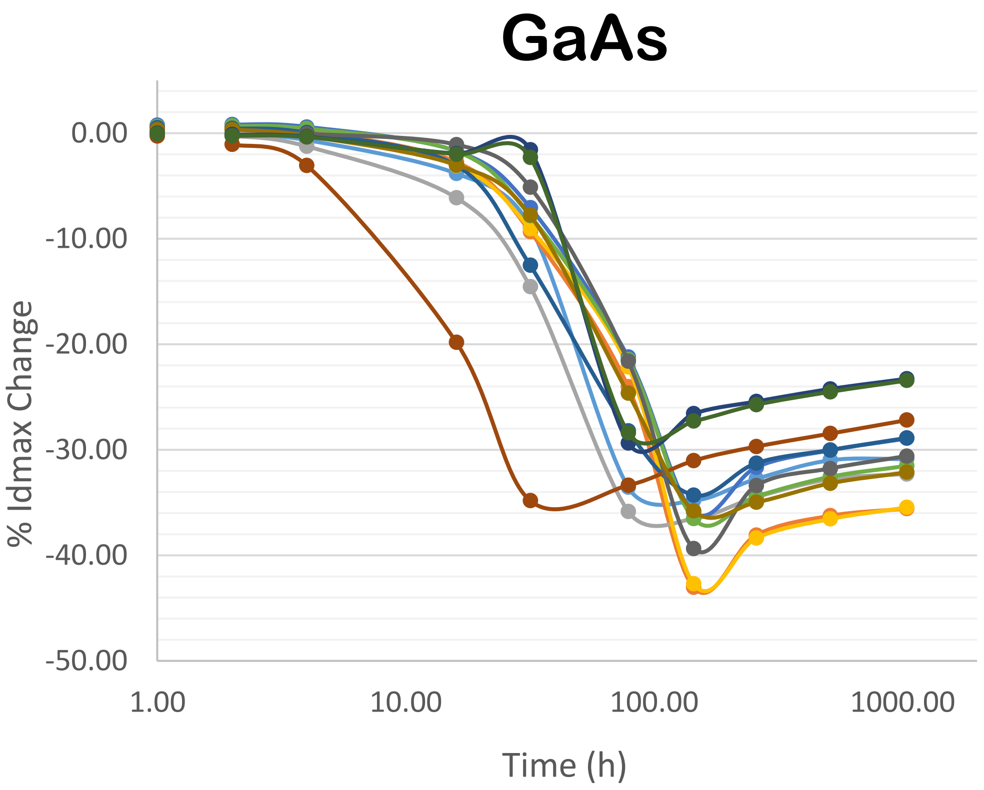




Hydrogen Sensitivity Test Idmax Plots

- GaN shows no Idmax shift under 1000 h 10% H_2 exposure in comparison to ~ 35 % Idmax drop for a hydrogen-sensitive GaAs process





Hydrogen Sensitivity Test Results Summary

GaN

Parameter	Min	Max
(% change from 0 to 1043 hours)		
Vp (Pinch Off)	0.74	6.8
Gm0 (Gm @ 0V Vg)	-4.91	3.73
Idss	-1.57	2.1
Idmax	-0.85	1.95

GaAs

Parameter	Min	Max
(% change from 0 to 1043 hours)		
Vp (Pinch Off)	22.22	49.01
Gm0 (Gm @ 0V Vg)	-20.37	5.54
Idss	-77.03	0.53
Idmax	-43.03	0.81

Radiation Hardness Tests

GaN Radiation Hardness Testing

Summary

- **Testing conducted by Qorvo lead customers/partners**

Activity	Description
Total Ionizing Dose	GaN25 has been subjected to Ionizing (Co-60) gamma radiation testing at doses ranging from 10 kRad to 500 kRad under bias conditions corresponding to normal amplifier operation. No significant changes were observed. Testing passed. 500 kRads is the equivalent of 11.9 years at GPS orbit.
Proton Radiation Testing	2 MeV proton radiation testing of 2x50 μm GaN15 test FETs conducted to evaluate displacement damage effects. The fluence schedule ranged from $1x10^{12}$ to $6x10^{14}$ H^+ /cm^2 and was designed to induce clear degradation in the DC FET characteristics. The onset of degradation occurred at ~$1x10^{14}$ H+/cm^2, approximately the equivalent of 1,000 years in low earth orbit.
Heavy Ion Testing (SEE)	Heavy ion radiation testing performed on GaN15 product at Vd = 22 V & 28 V with the following ions: Ar, Cu, Kr and Xe. The result showed this part does not latch under any pulsed exposure up to and including the heaviest ion of Xe (LET = 58.8 MeV/cm/g/cm^3). An enhanced RF power condition of Pin ≈ +17 dBm was also tested and no latch-up occurred. Temporary current changes occurred most significantly at the highest ion level of Xe pulse. Nevertheless, the post radiation testing showed no permanent performance change on any device.
Heavy Ion Destructive Single Event Effect (DSEE) Testing	Heavy ion DSEE testing performed on Qorvo GaN HPA using the K500 Heavy Ion Cyclotronat Texas A&M University. Samples of 2 parts were tested using 15 MeV Au ions up to a fluence of 1E7 ions/cm2. All parts were electrically tested before, during and after radiation by measuring Pout vs Pin characteristics at various frequencies in their operating band, up to the 6 dB compression point. Results show the part is immune to destructive Single Event Effects up to a Linear Energy Transfer (LET) of 82.8 MeV/mg/cm2 (Silicon).
Proton Dose Testing (Displacement damage):	Total Ionizing Dose (TID) testing was conducted on the Qorvo HPA at the Loma Linda Proton Facility using 200 MeV protons which generated 5.82E-11 krad(Si)/(proton/cm2). Flux achieved was 1E10 p/cm2/min (0.58 krad(Si)/min). The tested parts were each subjected to differing total ionizing doses and electrically tested before, during and after radiation by measuring the RF power in versus power out characteristics at various frequencies in their operating band, up to the 6 dB compression point. Two of the samples achieved a TID of 40 krad (Si) while 3 additional parts achieved a TID of 15 krad (Si).

Wafer & Die Level Tests

GaN Wafer- and Die-Level Testing and Screening

Qorvo GaN Routine Inspections & Testing Summary

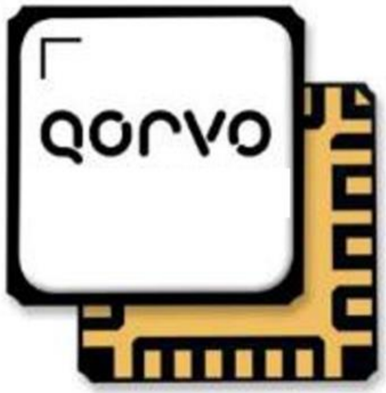
- **Addition tests establishing wafer quality and reliability + known-good die**

Test	Description	Purpose
In-line inspections & CD measurements	Optical and SEM inspection and CD measurements on each wafer at multiple steps throughout process	Ensure defect-free processing and proper critical dimensions
In-line electrical Process Control Monitor test	Measure key electrical parameters on special Process Control Monitor coupons on each wafer at three processing stages	Ensure nominal electrical performance of circuit building blocks—FETs, capacitors, resistors, interconnect
Die-level DC and RF Testing	Die-level electrical screen per product-based specifications	Ensure electrically functional & meeting performance specs die
Die-level Final Visual Inspection	Die-level visual screen per several different specs, including a tightened specification for use in space	Ensure visually good, defect-free die
Reliability Process Monitor	DC life tests performed on Reliability coupons from each lot	Confirm lot reliability meets 10^6 h median life spec at Tch = 200 °C
Back-metal and front-side dielectric adhesion test	Sample coupons (each wafer for space) undergo soldering-temperature exposure and are then inspected for delamination	Rule out trapped contamination/adhesion issues
Front metal pad and back-metal bond pull	Sample coupons (each wafer for space) undergo bond-pull testing	Ensure metal adhesion

Product Level Qualification Tests

GaN Product-Based Qualification Tests

- **Additional environmental and mechanical tests have been conducted at the product level**
  - HAST / THB, Temperature Cycling, High / Low Temperature Storage, Vibration, Thermal Shock, Solderability, Mechanical Shock
- **Additional electrical robustness tests have been conducted at the product level**
  - HTOL
  - ESD (HBM, CDM)



Summary

- In this presentation we summarized results of testing conducted at Qorvo, pertinent to the qualification of GaN for space applications
- Reliability data collected over a 20-year span was reviewed, covering FETs, passives, and interconnect, as well as circuit RF reliability and environmental testing
- Details were provided about each test and the resulting predicted reliability
- Qorvo GaN has been successfully flown in space

Thank You