

Standards of PEM Qual and Technical Requirements Review

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Celebrating Over 35 Years of Providing High Quality Semiconductor Services



What are PEMs?

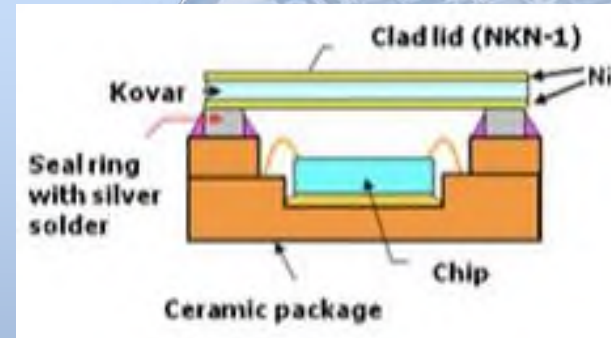
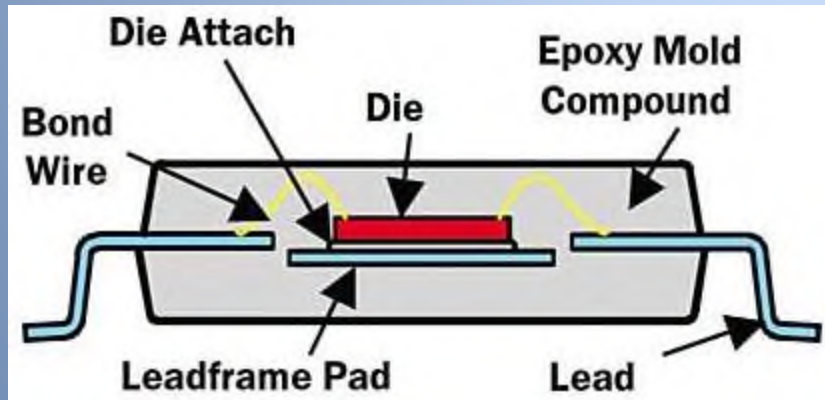
- **PEM stands for Plastic Encapsulated Microcircuits**

For this presentations, PEM includes

- **Microcircuits and Hybrids assembled in plastic package**
- **Discretes (Diodes and Transistors) assembled in plastic package**
 - **Plastic encapsulated Transistors and Diodes are typically referenced as PEDs.**
- **General concept of PEM applies to Flip Chip but not entirely applicable**
- **EP (Extended Plastic)**

Pictorial View of Typical PEMs

- A PEM device typically uses organic packaging material, either injection or transfer molded or coated for environmental protection.
 - Plastic encapsulated IC's or Microcircuits are commonly referred to as, PEMs.
 - Plastic encapsulated Transistors and Diodes are typically referenced as PETs and PEDs, respectively.



Reasons to use PEMs

- **Wide spread availability**
- **Higher volume/more cost effective production**
- **Shorter leadtimes – many products off-the-shelf**
- **Generally lower cost**
- **Greater product variety**
- **Mechanically more rugged**
- **Lighter weight - available in smaller/thinner packages**
- **All of the above items help reduce end system costs and accelerates time to market.**

Do PEMs Help Obsolescence Issue

- **Yes – because of need for inexpensive consumer electronics, inexpensive plastic parts are by far the dominant package type – which means semiconductor manufacturers are more likely to support these technologies for a longer period of time.**
- **It does not meet the EOL support required by most Aerospace and Defense contractors, but all other things being equal, plastic parts will likely be available longer than hermetic.**

Potential Concerns with PEMs

- **PEMs have predominately been designed for commercial and industrial applications – not Aerospace and Defense (A&D).**
- **Higher military temperature ranges are not generally available (except EP)**
- **Typical PEMs are COTs and screening by OCM are not always as stringent as A&D end applications require.**
- **Qualifications are typically at the inception of product release and is not lot-by-lot.**
- **Qualifications are typically not sequential as used by A&D.**
- **Reliability of plastic packages could vary dramatically from supplier to supplier.**
- **Copper bond wire PEMS are known to have Reliability concerns if not properly manufactured**

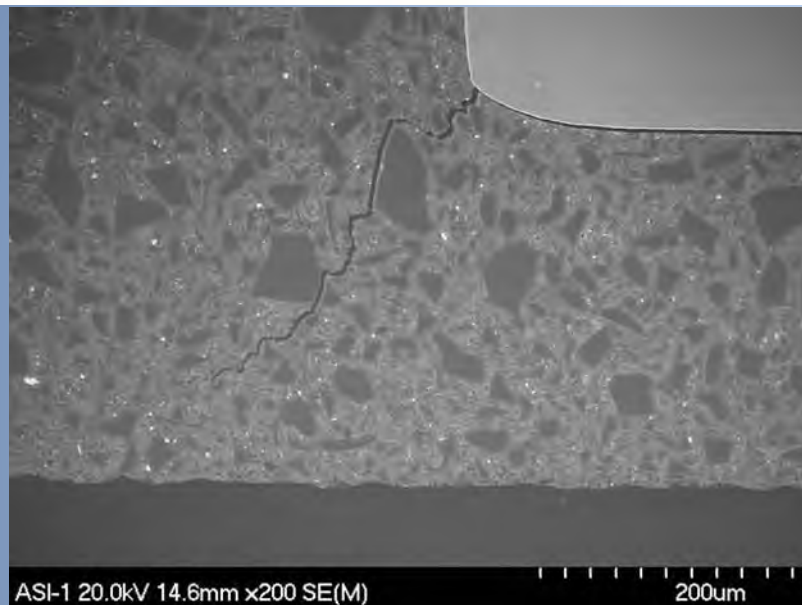
Typical PEM Qual Failure Modes

- 1. Pop Corning of Plastic Package**
- 2. Delamination**
- 3. Die Attach Voids**
- 4. CTE Mis-match Between Molding Compound and Base Material**
 - a. Cracked Package**
 - b. Wire breaks**
 - c. Cracked Die**
- 5. Corrosion**
- 6. Wire Lift**
- 7. Contamination**
- 8. Moisture Ingression / Current Leakage**
- 9. Cracked Passivation**

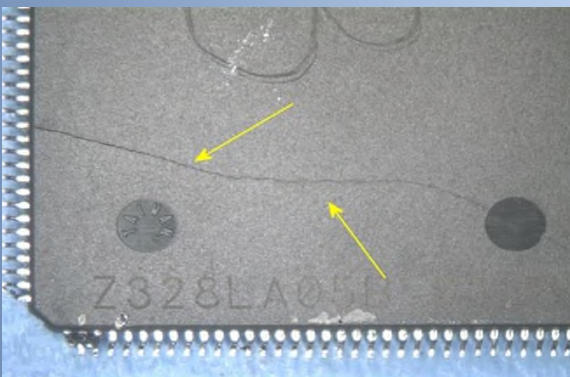
Additional Concerns with Copper Bond Wire PEM

- Easily oxides in air – typically requires N₂ or special flow of forming gas during mfg.
- Cu is harder – bonding process difficult - Requires optimal bonding process otherwise impacts yield and reliability
- Typically Halogen free special molding compound required for Cu wire products
 - Biased humidity failures - corrosion
 - Green mold compound with a preferably low Cl content and high pH
 - Lower pH (more acidic) and the higher Cl content are, the poorer the reliability.
- Quality / Reliability concerns:
 - Bond pad aluminum deformation (splash)
 - Cratering / Cracks under the bond
 - Cu ball bond interface corrosion
 - IMC (intermetallic dielectric) cracking
 - Peeling of the bond pad interface – bond lifting is a major reliability concern

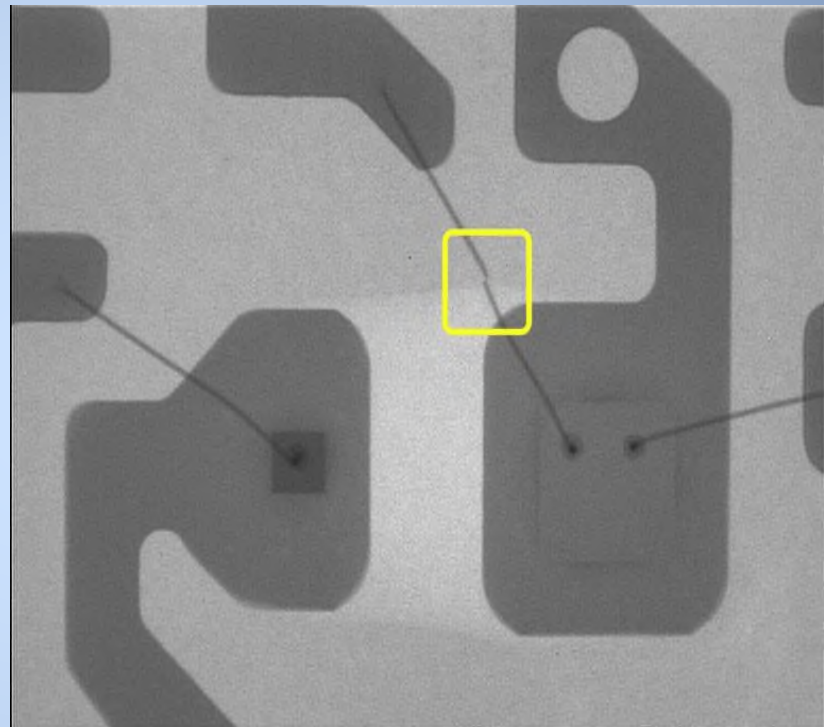
Images of Typical PEM Qual Failures



Pop-corning

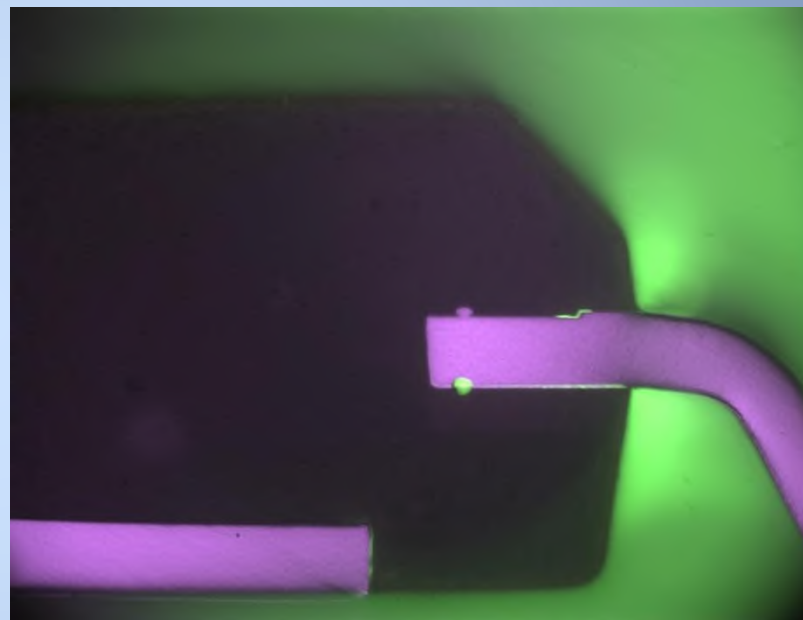
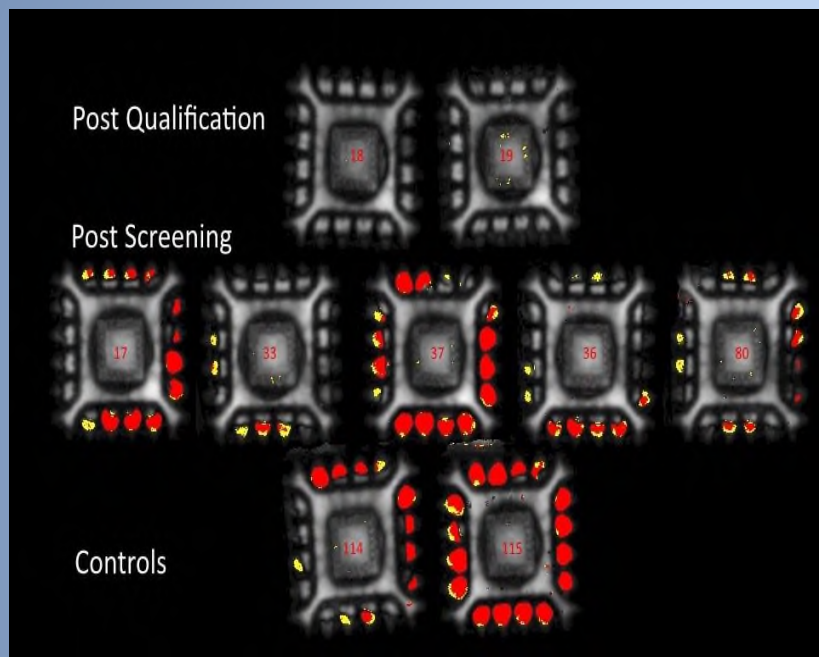


Package Cracks

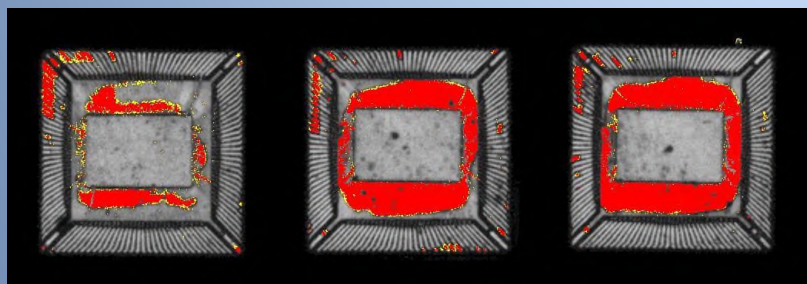


- Broken wire bond due to CTE mismatch
- Mismatch between molding compound and optical coupling material created shear forces resulting in a broken bond wire

Images of Typical PEM Qual Failures



Delamination (Dye Penetrant Test)



Delamination (SAM Images)

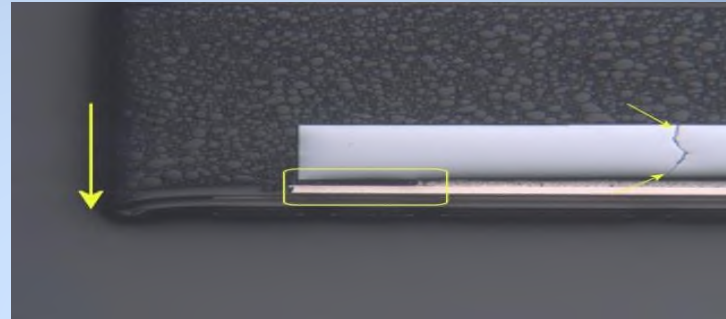
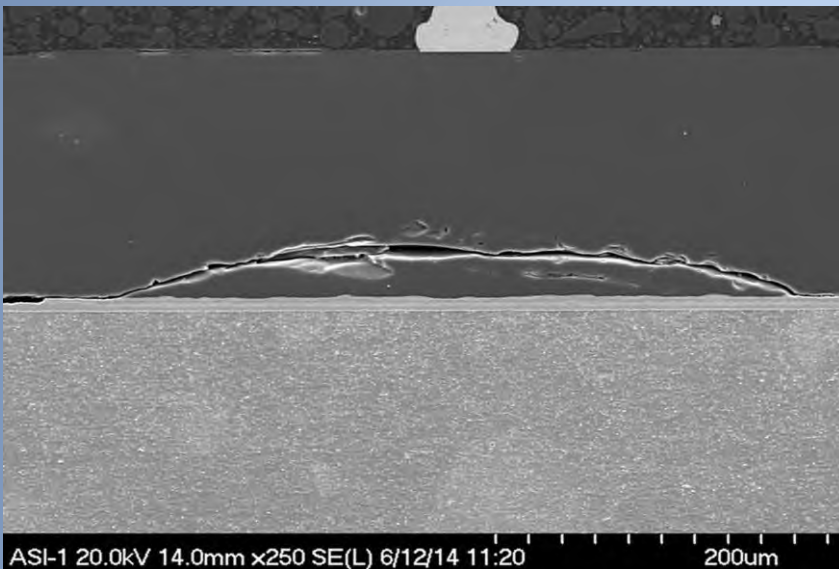
Dye Penetrant Test for PEMs

This technique is used to verify suspect delamination typically seen during Acoustic Microscopy. This technique utilizes a low viscosity liquid penetrant which is mixed with a fluorescent powder and an accelerator. After the device is subjected to dye penetrant it is potted and cross sectioned for inspection under a mercury lamp.





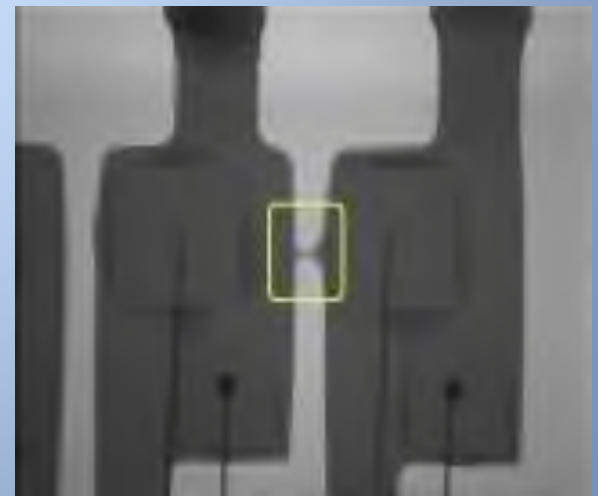
Images of Typical PEM Qual Failures



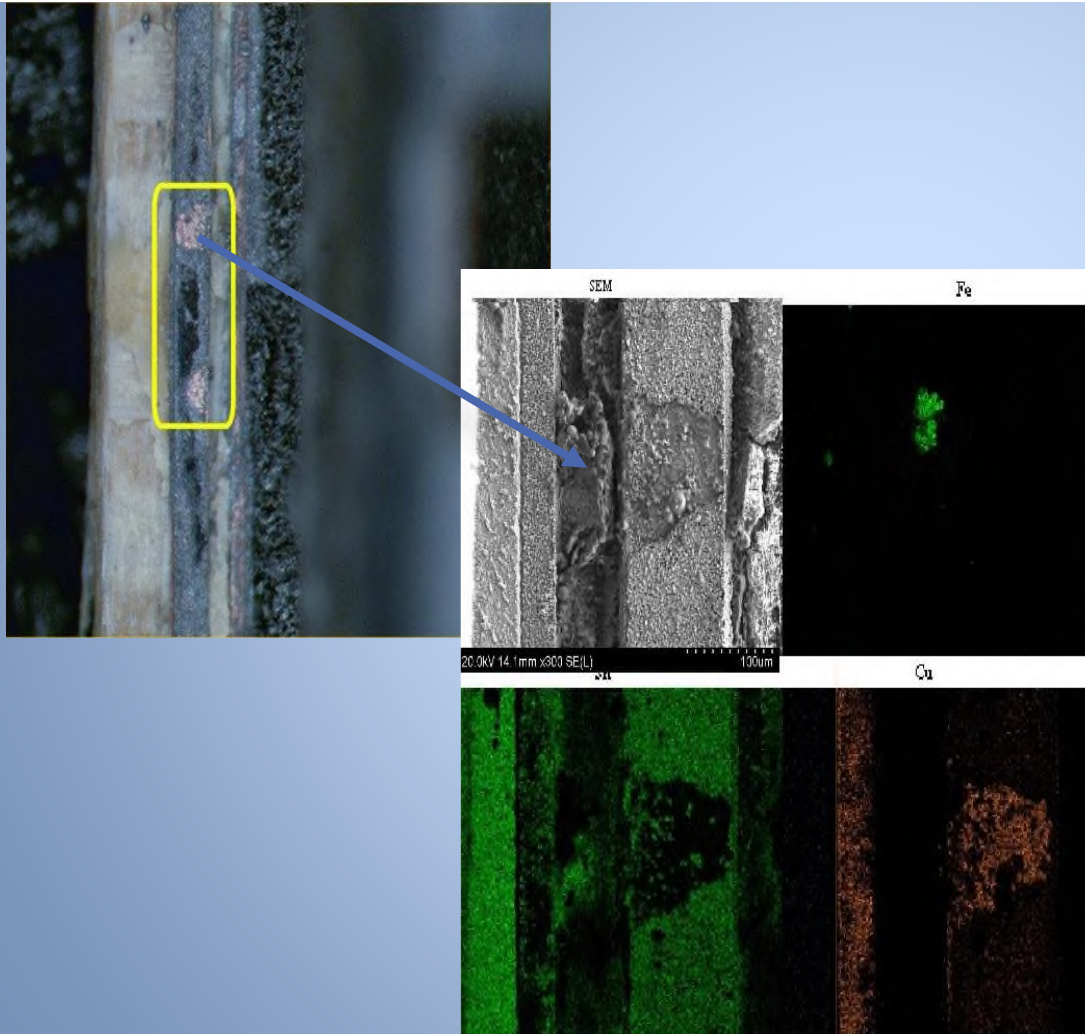
Cross section – PWB damage; void underneath the die and die cracking

Broken die due to CTE mismatch
AuSi Eutectic die attach used in a plastic encapsulated microcircuit. CTE mismatch between the molding compound and die attach resulted in die cracking and open backside contact

X-Ray – Shorts



Images of Typical PEM Qual Failures



Leakage Failures

- **Moisture Ingress with current leakages within hybrid device. SEM and elemental dot mapping indicates copper:iron:tin dendritic growth**

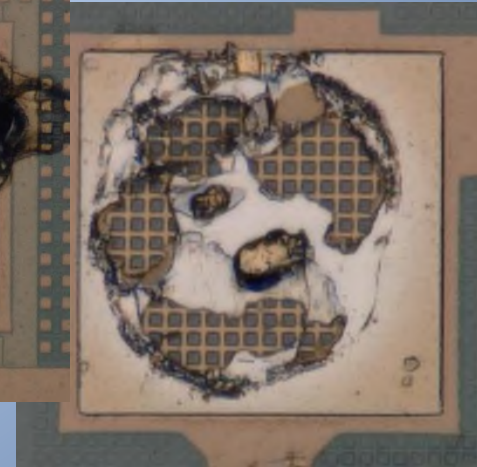
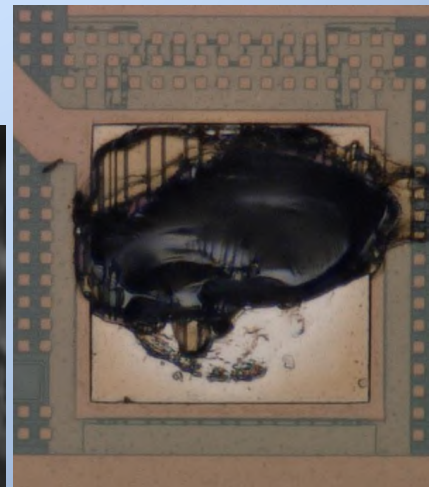
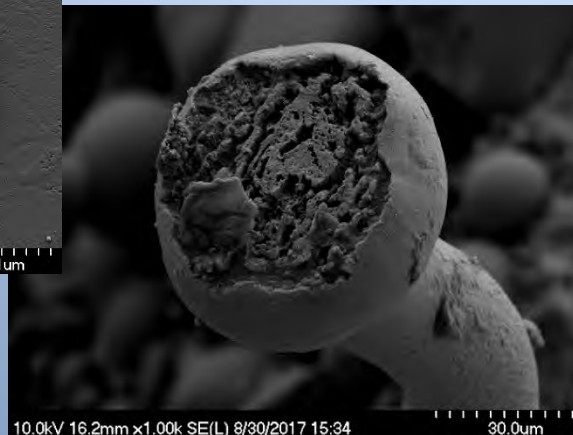


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Wire Bond Pull and Wire Bond Shear Failures

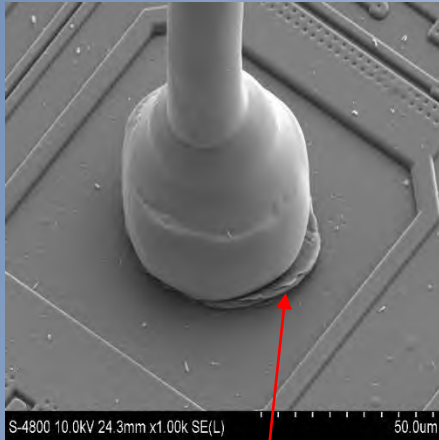
Wire bonds provide electrical connection between the silicon chip and the external leads of the device. The wire is typically made of gold (Au), aluminum (Al) and copper (Cu). In some cases, silver (Ag) wire is used.

- The purpose of Wire Pull testing is to measure wirebond strengths, evaluate bond strength distributions, and to determine compliance with specified bond strength requirements.
 - *MIL-STD-750 TM 2037 test condition C and MIL-STD-883 TM 2011 test condition D*
- Wire Bond Shear testing provides a means for determining the strength and integrity of the metallurgical bond of a ball bond to a die or package bonding surface.

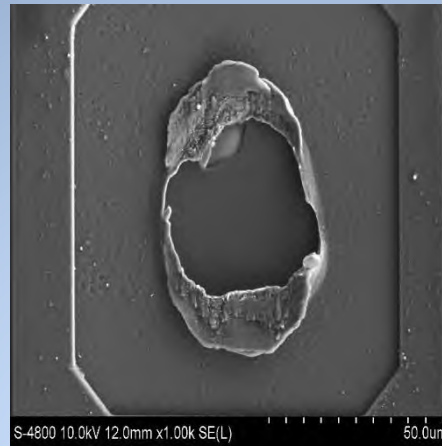




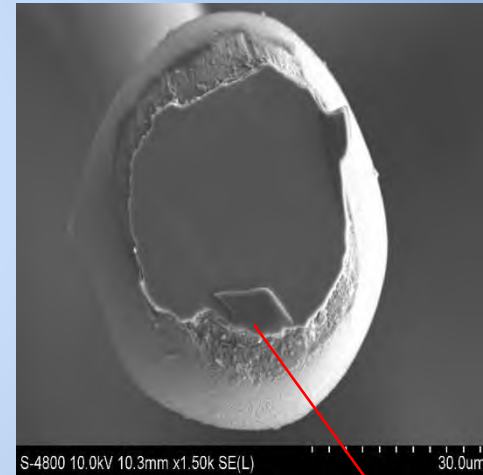
Cu Wire - Aluminum Splash / Cratering / Residual Silicon



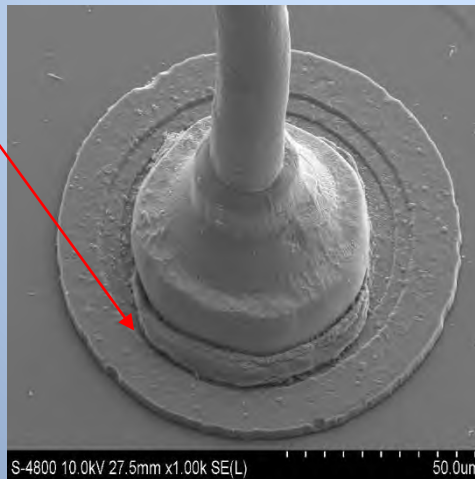
Aluminum Splash



Cratering



Residual Silicon





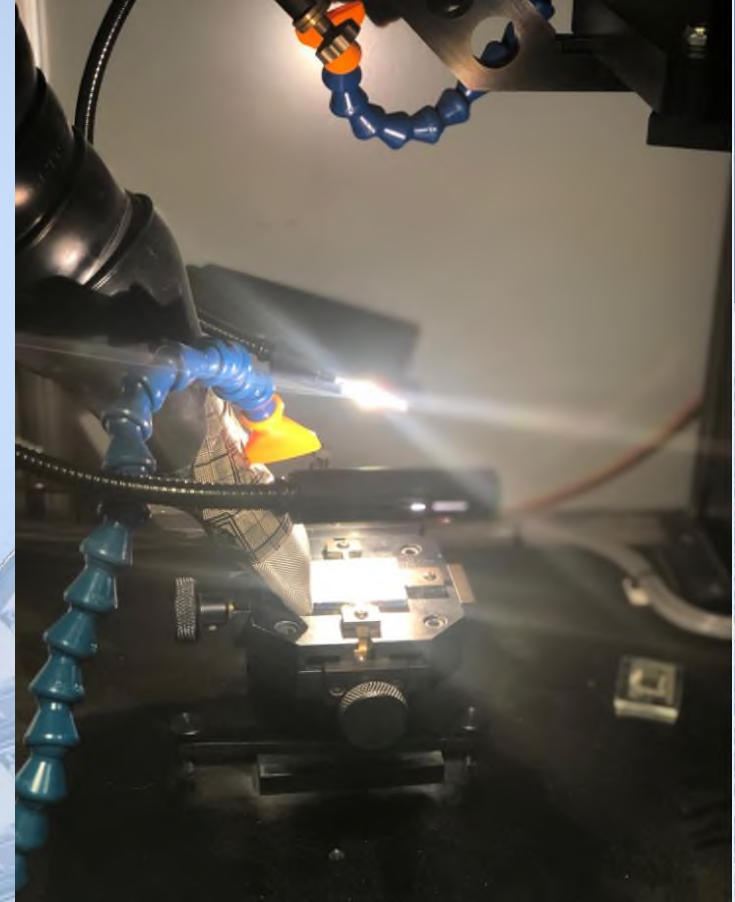
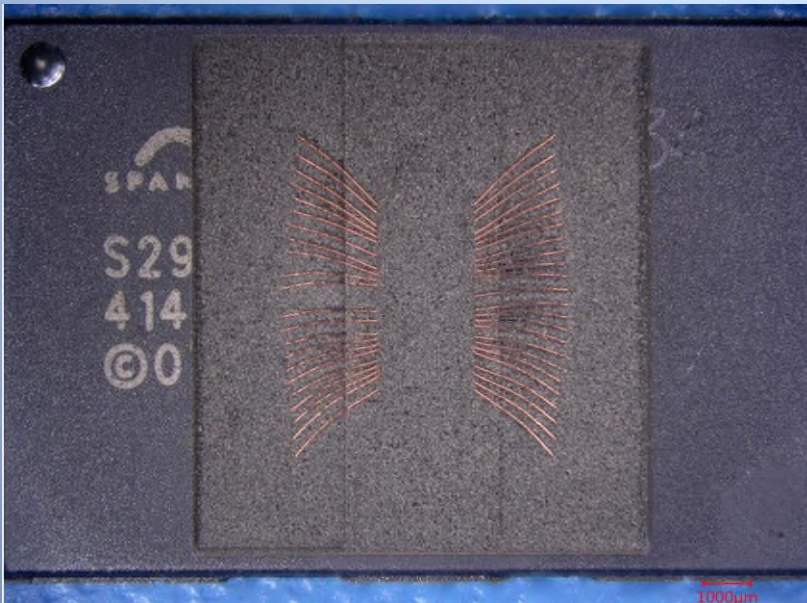


Laser Ablation Decapsulation

Laser ablation is the process of removing material from a solid surface by irradiating it with a laser beam.

This process is typically performed prior to chemical de-encapsulation as it helps to reduce the amount of chemical exposure.

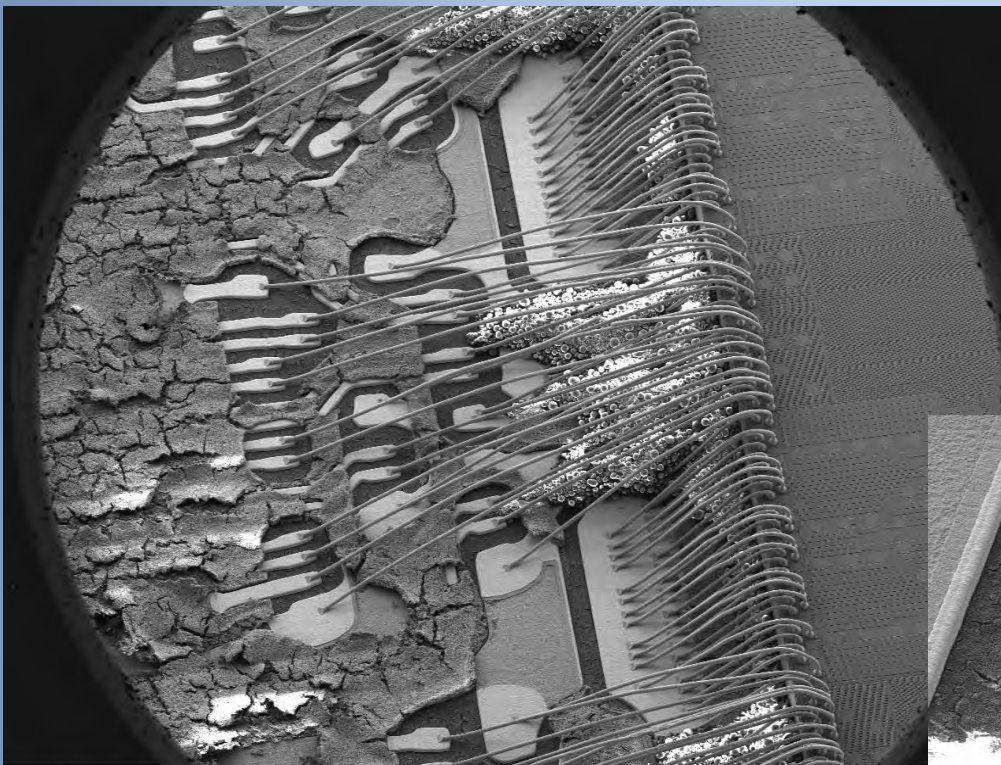
Laser ablation along with chemical application allows us to de-encapsulate Copper bonded devices with very minimal damage to the wire.





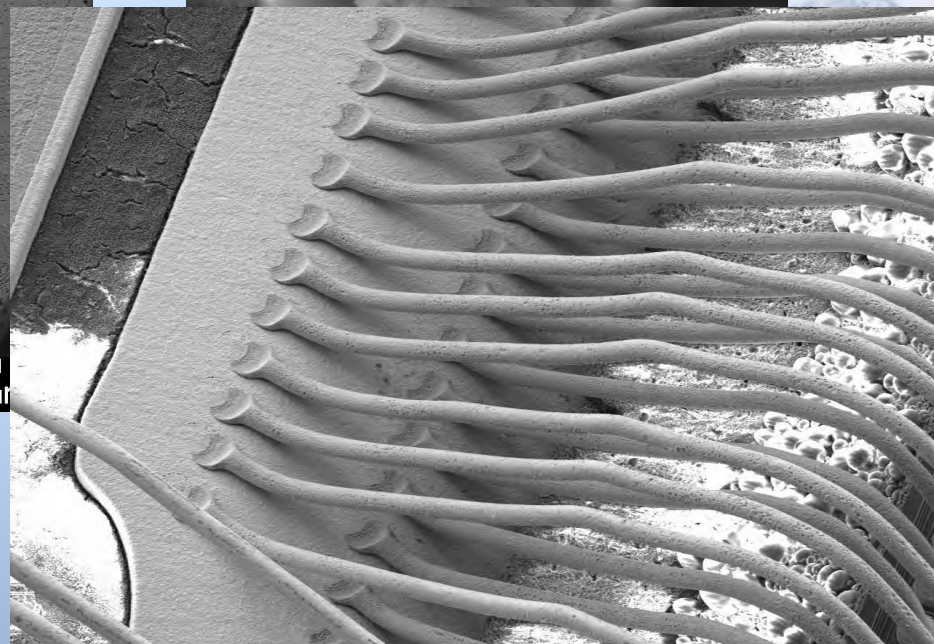
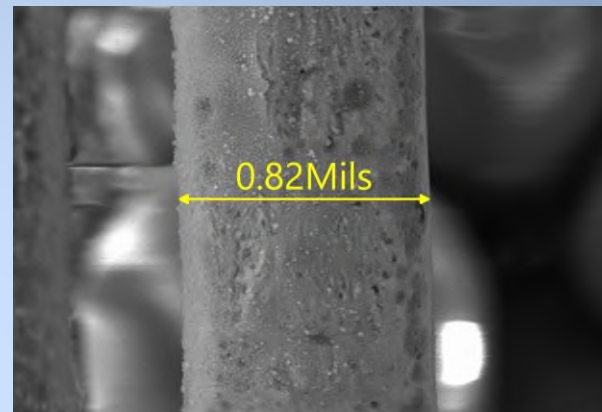
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Laser Ablation Decapsulation



Integra-II 10.0kV 15.2mm x25 SE(M) 5/11/2020 15:35

1.20mm



Integra-II 10.0kV 15.2mm x150 SE(M) 5/11/2020 15:32

200um

SEM images of a copper bonded device post decapsulation. Stitch bonds are free from resin.



EP (Extended Plastics)

- **Offered by Few OCMs Under Slightly Different Names (TI, Analog Devices etc)**
- **Main Features**
 - Compliments COTS or in some case military grade ceramic devices
 - Stand-alone data sheets
 - Beyond commercial temperature range – typically -55C to 125C depending upon the device
 - Typically comes from one assembly/test/fabrication site
- **What Makes The Part Enhanced Plastic**
 - Reliability tests at maximum recommended conditions
 - Electrical testing is done at extended temperature
 - May use special molding compound for enhanced package performance (3 temp electrical testing and enhanced moisture reliability)
- **Moisture Level**
 - Could be any of the levels depending upon the data



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PEM Qual Considerations

Know Your PEM Qual Standards

- **SAE Standards**
 - AS6294/1 for Space PEMs and AS9294/2 for Military PEMs
 - AS6294/3 for Space PEDs and AS6294/4 for Military PEDs
- **NASA Standards**
 - PEM-INST-001 (Goddard) (Under Revision at NASA)
 - MSFC-STD-3012 (Marshall Space Flight Center)
- **Mil Std**
 - MIL-PRF-38535: General Specification for Integrated Circuits (Microcircuits)
 - Class N (Screening and Qual tables are not separated)
 - Class P (Under development – Based on AS6294/1)
 - Class Y (Non- Hermetic Flip Chip – Typically not a PEM but is non-hermetic)
 - MIL-PRF-38534: General Specification for Hybrids
- **AEC (Automotive)**
 - AEC- Q100 – Microcircuits Quals
 - AEC - Q101: Discrete Semiconductor Quals
 - AEC-Q006: Copper Bond Wire Quals



We Know Your PEM Qual Standards

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- External Visual and Serialization: Qty=32
- Baseline SAM: Qty: 32
- Pre-Conditioning: Qty=32
 - Moisture Soak per appropriate MSL Level
 - Reflow at 235C
- Electrical Testing at 25C, min and max operating temp; Qty=32
- Sub-Group 1 Qual: Qty=22
 - 125C Life Test for 1000 or 1500 hours
 - Electrical Testing at 25C, min and max operating temp
 - Temp Cycle; 200 or 500 cycles
 - Electrical Testing at 25C, min and max operating temp
 - SAM; 22 units
 - DPA : 5 units
- Subgroup 2 Qual: Qty=10
 - Biased or Unbiased HAST; 96 hours at 130C/85%RH
 - Electrical Testing at 25C, min and max operating temp

Key Considerations of a PEM Qual Plan

- Perform a detailed construction analysis or DPA on package before the qual. You will learn a lot of package weakness data before start of qual.
- Understand available OCM data – Does the product already show delamination even before the qual has started? Available Qual data from OCM? Comprehensiveness of OCM electrical testing?
- Canned qual plans are a good start but prepare a device specific qual plan based on:
 - Application
 - Package used
 - Available data from OCM
 - Upscreening as part of qual plan
 - Types of tests to be included in the qual plan and why
 - Pass / fail criteria for individual tests
 - Pass / fail criteria for the qual

Key Considerations of a PEM Qual Plan

- **Over qualifying adds substantial cost while eliminating devices that might otherwise be reliable enough and lower priced.**
- **Even worse, under qualifying may lead to inadequate device reliability and system field failures.**
- **Electrical Testing Consideration**
 - **Understand how comprehensive electrical test coverage is your test supplier**
 - **Insufficient electrical test coverage will allow failing devices to be counted as passing and could lead to poor system and field reliability.**
 - **If package qualification, DC, some key AC (one or two) and functional test should be enough – select parameters that are sensitive to package related issues.**
- **Three temperature testing is recommended**
- **Screening before qual should take care of infant mortality failures**

Key Considerations of a PEM Qual Plan

- **Certain packages have inherent weakness to moisture ingress**
 - **Very thin packages**
 - **Small outline devices**
 - **Packages with back-side paddles**
 - **Flip chip packages with vents**
- **What is die to lead frame paddle or substrate ratio?**
Impacts SAM images
- **What is the thermal characteristic of the device (high power device)?**
- **Does the product use copper bond wires?**

Key Considerations of a PEM Qual Plan

- **Dynamic life test is recommended. Typically, PEMs are not subjected to burn-in at OCMs for commercial or industrial grade product. Life Test is typically considered a die level test. However; some package anomalies can be found with life test. Check OCM's data on the plastic package being subjected to PEM qual.**
- **Pre-conditioning is simulation for real life storage and board assembly conditions.**
- **Pre-conditioning typically impacts humidity tests much more than life test. Many customers forego pre-conditioning for life test due to extremely low failure rate.**

PEM Qual: Optimal Humidity Testing?

- **Always do pre-conditioning before any of the humidity testing.**
- **Recommend to do SAM pre and post preconditioning to see effect of stress due to pre-conditioning**
- **Customize pre-conditioning to the appropriate MSL level of the package**
- **Typical humidity tests post pre-conditioning:**
 - **Unbiased HAST - 96 hours, +130 °C, 85% RH**
 - **Biased HAST - 96 hours, +130 °C, 85% RH- Preferred – Promotes galvanic reaction**
 - **TH – unbiased - 1000 hours – 85C, 85% RH**
- **For biased testing; calculate power dissipation. If more than 200mW; need to use on/off power cycle to avoid drying of die surface per JEDEC standard for biased HAST / THB**

PEM Qual: How We Handle Delamination?

- **Most common interfaces looked at during SAM:**
 - Die surface, die attach, die paddle, and leads / lead frame
- **Delamination occurs due to:**
 - Stress-induced passivation damage over the die surface
 - Wire-bond degradation due to shear displacement
 - Accelerated metal corrosion
 - Die-attach adhesion
 - Intermittent electricals at high temperature
 - Popcorn cracking
 - Die cracking
 - Device latch-up
- **Typical SAM steps**
 - Before screening
 - After screening (same as pre-qual or before pre-conditioning)
 - Post pre-conditioning
 - Post stress (life test or temperature cycle or humidity test)

PEM Qual: Rejection Criteria from J-STD-020

6.2.1 Delamination The following delamination changes are measured from pre-moisture soak to post reflow. A delamination change is the change between pre- and post-reflow. The percent (%) delamination change is calculated in relation to the total area being evaluated.

6.2.1.1 Metal Lead frame Packages:

- a. No delamination on the active side of the die.
- b. No delamination change >10% on any wire bonding surface of the die paddle (downbond area) or the lead frame of LOC (Lead On Chip) devices.
- c. No delamination change >10% along any polymeric film bridging any metallic features that is designed to be isolated (verifiable by through transmission acoustic microscopy).
- d. No delamination/cracking change >10% through the die attach region in thermally enhanced packages or devices that require electrical contact to the backside of the die.
- e. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes: lead fingers, tie bars, heat spreader alignment features, heat slugs, etc.

6.2.1.2 Substrate Based Packages (e.g. BGA, LGA etc.):

- a. No delamination on the active side of the die.
- b. No delamination change >10% on any wire bonding surface of the laminate.
- c. No delamination change >10% along the polymer potting or molding compound/laminate interface for cavity and overmolded packages.
- d. No delamination change >10% along the solder mask/laminate resin interface.
- e. No delamination change >10% within the laminate.
- f. No delamination/cracking change >10% through the die attach region.
- g. No delamination/cracking between underfill resin and chip or underfill resin and substrate/solder mask.
- h. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, laminate, laminate metallization, PTH, heat slugs, etc.

Figure 3-1. Rejection criteria from JEDEC-J-STD-020D

PEM Qual: Is Delamination Rejectable?

Not Always!

6.2 Criteria Requiring Further Evaluation Delamination is not necessarily a cause for rejection. To evaluate the impact of delamination on device reliability, the semiconductor manufacturer may either meet the delamination requirements shown in 6.2.1 or perform reliability assessment using JESD22-A113 and JESD-47 or the semiconductor manufacturer's in-house procedures. The reliability assessment may consist of stress testing, historical generic data analysis, etc. Annex A shows the logic flow diagram for the implementation of these criteria.

If the SMD Packages pass electrical tests and there is delamination on the back side of the die paddle, heat spreader, or die back side (lead on chip only), but there is no evidence of cracking, or other delamination, and they still meet specified dimensional criteria, the SMD Packages are considered to pass that level of moisture sensitivity.

From JEDEC-J-STD-020D

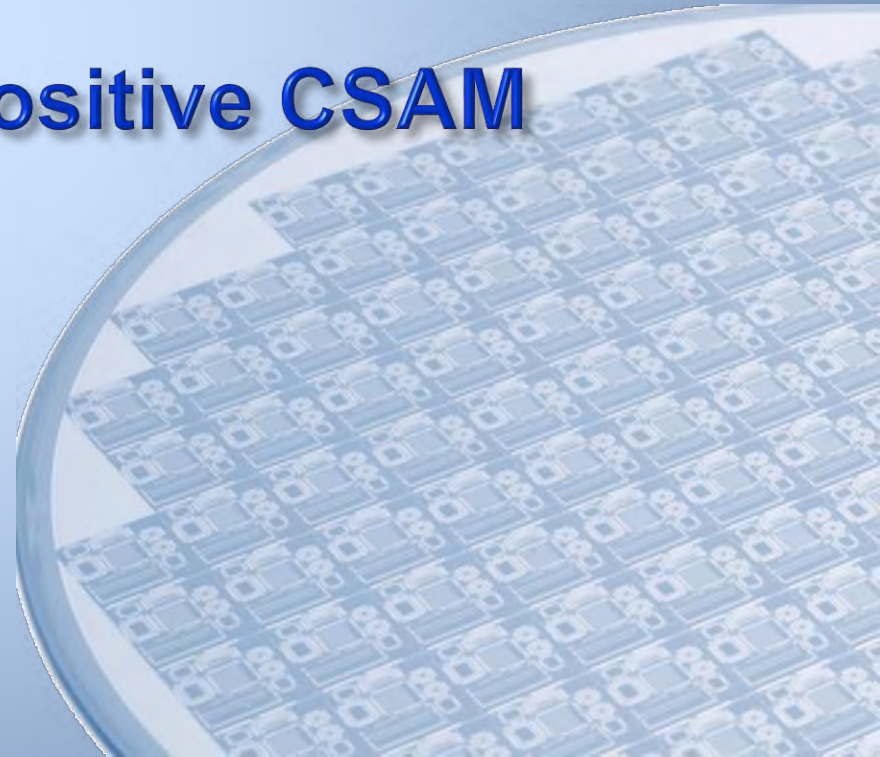
PEM Qual: What To Do If There Are Failures?

- Understand the failure mode
- Not all failures are related to PEM qual
 - Ex: A single bit failure is most likely die related; not due to PEM
- Even delamination is not necessarily a failure if the Reliability tests passed
- Trust electrical test post reliability test results
- Do additional testing to validate suspected failure mode



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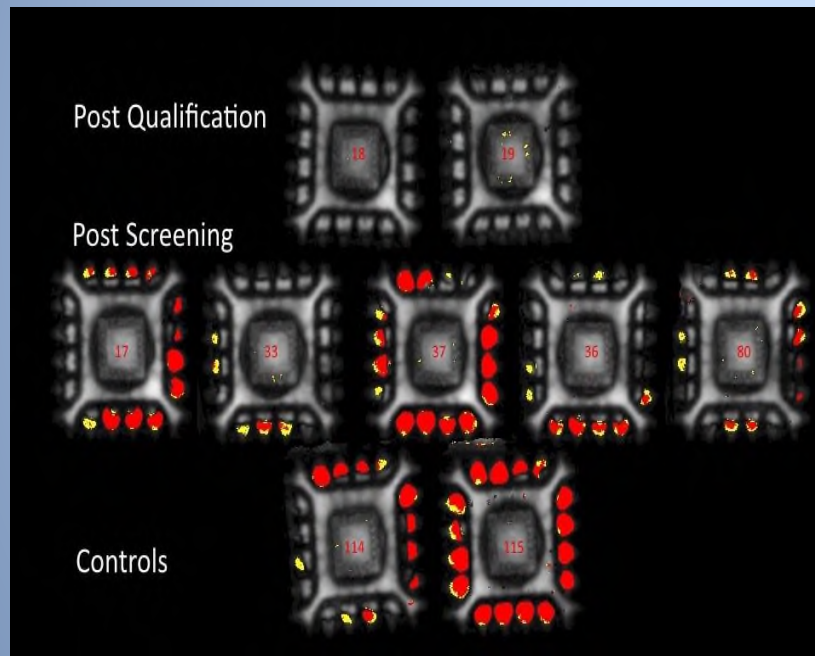
A Case of False Positive CSAM



Background

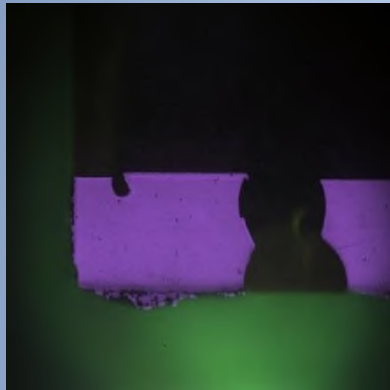
- **Device:** NB6N14SMNG
- **Package:** 16 QFN
- **Problem**
 - Post Screening samples subjected to Qualification per NASA PEM-INST-001
 - Pre-Qualification SAM revealed delamination on 33/36 devices in the area of wire bonds.
 - Post- Qualification SAM on 22 parts had no delamination or electrical test failures.
 - 2 Control samples did not change from pre-qualification to post-qualification indicating that the SAM setup was unchanged.
- **Qualification Tests:**
 - ✓ Pre- Conditioning - JESD22 Method A113 68 hours, +85 °C, 60% RH).
 - ✓ 1000 hours Life Test at 105C
 - ✓ -55 to 125C Temp Cycle – 200 Cycles
- **SAM Images:** Taken per PEM-INST-001; section 5.3.3

CSAM Comparison



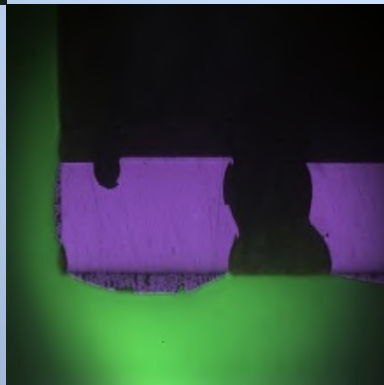
- **Pre-Qual / Post-Screening Images:** Delamination indications on the leads
- **Post Qual Images:** No signs of delamination
- **Control units Images:** Delamination

Dye Penetrant Test



Dye Penetrant
Pre
Qualification

Dye Penetrant Post
Qualification



No Dye penetrated to the internal package interfaces on either the post screening or post qualification samples.

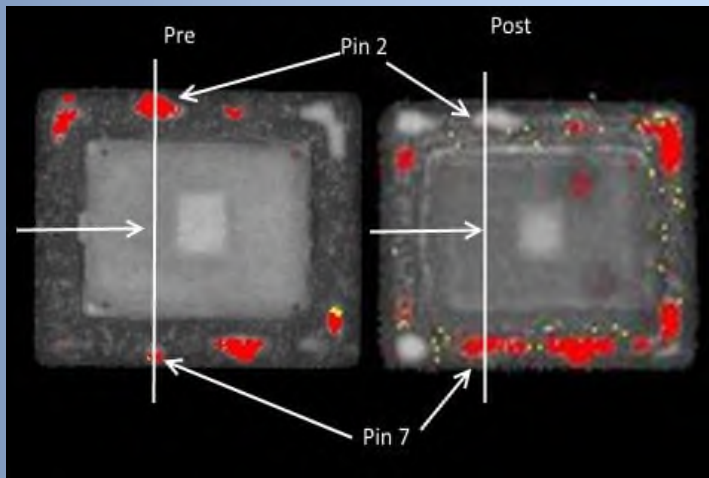
No path for moisture ingress was observed in post screening or post qualification samples.



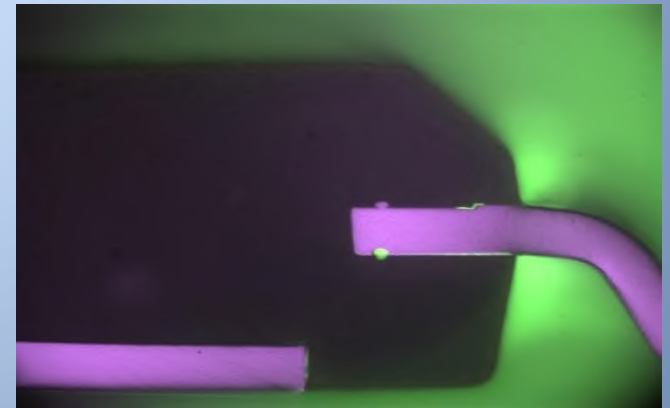
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Example of Water Ingress Masking Delamination in CSAM

Pin 7 (Die Penetrant shows delamination)



Pin 2 (Die Penetrant shows delamination)



Integra PEM Qual Data Overview

Total Number of Parts Processed:	111,183
Total Number of Lots:	791
Total Number of Passing Lots:	496
Passing Lot Percentage:	63%
Total Number of Failing Lots:	295
Failing Lot Percentage:	37%
Total Customer Part Numbers:	455
Total Manufacturer Part Numbers:	410
Total Number of Manufacturers:	73
Total Number of Customers:	42
Unique Pin/Package Combinations:	165

Notes:

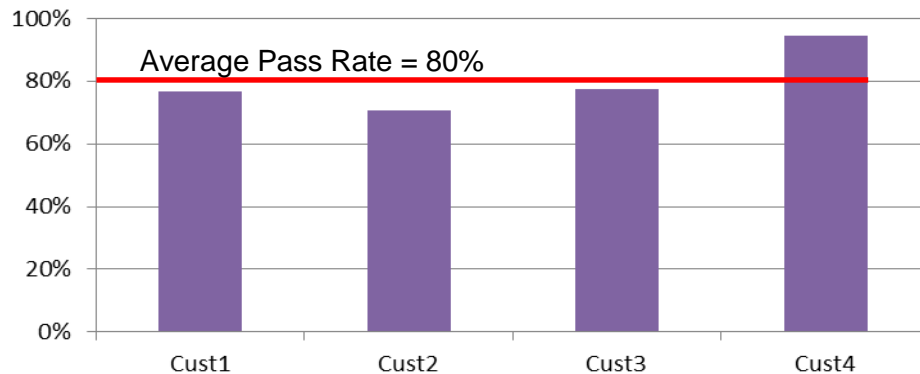
- No qualifications conducted by semiconductor manufacturers are included.
- Plastic packaged semiconductor devices only - no passives.
- Predominant test temperatures are -40, 25 85 and -55, 25 125.
- Testing temperature order is usually room, cold, hot.
- Once a qual fails it is usually stopped.
- Failures are for electric test only (no mechanical failures).
- Vast majority of testing performed to manufacturers datasheet limits.
- Virtually all electrical test programs written by Integra Technologies.



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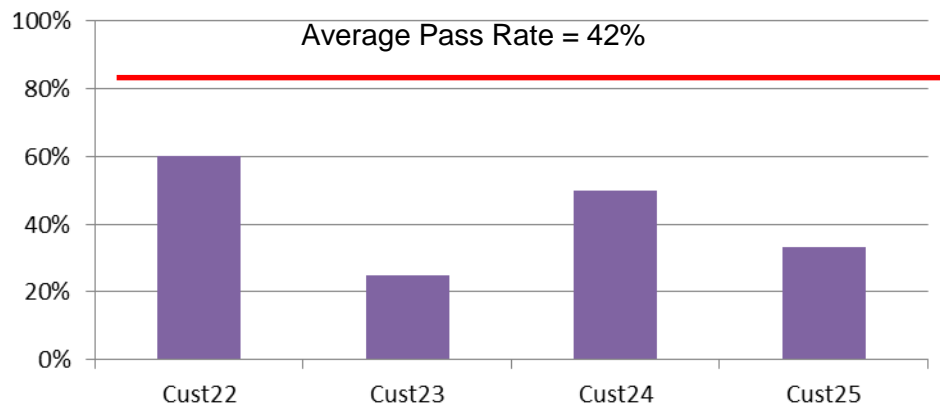
Overall Customer PEM Qual Success Rate

**% Passing Lots for Customers Doing
Frequent PEM Quals**



Customers who are more experienced with PEM Quals tend to have better success. These 4 customers averaged over 100 PEM Qual lots each over the 15 year analysis period.

**% Passing Lots for Customers Doing
Infrequent PEM Quals**



The average pass rate over the entire population is 63%.

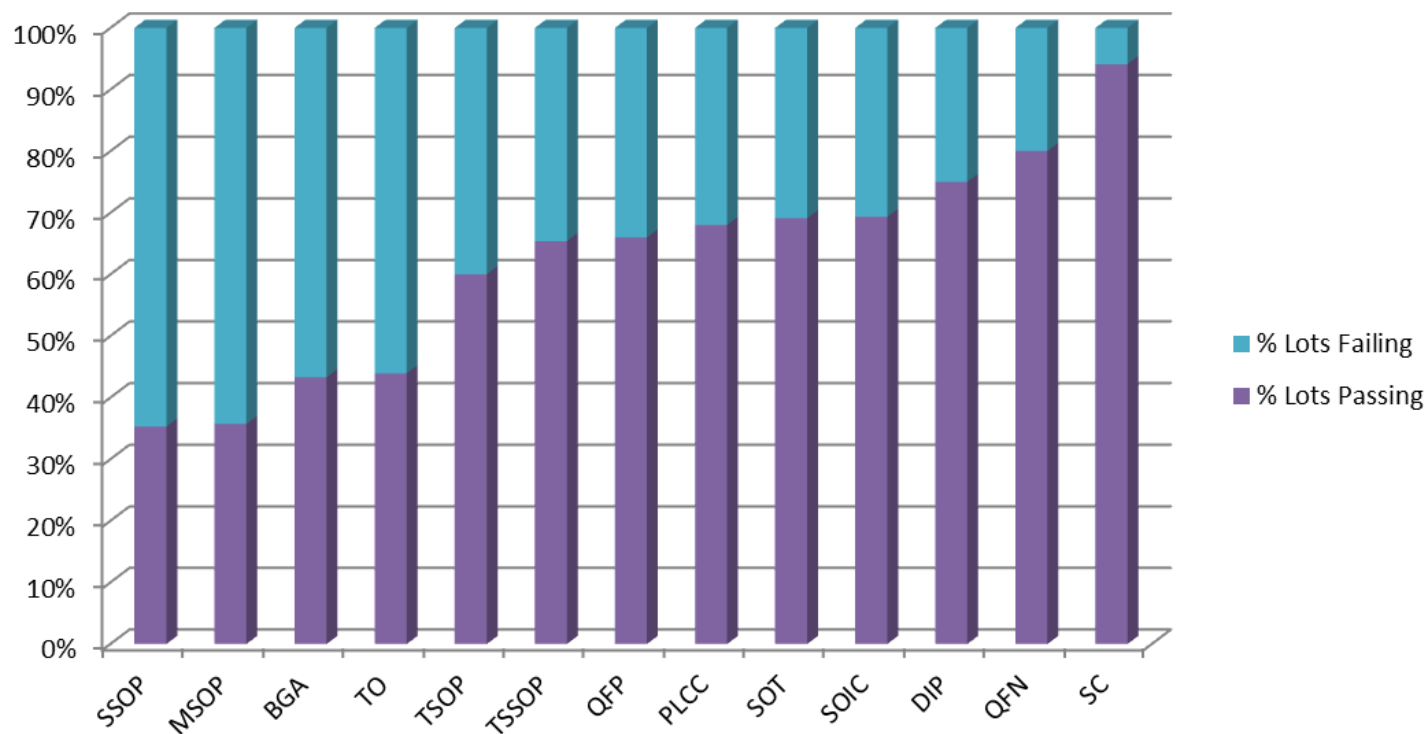
Customers who are less experienced with PEM Quals tend to have less success. These 4 customers averaged ~4 PEM Qual lots each over the 15 year analysis period.



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Overall PEM Qual Success Rate by Package

PEM Qual Pass/Fail Rate by Package



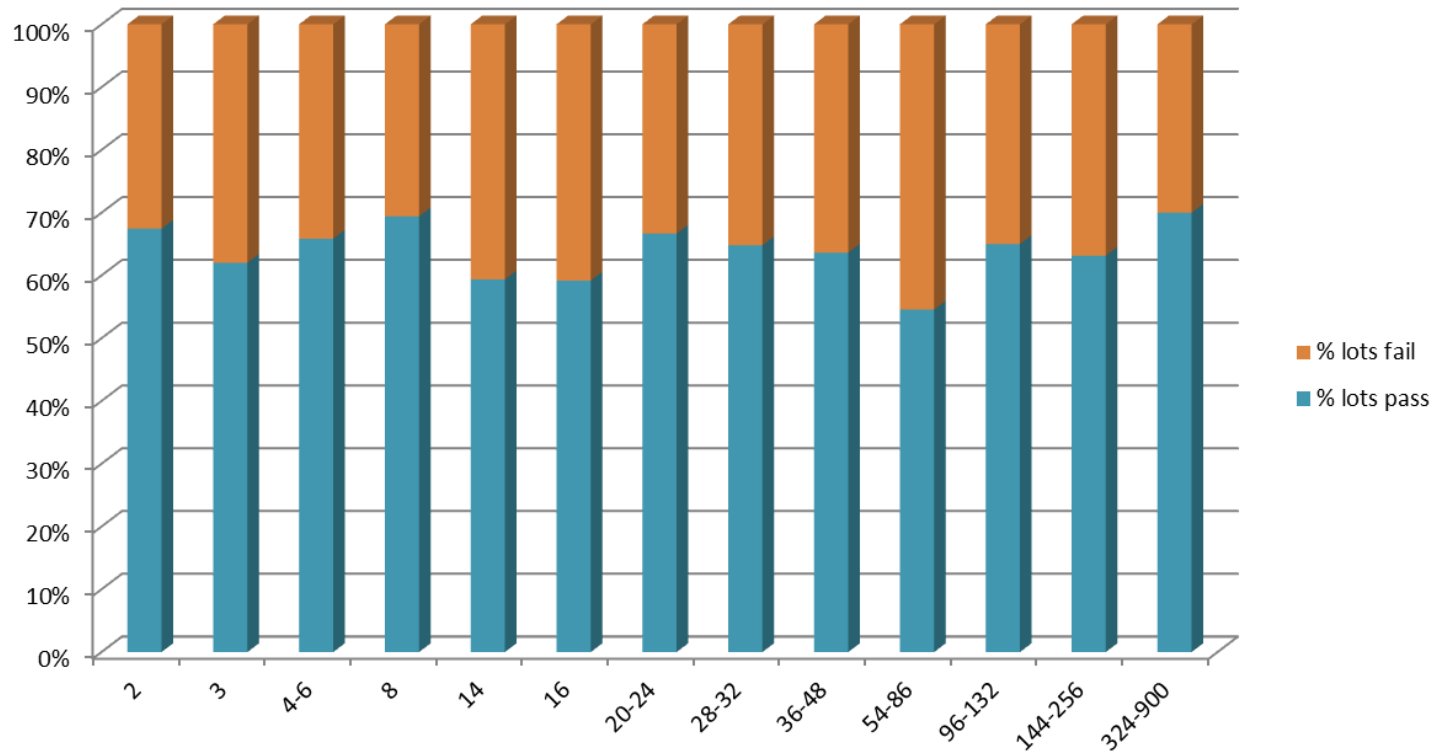
There are meaningful differences between package types in their ability to pass a PEM Qual.



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Overall PEM Qual Success Rate by Pkg Pin Count

PEM Qual Pass/Fail % by Package Pin Count

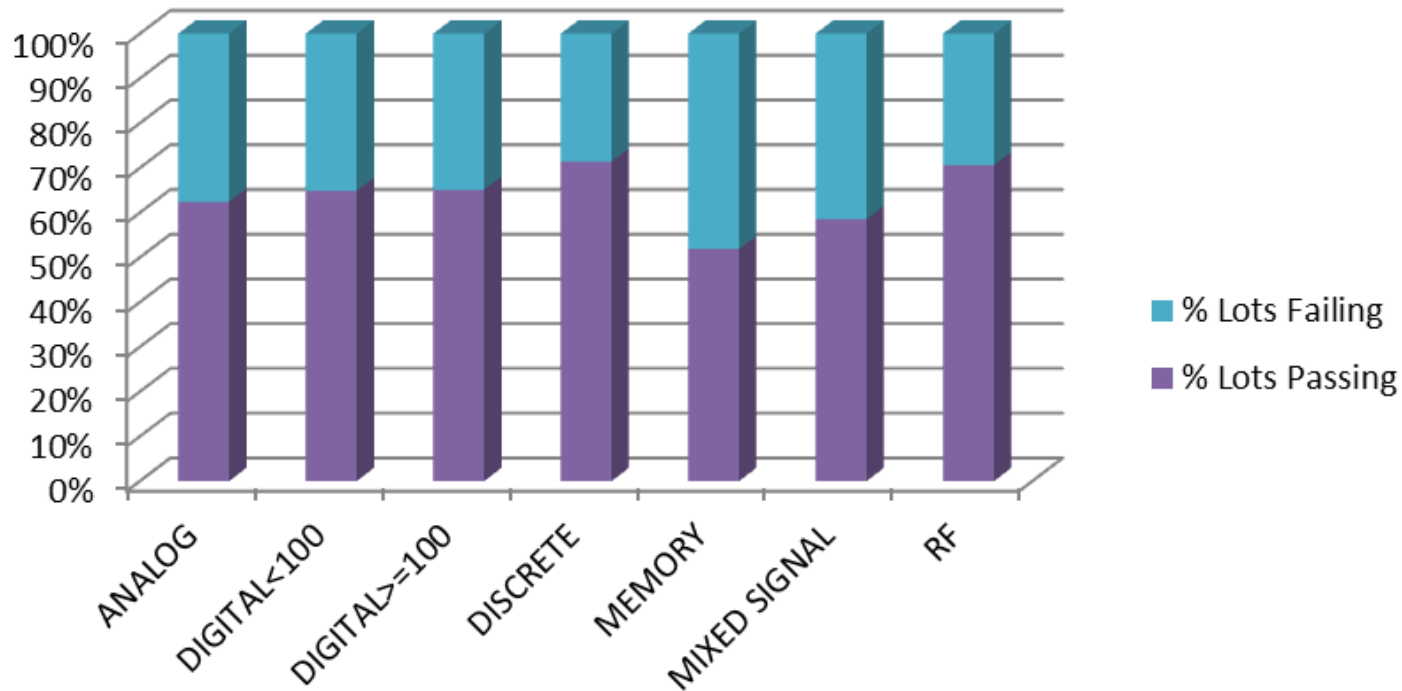


Despite the sensitivity to package type shown on the previous page, there does not appear to be a meaningful sensitivity to package pin count.



Overall PEM Qual Success Rate by Device Technology

PEM Qual Pass/Fail Rate by Technology

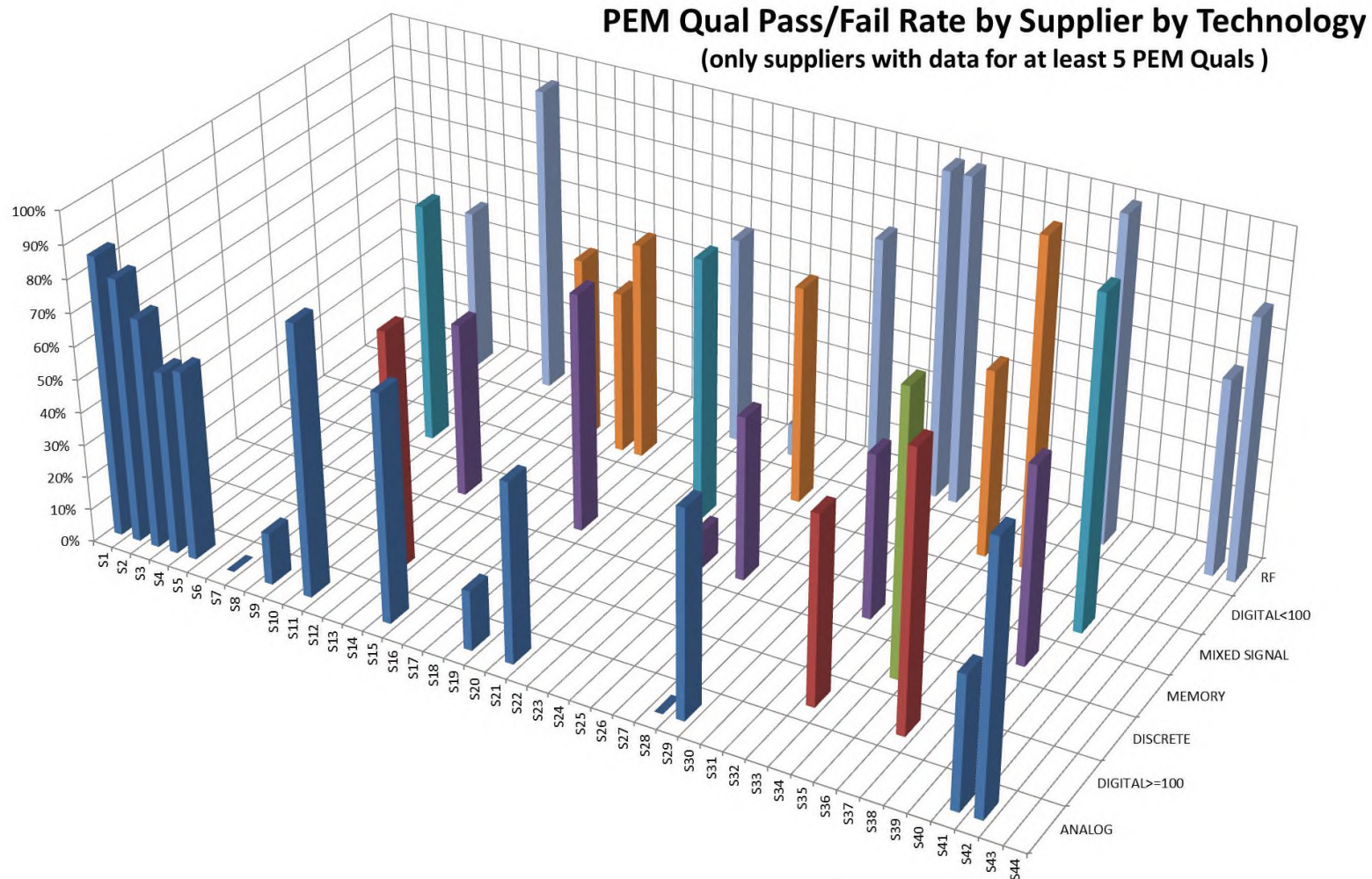


There is not a great deal of sensitivity to technology, with the exception of memory. It should be noted that the memory devices we evaluated tended to more often come in packages that were previously shown to be less reliable.



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Overall PEM Qual Success Rate by Device Technology by Supplier

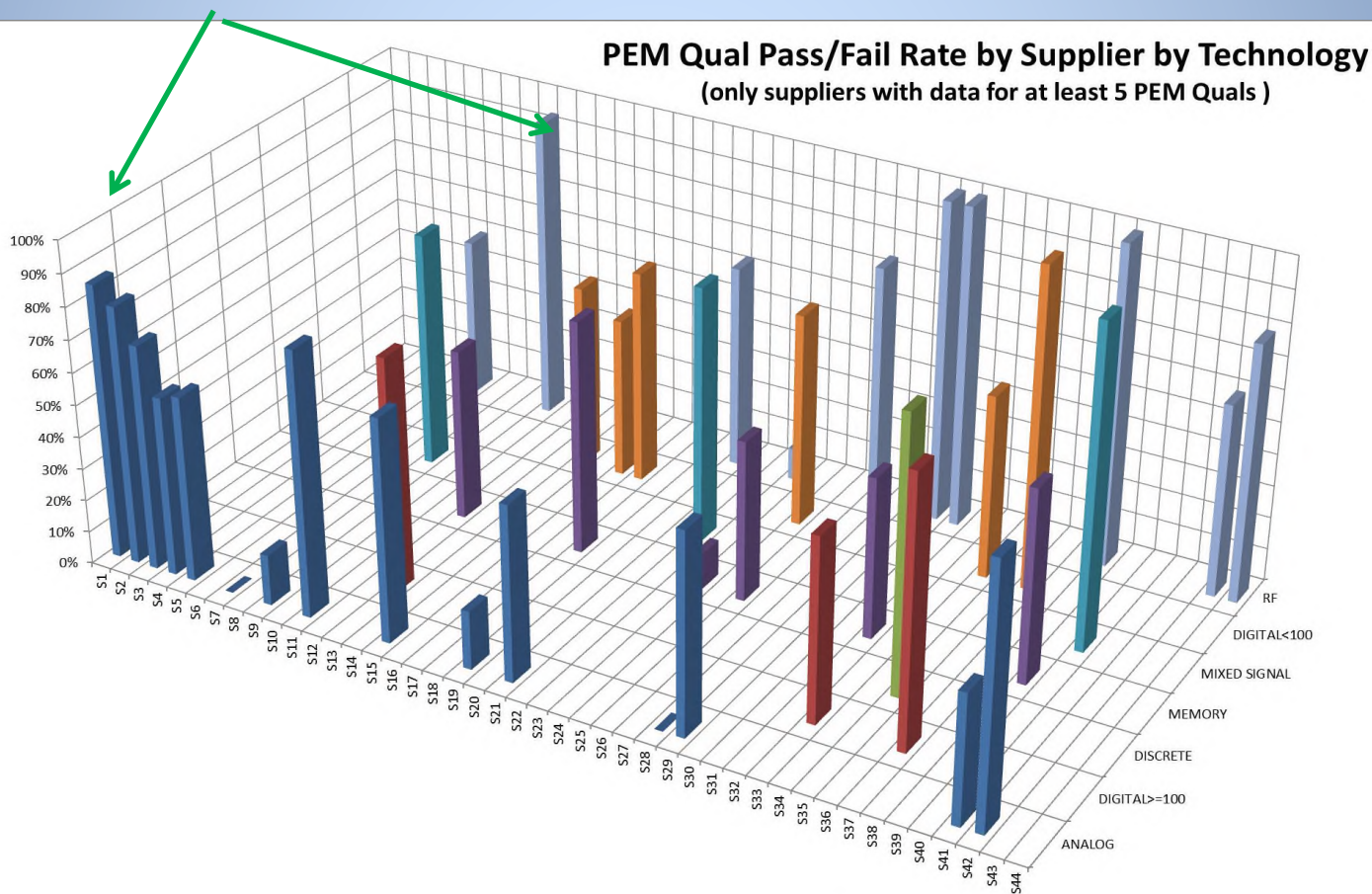




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Overall PEM Qual Success Rate by Device Technology by Supplier

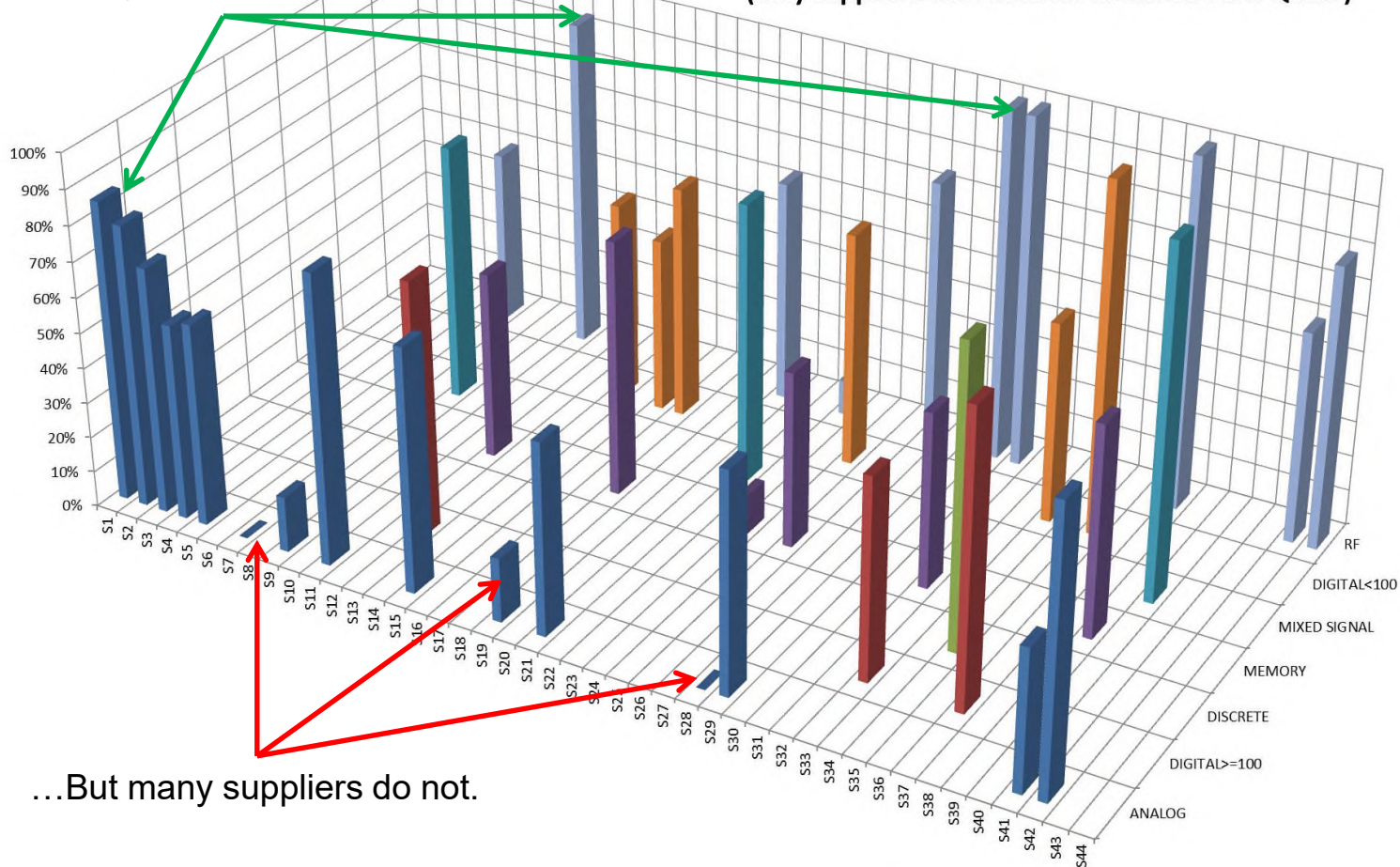
Many suppliers have good
PEM Qual results....



Overall PEM Qual Success Rate by Device Technology by Supplier

Many suppliers have good PEM Qual results....

PEM Qual Pass/Fail Rate by Supplier by Technology
(only suppliers with data for at least 5 PEM Quals)

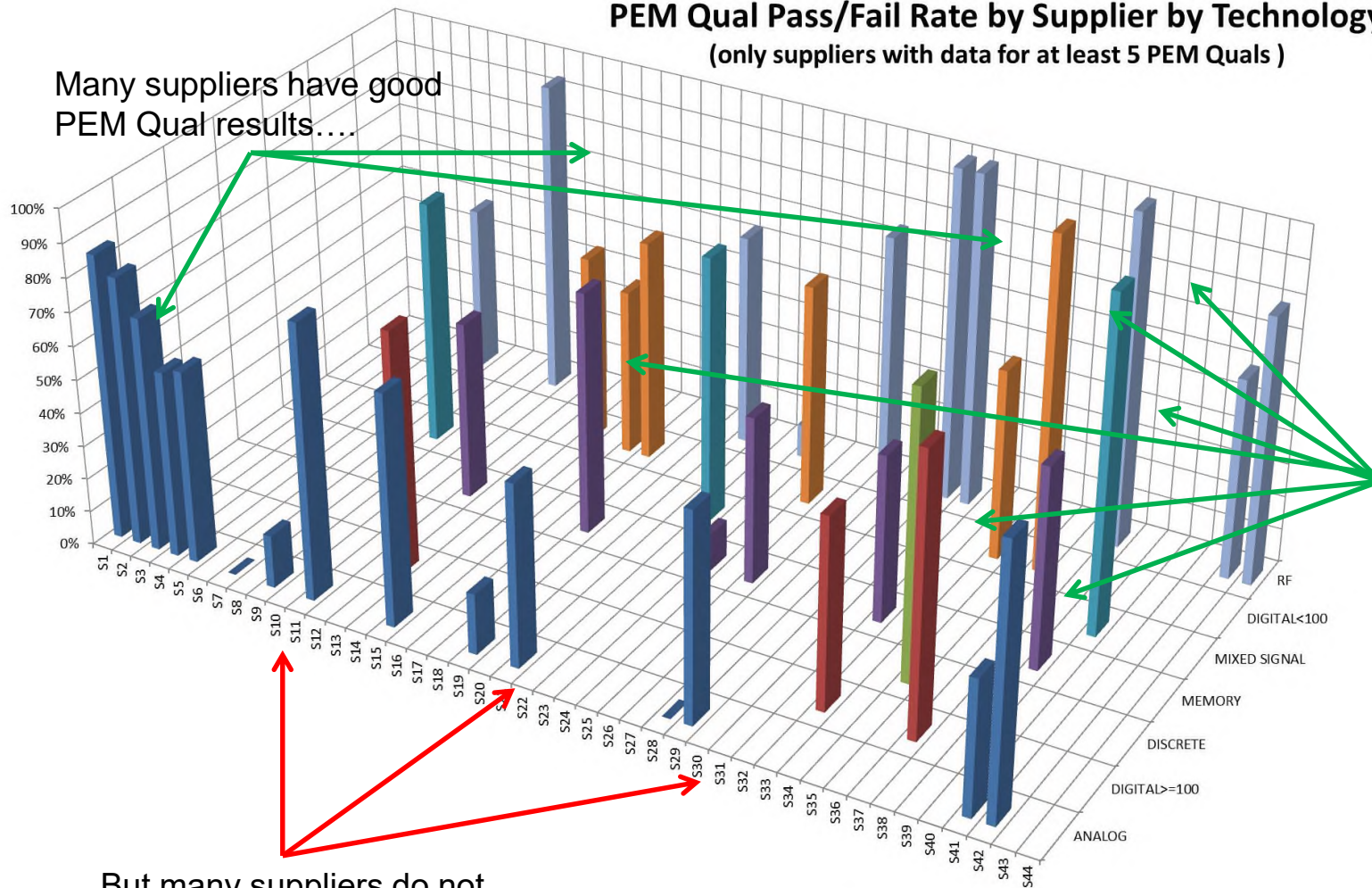


...But many suppliers do not.

PEM Qual Pass/Fail Rate by Supplier by Technology

(only suppliers with data for at least 5 PEM Quals)

Many suppliers have good PEM Qual results....



...But many suppliers do not.

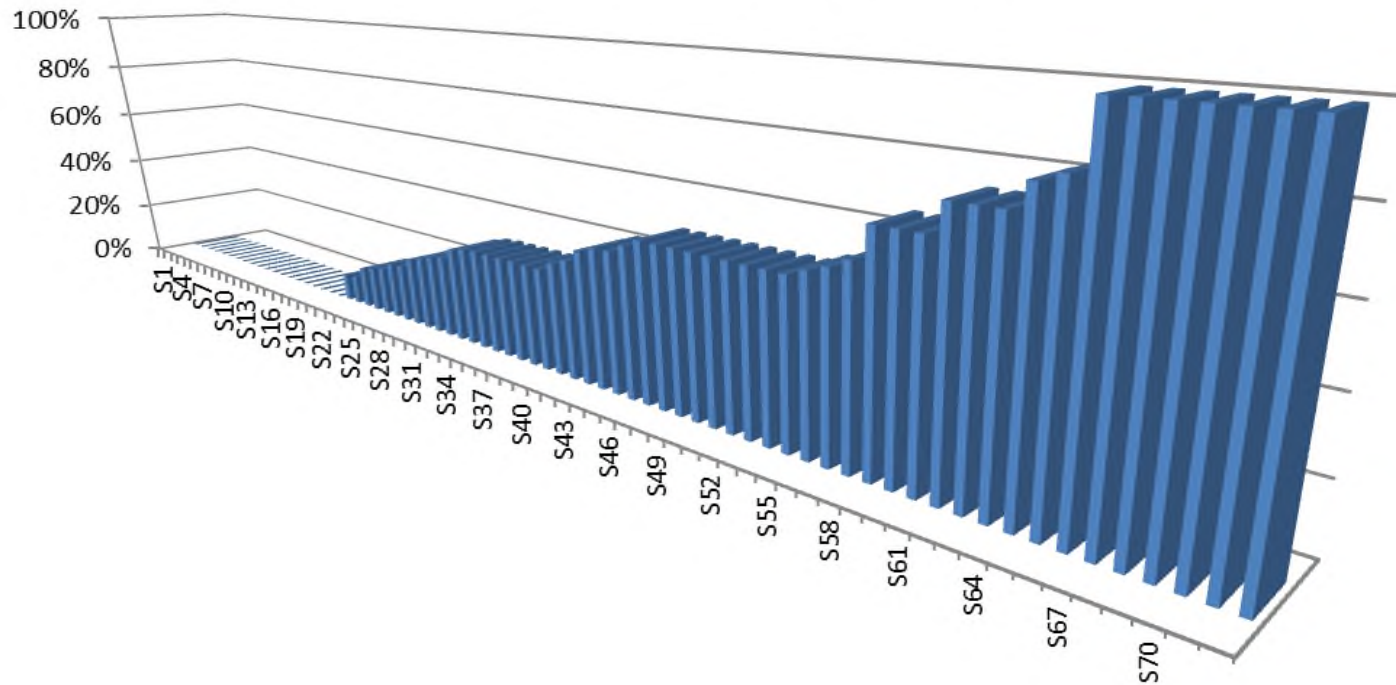
Acceptable suppliers can be found for most technologies.



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Overall PEM Qual Success Rate by Supplier

% of Lots Passing by Supplier



This is arguably the most important point of this data analysis – that PEM Qual success rates vary dramatically from supplier to supplier.

Overall PEM Qual Conclusions

- 1. There is a great variation in the success rate depending upon the supplier that is being evaluated, so it is prudent to evaluate multiple suppliers.**
- 2. Success rate is also influenced by the package being evaluated, although not to as great an extent as by the supplier.**
- 3. Acceptable PEM Qual success rates can be obtained with most technologies and pin counts.**
- 4. Understanding your application needs is essential for selecting the best PEM Qual flow. By matching the PEM Qual flow to the application needs, an accurate assessment can be made at the lowest evaluation cost.**



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Overall PEM Qual Conclusions (continued)

- 5. Clearly understand how comprehensive the electrical test coverage is that your test supplier is providing. Insufficient electrical test coverage will allow failing devices to be counted as passing and could lead to poor system and field reliability.**
- 6. PEM Quals are very complex flows with hundreds of processing steps and thousands of data points. Assure that trained project management staff is present at your test supplier to manage the flow execution and assure data integrity.**
- 7. Overall, PEM Quals can be used to effectively select devices for use in non-commercial environments. In this study, approximately two-thirds of industry devices will pass PEM Qualification.**
- 8. These conclusions are consistent with the conclusions when we last analyzed our database, although our data indicates that PEM Qual success rates are improving.**



Integra Technologies

Questions?

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Thank you from the Employee
Owners of Integra Technologies!!



Next Tutorial – June 29th at 3:30pm EST

This interactive tutorial will include information regarding:

- **System in Package Benefits**
- **Key Considerations**
- **Substrates and Design Rules**
- **Assembly Considerations**
- **Testing and Qualification**

Hosts: Matt Bergeron and Sultan Lilani, Integra Technologies

Presented by: Tony Lowry, SEAKR Engineering, Richard Mailloux, NRDSI, Jeff Schaefer, Integra Technologies, and Sultan Lilani, Integra Technologies