Active Parts – Larry Harzstark

Executive Summary

- The management of PMP (Parts Material Process) activities at the contractors is a critical task that requires personnel with expertise in many areas
- PMP tasks establish the heart of the system reliability based upon part selection, procurement and testing
- The military parts are divided into many classes for different applications
- A major part of PMP management is to understand the nuances of the classes and select the "best" part for the application and balance reliability, cost and schedule for the program

PMP management is critical to ensure long term system reliability

Overview

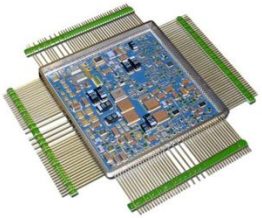
Device Flows	Defines the specific tests and inspections a commodity type will be exposed to based on the quality level Governs the test routine based on specific technologies and failure mechanisms to provide a reliable part for military and space applications
New technology	New technology (part, material or process) must be completely evaluated (characterized and qualified) for space utilization Important because previous failures occurred because parts were not properly characterized or their failure mechanisms understood
Lessons learned	Space or Military level devices requirements are more stringent than lower quality level devices Space level devices require tighter process controls at the wafer fabrication process than lower quality level devices Commercial parts may not be capable of successfully meeting space requirements Important because space requirements are unique and drives characteristics (design, construction and testing) of parts

Overview

Purpose	Provide an overview of Parts, Materials and Processes (PMP) concepts for active device types and explain the importance of the approach
Terminology	Active Parts—microelectronic/semiconductor electrical or electronic piece parts Important to understand the distinction between device types because requirements are based on type
Military Specifications	Component requirements (design, construction, quality and reliability) are governed by military specifications Mil specs define multiple levels of quality assurance invoking specific controls and testing requirements
Overall Manufacturing Flows	• Wafer fabrication – semiconductor process using masks or blueprints to build device in layers • Wafer probe test – lowest level of electrical test to validate functionality of devices and weed-out non-working devices • Packaging – Assembly into a completed device • Final Testing – complete parametric & functional testing over environments to verify device meets specification Governs how a part is manufactured and tested
Part Testing	Device testing Consists of a)100% screens (electrical & environmental) to eliminate weak or marginal parts. b) Qualification to determine whether part design and construction is adequate for space usage c) Quality Conformance Inspection or lot conformance tests to validate specific lot of parts to be used in flight hardware meets requirements Governs the determination of a good versus bad part

Terminology

- Active Parts-- electrical or electronic piece parts that have the ability to control electron flow
  - Discrete Semiconductors – 1 die of either a diode function (conduct electricity in one direction) or transistor function (amplify and switch electronic signals and power).
    - Example: Schottky Diode, Rectifier, Zener Diode, Switching Transistor
  - Integrated Circuits also known as microcircuits – 1 die containing multiple transistors and diodes inter-connected by a metalization pattern to provide a specific circuit function.
    - Example: ASIC, Static RAM, EEPROM, Microprocessor, FPGA
  - Hybrid Microcircuits also known as Hybrids – contains multiple die (usually transistors, diodes, integrated circuits and passive elements) connected on a substrate within a package to provide a specific function
    - Example: DC-DC Converter
  - Multi-Chip Modules also known as MCM's – similar to a hybrid but only contain multiple integrated circuits.
    - Example: Memory Modules (64M SRAM)



Terminology

- Active Parts-- electrical or electronic piece parts that have the ability to control electron flow
  - Application Specific Integrated Circuit (ASIC) – an integrated circuit device designed and fabricated to perform a specific function for an application
  - Field Programmable Gate Array (FPGA) – an integrated circuit designed for a specific function within an application chain. The device manufacturer fabricates the generic unprogrammed device and delivers to a customer who then programs it for the application
  - ASICs usually used for speed (faster than FPGA & general microprocessor)
  - FPGAs often used to prove out an ASIC design
  - FPGAs cheaper & can be reprogrammed.

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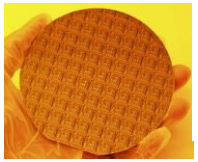

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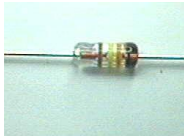

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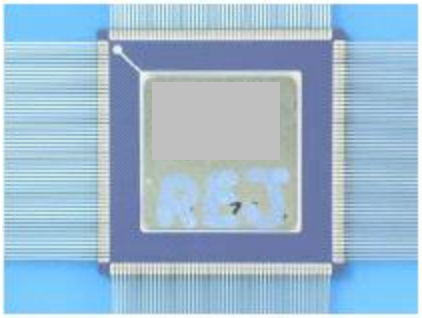
Part Identification

- Devices are identified either with the military part number or contractor part number
  - Examples
    - 5962-10101VXA – Integrated Circuit
    - M38510/10101SXA – Integrated Circuit
    - JANS2N2222A – Transistor
    - 3M114ABC – Contractor Integrated Circuit



- Devices are manufactured and identified with a lot date code that allows traceability to a specific manufacturing lot
  - Lot date code represents the specific date when the device package was sealed

Part number and traceability are important – allows for trending and reachback of problems

Quality Assurance Levels in MIL-SPECS

	Space Level Hermetic*	Space Level Non-Hermetic*	Avionics Level (launch vehicles, planes, tanks, etc) Hermetic*	Commercial Hermetic	Non-Hermetic Plastic
Integrated Circuits MIL-PRF-38535	Class V Extensive testing & documentation includes x-ray, tighter visual inspection, nondestruct bond pull, longer more stressful burn-in	Class Y/P Essentially the same testing reqts as Class V but no seal tests, no bond pulls, addtl visual reqts	Class Q Less testing and process controls than Class V/Y. No xray or non-destruct bond pull, less stringent visual inspection and shorter burn-in times	Class T Geared for commercial space. Reqts decreased from Class V to allow less costly parts but has increased risk due to less testing	Class N/P All requirements are determined by manufacturer and each manufacturer flow will be different.
Hybrids MIL-PRF-38534	Class K Reqts similar to Class V	Class L Reqts similar to Class Y	Class H Reqts similar to Class Q	Class D & E Reqts determined by manufacturer	Class F Reqts similar to Class H
Discrete Semiconductors MIL-PRF-19500	JAN S Requirements similar to Class V	N/A	JANTXV Non-critical JANTX Reqts similar to Class Q	JAN J or JAN Reqts similar to Class T	In Development

*Hermetic has the quality of being **airtight**. In common usage, the term implies not letting the ingress or egress of gasses, moisture, contaminants and is defined by a leak rate.

Different quality levels define the requirements for design, construction, reliability and testing for the intended application

MIL-PRF-ATM Purpose and goals

- MIL-PRF-ATM (Advanced Technology Microcircuit) intended to bring heterogeneous integrated (HI) components into the military specification (QML) arena

- HI parts procured as COTS, SCD, or MFG specific flows have been and continue to be used by various USG programs. ATM intends to standardize test and documentation expe

- ATM intended to be technology and MFG approach agnostic
  - Some technologies not addressed (integrated photonics, some III-IV items, etc.)
  - Fan out method agnostic

- Primary drivers from MIL-PRF-38535/34 to ATM are TSVs, chiplet use, >2D configuration

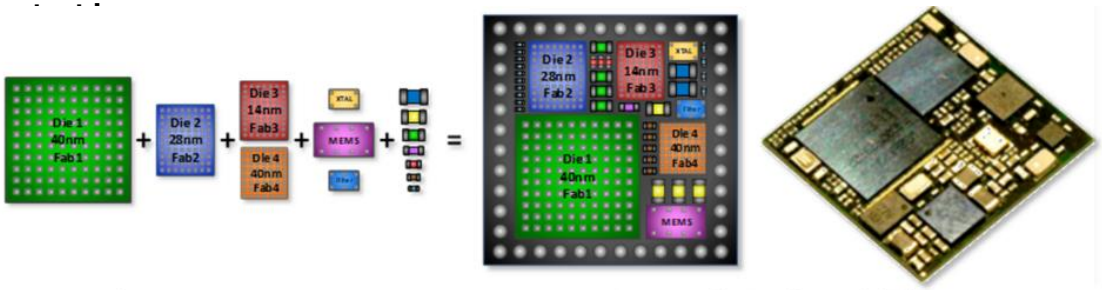


Figure 6. Heterogeneous Integration and System in Package (SiP). Source: ASE

Ref: Heterogeneous Integration Roadmap - IEEE Electronics Packaging Society

Difference of ATM product vs. MIL-PRF-38534/38535 legacy

- Each ATM product will have a SMD, Qualification plan, and Production plan
  - Production plan is similar to legacy 38535 Appendix A material but may also address "test optimization" as part of initial production
    - Intent is to provide OEM flexibility to optimize test flows aligned with product capabilities vs. arbitrary recipe applied to all products
  - Qualification plan incorporates multiple documents including radiation plan (RPP), Package integrity plan (PIDTP), and other elements to address qualification
    - ATM product typically have already undergone qualification and technology verification at OEM
    - Qualification differences addressed vs. failure mechanisms needing to be address for military / space needs
  - Intent of SMD is to provide opportunity for OEMs to capture and make available to the community additional information not currently within SMD scope
- Each ATM product is expected to have a specification written by the manufacturer that is not approved by the qualifying activity
- ATM products tend to be OEM specific with multiple levels of IP integrated
  - Availability of information to purchaser may require NDA
- Intent of documentation change is to simplify and streamline where possible and ensure content is aligned with HI products vs legacy monolithic or hybrid products

Status

- Using MIL-PRF-38535 as basis, pulling in 38534 material and modifying to make applicable to HI production, test flows, radiation capabilities, etc.
- OEMs provided flexibility to identify best method to validate product capabilities vs. failure mode
- Integrating NASA and Aerospace industry activities as applicable

Source	Section	Main body text	Main body tables	Appendix A	Appendix B	Appendix C	Appendix D	Appendix E	Appendix F	Appendix G	Appendix H	Appendix J
38535	Used	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
	Title	Specification	Specification	Quality	Space requirements	Radiation	Sampling	Qualification of offshore processes	Tape bonded items	QML program	Cert, Val, Qual	TCI and screening
	ATM use	Baseline for main body text	Baseline for main body tables	Baseline for Appendix A	Integrate into main body	Redlines and incorporate	TBD	Keep letter for potential future use	Keep letter for potential future use	Incorporate as needed into other sections	Baseline for PIDTP	Incorporate as needed into other sections
38534	Used	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	No	No
	Title	Specification	Specification	Quality	Don't use	Hermetic element	Non-hermetic element	Design and construction criteria	Sampling	RHA	Don't use	Don't use
	ATM use	Incorporate elements as needed	Incorporate elements as needed	Don't use	Don't use	Integrate into main body tables as needed	Integrate into main body tables as baseline	Integrate into Appendix A, H as needed	Merge with Appendix D as appropriate	Baseline for Appendix C	Don't use	Don't use
ATM	Used	Yes	Yes	Yes	No	Yes	TBD	No	No	No	Yes	No
	Title	Specification	Specification	Quality	Don't use	Radiation	Sampling	Don't use	Don't use	Don't use	Cert, Val, Qual	Don't use
	Rationale	See applicable file DRAFTED	See applicable file IN WORK	See applicable file DRAFTED	Integrated into main body text and tables	See applicable file IN WORK	Is the sampling rationale applicable to ATM devices? Merge 35/34 sampling appendixes into 1?		Tape not expected to be applicable to ATM devices	Integrate into main body and Appendix A	PIDTP material ON DECK	May integrate into Appendix H and other locations

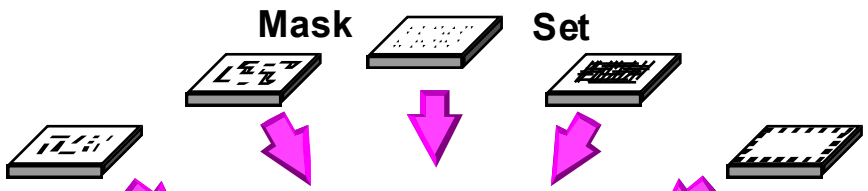
- Shifting format from legacy MIL-STDs to focus on failure modes, mechanisms and intent behind tests
- Core issue with HI product is that legacy approaches to quality and reliability verification may not be applicable due to application dependencies resulting in need to identify alternative community acceptable approaches for "standard" quality and reliability validation products

SAE INTERNATIONAL

Fabrication flow of an Active Device

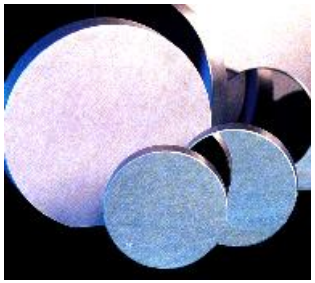
Wafer Fab ➡ Wafer Test ➡ Packaging ➡ Package Test

Issues Observed
- Incorrect/errors on masks
- Immature process
- Bad/dropped wafers
- Furnace errors

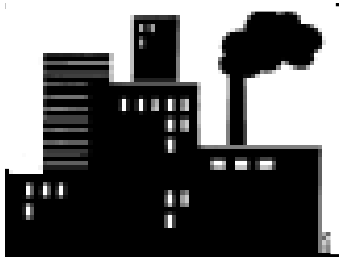


A topology of transistors, interconnects, & insulators defined by a "mask set" is built up layer by layer on the blank wafers

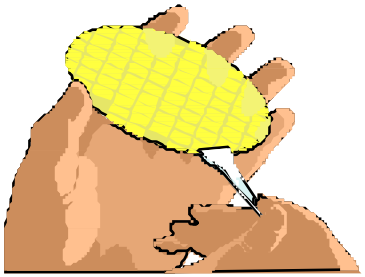
A layer by layer build up of patterns created on the blank wafer to define the designed function & performance desired. The patterns are made by the use of masks & etching processes which create the final device layout.



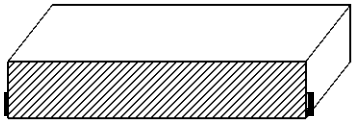
"Blank" Wafer



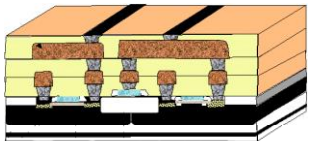
Integrated Circuit (IC) Factory



Finished IC "Die" on Wafer



Cross-section



Cross-section

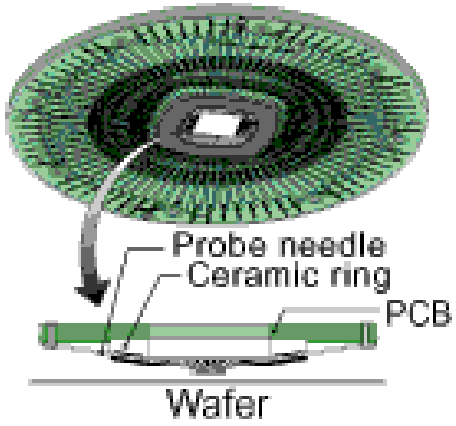
Pictorials developed by Aerospace from various sources

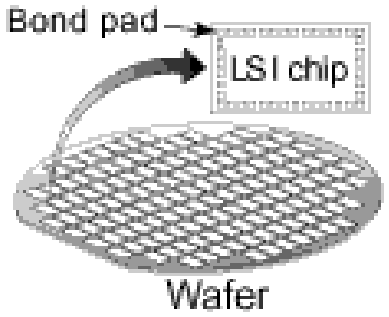
SAE INTERNATIONAL

Wafer Test

- Wafer die automatically "probe tested"
  - First point of evaluating electrical characteristics after fabrication
- Purpose to "screen out" defective die prior to the expensive packaging step
- DC tests & slow speed dynamic tests
- Early look at Proof Of Development (POD) functionality
- Room & high temperature tests
- Die destined for multi-chip packaging require more stringent screening
- Issues Observed
  - Bad/Wrong test program or fixture
  - Overstressed/ESD causing yield problems

Wafer-level tests screen defective parts before proceeding to higher levels of assembly

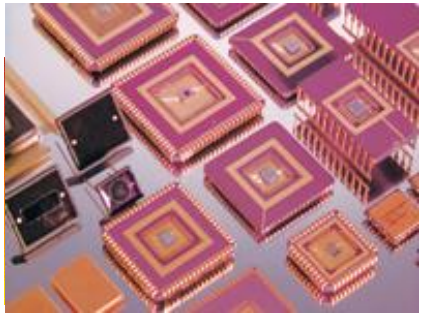


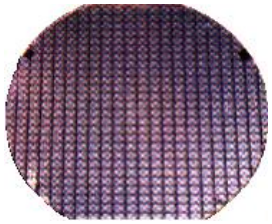


Pictorials Courtesy of Unknown Origin on Internet

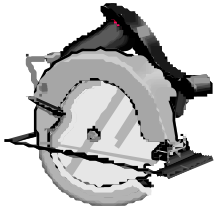
Packaging (Assembly)

ICs that pass preliminary wafer test (probe) are then marked, cut into die and packaged

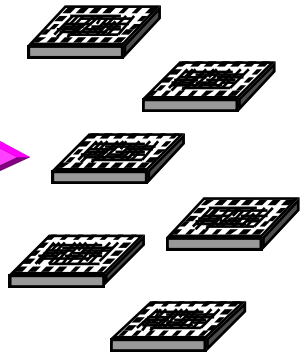




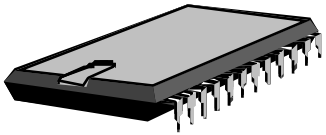
Finished Wafer

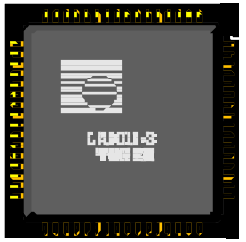


Wafer "Dicing"



Integrated Circuit Die or "Chips"





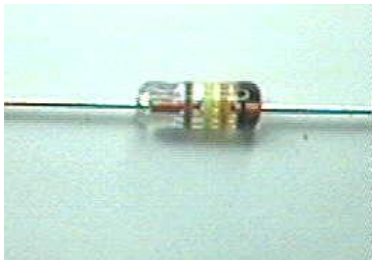
Die can be Mounted in a Variety of Package Types

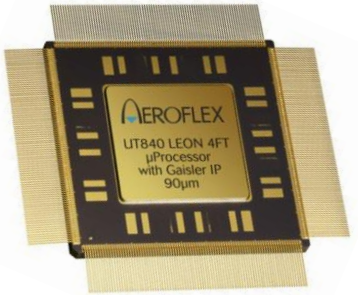
Issues Observed
- Chipped/scratched die
- Bad die attach
- Bad wire bonds
- Poor lid seal
- Cracked seals

Pictorials Courtesy of Unknown Origin on Internet

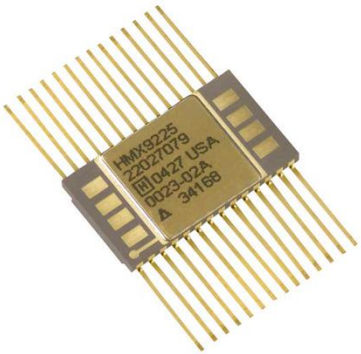
Packaging

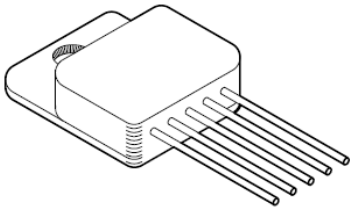
- Packages for microelectronic devices come in many varieties and styles
  - Hermetic
    - Glass Body
    - Metal Can
    - Ceramic/Metal Flat Packs
    - Ceramic Dual-In-Line
    - Surface Mount
    - Leadless Chip Carrier
    - Custom
  - Non-Hermetic
    - Plastic
    - Flip-Chip





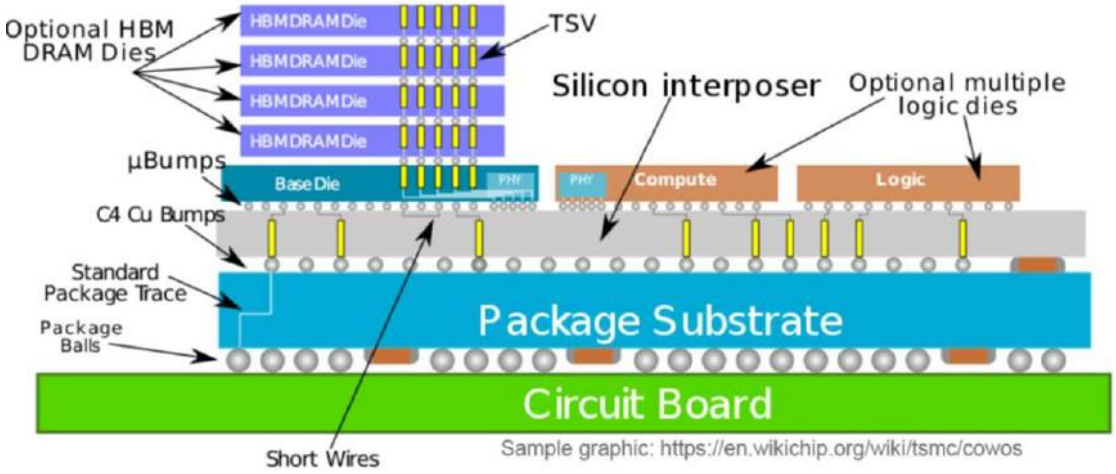




Many styles of packages

Advanced Packaging

- Manufacturers using advanced packaging techniques for enhanced performance
  - Flip-chip die attachment
  - Column Grid Arrays
  - Non-hermetic
  - External capacitors for bypass and filtering



Pictorial courtesy of Xilinx Corporation

Specification History

- In the early 1960's, the IC industry was developing, and IC failures were common. It was recognized that a series of standard screening tests could reduce or eliminate these "infant mortality" type failures
- The USAF Rome Air Development Center (RADC) was given the task and in 1968 developed MIL-STD-883
- 883 was intended for military hermetic parts
  - In the context of microelectronics, it implies an airtight seal that will keep moisture and other harmful gases from penetrating the sealed package.
  - Metals, ceramics and glasses are the materials used to form the hermetic s, al and prevent water vapor from accumulating inside the package.
  - A properly made hermetic seal with a sufficiently low leak rate can keep a package dry and moisture free for many years
- Concurrent with the development of MIL-STD-883 RADC established Mil-M-38510 procedures to specify the electrical and package outlines for standardization
- MIL-M-38510 set out the procedures to obtain a QPL listing for a given slash sheet and quality level
  - This is the predecessor of the modern Mil-Prf-38534/5
- This was a very effective system for the simpler part types and JAN slash sheets are still in use today.

Specification Today

- A result of the Perry Initiative of the mid 1990's was to change the philosophy of rigid requirements in mil-specs and go to "performance specifications"
- The performance spec establishes the general requirements for the item (discrete semiconductor, monolithic integrated circuit or hybrid) and the verification requirements for ensuring that these devices meet the applicable performance as defined
- Performance Specs encourage and allow for alternate verification testing methods to meet performance requirements and foster ingenuity and growth within the supplier base.
- Performance Specifications
  - General Hybrid Spec MIL-PRF-38534L (3 DEC 2019) FSC 5962
  - General Specification for Microcircuits MIL-PRF-38535 FSC 5962
  - General Specification for Semiconductor Devices MIL-PRF-19500 FSC 5961
- Military Standards
  - Standard Test Methods for Microcircuits MIL-STD-883L
  - Standard Test Methods for Semiconductor Devices MIL-STD-750

MIL-PRF-19500, MIL-PRF-38534 and MIL-PRF-38535

- These specifications are performance specifications with the purpose of establishing the general requirements for the item (monolithic integrated circuit. Hybrid or discrete semiconductor) and the verification requirements for ensuring the devices meet the applicable performance as defined.
- The documents cover the following:
  - Design and Construction
  - Packaging
  - Traceability
  - Quality Assurance
  - Performance
  - Verification
  - Screening
  - Qualification
  - Quality/Technology Conformance Inspection
  - Test Optimization
  - Non-conformances
  - Audits
  - New Technology Insertion

MIL-STD-883 and MIL-STD-750

- A collection of destruct and non-destruct test methods used as screening and qualification tests to verify microelectronic (monolithic and hybrids) performance requirements and to assess the reliability of devices
- 1000 series TMs… Environmental Tests
- 2000 series TMs… Mechanical Tests
- 3000 series TMs… Electrical Tests (Digital)
- 4000 series TMs… Electrical Tests (Linear)
- 5000 series are Test Procedures e.g. TM 5011, TM 5008
- When testing to 883 one MUST further specify the test condition, quality level and other details contained in the individual test method.
- MIL-STD-750 test methods are used for discrete devices and mirror test methods for the integrated circuits and hybrid devices

Plastic Encapsulated Microcircuits (PEMs) and Plastic Encapsulated Devices (PEDs)

- As described earlier, the mil-specs were developed for the use of hermetic packages, but most new complex devices are manufactured in plastic encapsulated packages
- Various organizations are generating requirements for military/space systems to utilize plastic devices
- The utilization for plastic parts in military and space applications have to ensure the parts are rugged and will meet the mission requirements
  - Temperature
  - Mechanical
  - Radiation
  - Reliability
- SAE with industry, and government support developed documents for utilization of commercial, COTs and other types of parts
  - AS6294/1 space and AS694/2 for terrestrial
  - AS6294/3 space discrete semiconductors and AS6294/4 discrete terrestrial
  - Task groups assigned to implement requirements in applicable mil-specs
  - Supplier buy-in mandatory
- JEDEC has various task groups assigned to implement these SAE documents into the mil-spec system to ensure a standardized flow for customers

Package Level Testing

- Purpose to "screen out" defective or marginal devices not meeting performance requirements
- All parts are tested for DC, AC and functional performance
- Room, cold & high temperature tests are performed
- Issues Observed
  - Bad/Wrong test program or fixture
  - Overstressed/ESD causing yield problems

Pictorials Courtesy of
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First complete evaluation of electrical performance

Some Intrinsic Failure Mechanisms of Active Devices

- Electromigration
  - transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. It can cause the eventual loss of connections or failure of a circuit
- Time Dependent Dielectric Breakdown
  - when the gate oxide breaks down as a result of long-time application of relatively low electric field
- Negative Bias Temperature Instability
  - manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance of a MOSFET
- Bond Wire
  - Broken
  - Nicked
- Die Attach
  - Voiding
  - Thermal Conduction
- Thermal Runaway
  - an increase in temperature changes the conditions in a way that causes a further increase in temperature, often leading to a destructive result.
- Corrosion
  - an electrochemical process in which one metal corrodes preferentially to another when both metals are in electrical contact and immersed in an electrolyte

DEVICE FLOWS

Screening and Qualification/Quality Conformance Inspection

Governs the test routine based on specific technologies and failure mechanisms to provide a reliable part for military and space applications

QML Monolithic IC Class Q, V and T Screening

Item #	Screen	Class Q	Class V/Y space	Class T	Rationale for Test
1	Wafer Lot Acceptance	QM Plan	QM Plan or 883/5007	QM Plan	Quality of wafer
2	Non-Destruct Bond Pull	No	Yes – 883/2023	No	Quality of wire bonds
3	Internal Visual Insp	Yes – 883/2010 cond B	Yes – 883/2010 cond A	Yes – 883/2010 cond A	Ensures no defects internal to pkg
4	Temp Cycle	Yes – 883/1010C; 10 cyc, Y1 only	Yes – 883/1010C ; 10 cyc	Yes- 883/1010C ; 10 cyc	Ensure die attach and wire bond integrity
5	Constant Accel	Yes- 883/2001E	Yes- 883/2001E	Yes- 883/2001E	Ensures die is attached well

QML Monolithic IC Class Q, V and T Screening

	SCREEN	CLASS Q	CLASS V (Space)	CLASS T*		Rationale for Test
6	Visual Inspection	Req'd 100%	Req'd 100%	Req'd 100%		
7	Particle Impact Noise Detection (PIND) (MIL-STD-883/Method 2020, Cond A)	Not Req'd	Req'd 100%	Not Req'd		Ensures device cavity is free of particles that could potentially cause failures
8	Serialization	Not Req'd	Req'd 100%	Not Req'd		Allows for read and record measurements to be recorded
9	Pre-burn-in Electrical	Req'd 100%	Req'd 100%	Req'd 100%		Defines electrical performance of devices
10	Burn-in (MIL-STD-883/Method 1015)	Req'd 100%	Req'd 100%	Req'd 100%		Stresses devices to weed out marginal performance and process drift failures
		125˚C, 160 hrs	125˚C, 240 hrs	125˚C, 160 hrs		
11	Interim Electrical	Not Req'd	Req'd 100%	Not Req'd		Defines electrical performance post burn-in
			Read & Record			
12	Reverse Bias Burn-in	Not Req'd	Req'd 100%	Not Req'd		Stresses devices to weed out marginal performance and process drift failures
	(MIL-STD-883/Method 1015, Cond A or C) 72hrs, 150˚C					
13	Interim Electrical	Req'd 100%	Req'd 100%	Req'd 100%		Defines electrical performance post burn-in (HTRB or static)
			Read & Record			

QML Monolithic IC Class Q, V and T Screening (cont'd)

	SCREEN	CLASS Q	CLASS V (Space)	CLASS T*		Rationale for Test
14	Percent Defective	Req'd 5%	Req'd 5%	Req'd 5%		Evaluates good versus marginal lots
	Allowable (PDA)		3% functional			
15	Final Electrical	Req'd 100%	Req'd 100%	Req'd 100%		Defines electrical performance (DC,AC, functional, switching across full mil-temp range)
16	Seal (Fine & Gross) (MIL-STD-883/Method 1014)	Req'd 100%	Req'd 100%	Req'd 100%		Weeds out marginal seal leak devices
17	X-Ray (MIL-STD-883/Method 2012), 2 views	Not Req'd	Req'd 100%	Not Req'd		Weeds out marginal devices due to lid seal, particles, etc
18	External Visual (MIL-STD-883/Method 2009)	Req'd 100%	Req'd 100%	Req'd 100%		Weeds out visual defects
19	Radiation Latch-up (MIL-STD-883/Method 1020)	Optional	Optional	Optional		Weeds out devices susceptible to radiation latchup
20	Technology Review Board	Req'd	Req'd	Req'd		Responsible for QML program within supplier

*Class T product shall be capable of Class Q reliability unless otherwise delineated in the SMD.
Class T flow shall be defined in the suppliers QM plan.

QML Monolithic IC Class Q, V and T Quality Conformance Inspection

	GROUP	GLASS Q	CLASS V	CLASS T
1	Group A (electrical)	Required	Required	As defined
	DC, AC, Functional, Switching	sample basis	sample basis	in the suppliers
	25°C, 125°C and -55°C			QM Plan
2	Group B	Required on a sample basis	Required on a sample basis	As defined in the
		every inspection lot	every inspection lot	suppliers QM Plan
		Resistance to Solv	Phy Dimensions	
		Solderability	Intl Water Vapor	
		Bond Strength	Resis to Solvents	
			Int Visual/Mech	
			Bond Strength	
			Die Shear	
			Solderability	
			Lead Integrity	
			Seal	
			Lid Torque	
			Life Test	
			Temp Cycle	
			Acceleration	
			Seal	
3	Group C	Life Test	N/A	As defined in the
		periodic - every quarter		suppliers QM Plan
4	Group D(package related)	Req'd	Req'd	As defined in the
	periodic - every 6 months	(same tests)	(same tests)	suppliers QM Plan
5	Group E (radiation assurance tests)	Req'd if offerred as a radiation	Req'd if offerred as a radiation	Req'd if offerred as a radiation
		device	device	device

QML Monolithic IC Class Q, V, T and P Screening

3	Group C	Life Test initially and only after design or process changes	1000 hours every lot at 125C	1000 hours every lot at 125C	1000 hours every lot at 125C
4	Group D (package related)	Req'd - same tests performed	Req'd - same tests performed	Req'd - same tests performed	Req'd - same tests performed
5	Group E (radiation assurance tests)	Req'd if offerred as a radiation device	Req'd if offerred as a radiation device	Req'd if offerred as a radiation device	Req'd if offerred as a radiation device

Important Truths to Remember

- Space and Military level devices requirements are more stringent than lower grade level devices
- Space and Military level devices require tighter process controls at the wafer fabrication process than lower quality level devices
- Contractors will state their devices are space and military level equivalent
  - Many contractors actually believe this statement, but do not really understand the requirements of space devices
  - Many contractors will tell you the devices have been 100% screened or up-screened (procure a lower quality level part and perform tests to bring up to a higher quality level) to the space level requirements, but do not address the wafer fabrication, design or assembly requirements for space devices
  - Some parts actually meet all space requirements, but suppliers do not want to expend the funds to maintain a compliant space line

Evaluate and understand each contractor claim for space and military equivalent devices

Hybrid Microelectronics

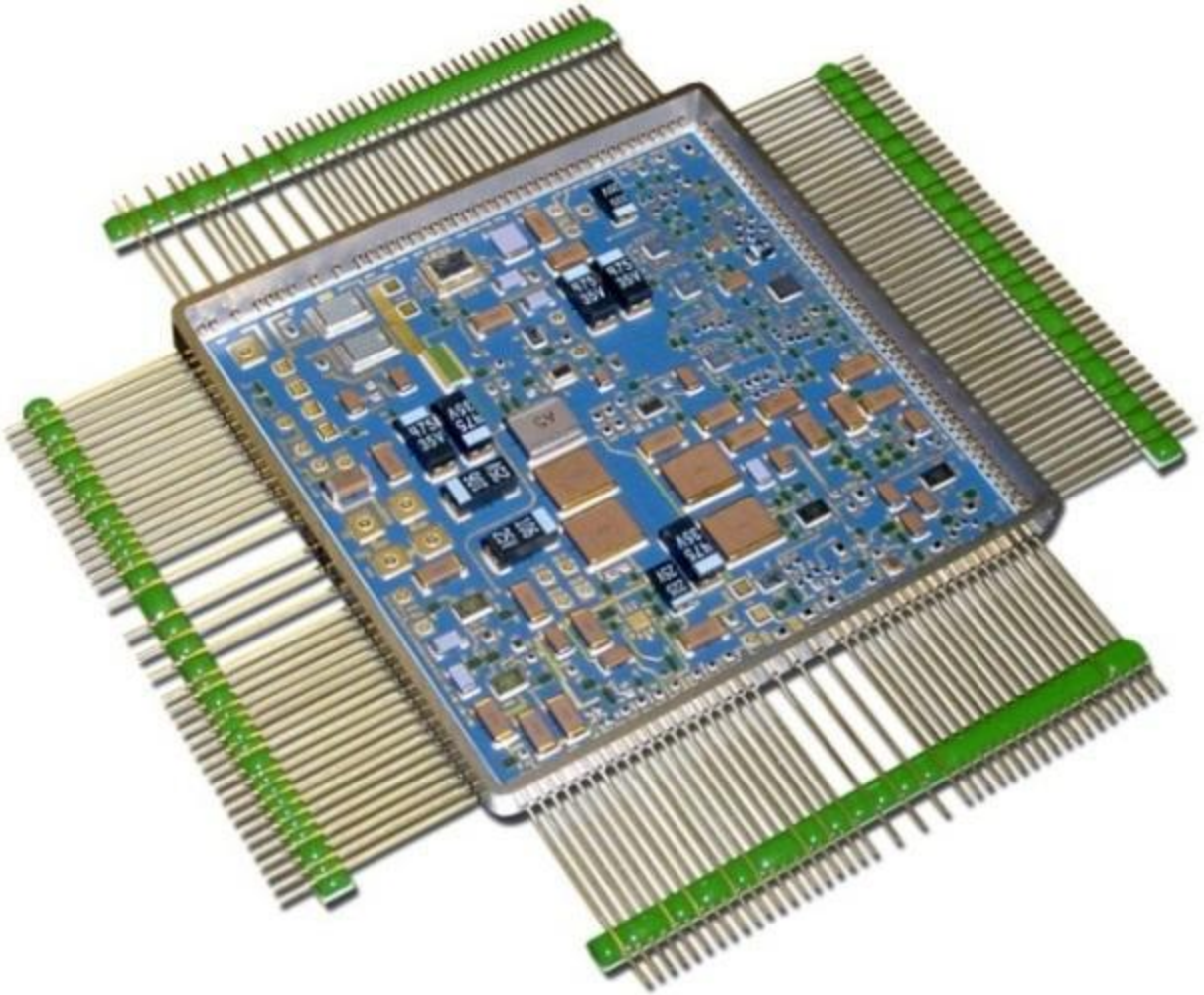
- Hybrid Microelectronic devices are very complex in nature due to the assembly of different die types and assembly techniques used for fabricating hybrids
- Many issues have been observed at all stages of design, manufacturing, testing and usage
  - Design Issues
    - Components/elements not correctly selected or not properly derated
    - Use of commercial components versus military or space grade
    - Characterization
      - Components/elements not completely characterized
      - Temperature range
      - Environmental conditions
      - Radiation environment
    - Failure mechanisms of components/elements not identified or understood
  - Manufacturing
  - Processes not completely understood or characterized
  - Processes not qualified to application environments
  - Use of techniques not allowed for space
    - Components stacked on other components or touching underside of lid/package
    - Wire dress and support
  - Loose particles inside cavity
  - Components coming loose and/or lifting
  - Use of prohibited materials – i.e., pure tin

Hybrid Microelectronics (continued)

- Many issues have been observed at all stages of design, manufacturing, testing and usage
  - Testing
    - Components/elements not tested completely or at all
    - End item not tested completely (Limited environments)
    - Ignoring failures
    - Wire bonds lifting/breaking
    - Elements/substrates/components lifting
    - Radiation failures
- In order to reduce and/or eliminate problems, the following are some recommended solutions
  - Select suppliers/manufacturers with a known high reliability track record for similar product
  - Select the proper components and materials for the application requirements – quality level, electrical, mechanical, thermal and radiation performance
  - Characterize the complete operation of the component, hybrid, module, circuit in the application conditions and understand the margin available
  - Evaluate the physics of failure and understand all the potential failure mechanisms to allow mitigation
  - Evaluate and characterize the manufacturing processes
  - Qualify the item to the full application requirements with margin

Hybrids continue to be a major source of problems and must be evaluated in detail

Hybrid Photo



New Technology

- New technology/devices that are to be utilized for space applications and have no space heritage, must be characterized and qualified to ensure they will meet space mission requirements
- Military level grade parts do receive same level characterization as space level
- Characterization – all aspects of the device technology must be evaluated to ensure all failure mechanisms are known and understood, the process is well controlled, the long-term reliability of the product is established, radiation characteristics are identified, and overall parametric performance is well defined in terms of margins and areas of concern
  - Wafer Level Reliability (i.e., Electromigration, TDDB, Antifuse, etc.)
  - Failure Modes Effects Analysis – evaluation of all potential failure modes and the impacts
  - Physics of Failure approach
  - Process variability analysis
  - Wafer Lot Acceptance
  - Long Term Reliability Testing
- Qualification
  - Standard mil-spec tests

New technology must be completely evaluated for space utilization

Summary

- The management of PMP activities at the contractors is a critical task that requires personnel with expertise in many areas
- PMP tasks establish the heart of the system reliability based upon part selection, procurement and testing
- The military parts are divided into many classes for different applications
- A major part of PMP management is to understand the nuances of the classes and select the "best" part for the application and balance reliability, cost and schedule for the program
- Hybrids continue to be a major source of problems and must be evaluated in detail

PMP management is critical to ensure long term system reliability

Other Flows

QML Hybrid IC Class D, E, G, H and K Screening

	Class H - General Military/Avionics					
	Class K - Space					
	Class G - Meets Class H Tests & Inspections except incoming. Conformance Inspection guarante					
	by supplier					
	Class E - Meets Class K, H or G with some exceptions defined in SCD					
	Class D - Built and tested to manufacturers flow (commercial)					
	SCREEN	**CLASS H**	**CLASS K**	**CLASS E**	**CLASS D**	**CLASS G**
1	Element Evaluation	Required Each lot of elements (minimal testing)	Required Each lot of elements (extensive testing including 1000 hr. life test	Same as H or K as applicable	Manufacturer specified	Same as Class H
2	Pre-seal Burn-in	Optional	Optional	Same as H or K as applicable	Manufacturer specified	Same as Class H
3	Non-destructive Bond Pull	Not Required	Req'd 100%	Same as H or K as applicable	Manufacturer specified	Same as Class H
4	Internal Visual	Req'd 100%	Req'd 100%	Same as H or K as applicable	Manufacturer specified	Same as Class H
		Condition H	Condition K	Same as H or K as applicable	Manufacturer specified	Same as Class H
5	Temperature Cycling, 10 cyc	Req'd 100%, Cond C	Req'd 100%, Cond C	Same as H or K as applicable	Manufacturer specified	Same as Class H
6	Constant Acceleration	Req'd 100%, Y1, 3000 Gs	Req'd 100%, Y1, 3000 Gs	Same as H or K as applicable	Manufacturer specified	Same as Class H

QML Hybrid IC Class D, E, G, H and K Screening (Cont.)

	SCREEN	CLASS H	CLASS K	CLASS E	CLASS D	CLASS G
7	Particle Impact Noise Detection (PIND)	Not Req'd	Req'd 100% per 883/2020 Cond A	Same as H or K as applic.	Manufacturer Specified	Same as Class H
8	Serialization	Not Req'd	Req'd 100%	Same as H or K as applic.	Manufacturer Specified	Same as Class H
9	Pre-burn-in Electrical per SMD or SCD	Optional	Req'd 100%	Same as H or K as applic.	Manufacturer Specified	Same as Class H
10	Burn-in per 883/Method 1015	Req'd 100%, 125˚C, 160 hrs.	Req'd 100%, 125˚C 320 hrs.	Same as H or K as applic.	Manufacturer Specified	Same as Class H
11	Final Electrical per SMD or SCD	Req'd 100%,	Req'd 100% Read & Record	Same as H or K as applic.	Manufacturer Specified	Same as Class H
12	Percent Defective Allowable (PDA)	Req'd 10% or 1 device whichever is greater	Req'd 2% or l device whichever is greater	Same as H or K as applic.	Manufacturer Specified	Same as Class H
13	Seal (Fine & Gross)	Req'd 100%	Req'd 100%	Same as H or K as applic.	Manufacturer Specified	Same as Class H
14	X-ray	Not Req'd	Req'd 100%	Same as H or K as applic.	Manufacturer Specified	Same as Class H
15	External Visual	Req'd 100%	Req'd 100%	Same as H or K as applic.	Manufacturer Specified	Same as Class H
16	Radiation*	Optional	Optional	Same as H or K as applic.	Manufacturer Specified	Same as Class H

* Determined by manufacturer whether radiation testing is performed at element, hybrid level or both

QML Hybrid IC Class D, E, G, H and K Screening Quality Conformance Test (In-line or End of Line Options)

	GROUP	CLASS H	CLASS K	CLASS E	CLASS D	CLASS G
1	Group A (electrical) (every lot)	Required Sample Basis	Required Sample Basis	Same as H or K as Applicable	Manufacturer Specified	Same as Class H (Guaranteed but may not be tested)
2	Group B (every lot)	Phy Dimensions Solderability Bond Strength Resistance to Solv InternVisual/Mech Die shear	Phy Dimensions Resis to Solvents Int Visual/Mech Bond Strength Die Shear Solderability Seal	Same as H or K as Applicable	Manufacturer Specified	Same as Class H (Guaranteed but may not be tested)
3	Group C (once for qual and only w hen design or process changes)	Resistance to Soldering Heat External Visual PIND Temp Cycle Mech Shock/Accel Random Vib Seal PIND Visual Electrical Life Test Int Water Vapor Internal Visual Wire Bond Strenth Element Shear ESD	Resistance to Soldering Heat External Visual PIND Temp Cycle Mech Shock/Accel Random Vib Seal PIND Visual Electrical Life Test Internal Water Vapor Internal Visual Wire Bond Strenth Element Shear ESD	Same as H or K as Applicable	Manufacturer Specified	Same as Class H (Guaranteed but may not be tested)

QML Hybrid IC Class D, E, G, H and K Screening Quality Conformance Test (In-line or End of Line Options)

	GROUP	CLASS H	CLASS K	CLASS E	CLASS D	CLASS G
4	Group D (package related) (once for qual and every 6 months)	Thermal Shock Stabilization bake Lead Integrity Seal Salt Atmosphere Metal Pkg Isolation	Thermal Shock Stabilization bake Lead Integrity Seal Salt Atmosphere Metal Pkg Isolation	Same as H or K as Applicable	Manufacturer Specified	Same as Class H (Guaranteed but may not be tested)

QML Discrete Device JAN, JANTX, JANTXV, JANS and JANJ Screening

	SCREEN	JANS	JAN TXV	JAN TX	JAN J	JAN*	Rationale for Test
1	Internal Visual	Required 100%	Required 100%	Not Applicable	Required	*	Eliminate potential visual failures
2	Stabilization Bake	Optional	Optional	Optional	Optional	*	High temperature bake to stabilize process paramters
3	Temp Cycle 20 cycles	Required 100%	Required 100%	Required 100%	Required 100%	*	Eliminate marginal wire bonds and die attach
4	Surge	Required 100%	Required 100%	Required 100%	Required 100%	*	Eliminate marginal electrical devices
5	Thermal Impedance	Required 100%	Required 100%	Required 100%	Required 100%	*	Measure thermal impedance of actual devices
6	Constant Acceleration	Required 100%,Y1 20,000G	Optional	Optional	Optional	*	Weeds out marginal die attach devices
7	PIND, Cond A	Required 100%	Not Applicable	Not Applicable	Required 100%	*	Eliminates loose particles that can cause failure
8	Instability Shock (Axial Lead Diodes)	Required 100%	Not Applicable	Not Applicable	Not Applicable	*	Detect any semiconductor device discontinuity "ringing" or shifting of the forward dc voltage characteristic monitored during shock.
9	Seal	Optional	Optional	Optional	Optional	*	Eliminates marginal seals
10	Serialization	Required 100%	Not Applicable	Not Applicable	Not Applicable	*	Ability to record measurements

* JAN devices are not screened. They are manufactured on a certified line.

QML Discrete Device JAN, JANTX, JANTXV, JANS and JANJ Screening

	SCREEN	JANS	JAN TXV	JAN TX	JAN J	* JAN	Rationale for Test
11	Interim Electrical	Required 100%	Not Applicable	Not Applicable	Required 100%	*	Provides measured performance values to determine marginal devices
12	High Temp Reverse Bias	Required 48 hrs min	Required 48 hrs min	Required 48 hrs min	Required 48 hrs min	*	Stresses devices to look for ionic mobile contamination failure mechanisms
13	Interim Electrical & Deltas	Required 100%	Required 100%	Required 100%	Required 100%	*	Provides measured performance values to determine marginal devices
14	Burn-In	Required 100%	Required 100%	Required 100%	Required 100%	*	Sresses device to weed out marginal devices based on failure mechanisms of technology
15	Final Electrical	Required Subgp 2 & 3	Required Subgp 2	Required Subgp 2	Required Subgp 2 & 3	*	Provides measured performance values to determine marginal devices
		Deltas	Deltas	Deltas	Deltas	*	Provides measurement of stability performance
16	Seal	Required	Required	Required	Required	*	Weeds out marginal devices based on seal issues
17	Radiography	Required	Not Applicable	Not Applicable	Required	*	Provides evaluation of bond issues, seal issues and foreign material
18	External Visual	Required	Not Applicable	Not Applicable	Required	*	Weeds out devices visually with issues such as bent or broken leads, contaminatioin, etc
19	Case Isolation	Required 100%	Required 100%	Required 100%	Required 100%	*	Weeds out marginal case isolation on packages
	* JAN devices do not see screen test. Built on a certified line.						

QML Discrete Device JAN, JANTX, JANTXV, JANS and JANJ Quality Conformance Test

	GROUP	JANS	JAN TXV	JAN TX	JAN J	JAN*
1	Group A (electrical) sample basis	Required (every lot) 15/0	Required (every lot) 116/0	Required (every lot)	Required (every lot)	Required (every lot)
				45/0	15/0	45/0
2	Group B	(every lot)	(every lot)	(every lot)	(every lot)	(every lot)
	sample basis	Phy Dimensions	Solderability	Same as TXV	Same as TXV	Same as TXV
		Solderability	Resis to Solvents			
		Resistance to Solv	Temp Cycle			
		Temp Cycle	Thermal Schock			
		Thermal Shock	Surge			
		Surge	Seal			
		Seal	Electrical			
		Electrical	Op Life/Electrical			
		Decap-Internal Vis	Bond Strength			
		Bond Strength	Decap-Internal Vis			
		SEM	Thermal Resistance			
		Die Shear	High Temp Life (non-op)			
		Intermittent Op Life	Electrical			
		Seal/Electrical				
		Acelerated Op Life/Electrical				

QML Discrete Device JAN, JANTX, JANTXV, JANS and JANJ Quality Conformance Test

	GROUP	JANS	JAN TXV	JAN TX	JAN J	JAN*
3	Group C		Physical Dimensio	Same as TXV	Same as TXV	Same as TXV
	(once per year for all classes)	Thermal Shock	Thermal Shock			
		Terminal Strength	Terminal Strength			
		Temperature Cycle	Temperature Cycle			
		Seal	Seal			
		Moisture Resistance	Moisture Resistance			
		Electrical	Electrical			
		Shock	Shock			
		Vibration	Vibration			
		Constant Accel	Constant Accel			
		Electrical	Electrical			
		Salt Atm	Salt Atm			
		Thermal Resistance	Thermal Resistance			
		Op Life/Seal/Electrical	Op Life			
		IGA	IGA			
4	Group D (radiation)	As Required	As Required	Not Applicable	As Required	Not Applicable

QML Discrete Device JAN, JANTX, JANTXV, JANS and JANJ Quality Conformance Test

	GROUP	JANS	JAN TXV	JAN TX	JAN J	JAN*
5	Group E	Thermal Shock or	Same as JAN S	Same as JAN	Same as JAN S	Same as JAN S
	Qual only for all classes	Temp Cycle				
		Life Test				
		DPA				
		Thermal Resistance				
		Barometric Pressure				
		ESD				
		Resistance to Sold Heat				
		Visual				
		Seal Electrical				
		Reverse Stability				
		Resistance to Glass				
		Cracking				

Concluding Comments

- JEDEC JC13 and SAE CE-11 / 12 are as effective as we want them to be. Inputs from user community is very important. We need your active participation in various sub-committees. It is valuable

- We would appreciate your inputs on this tutorial – please tell us what worked and what did not work.

- Please feel free to contact us anytime for any questions related to Mil Stds, SAE and JEDEC JC13 workings or any parts / component engineering related questions. Our emails are on page 1 of this tutorial

Thank You