Microelectronic Component Engineering Principles and Practices

April 29, 2025
Los Angeles, California

Instructors:

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Opening Remarks

Welcome

Instructor's Background

Scope / Objectives

Student Introductions

Review Course Outline

Soft Copy of all the Presentations

TUTORIAL #1
MICROELECTRONIC COMPONENT ENGINEERING PRINCIPLES and PRACTICES
PRESENTATION NOTES

PASSWORD: *CMSE-2025T*

https://www.tjgreenllc.com/cmse2025resourcestutorials/
Password: CMSE-2025T
Plus Tutorials Password: CMSE-2025T

Todays Agenda

0800-0815 *Welcome, intro, logistics and review agenda*

0815-0930 Ron Demcko …..Overview of Component Engineering

0930-1000 Coffee Break

1000-1100 Brian Ward……*Tantalum Capacitors*

1100-1200 Ron Demcko ……Electrolytics, *Ceramic, Film, Stacked Caps and SuperCaps*

Lunch (1200-1300)

1300-1415 Tom Green…… *Microelectronics Materials and Processes*

Coffee Break

1420-1530 Trevor Devaney… DPA, failure modes mechanisms

1600-1730 Understanding the Military Standards and Update on JEDEC and New Spec Initiatives (**International Ballroom**)

Todays Agenda

1730 - 1900

STUDENT/PROFESSIONAL NETWORKING RECEPTION

This is an opportunity for students and young professionals to interact with industry professionals actively working in the field of microelectronics. Come out and enjoy some drinks and hors d'oeuvres and learn about component engineering and exciting career opportunities in the aerospace industry.

Must Register To Attend - Register Free Here

This event is free for students, young professionals & conference attendees

SPONSORED BY:

Hi-Rel Laboratories

Back in this room MALIBU Please join us

Mil Specs and JEDEC Presentation (Tonight's Agenda)

Class time (1600-1730 hrs)

COURSE SUMMARY

The course will outline the basics of various military standards as it applies to EEE devices and what topics JEDEC JC-13, CE-12 and CE-11 are currently addressing. The course will also provide the current status of various standards on such items as PEMs, Derating, Advanced Technology, GaN and other initiatives.

1. Basics of MIL STDs and MIL PRFs for Microcircuits, Hybrids and Semiconductor
2. Workings of SAE CE-12/CE-11 and JEDEC JC13
3. What is the committee working on now from standards perspective
    a. PEMs
    b. Radiation
    c. GaN
    d. Advanced Technology Microcircuits
    e. COTs – Alternate grade
    f. Derating
    g. Long Term Storage
    h. IGA (Internal Gas Analysis)

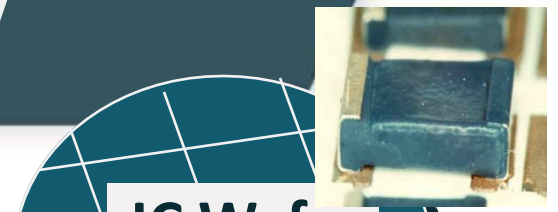
Course Goals and Objectives

- Learn about component engineering and the many hats required to succeed
- Understand capacitor technology
- Overview look at materials and processes used to assemble ICs and caps into a package aka Hybrids
- Learn the rationale for doing DPA (Destruct Physical Analysis) and see cool pics of component failures!
- Learn about our Military component specifications system and the latest committee work going on at JEDEC (later tonight so hang in there!)

Electronics' Packaging Hierarchy

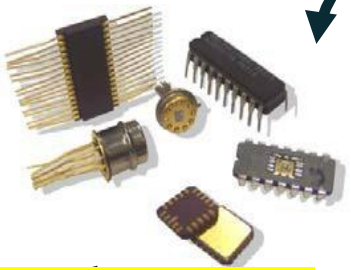
Microcircuit Packaging Levels:

Level I: Wafer Level (ICs and MMICs)
Level II: Hybrids, Monolithics Discrete ICs
Level III: Printed Circuit Board (PCBs)
Level IV: Black Box LRU
Level V: System

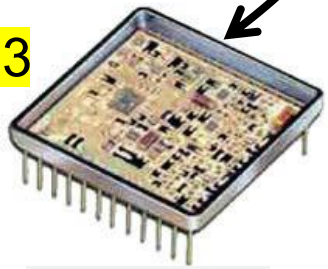


IC Wafer

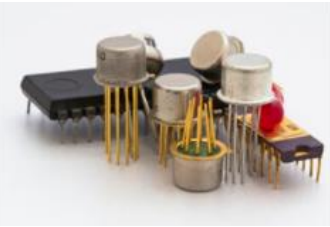
Monolithics



MIL-STD-883

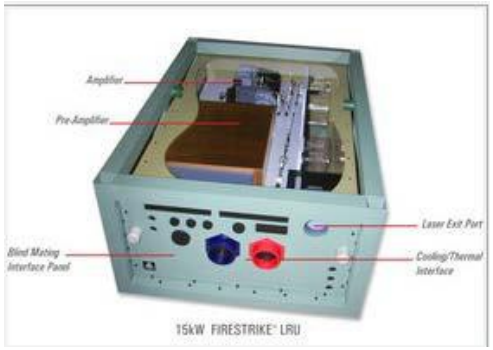


Hybrids



Discrete Semiconductors

MIL-STD-750



LRU

System Level

PWBs per IPC

MIL-STD-202

Performance Specs vs Mil Standards

Performance Specifications

General **Hybrid Spec** MIL-PRF-38534 FSC 5962
General Specification for Microcircuits MIL-PRF-38535 FSC 5962
General Specification for Semiconductor Devices MIL-PRF-19500 FSC 5961

Military Standards

Standard Test Methods for Microcircuits **MIL-STD-883L…NEW**
Standard Test Methods for Semiconductor Devices **MIL-STD-750**
This is the cousin of Mil-Std-883.

Performance Specs encourage and allow for alternate verification testing methods to meet performance requirements and foster ingenuity and growth within the supplier base . A result of the Perry Initiative of the mid 1990's

Mil Standards are rigid requirements …for Hybrids Test Methods in 883 and associated test conditions detail the exact testing required

Manny many parts are used in mil and space that do not fully qualify to these standards and we will be discussing "Alternate Grade" parts this week

How to Find the Latest Spec

DLA Link:

https://landandmaritimeapps.dla.mil/programs/milspec/

https://landandmaritimeapps.dla.mil/programs/milspec/DocSearch.aspx

Quick Assist Link

REVIEW HOW TO CHECK FOR DOCS AT DLA

This document and process conversion measures necessary to comply with this revision shall be completed by 03 June 2020

MIL-PRF-38534L
03 December 2019
SUPERSEDING
MIL-PRF-38534K
15 November 2017

PERFORMANCE SPECIFICATION

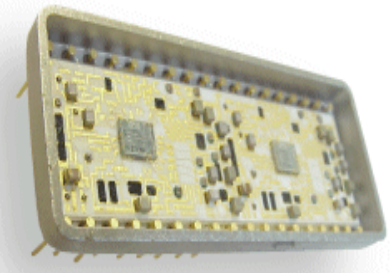
HYBRID MICROCIRCUITS,
GENERAL SPECIFICATION FOR

Defense Land and Maritime DLA

Office of Primary Involvement:	Hybrid Devices Branch (DLA LAND AND MARITIME-VQH)
Specification:	MIL-PRF-38534
Title:	Hybrid Microcircuits
Federal Supply Class (FSC):	5962 (Microcircuits, Electronic)

Hybrid Microcircuits, General Specification for
FSC: 5962

This specification establishes the general performance requirements for hybrid microcircuits, Multi-Chip Modules (MCM) and, similar devices and the verification requirements for ensuring that these devices meet the applicable performance requirements. Verification is accomplished through the use of one of two quality programs (Appendix A). The main body of this specification describes the performance requirements and the requirements for obtaining a Qualified Manufacturers List (QML) listing. The appendices of this specification are intended for guidance to aid a manufacturer in developing their verification program. Detail requirements, specific characteristics, and other provisions that are sensitive to the particular intended use should be specified in the applicable device acquisition specification.



Points of Contact:

MIL-PRF-38534 Group
Phone: 614-692-1081
Email: PRF38534@dla.mil

Listing of Hybrid QML Suppliers can be found at
www.landandmaritime.dla.mil (formerly known as DSCC Defense Supply Center Columbus OH)

QML List Hybrid QML Listing

Lab Suitability Listing Review DLA Links
https://landandmaritimeapps.dla.mil/offices/sourcing_and_qualification/labsuit.aspx

JEDEC Joint Electron Device Engineering Council

JEDEC Committee:

JC-13 Government Liaison

JC-13 is responsible for standardizing quality and reliability methodologies for solid state products used in military, space, and other environments requiring special-use condition capabilities beyond standard commercial practices. This includes long-term reliability and/or special screening requirements.Its purpose is to provide the member companies and their customers with uniform, cost-effective, proven, customer-accepted methodologies for specifying and evaluating special-use products, with the end goal of enhancing the performance and reliability of those products. Activities include the development, coordination, and maintenance of standards documents regarding product quality and reliability, validation systems, and process management.The committee also contributes to similar and related documents that are generated and maintained by other organizations. To accomplish this charter, the committee maintains liaisons with customers, other JEDEC committees, government agencies, and interested parties that have special application needs.

Subcommittees	
JC-13.1:	Discrete Devices
JC-13.2:	Microelectronic Devices
JC-13.4:	RadHard: Assurance-Characterization
JC-13.5:	Hybrid, RF/Microwave, and MCM Technology
JC-13.7:	New Electronic Device Technology

JEDEC Link: http://www.jedec.org/

Materials and Processes for Active Components

Hybrids, RF MMIC Modules, Monolithic and discrete devices

Basic manufacturing process flows and component ID

Wafer Fabrication Processes for ICs and MMICs

Substrate Manufacturing Technology
- Thin and thick film technology process fundamentals
- Laser trimming of resistors

Plating processes and industry specifications

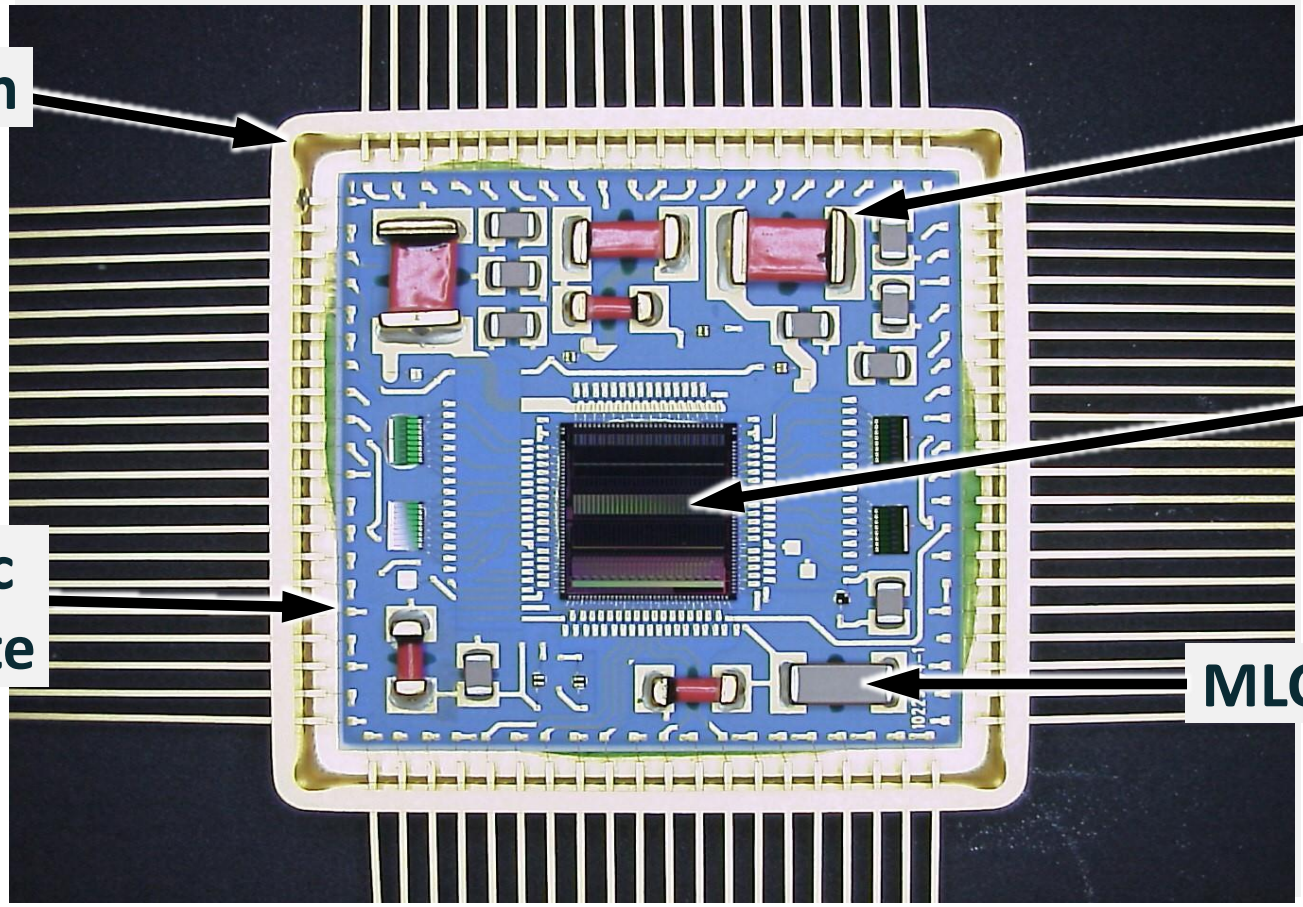
Material and Process Fundamentals for Component Attach
- Epoxy attach of substrates and ICs
- Eutectic soldering processes

Wirebonding and Interconnect Process Overview
- Ultrasonic/thermosonic bonding ball/wedge/ribbon bonding

Hermetic Packaging Process Overview and Test

Nom-Hermetic Packaging Options and testing

Hybrid Circuit (MIL-PRF-38534)



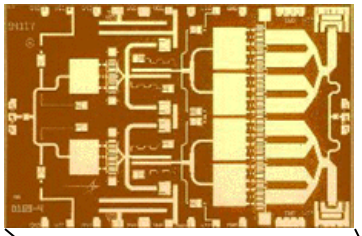
A Hybrid microcircuit contains two or more of a single type, or a combination of the following types of elements with at least one of the elements being active: Film microcircuit, Monolithic microcircuit, Semiconductor element, Passive chip or printed or deposited substrate elements.

MIL-PRF-38534

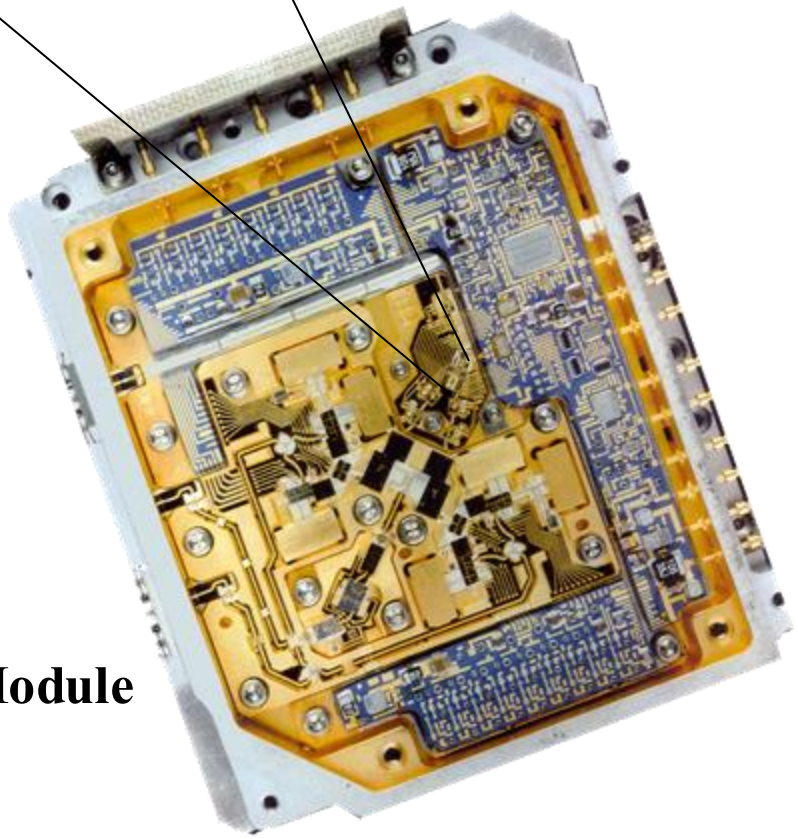
RF MMIC Modules

(Monolithic Microwave Integrated Circuit)

- **RF MMICs also known as microwave hybrids or "MIC" hybrids are very similar to conventional Hybrids in many ways, but operate at much higher frequencies and make use of gallium arsinde (GaAs) and gallium nitride (GaN) technology.**



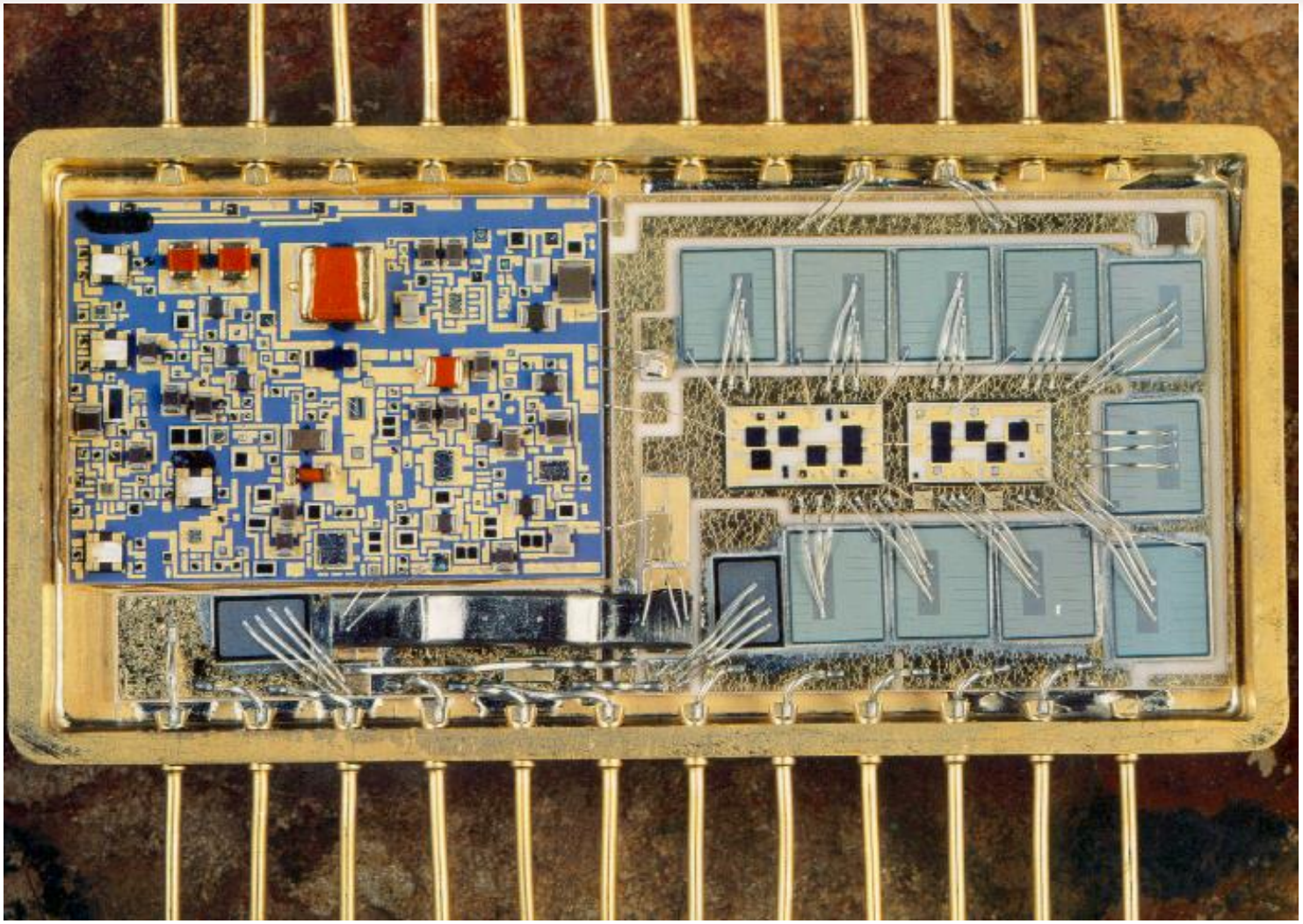
MMICs



RF MMIC Module

INSPECT PER TM 2017

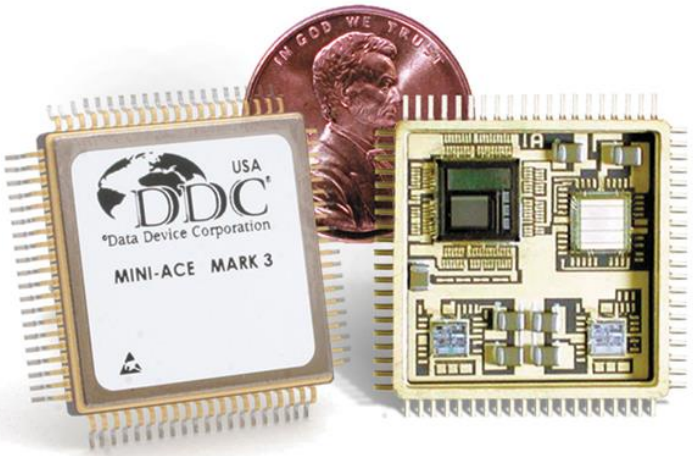
Power Hybrids

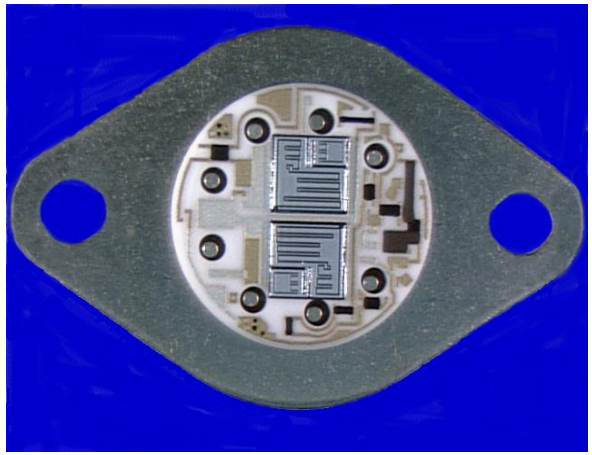


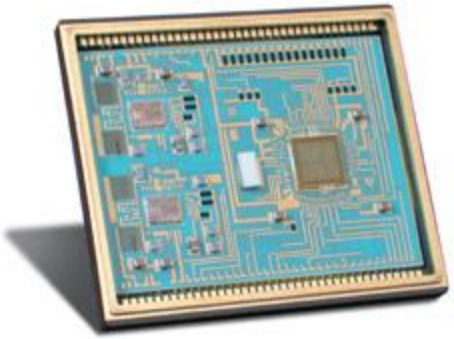
Hybrid Circuit (MIL-PRF-38534)

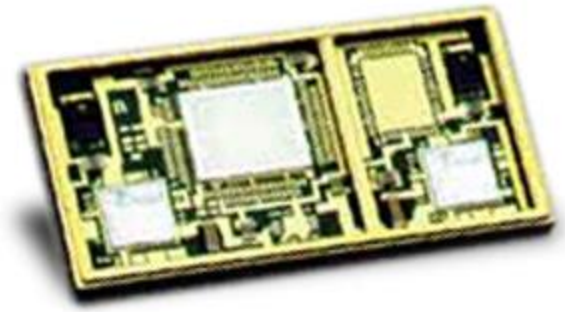
Ref: Teledyne Microelectronics

Typical Hybrids in Various Packages



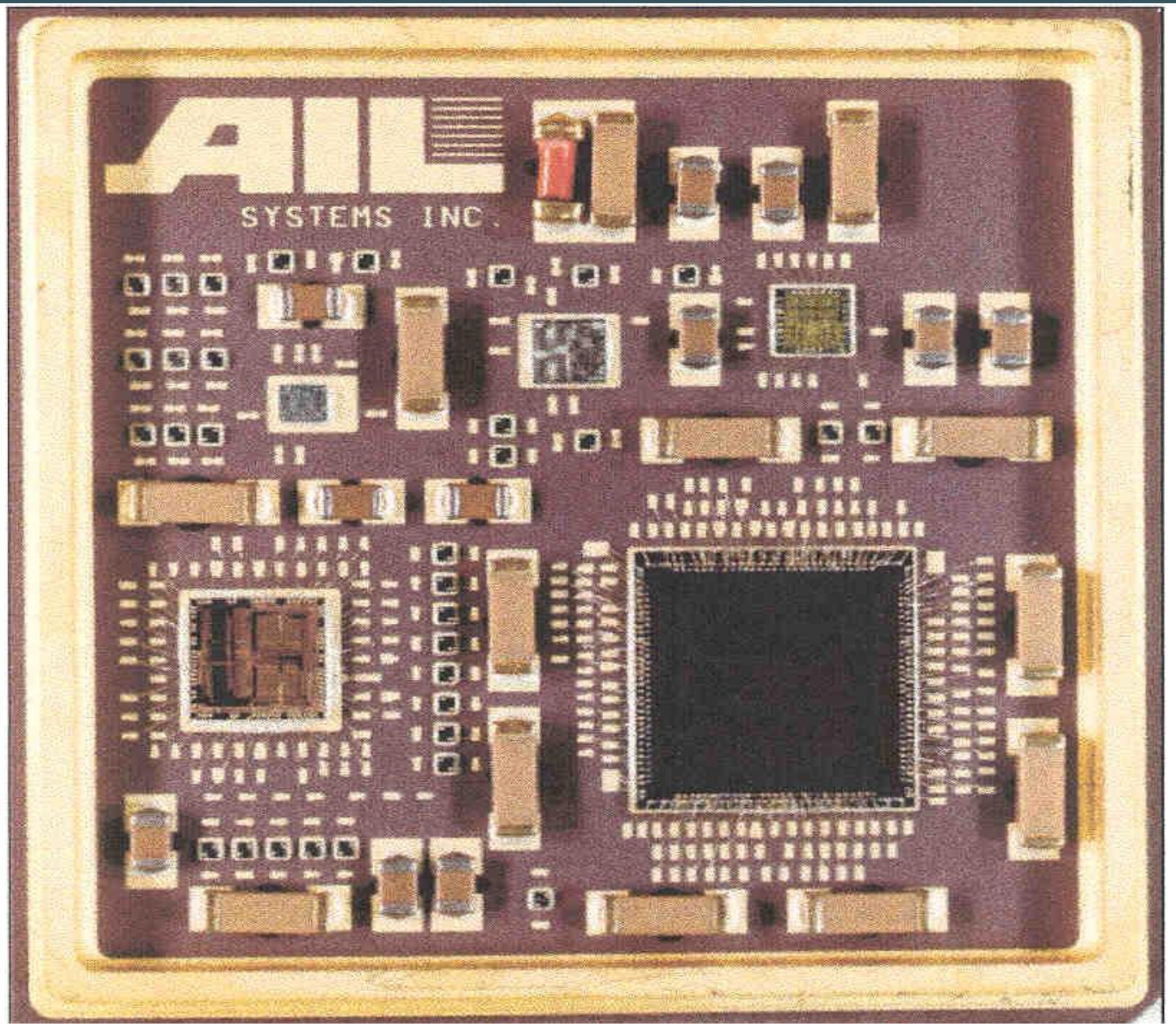






http://www.ddc-web.com/Products/MIL-STD-1553/Components.aspx

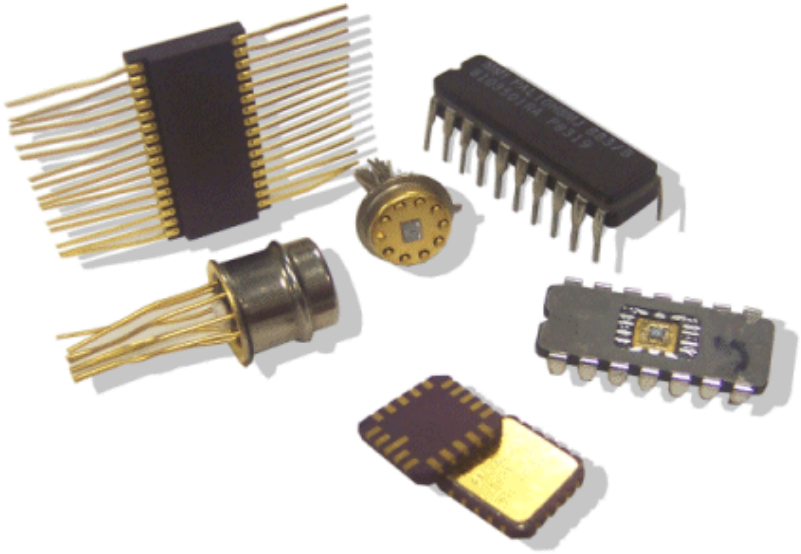
Ceramic MCM in a BGA Package



Monolithic Integrated Circuit (MIL-PRF-38535)

Single IC Chip in 32 Pin CERDIP

INSPECT PER TM 2010



DEFINITION

Monolithic microcircuit (or integrated circuit). A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate.

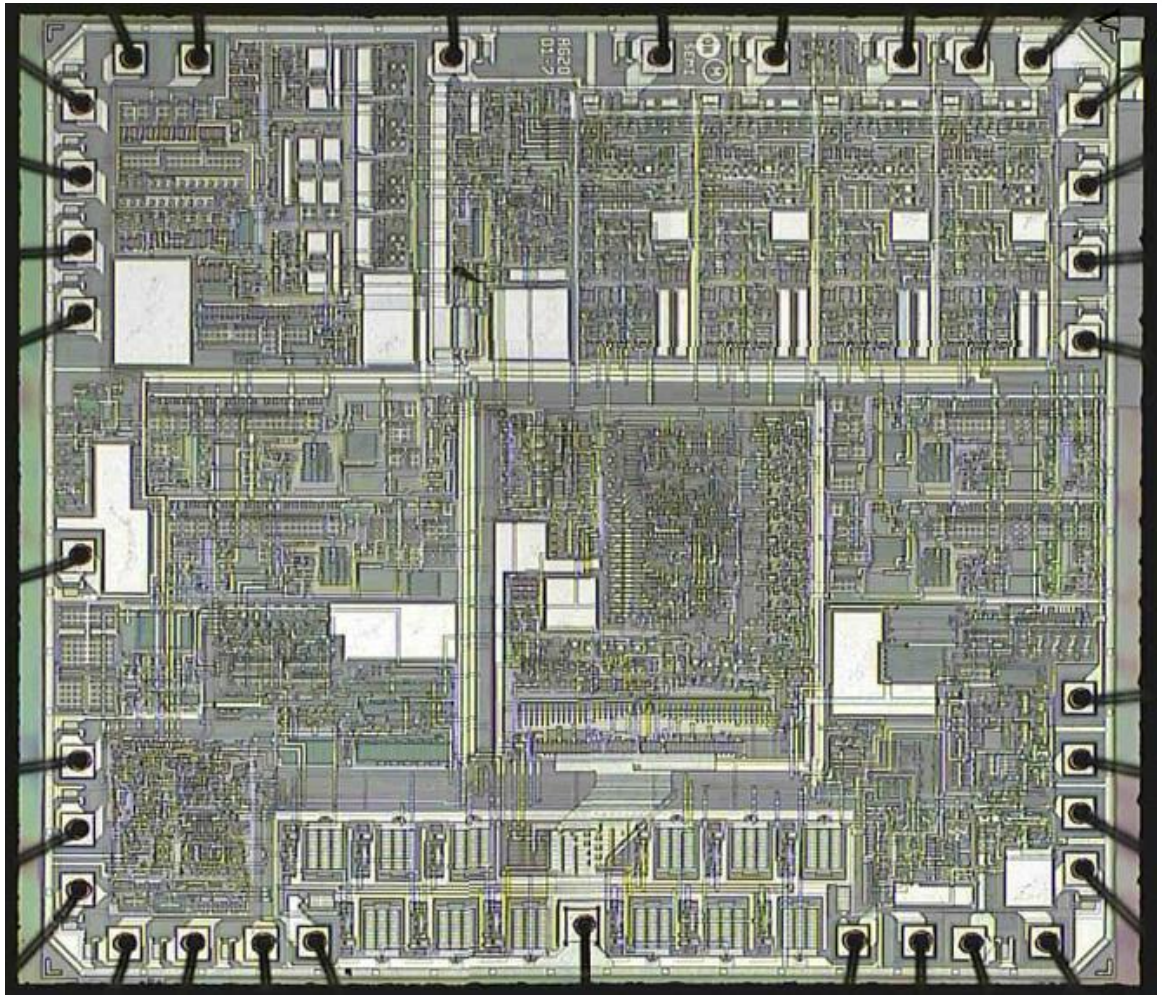
MIL-PRF-38535

Hermetic Cans ..all different shapes and sizes

Photo Courtesy of Tom Salzer

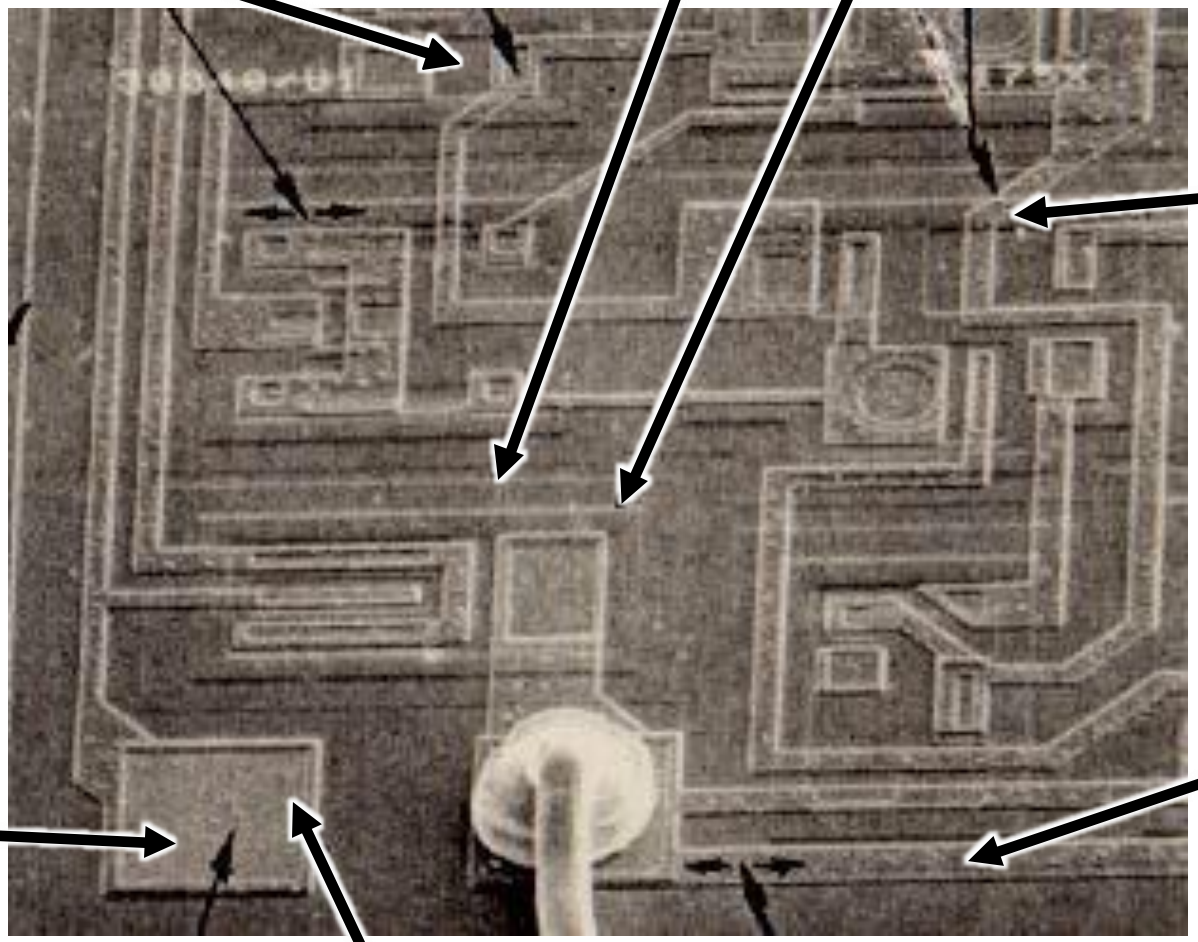
Older Silicon ICs

Many still used in Mil hardware



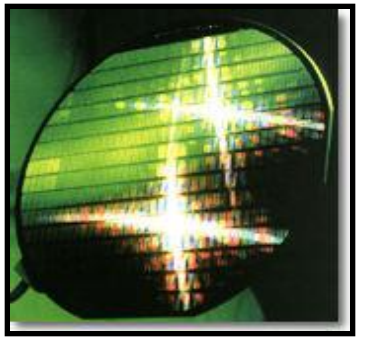
Silicon (not Silicone!) ICs (integrated circuit) are pervasive in military hardware. These chips have a glassivation on top to protect the sensitive Al metal runs except for the cutouts at the bond pads where the wire has to stick. They are densely packed with circuits and stand about 20 mils thick. Al wedge bonds or Au ball bonds interconnect these chips onto the substrate.

Silicon IC Device Features SEM Image



Silicon IC Wafer Terminology

SEMICONDUCTOR - A solid material with resistivity midway between that of a conductor and an insulator. Silicon, which comes from sand, is the most commonly used semiconductor.

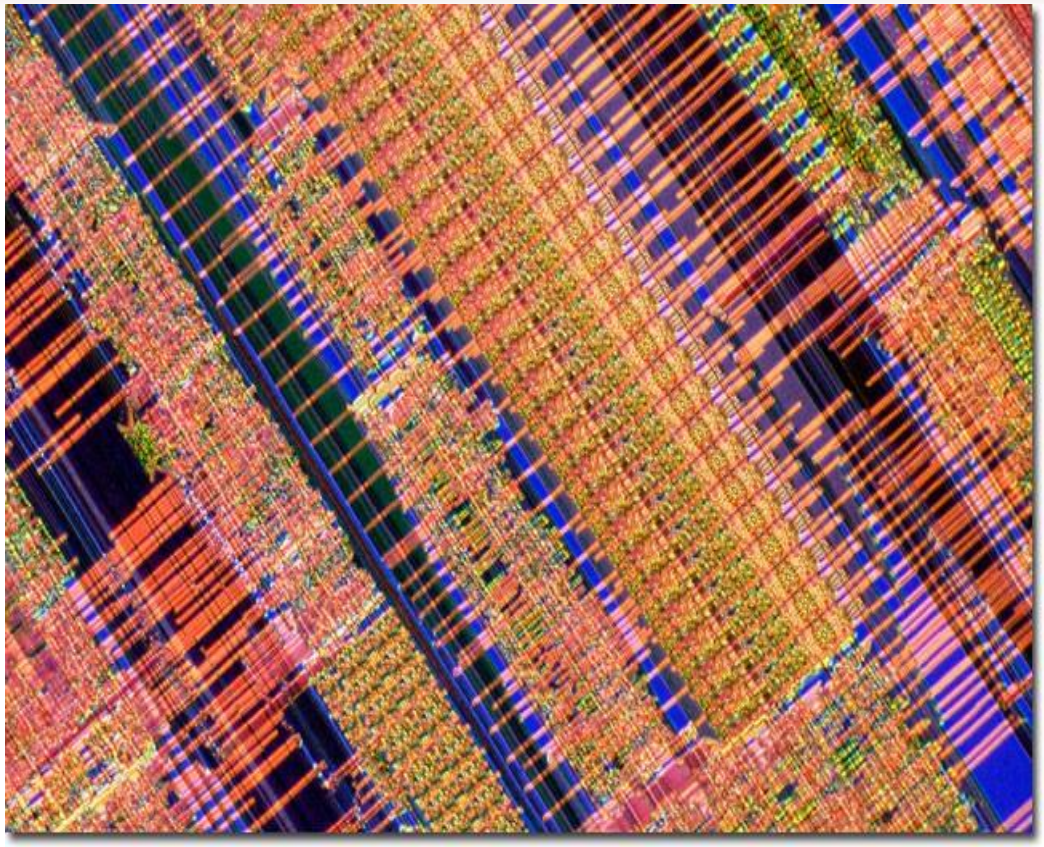


SILICON WAFER - A thin disk of silicon, up to 18 inches in diameter. Integrated circuits (ICs) are created on its mirror-shiny surface, then cut with diamond saws into individual chips.

- CHIP - A small piece of semiconducting material (usually silicon) on which an integrated circuit is embedded. A typical chip is less than 1 square inch and can contain millions of electronic components. Its purpose is to electronically process, store and move information.

- INTEGRATED CIRCUIT (IC) - Large numbers of integrated transistors and other circuit elements, which are built onto an individual chip to perform a particular function or task. i.e. memory chips, microprocessors etc.

IC under High Mag



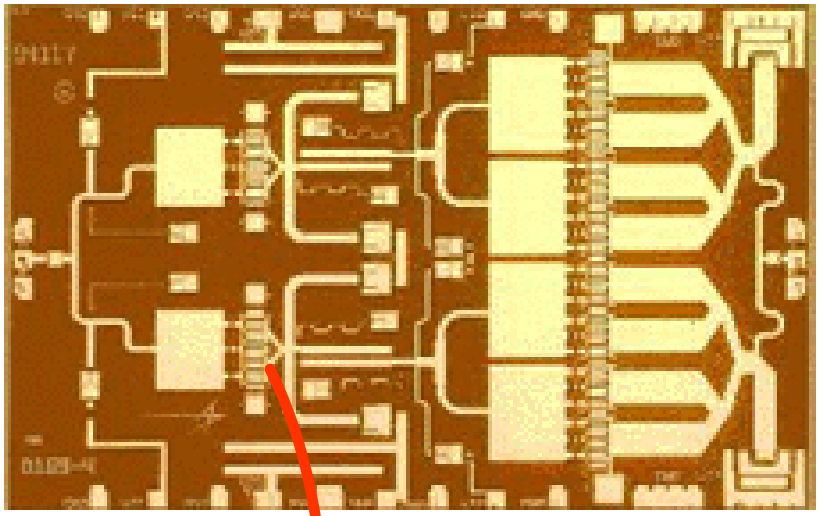
Modern day IC as seen through a high power microscope

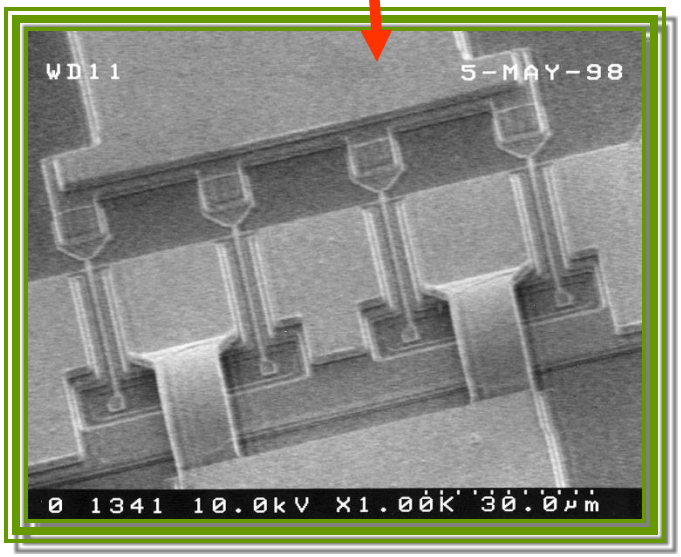
The various colors seen when inspecting and IC/MMICs are the result of light passing through the oxide (SiO_2) or silicon nitride and reflecting back to the optical receiver (aka your eye). There is a relationship between the color viewed and the thickness of this layer.

MMICs

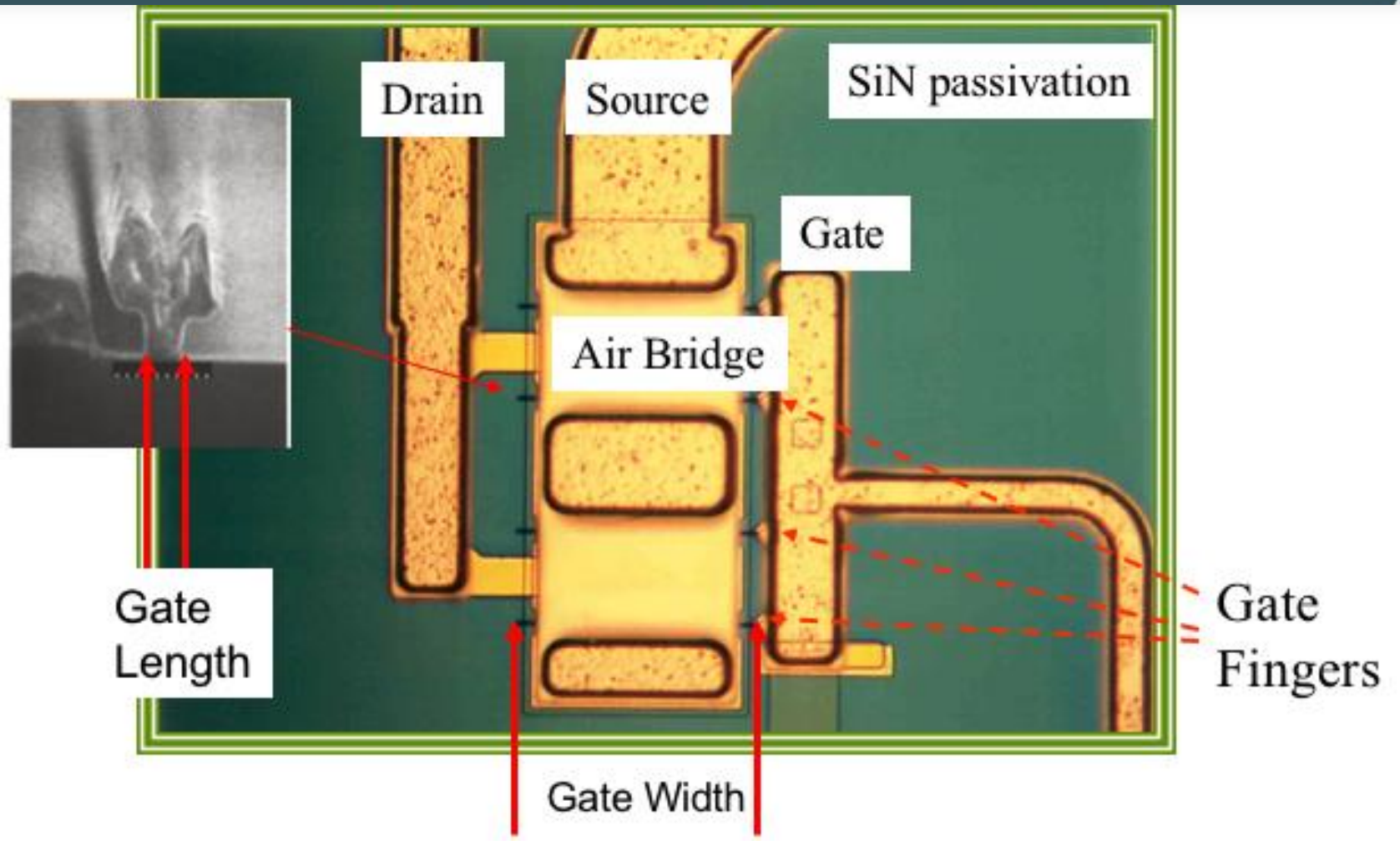
Inspect MMIC die surface per TM 2010 High Mag

MMIC (Monolithic Microwave Integrated Circuit) is a type of chip that's used in high frequency applications. In this case a compound semiconductor material GaAs (gallium arsenide) is used as the substrate upon which thin films are patterened and formed. These devices often contain delicate airbridged structures as shown on the right.



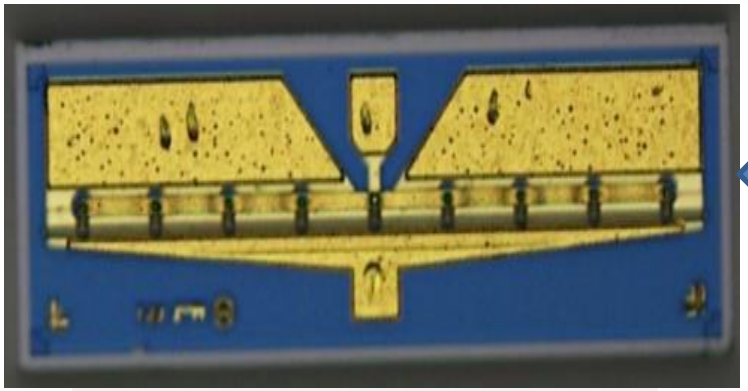


FET Features

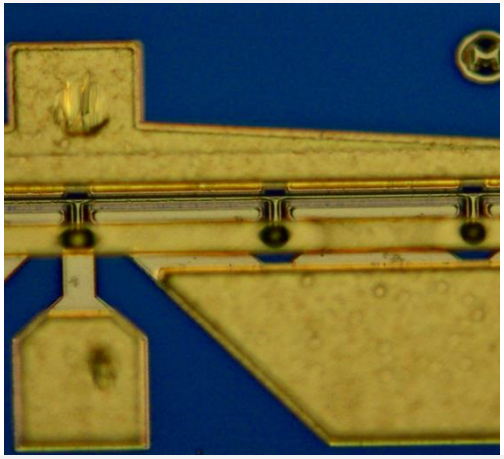


Gate Length …shorter gates operate at higher frequencies .25 microns ~ 60 GHz
Gate Width ….wider gates mean more DC and RF current, and therefore more power capability. Gate width must be sized appropriate to frequency

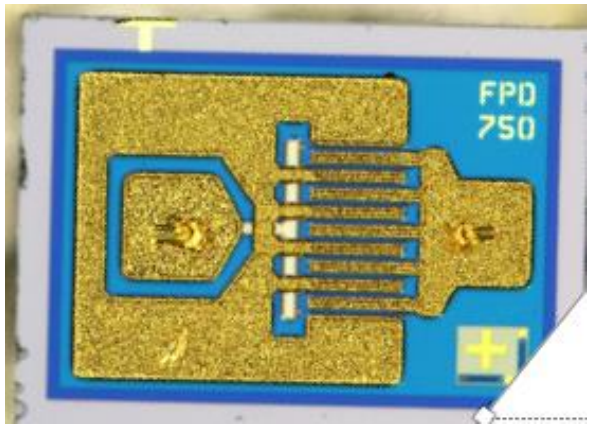
Discrete Microwave Devices
MIL-STD-750 TM 2070



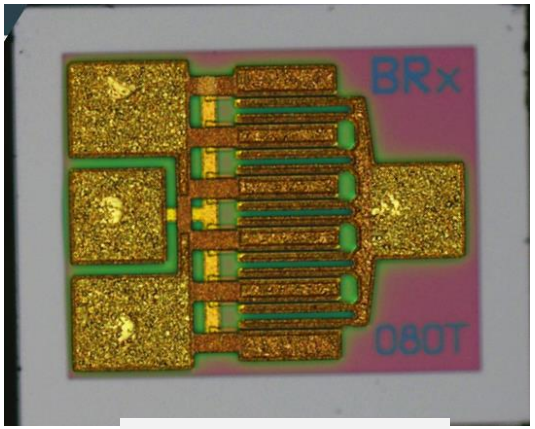
GaAs MESFET 100X



Enlarged Gate Area 500X



pHEMT

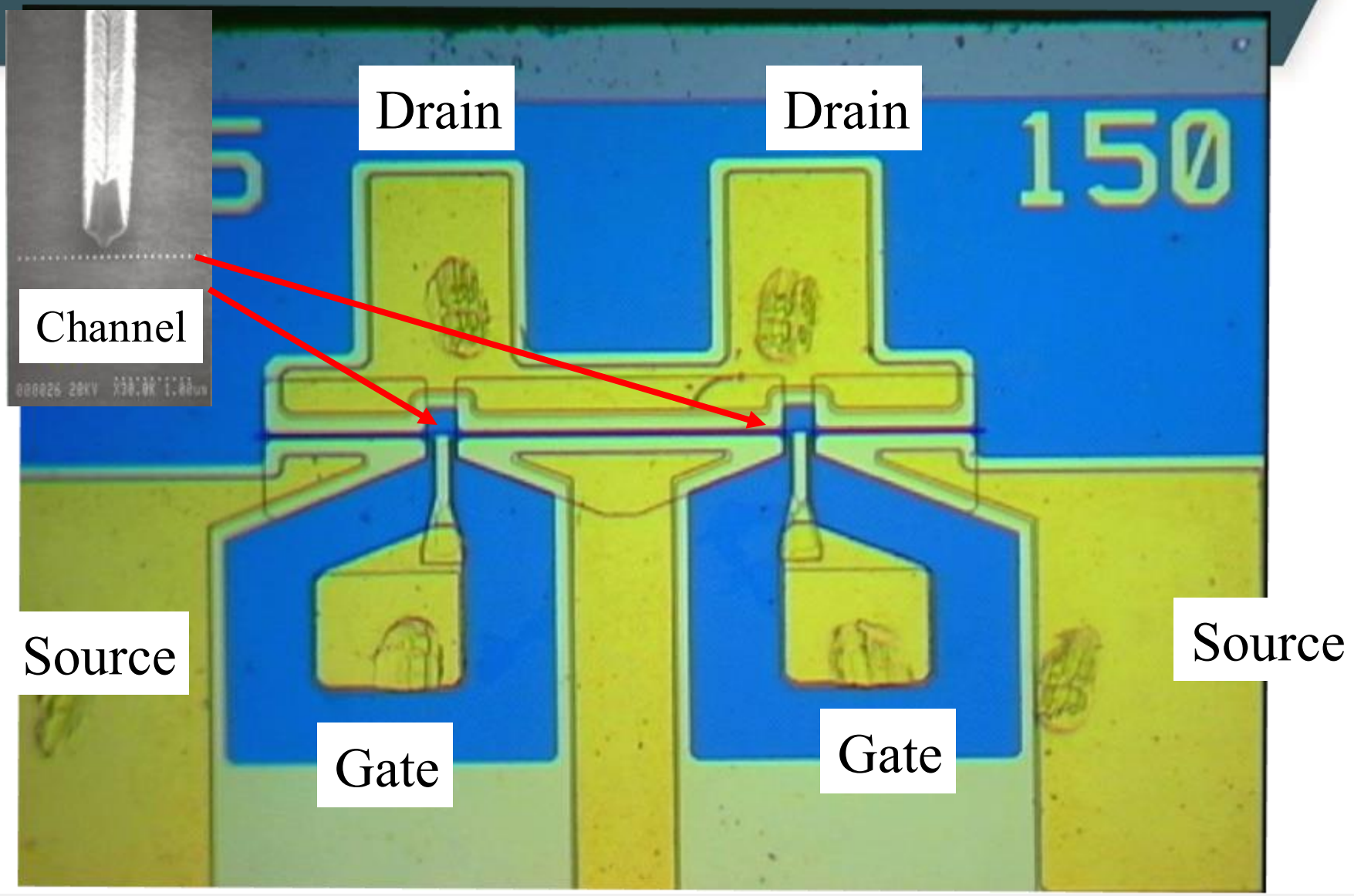


Power FET

pHEMPT (pseudomorphic High Electron Mobility Transistor)

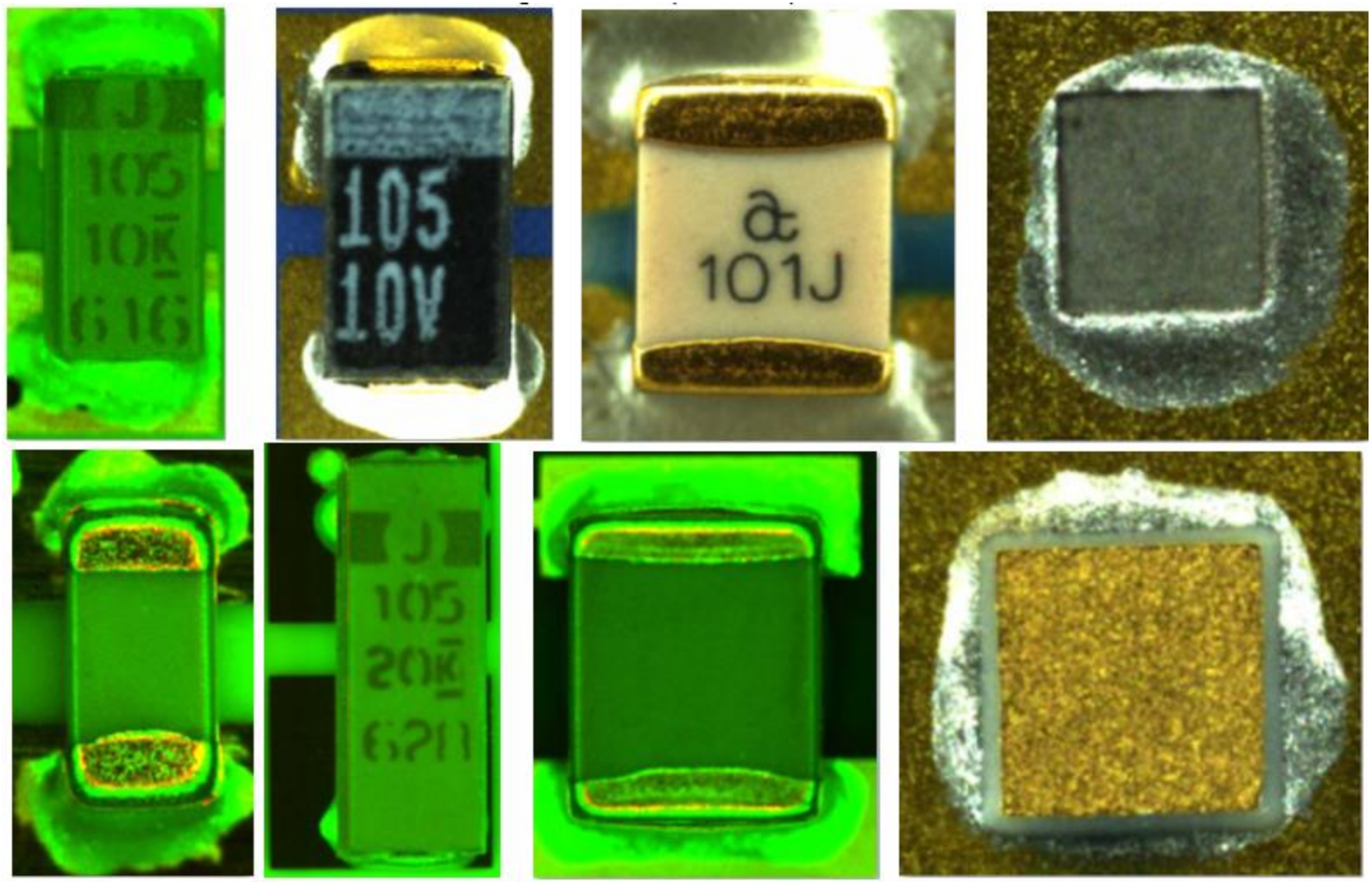
MESFET (metal–semiconductor field-effect transistor)

Dual Input FET



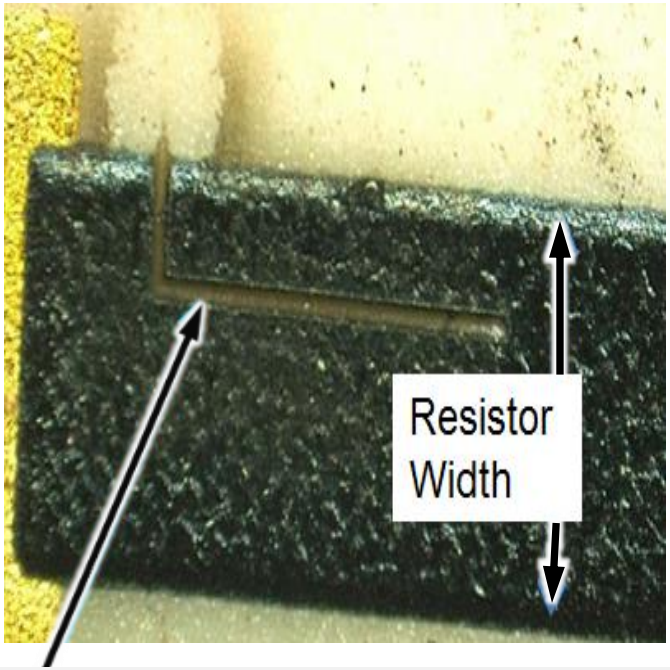
This is a discrete microwave FET (Field Effect Transistor). Note the probe marks on the bond pads. These are made at the end the wafer fab process to electrically test and sort the chips on the wafer.

Component ID:
Capacitors MIL-STD-883 TM 2032

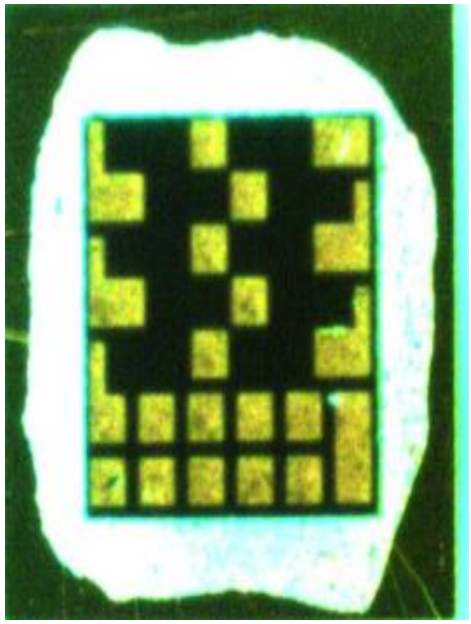


Capacitors are passive elements that store electrical energy. They come in a variety of shapes and sizes and the unit of measure is a Farad symbol F. Inspection criteria for these types of devices is found in TM 2032 para. 3.3. However, the epoxy attach criteria is found in TM 2017.

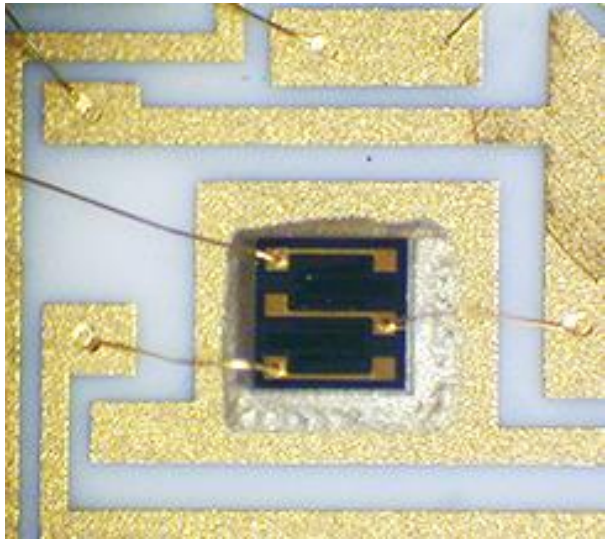
Component ID:
Resistors MIL-STD-883 TM 2032



Laser trimmed thick film resistor



Multi Tap Thin film resistor

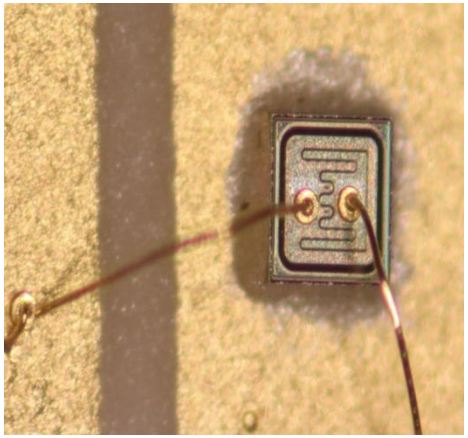


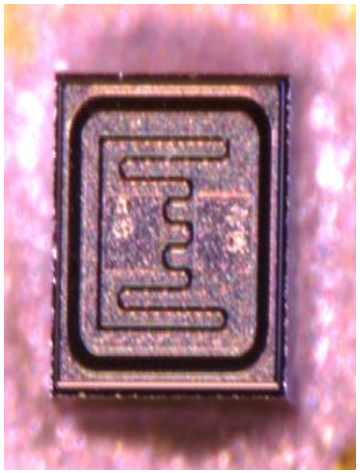
Select in test
Thin film resistor

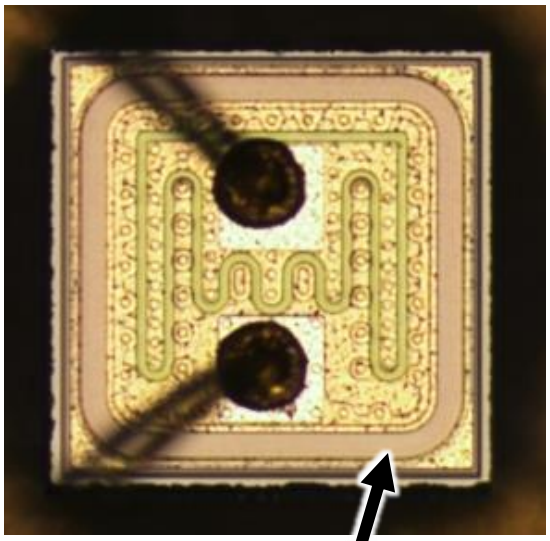
Visual inspection criteria for resistors is contained in TM 2032 . Section 3.1 Thin Film Resistors (100 to 200X) and Section 3.2 for Thick Film Resistors (10 to 60X).

As with the capacitors component attach and wirebond criteria is found in TM 2017.

Transistors
MIL-STD-750 TM 2072



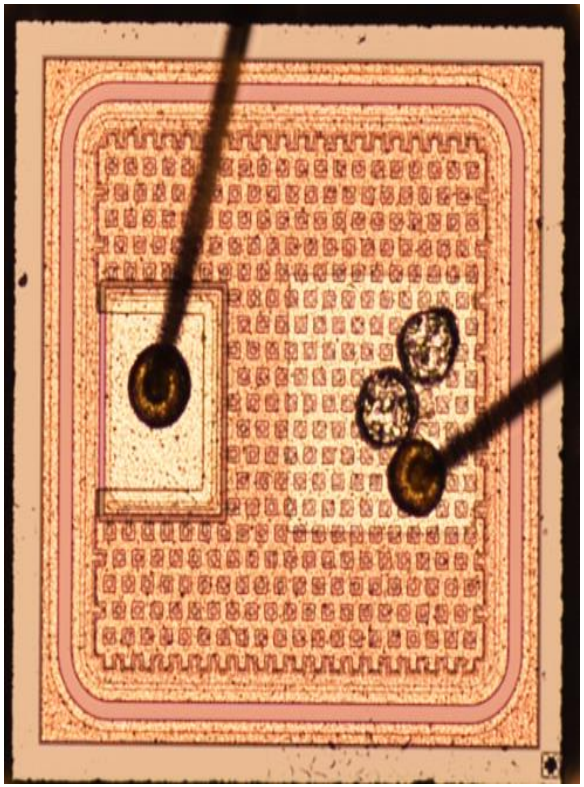


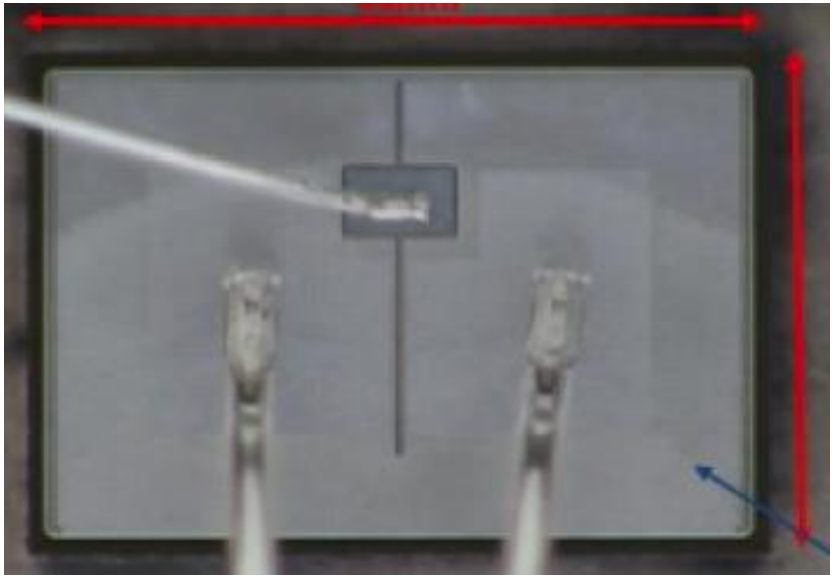


Guard Ring

Typical Bipolar NPN transistors with a diffused guard rind surrounding the active area. The guard ring is like a moat around the castle designed to protect the sensitive gate regions.
https://www.electronicshub.org/transistors-classification-and-types/

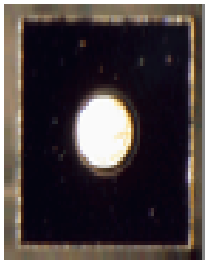
Power MOSFETS
MIL-STD-750 TM 2069

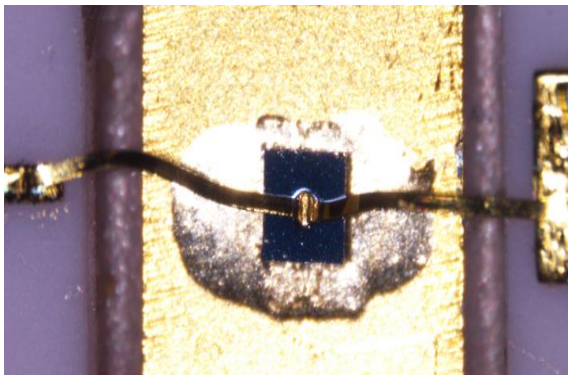
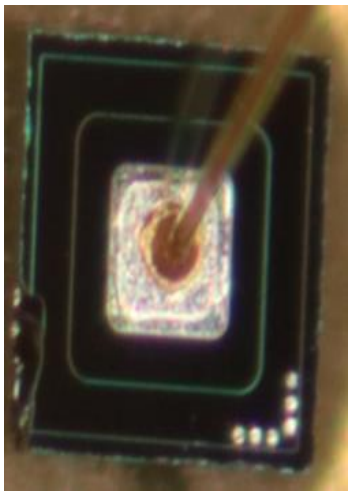


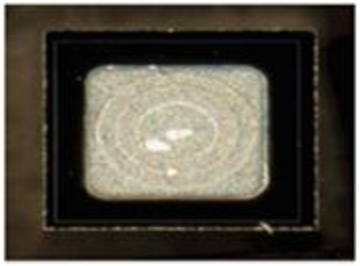


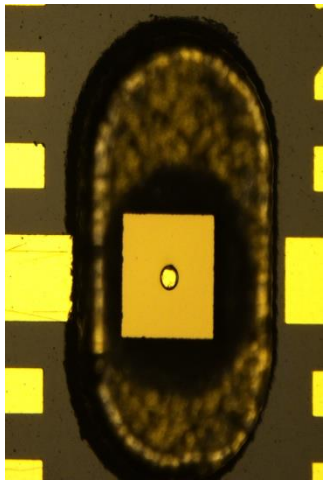
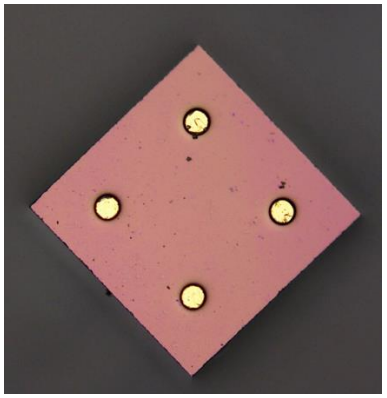
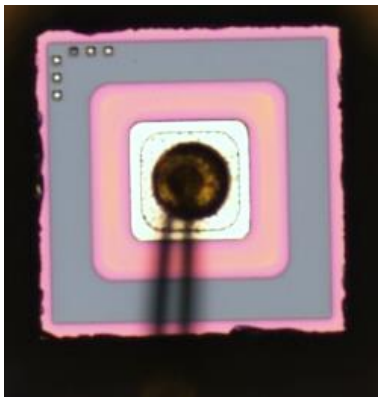
MOSFET in a TO 3 Package

Semiconductor Diode Inspection
MIL-STD-750 TM 2073



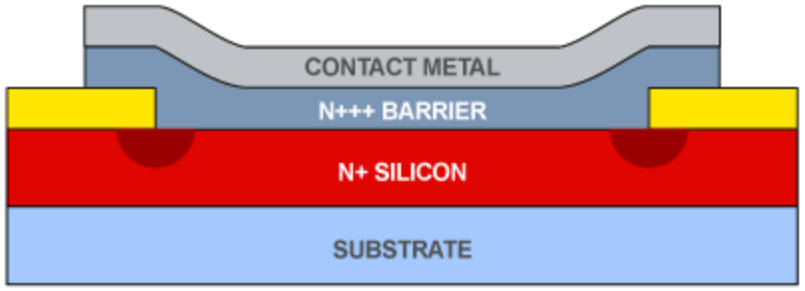


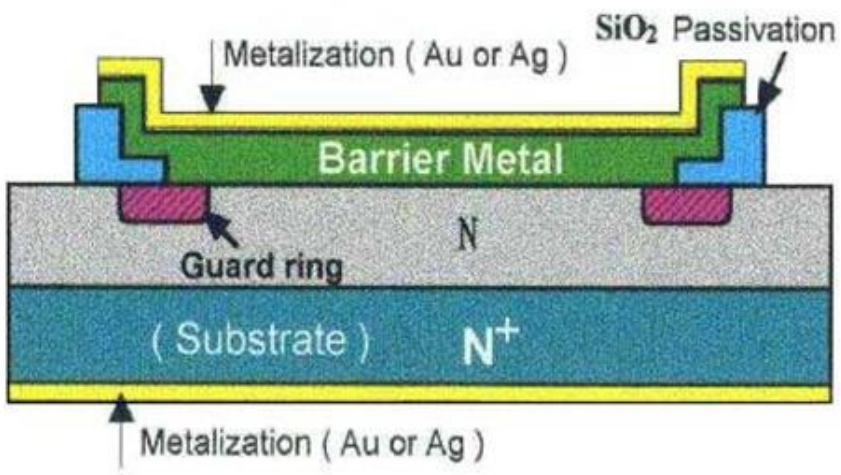




A semiconductor diode is a crystalline piece of semiconductor material with a p–n junction connected to two electrical terminals. A wirebond is generally placed on top and the backside of the device is the other connection. The flow of electrons is limited in one direction. There are many different types of diodes.

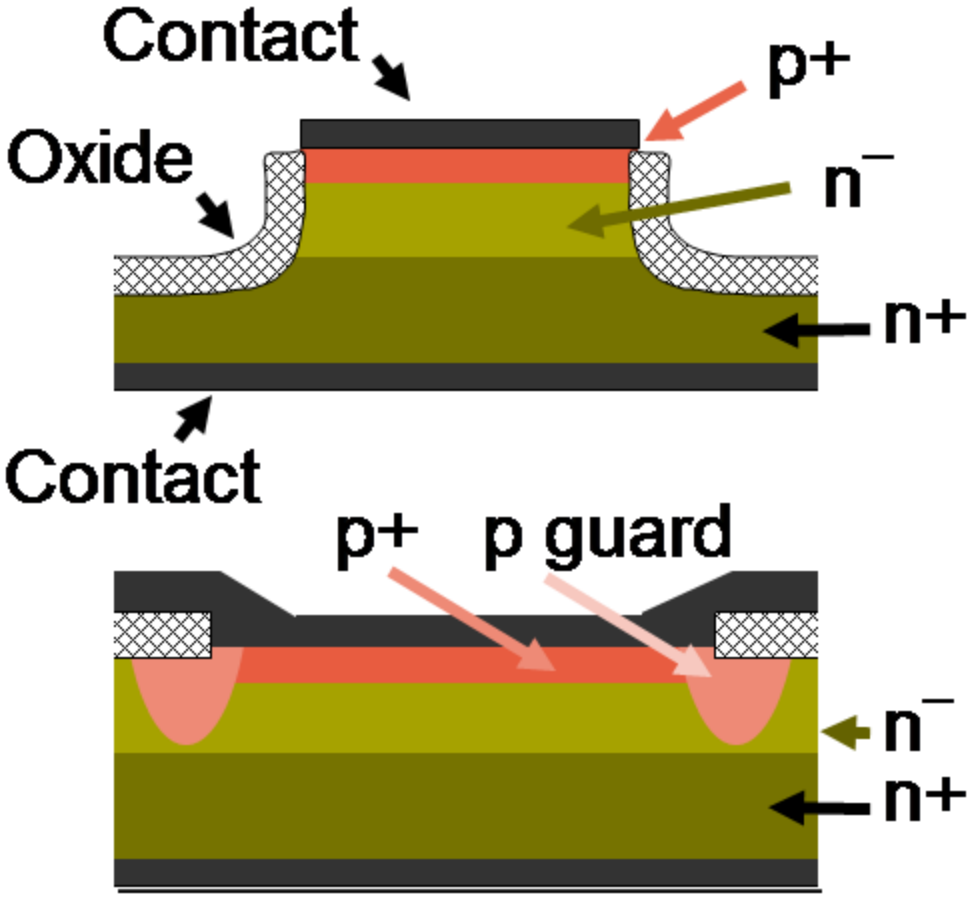
Planar Diodes (TM 2073)

A **p–n diode** semiconductor conducts current in only one direction





Schottky diode (top) with guard-ring (bottom).



Mesa diode structure (top) and planar diode structure with guard-ring (bottom).

Basic Microelectronics Processes

- *Wafer Fab Processes (Silicon and GaAs, SiC, GaN)*
- *Substrate Manufacturing*
  - *Ceramic (Thin and Thick film),*
  - *Laminate PWBs multilayers...Teflon boards (soft boards)*
- *Die/Component placement and attach*
  - *epoxies and solders*
- *Interconnect Processes*
  - *wirebond... flip chip*
- *Cleaning Processes… plasma, wet chemicals*
- *Packaging Processes*
  - *Plastic encapsulation... glob top, dam and fill*
  - *Hermetic enclosures*
- *Test…. at temperature -55C to 125C*

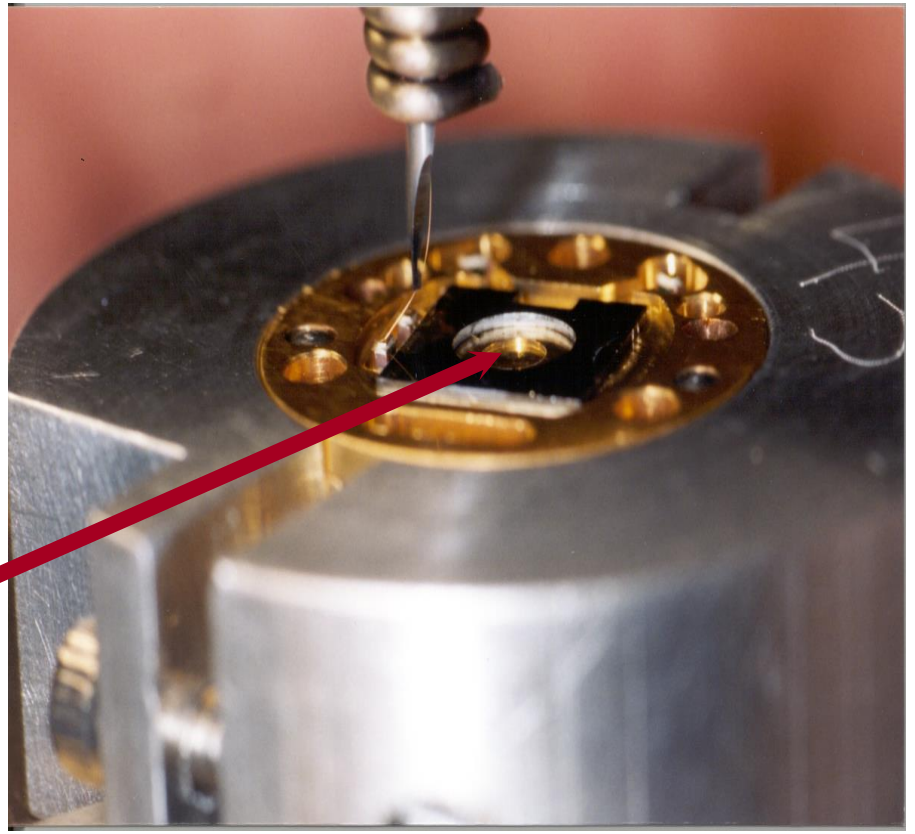
Hybrid Cleanroom Technology

www.technographmicro.com

Ref: Satcon

Wirebonding in the Cleanroom

Microelectronics Interconnect using a Wire Bonder

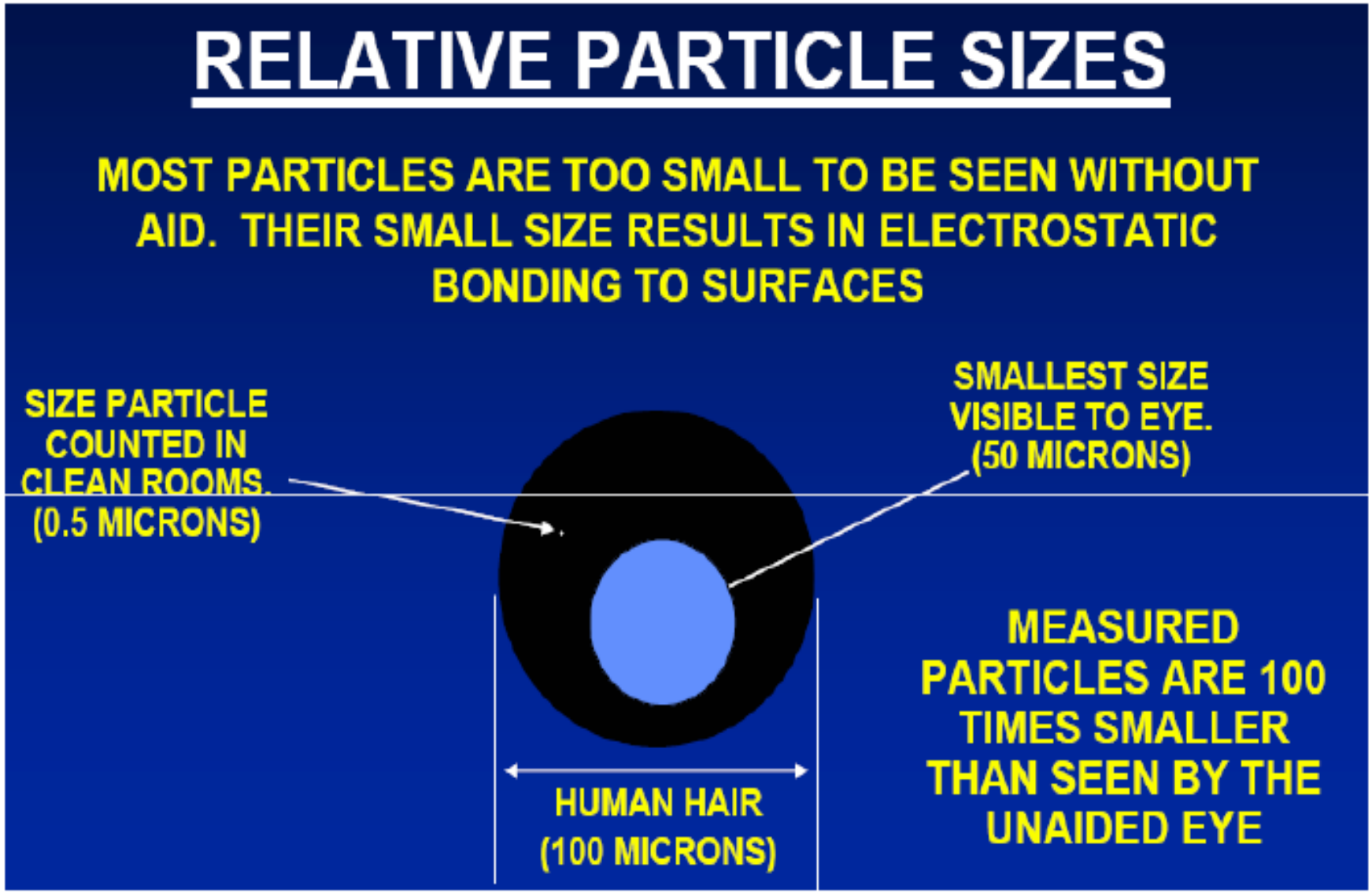


Bolometer Wire Bonded

ISO 14644-1 Clean Room Spec

- ✓Assembly is done in Class 100,000 cleanroom or better, inspection just prior to pre cap is done under a laminar flow bench
- ✓The cleanliness classification levels defined by FS209E and ISO 14644-1 are approximately equal, except the new ISO standard uses new class designations, a metric measure of air volume and adds three additional classes
  - ✓- two cleaner than Class 10 and
  - ✓- one beyond than Class 100,000.
- ✓ The second new ISO standard, ISO 14644-2, gives requirements for monitoring a cleanroom or clean zone to provide evidence of its continued compliance with ISO 14644-1
- ✓Fed Std 209 Class 100,000 equals ISO Class 8

Loose Conductive F/M…FOD



Foreign Material or F.O.D.

Definition...anything foreign to the process or displace material from a previous process step e.g. loose chips of silver epoxy and wire that are generated during rework can cause shorts.

- Need to assess **attached** vs. **unattached** or the threat of becoming unattached
  - All foreign material shall be considered to be **unattached** unless otherwise verified to be attached
- The size of the particle relative to the shortest distance between two non-common conductors
- Liquid droplets or any chemical stain that bridges any combination of unglassivated or unpassivated active circuit areas

Foreign Material Mil Spec Requirements

The Primary source for FM/FOD criteria applicable at Pre Cap can be found at:

Hybrids (MIL-STD 883 TM 2017, para. 3.1.9)

There are additional referenced criteria (see Table 1) regarding FM/FOD applicable for FM/particles on the surface of the IC/MMIC

Monolithics (MIL-STD 883 TM 2010, ¶3.2.5)

Passives (MIL-STD-883 TM 2032, ¶3.1.5 / 3.2.3)

Pre-cap Power MOSFETS (MIL-STD 750 TM 2069.2, ¶3.3.1)

Pre-cap Discrete and Multichip Transistors (MIL-STD-750 TM 2070.2, ¶3.6.1)

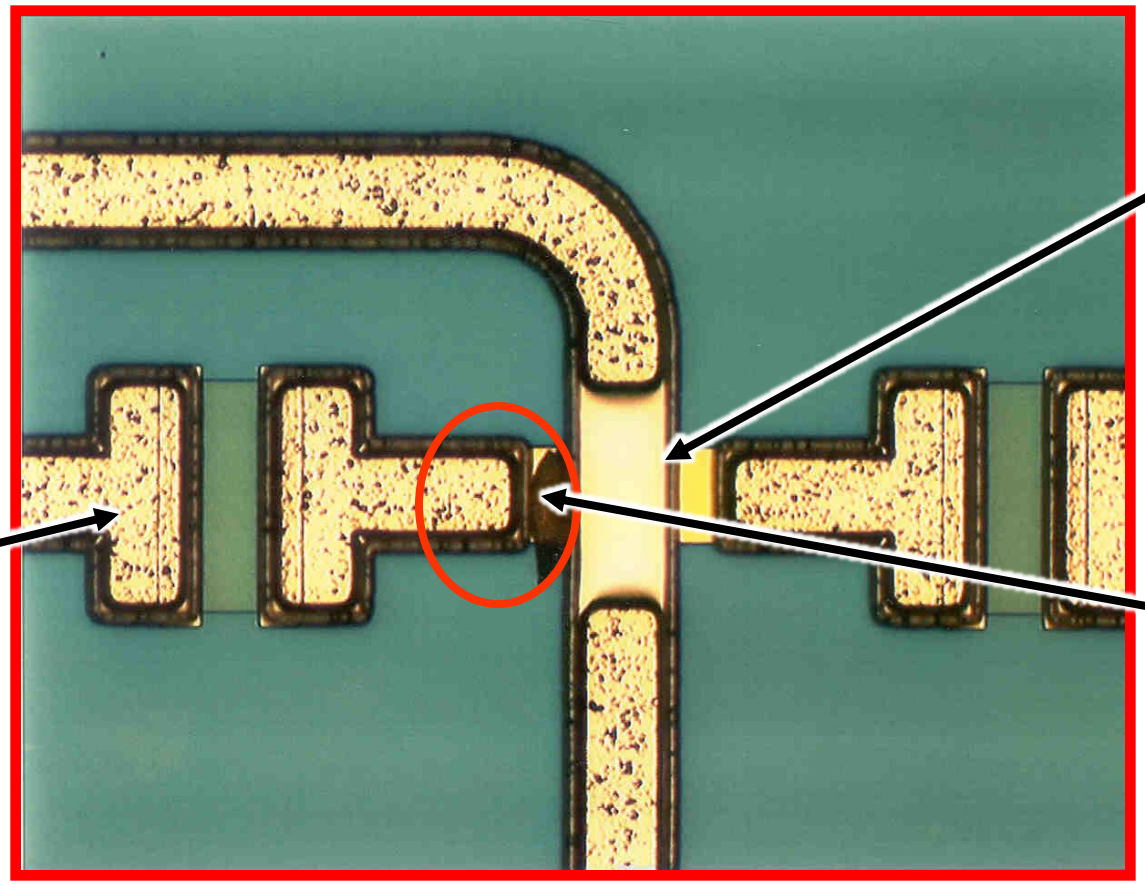
Internal Visual Transistor Inspection (MIL-STD-750 TM2072.8, ¶4.1.6)

Visual Inspection Of Die (MIL-STD-750 TM 2073.2, ¶4.3)

Conductive FM Under Air Bridge

REJECT

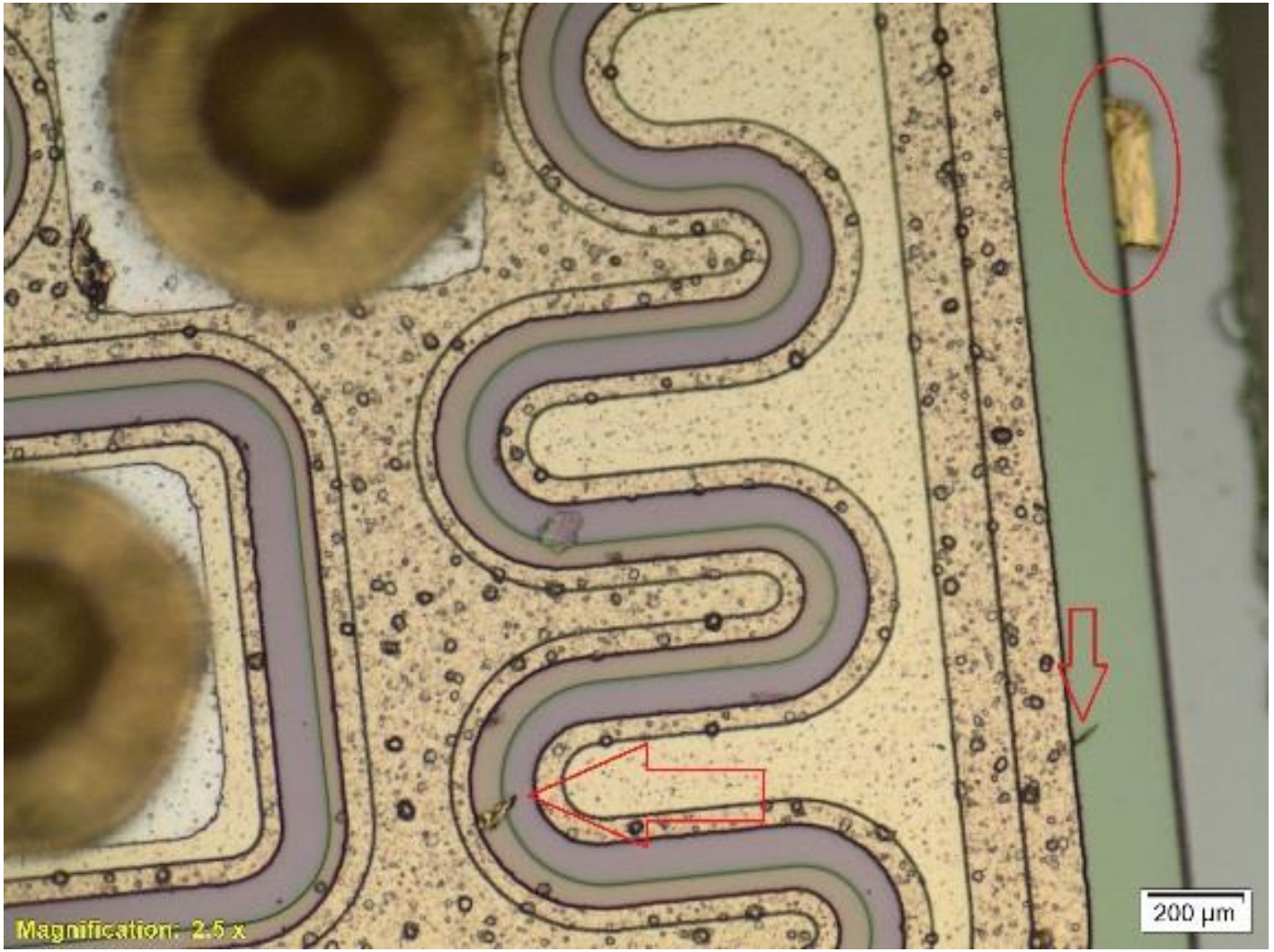
Loose particles may be removed by subjecting the device to a nominal 20 PSIG N2 blow off



REJECT: Attached and bridging foreign material underneath and adjacent to air bridge. (200X)

F/M Loose Conductive Particles

REJECT

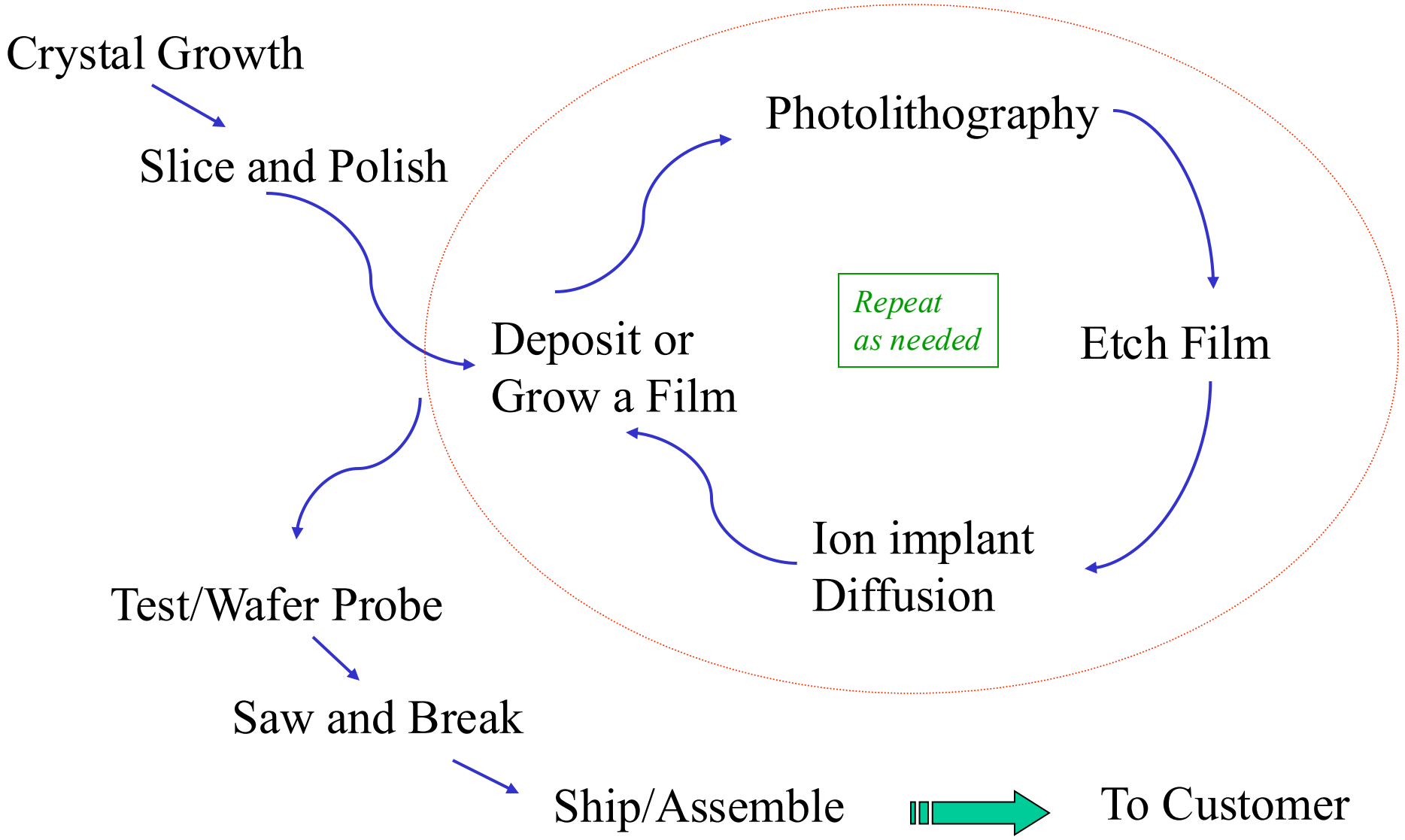


Non-embedded foreign particles on the surface of the die that are large enough to bridge the narrowest unglassivated active metal spacing

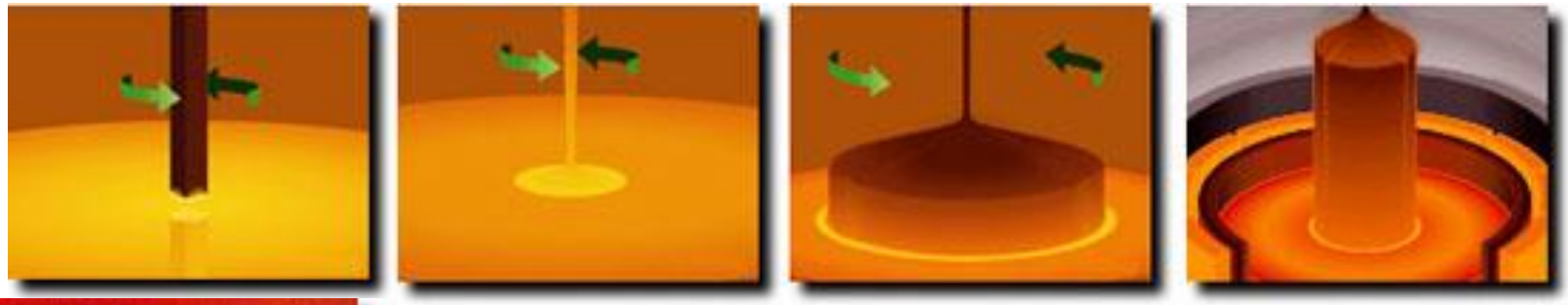
TM 2017 Para. 3.1.9.a

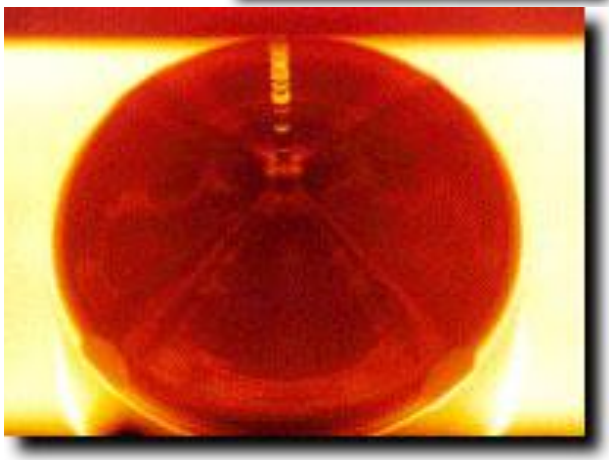
Wafer Fab Process Flow

Lots of great U-Tube videos on wafer fab. Check them out and take the time to learn.

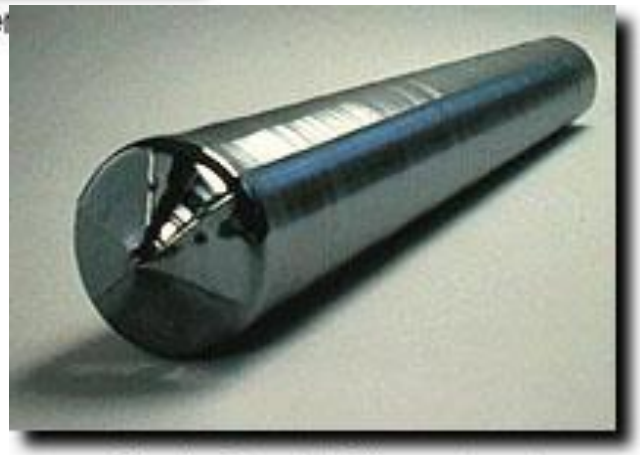


Growing the Ingot





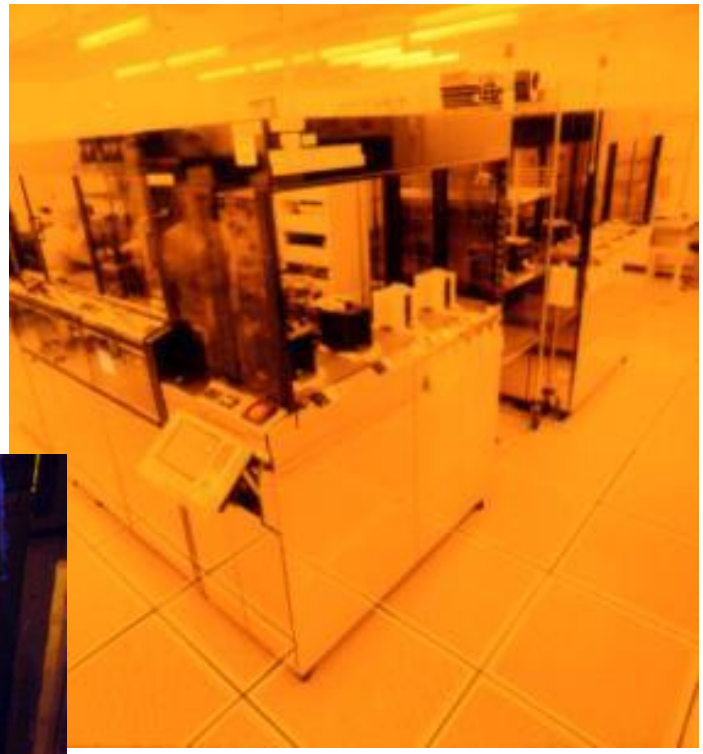
Inside CZ Puller
(MEMC)

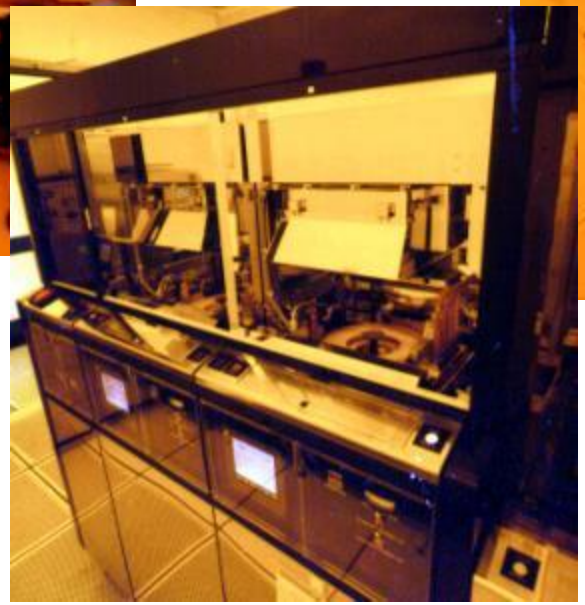


Single Crystal Silicon Ingot

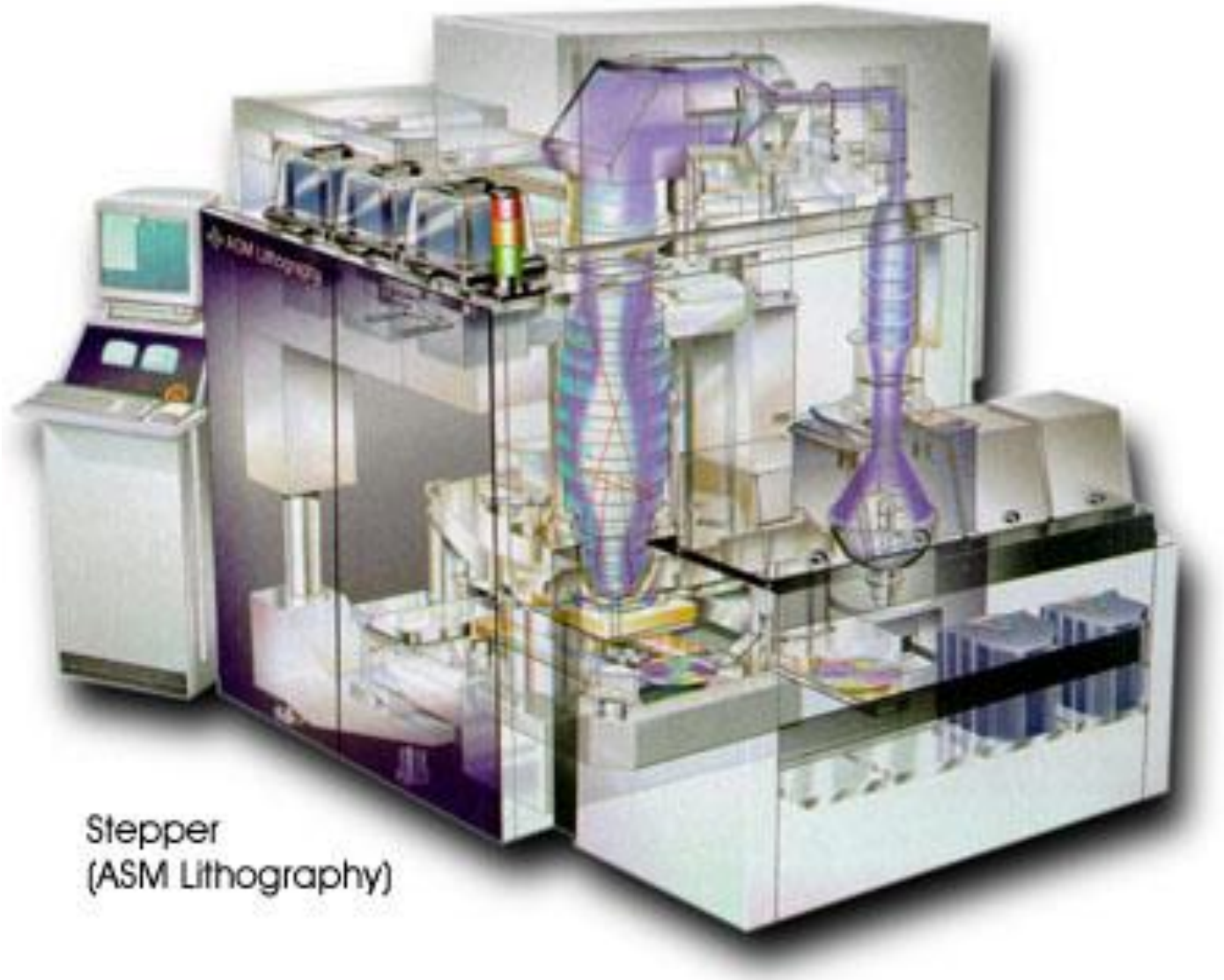
CZ Crystal Pullers
(Mitsubishi Materials Silicon)

Photolithography

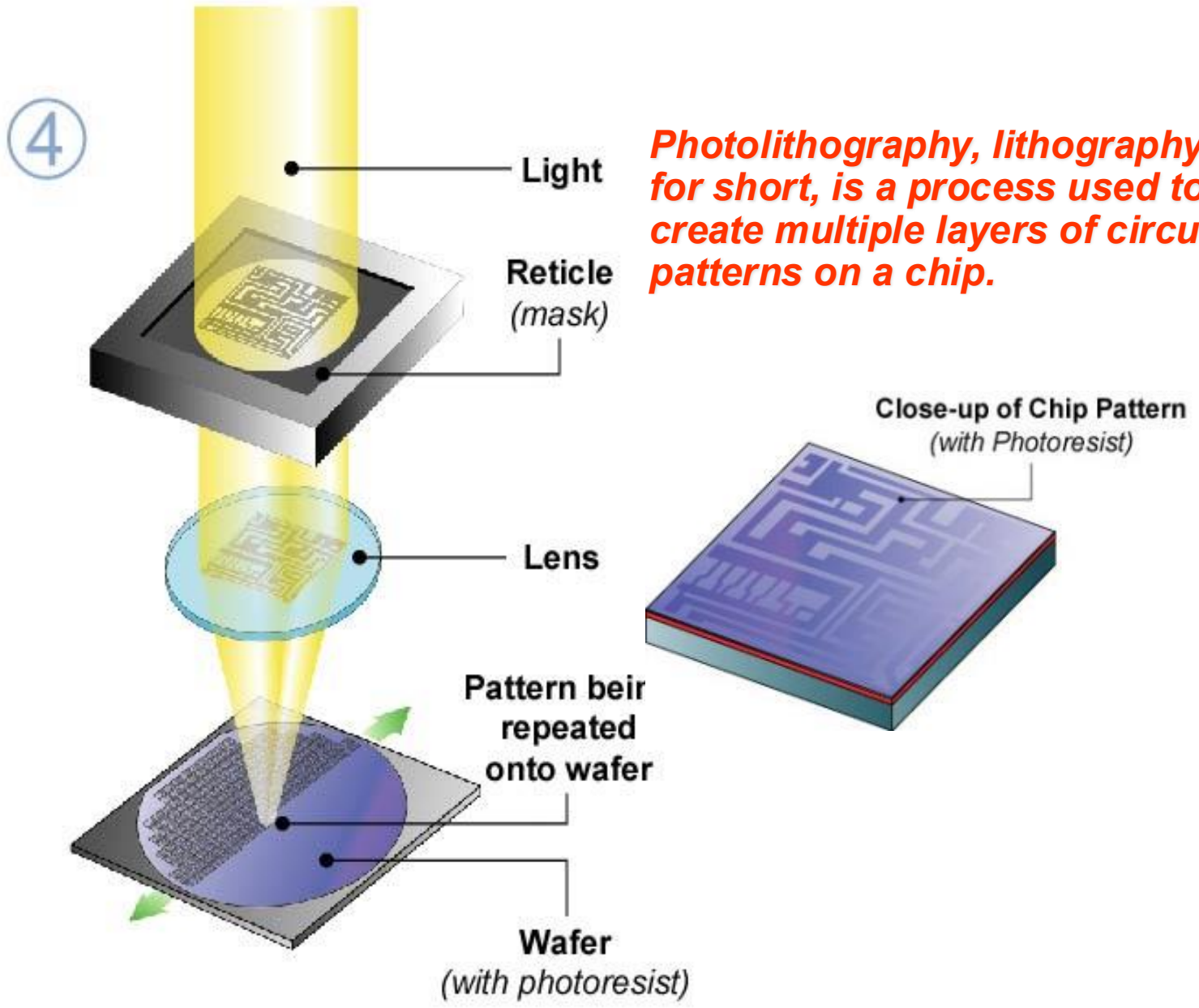




Photolithography Equipment

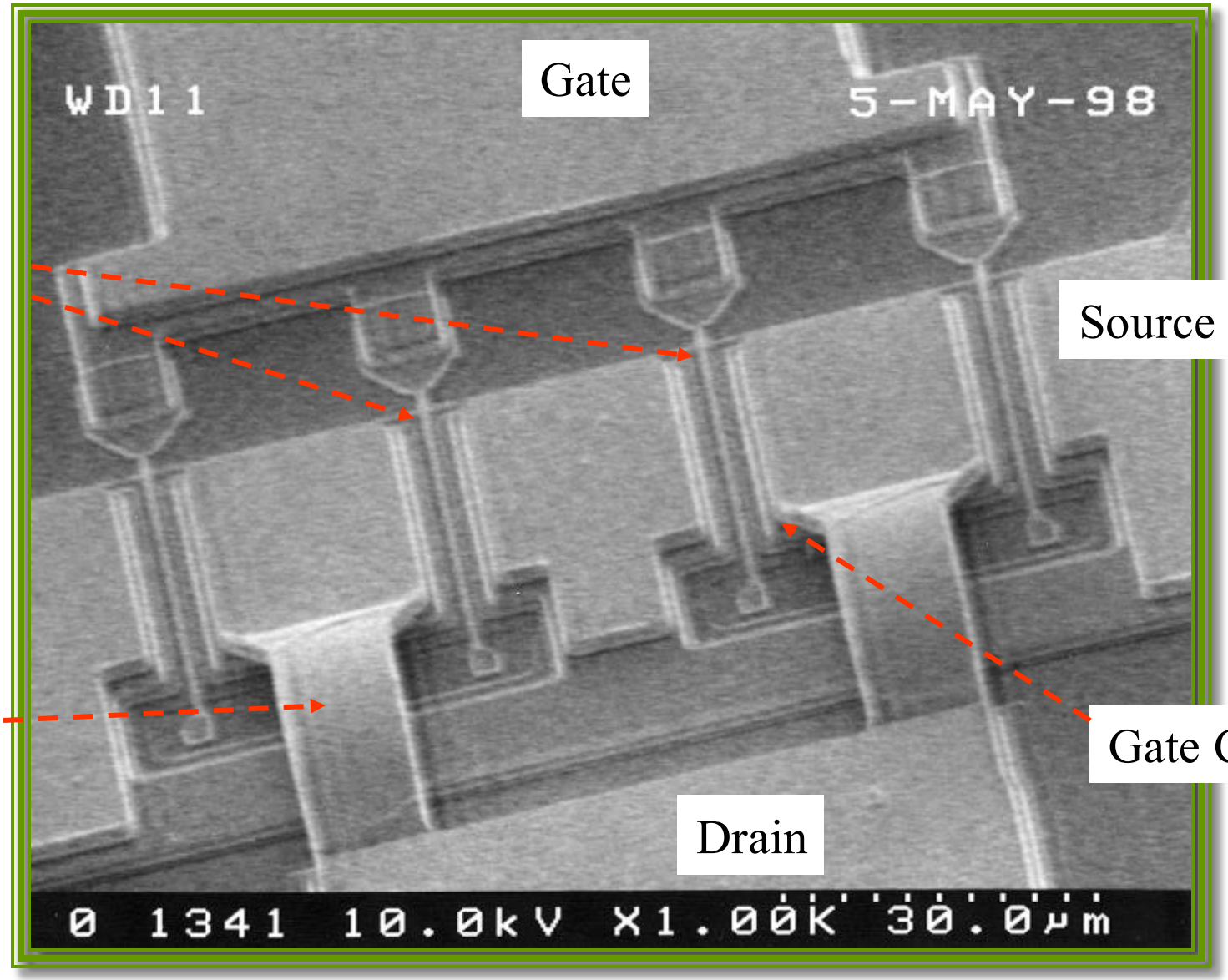


Stepper
(ASM Lithography)



Photolithography, lithography for short, is a process used to create multiple layers of circuit patterns on a chip.

GaAs FET



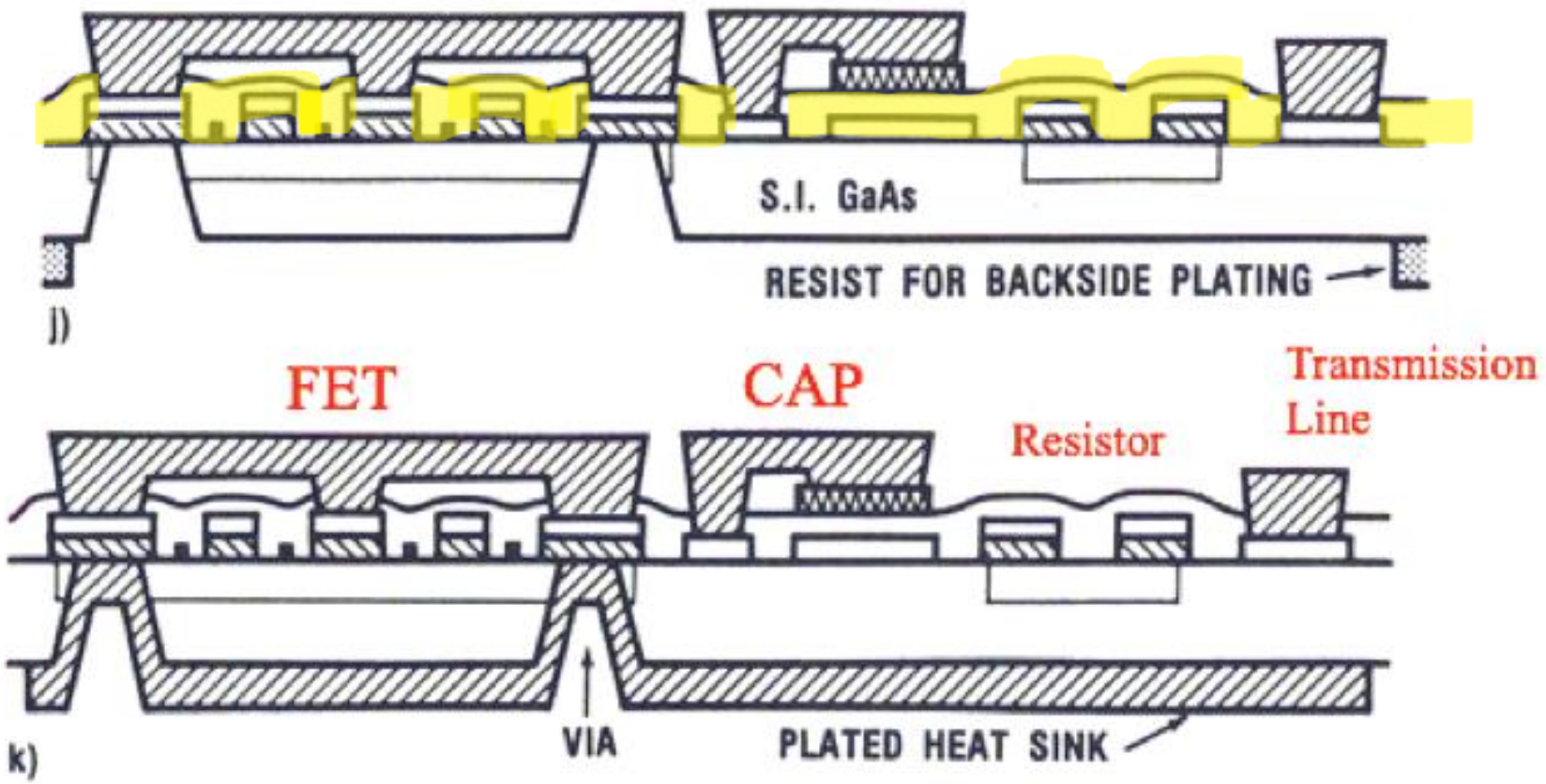
Gate Fingers

Airbridge

Gate Channel

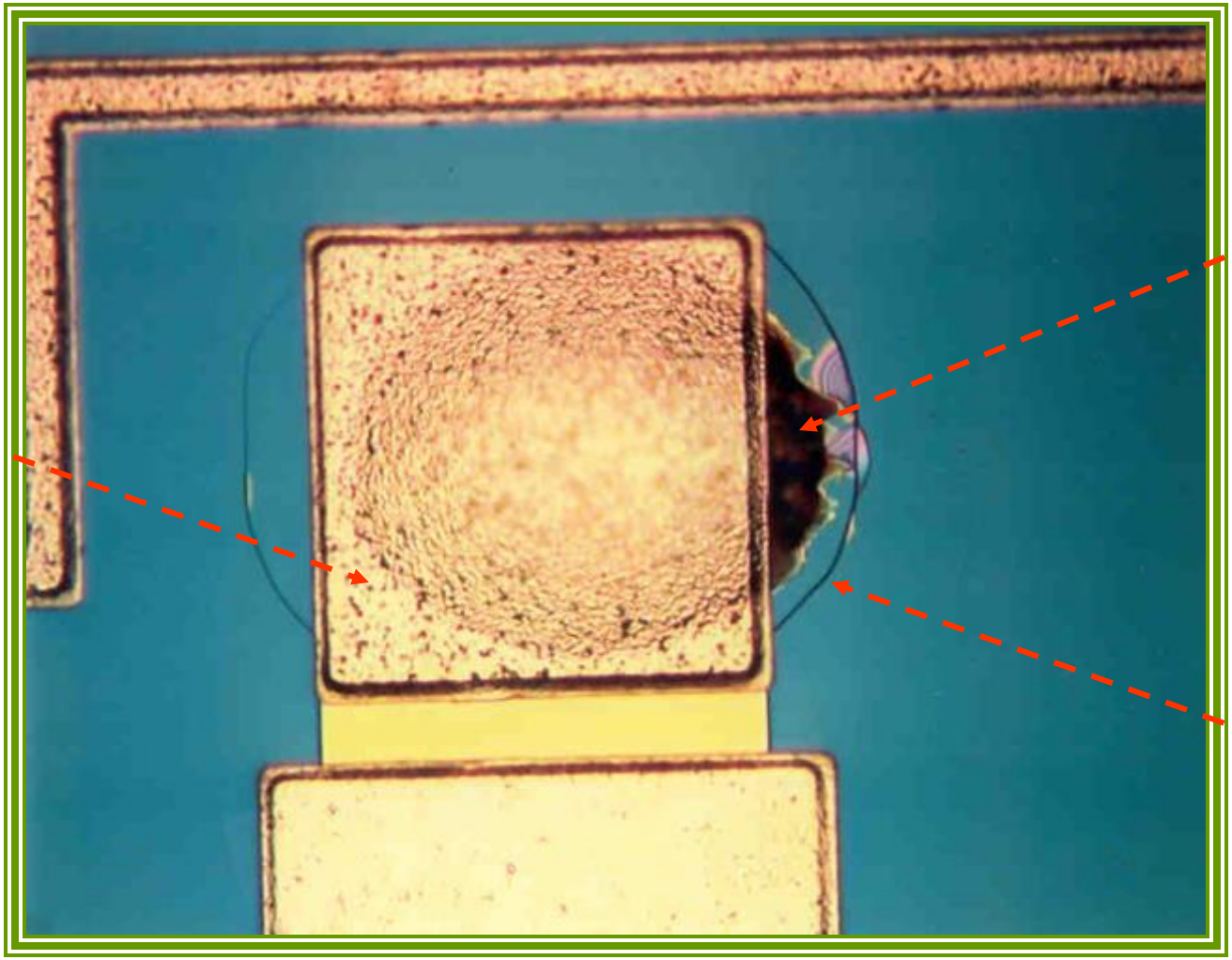
NOTES: Preferred condition air bridge and FET Circuitry (4 x 37.5µm FET) 1341X

MMIC Fab Cross Sectional View



Shown above with the yellow highlight is the silicon nitride field passivation which serves to passivate the resistors, becomes the dielectric for the capacitor and in some cases helps to protect the gate area. Thinning or missing passivation in any of these areas is a REJECT. For metal runs OK to have thinning at the edge of the run or in any non-active area.

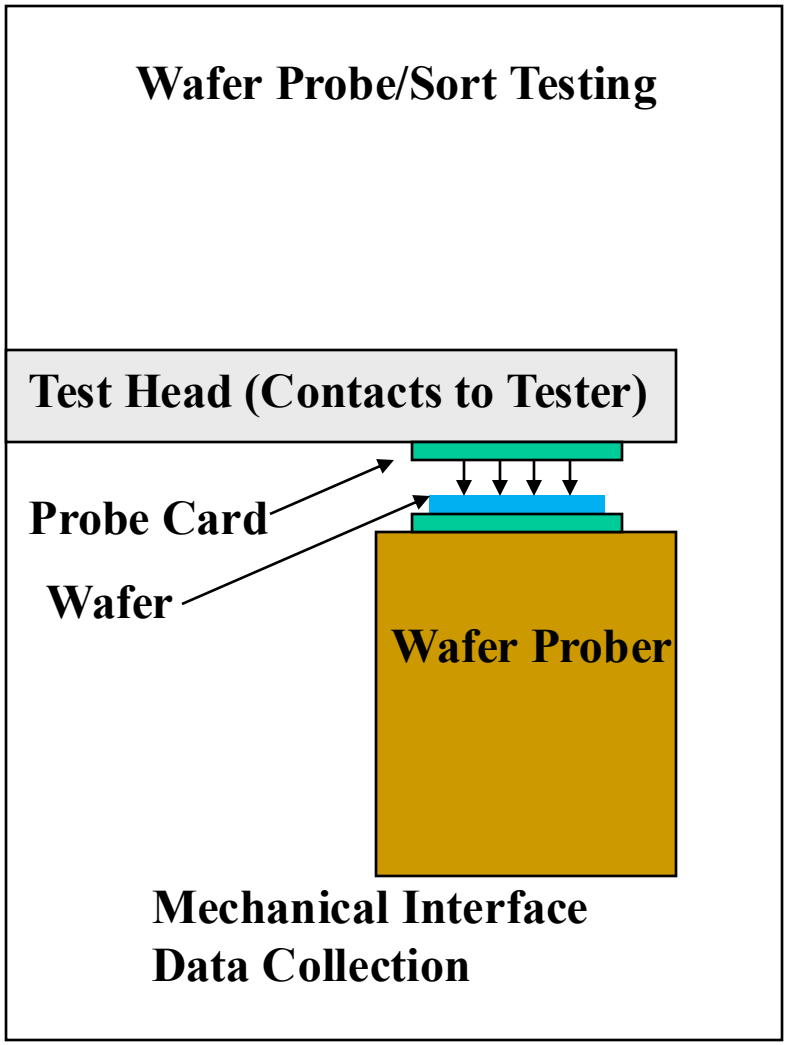
Over Etched Via



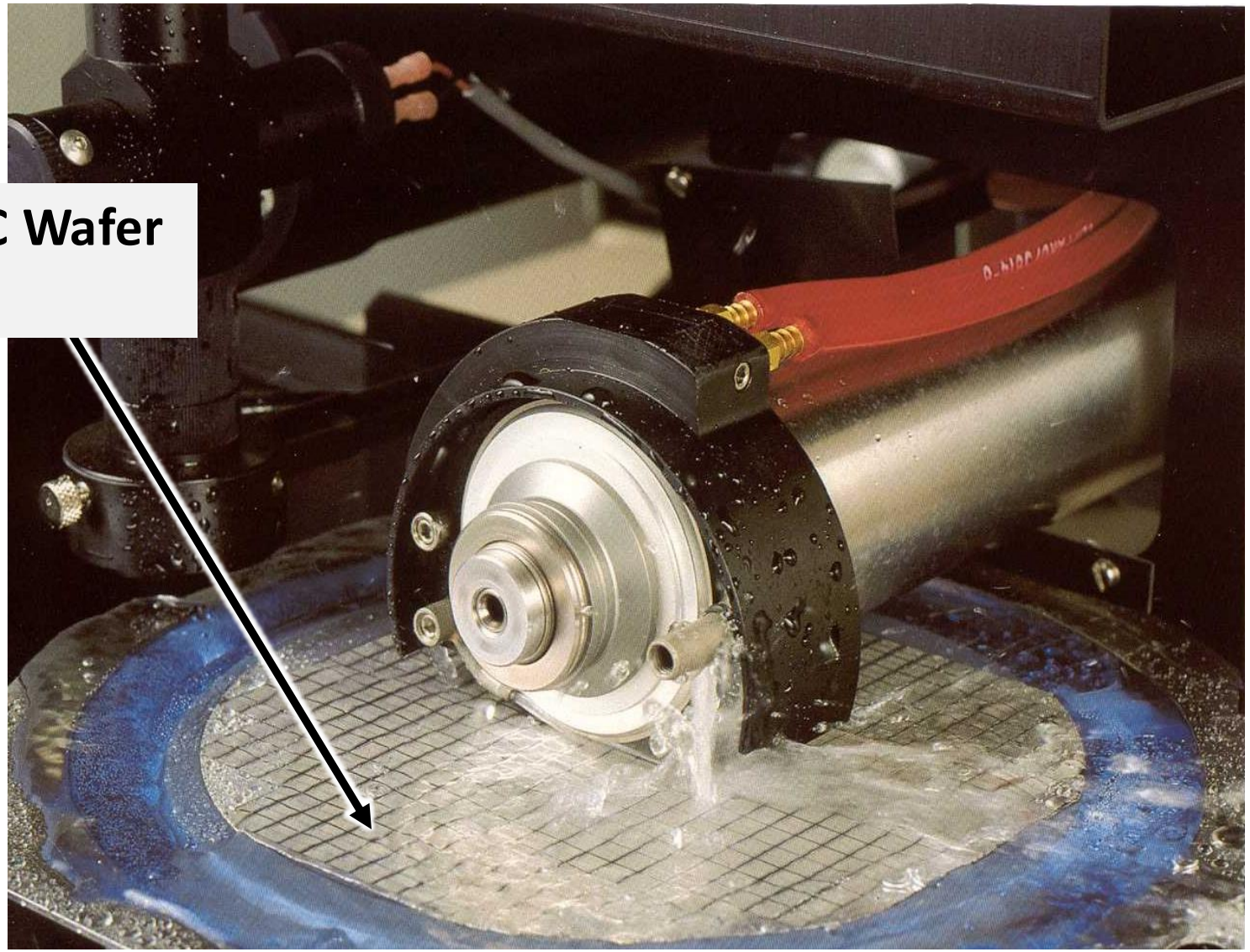
NOTES: Reject..Via is mistargeted and oversized. Square pad over circular via (400X)

Wafer Probe and Sort Testing

- **Devices normally go through a functional and then a full parametric test to the customers' specifications.**
- **After wafer processing not all chips are good, chips that fail wafer test are "ink-dotted" for separation after saw and break**
- **It's at this step in the wafer fab sequence that probe marks are made on the wirebond pads.**



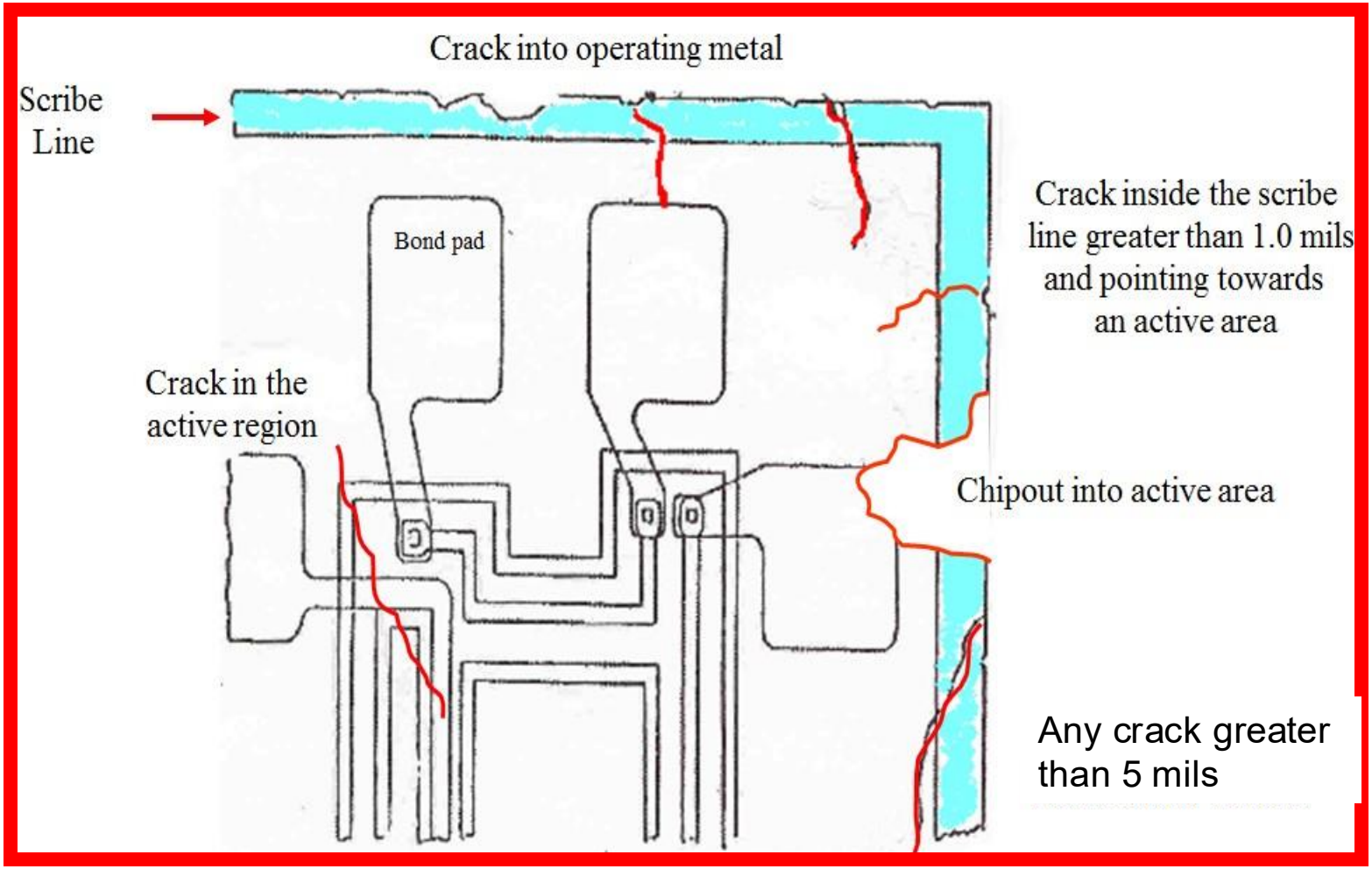
Wafer Saw Process



Ref Kulicke and Soffa product literature

Scribing and Die Defects

REJECT



Chips and cracks caused by the wafer saw and/or handling during the assembly process can further propagate in field use or after temp cycling. This graphic is applicable to both MMICs and silicon ICs.

TM 2010 FIG 2010-22

Thin Film vs. Thick Film Substrate Technology

Different processes used to create passive circuit elements such as resistors, capacitors and inductors.

Thick film is thicker, but also appears bumpy under a microscope and slightly ragged along the edge.

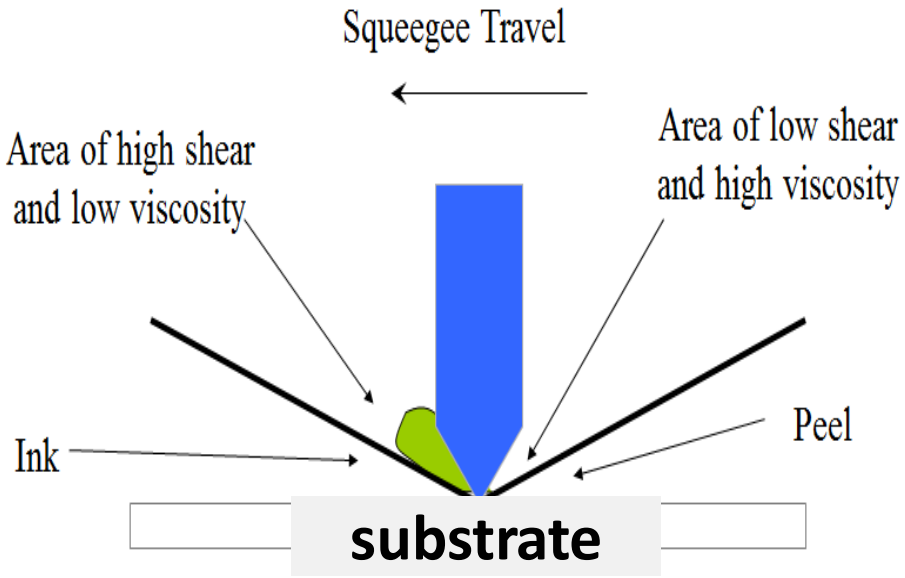
Thin films are surface smooth and the lines are edge sharp…. better for high frequency microwave applications.

CAUTION: TM 2032 inspection criteria is organized according to technology . . . make sure you know what you are looking at! If you don't know, ask

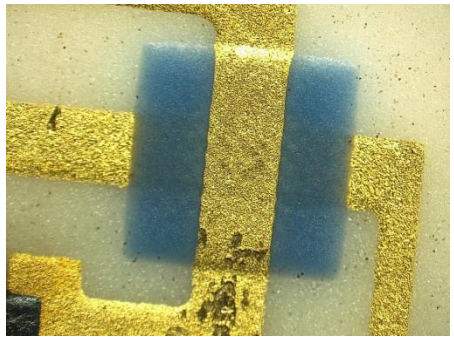
Thick film - is conductive, resistive or dielectric material screen printed onto a substrate and fired at temperature to fuse into its final form.

Thin film - is conductive, resistive or dielectric material, usually less than 50,000Å in thickness that is deposited onto a substrate by vacuum evaporation, sputtering, or other means.

Thick Film Process



Wirebonding to Thick Film



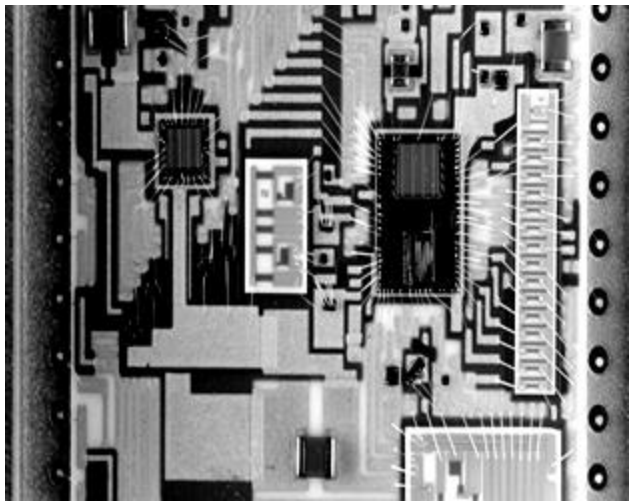
Thick Film Crossover . . .
blue is dielectric

Thick film is a screen printing process where conductors, insulators and resistors material are squeegeed onto the substrate and then dried and fired at high temp.

Thick Film Process

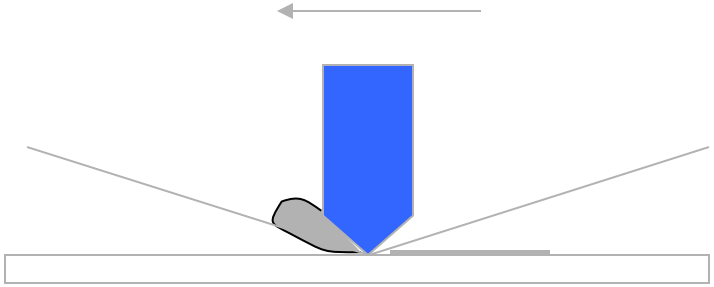
- Uses a ceramic substrate usually Al_2O_3(96%)
- Sequential print dry fire process
- Glass dielectric constant about 7-10
- Conductor Metallurgy Ag, Au, Pd-Ag, Cu
- Resistors, capacitors and inductors can be patterned

Thick Film Process Flow



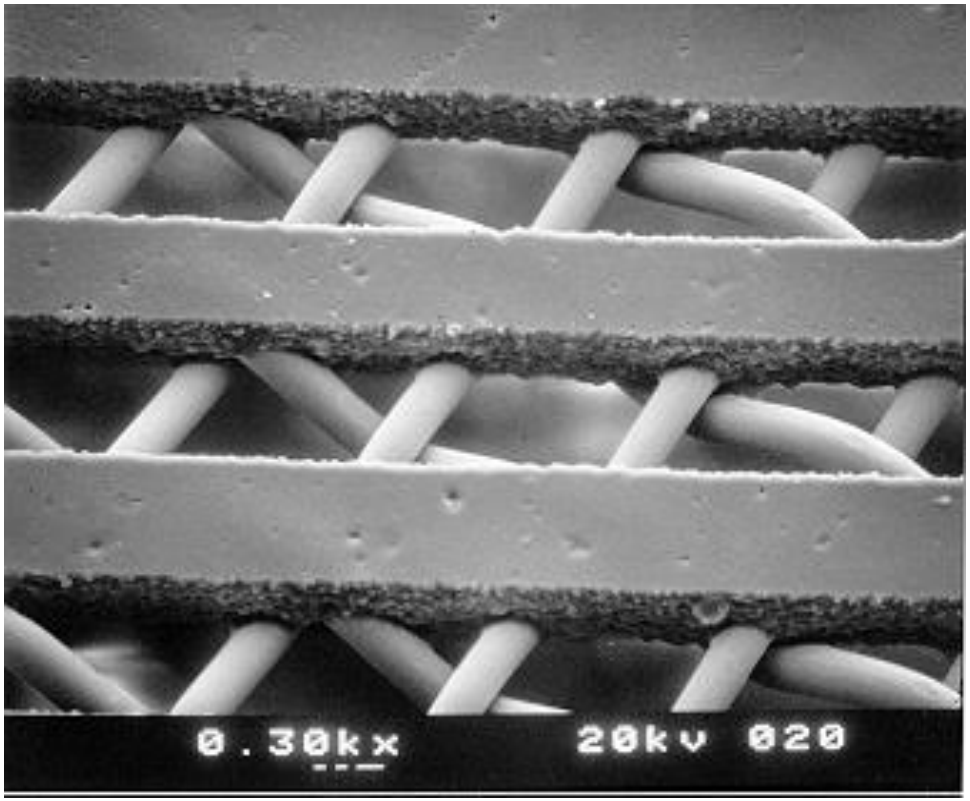
The Screen

- Tension
  - Screen Printing works because the screen mesh is under tension causing it to peel up after the squeegee passes.
- Mesh
  - Count, wire diameter, angle, weave type
- Emulsion
  - Thickness, type



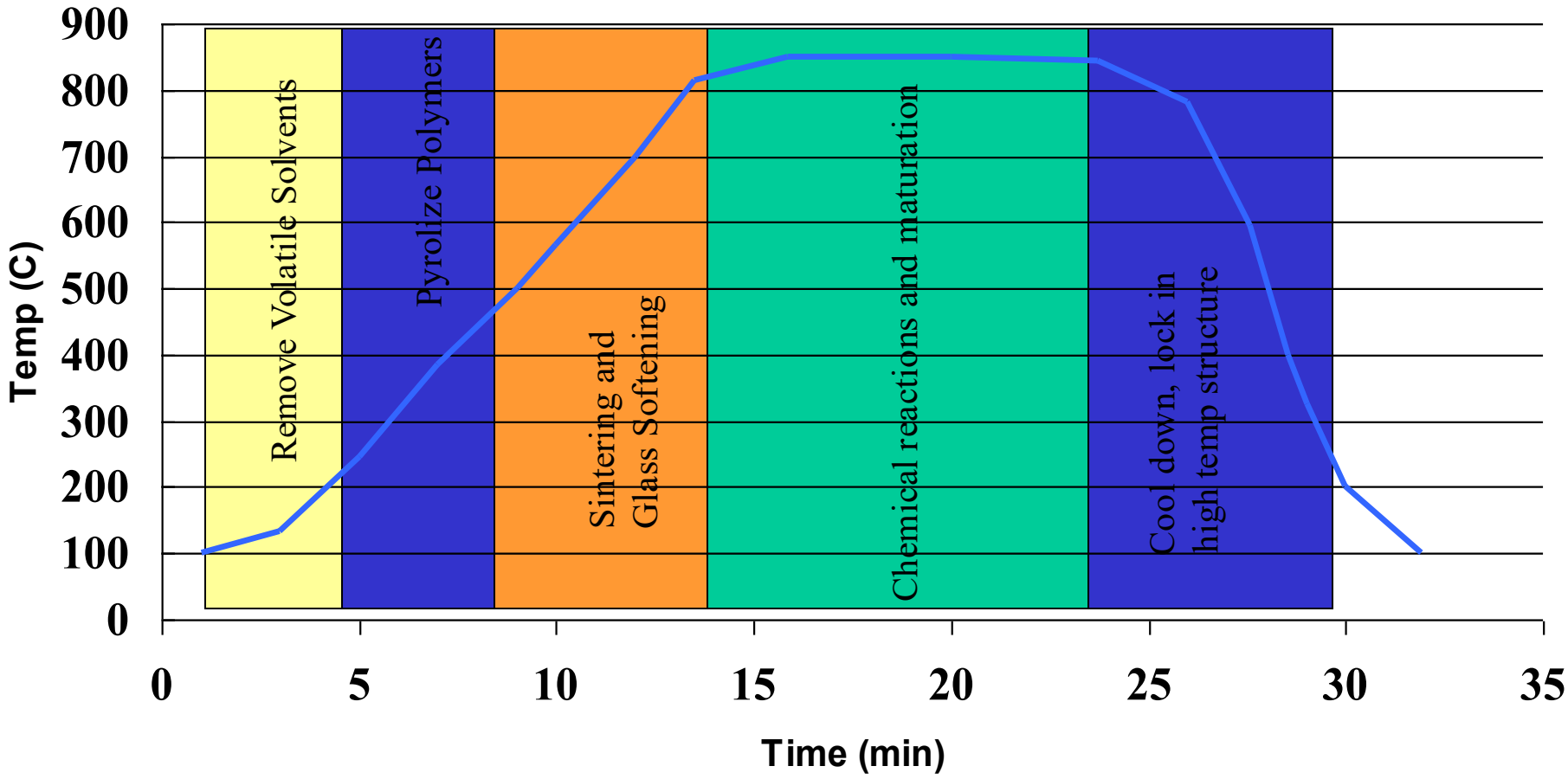
Emulsion

- UV sensitive polymer that defines pattern to be printed.
- Thickness of emulsion directly effects thickness of print
- Dual-curing emulsions can resolve 3 mil lines and spaces
  - 2 sensitizing agents
  - Better solvent resistance
  - Longer Shelf Life



Typical Firing Profile

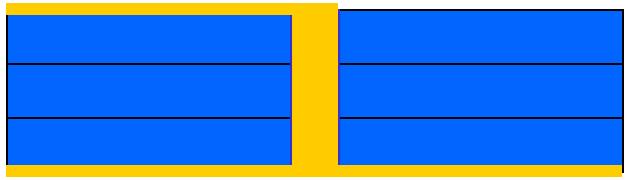
Critical paramaters: Time & Temperature uniformity,
Cleanliness of Atmosphere, Flushing Action of Atmosphere



Dielectrics

- Used as an electric insulator between layers of conductors
- Multilayer, crossover, and covercoats
- Glass + Crystalline Ceramic + Vehicle
  - Crystallizable glasses
- Must be dense and hermetic
- Vias are used to connect layers of conductors

(3 dielectric and one via print)

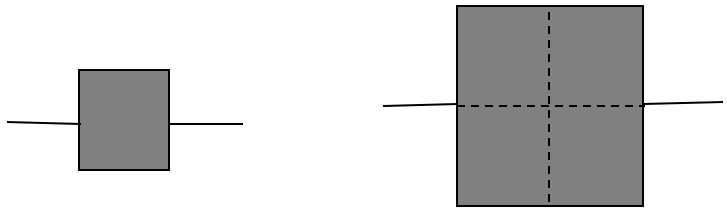


Resistors

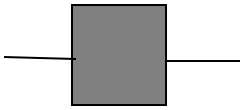
- Conductive phase + glass + vehicle
  - Conductive phase is either a metal, conductive oxide (RuO2), or a Ru containing crystal (pyrochlore or perovskite).
- Behavior ranges from conductors to semiconductors
- Used for power dissipation, impedance matching, filtering
- Electrical properties are everything
  - Resistor stability under load
  - Resistor stability under adverse environmental conditions

Sheet Resistivity

- Manufacturers report Ohms/Square, Ω/•
- Theoretically at a specified thickness, a square resistor print will have the same resistance whether size it is, 40 X 40 or 200 X 200
- To change resistance use multiple squares or partial squares

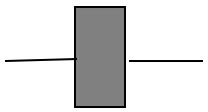


R= 5Ω R = 5 Ω



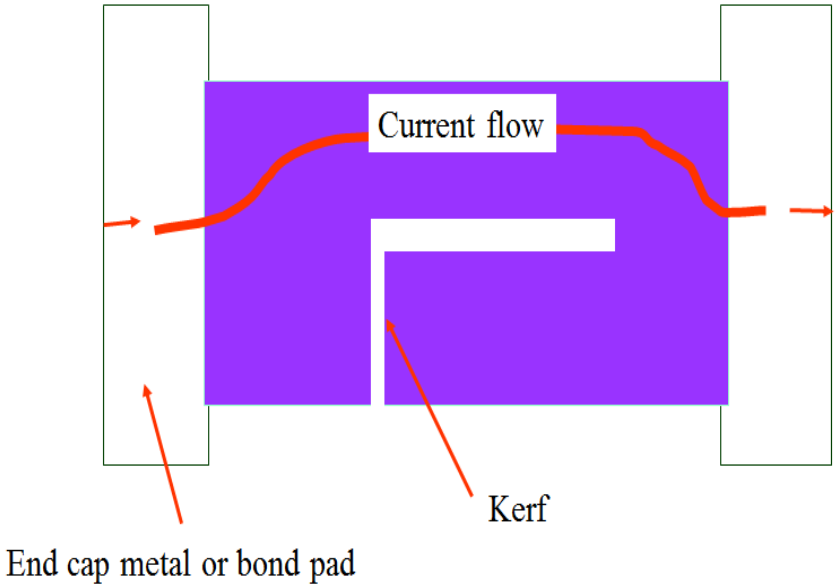
R= 5Ω

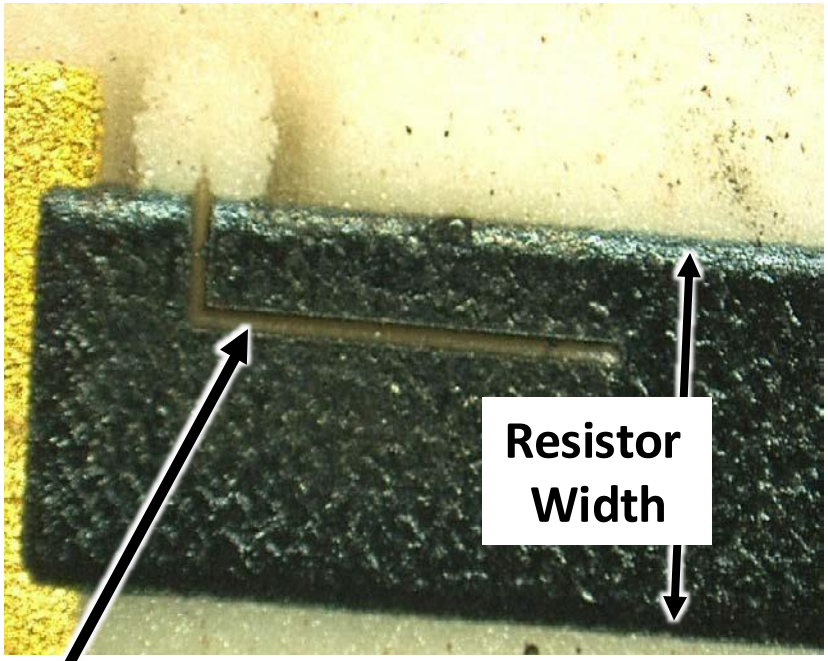
R= 10 Ω



R=2.5 Ω

Laser Trimmed Thick Film Resistors





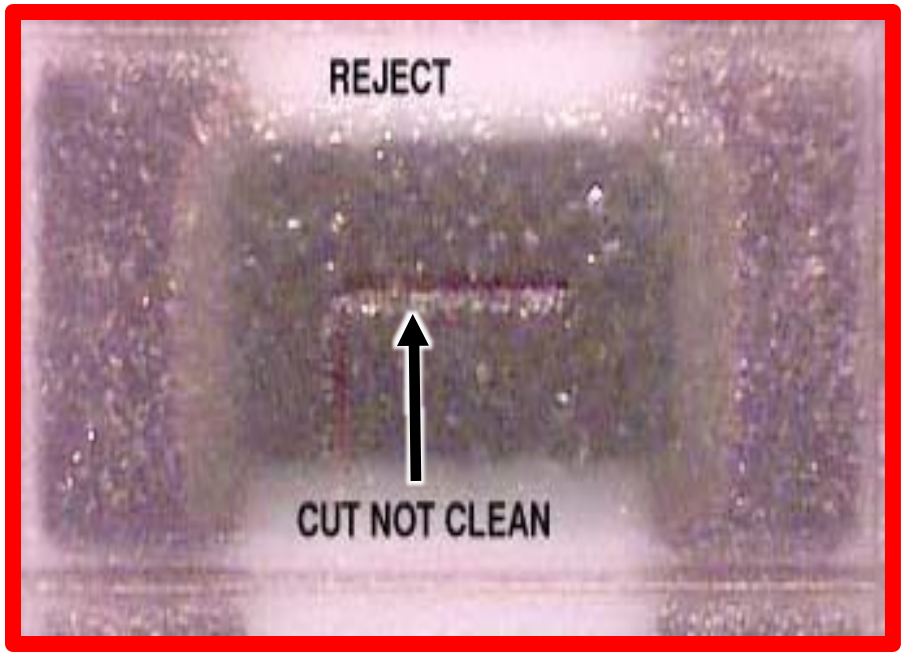
Laser trim cuts into a printed thick film resistor. Notice the nice clean kerf and trim cut less than 50% of the resistor width.

SEE TM 2032 para. 3.2.5 for detailed inspection criteria.

TM 2032 para. 3.2.5

Laser Trim Criteria "Detritus in the Kerf"

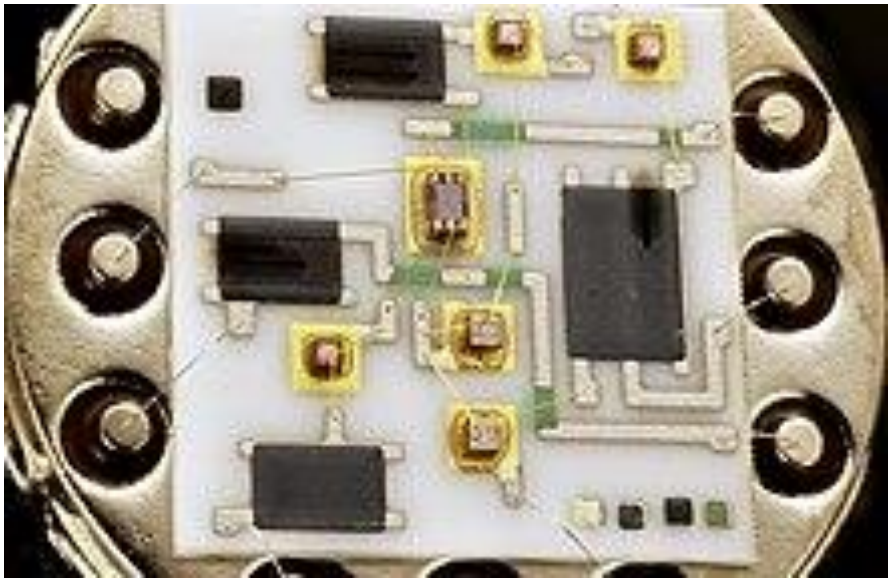
REJECT

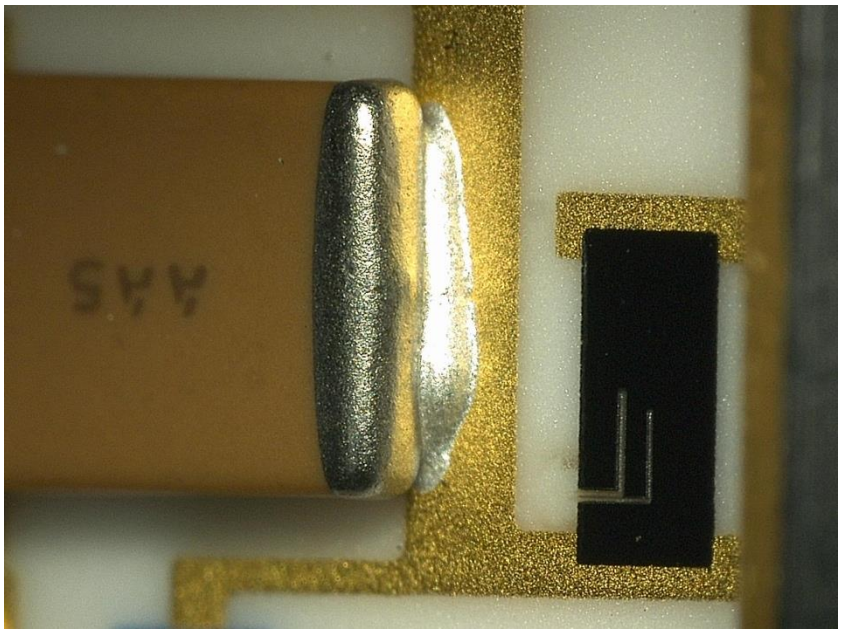


In both of the above photos there is evidence of material bridging across the kerf area. A good laser trim cut should produce a clean-cut path with no residual resistor material remaining in the cut area.

TM 2032 para. 3.2.5.b

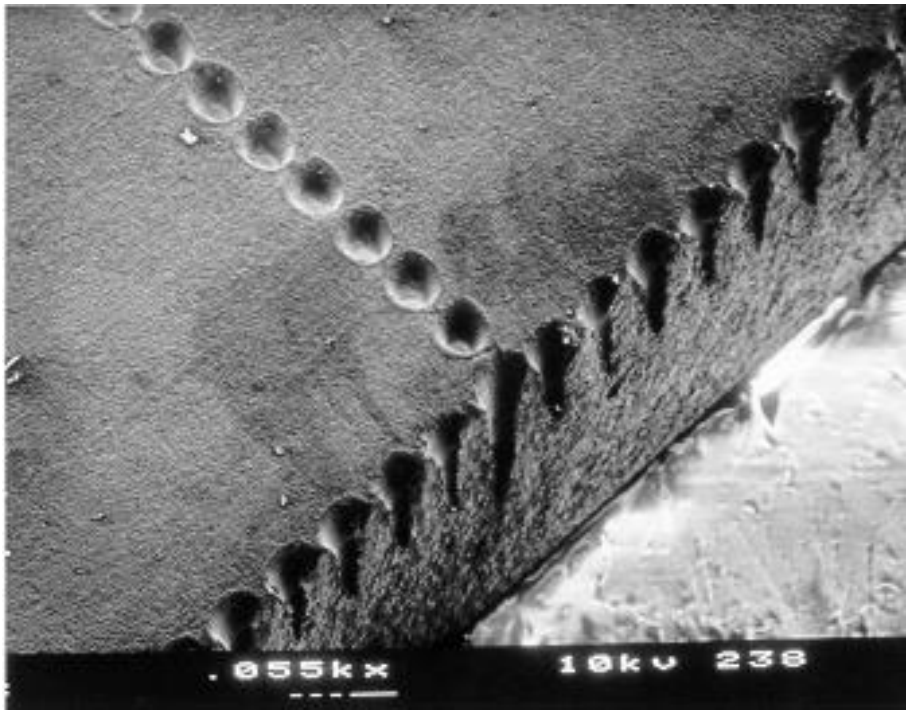
Thick Film Laser Trim Cuts

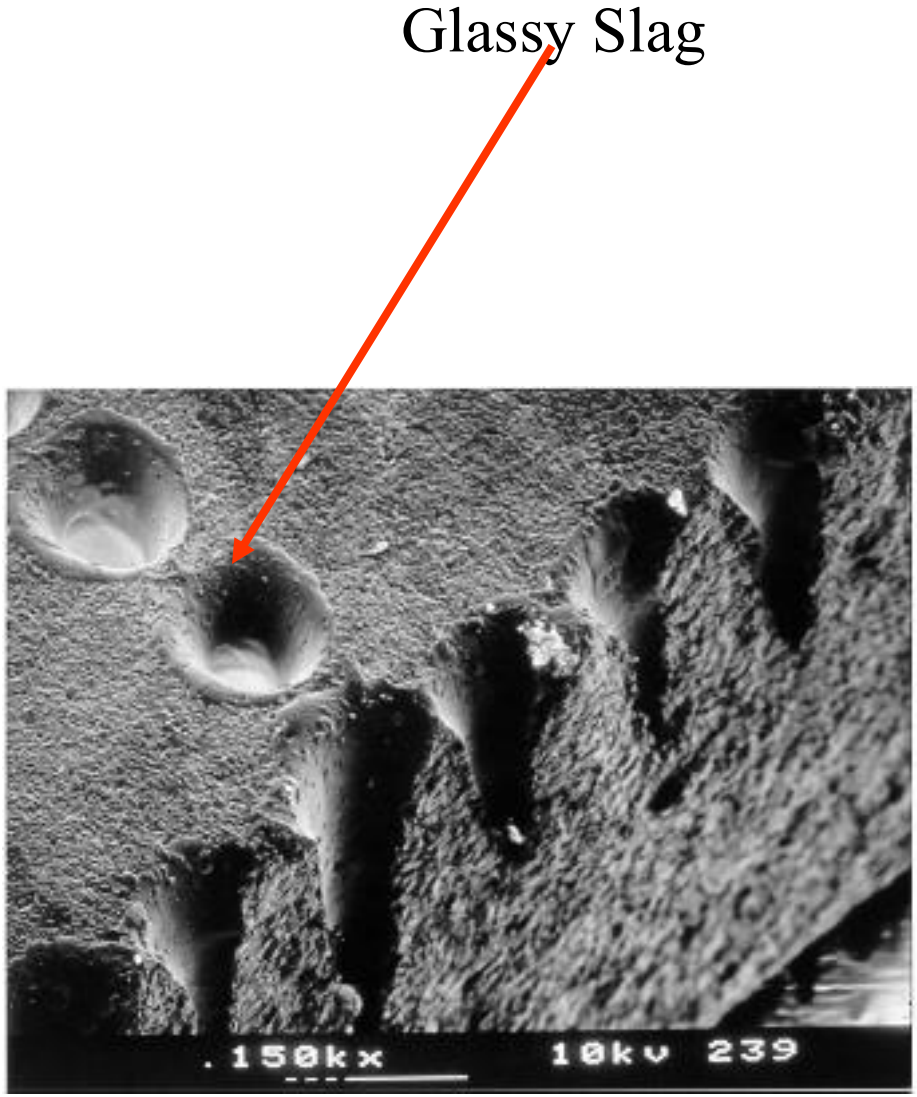




Thick Film Resistor Video

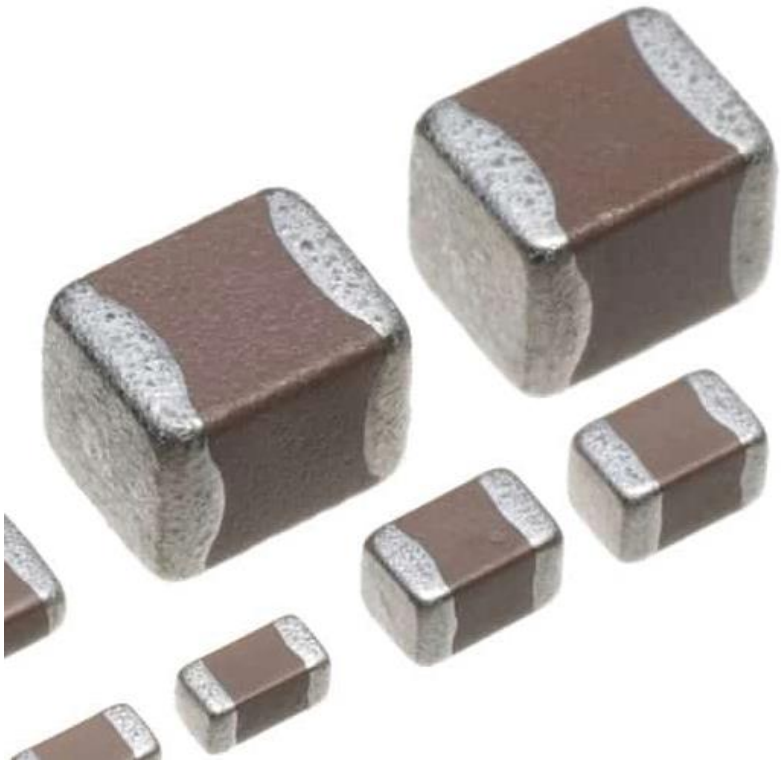
Laser Scribed Ceramic Substrates

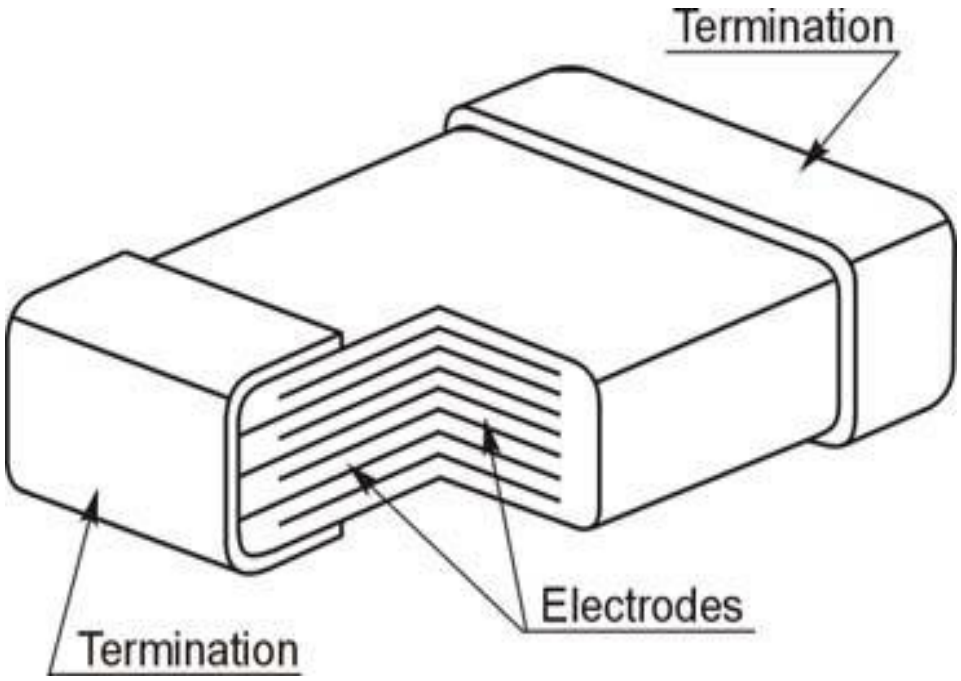




Thick Film is used to make capacitors

MLC Ceramic Capacitor

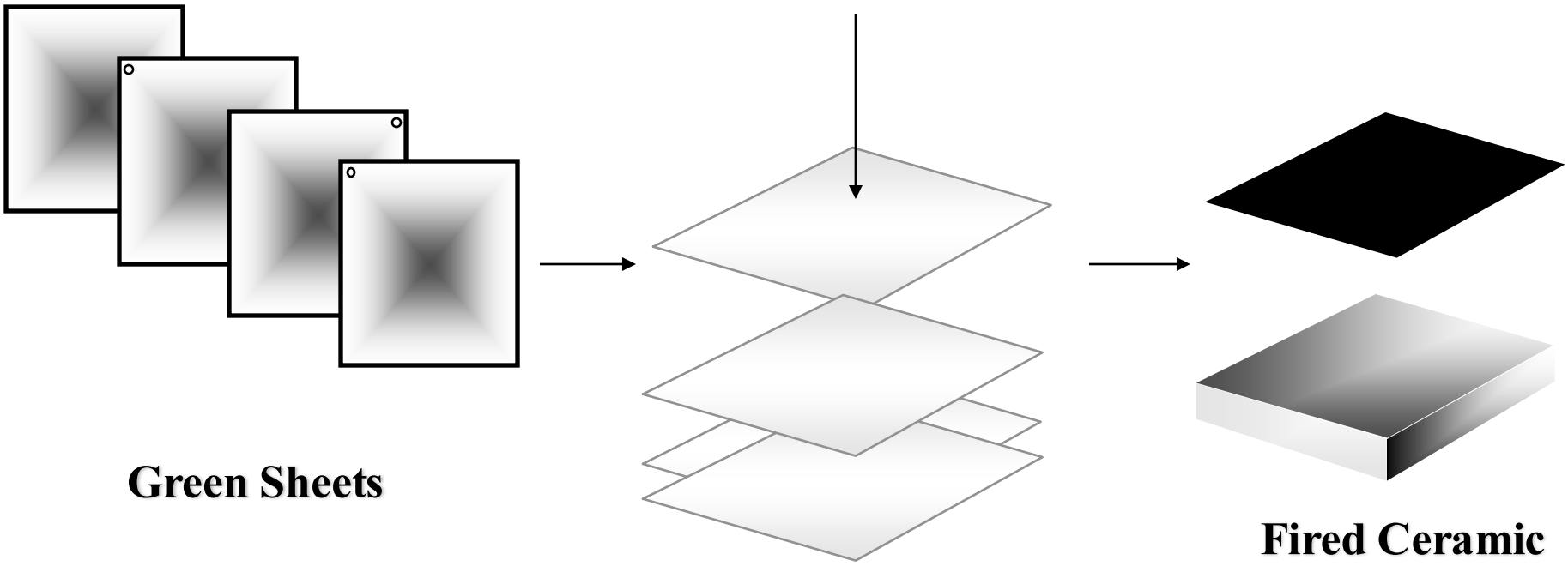




MLCCs (Multi layered ceramic chip) contain interdigitated parallel metal conductive plates separated by an insulator. Any chipping or cracks in the protective coating will allow moisture to seep in and change the capacitance or cause device failure.

LTCC PROCESS

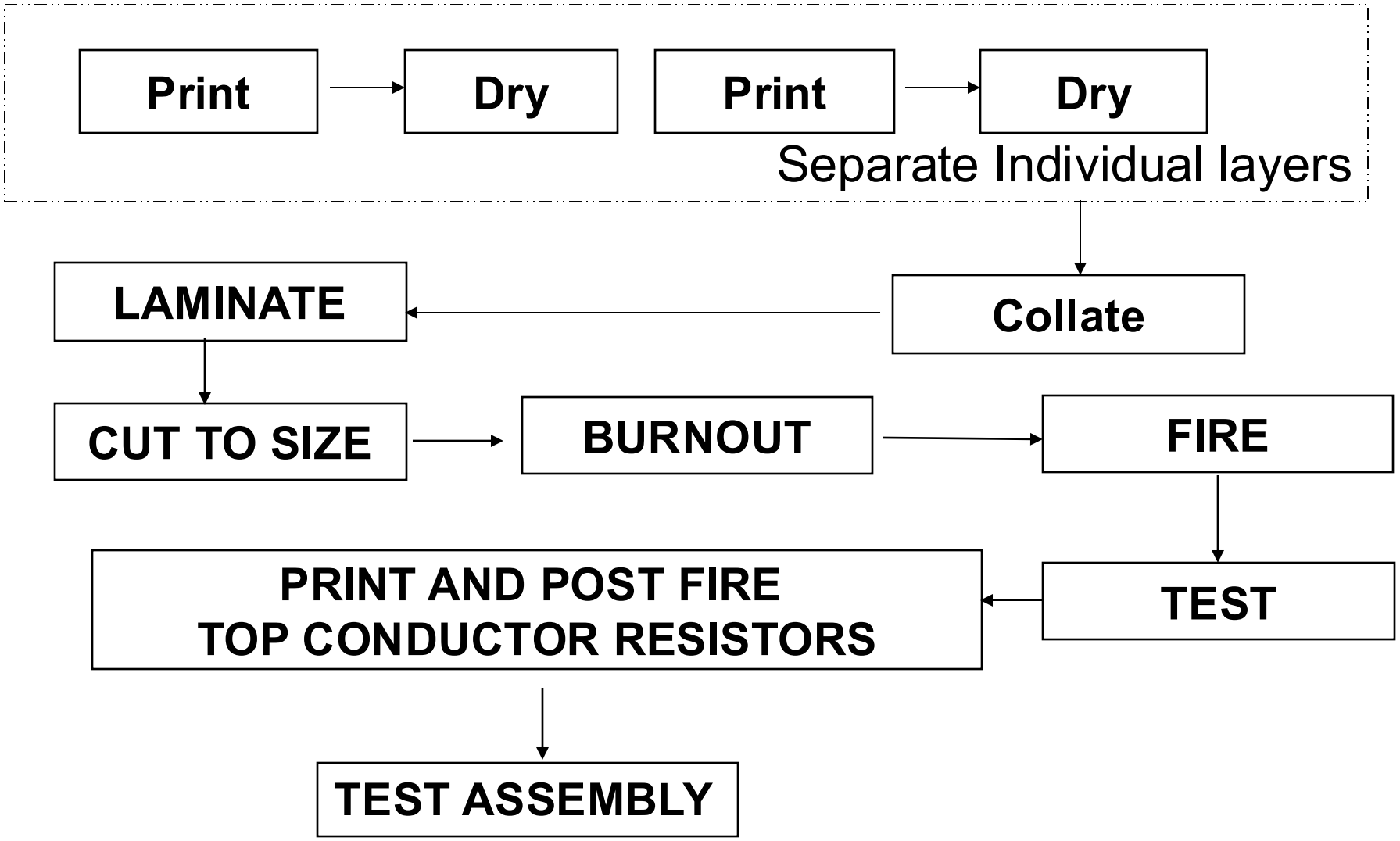
- A multilayer circuit or component made by laminating together green (unfired) sheets containing printed interconnection & components and then firing the structure to form a rigid monolithic ceramic multilayer circuit.



Low Temperature (LTCC)

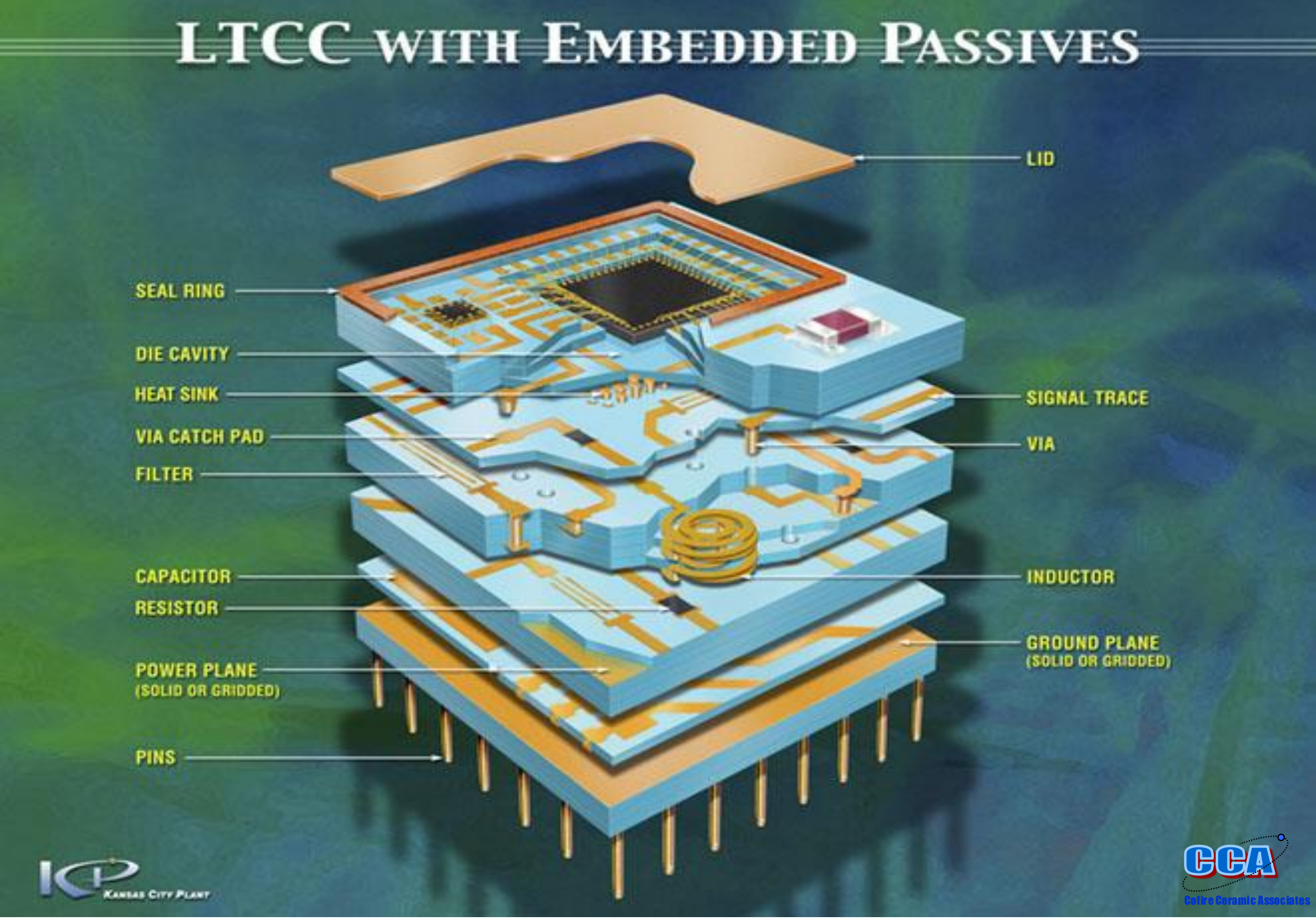
- Green Tape System screen printed and layered
- Air fired in conventional thick film furnaces about 850 C for 15 minutes
- Parallel processing (i.e. all layers are punched, printed and dried in parallel)
- Control of tape shrinkage is critical during fire
  - 12 to 14% X and Y direction is typical
  - 12 to 25% in Z direction typical

LTCC Process Flow



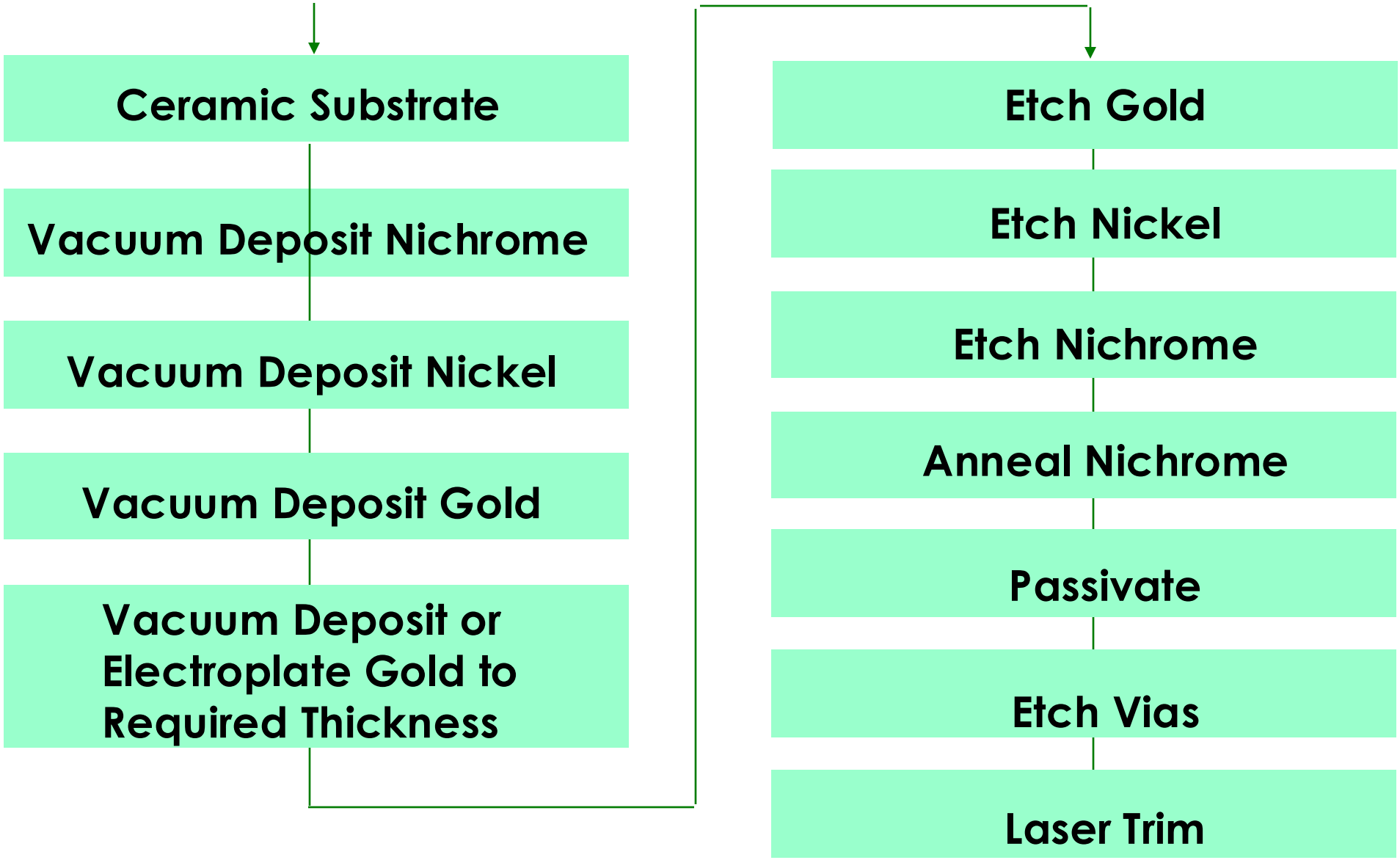
Ref NATEL Brief

LTCC WITH EMBEDDED PASSIVES

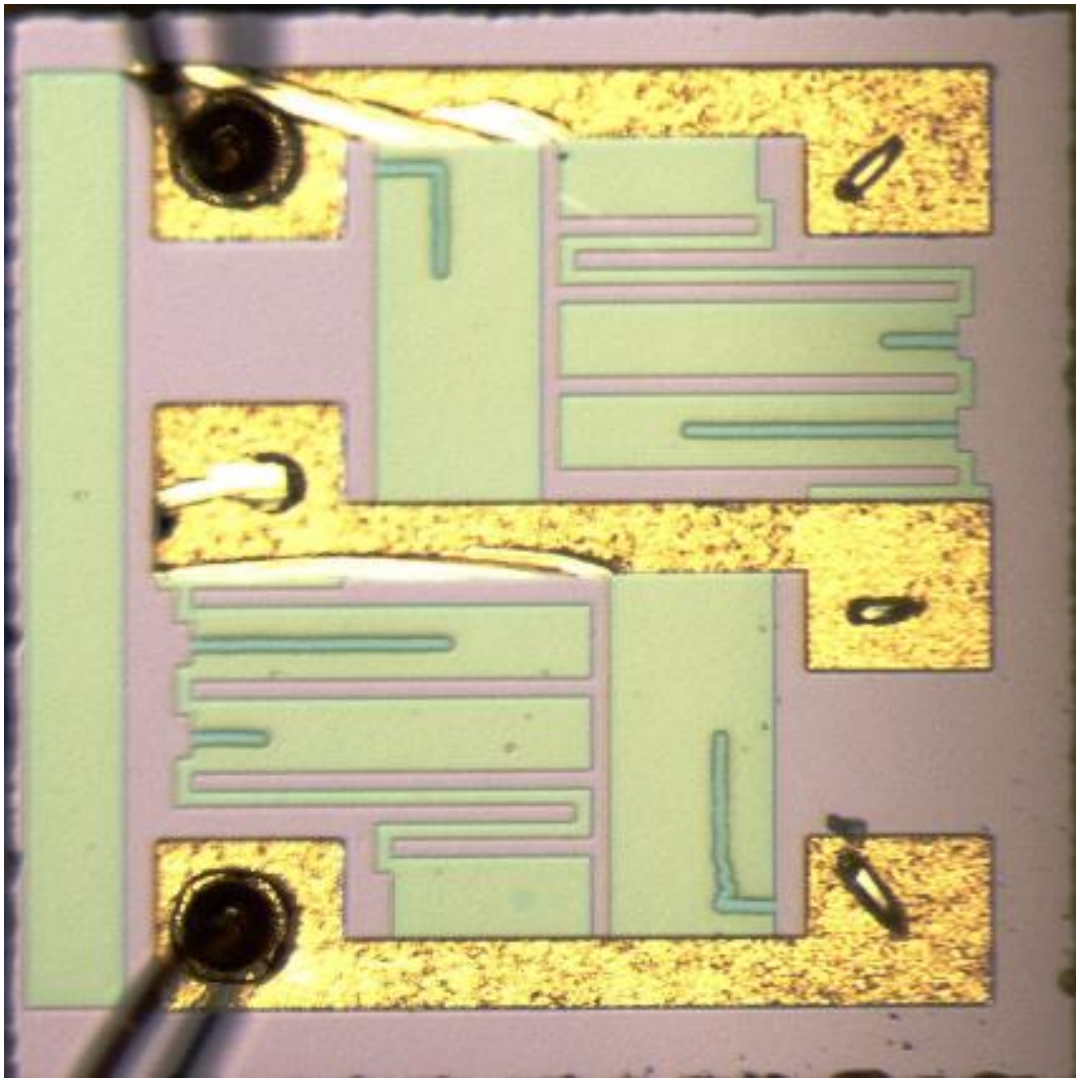


Ref: Howard Morgenstern

Thin Film Flow Chart

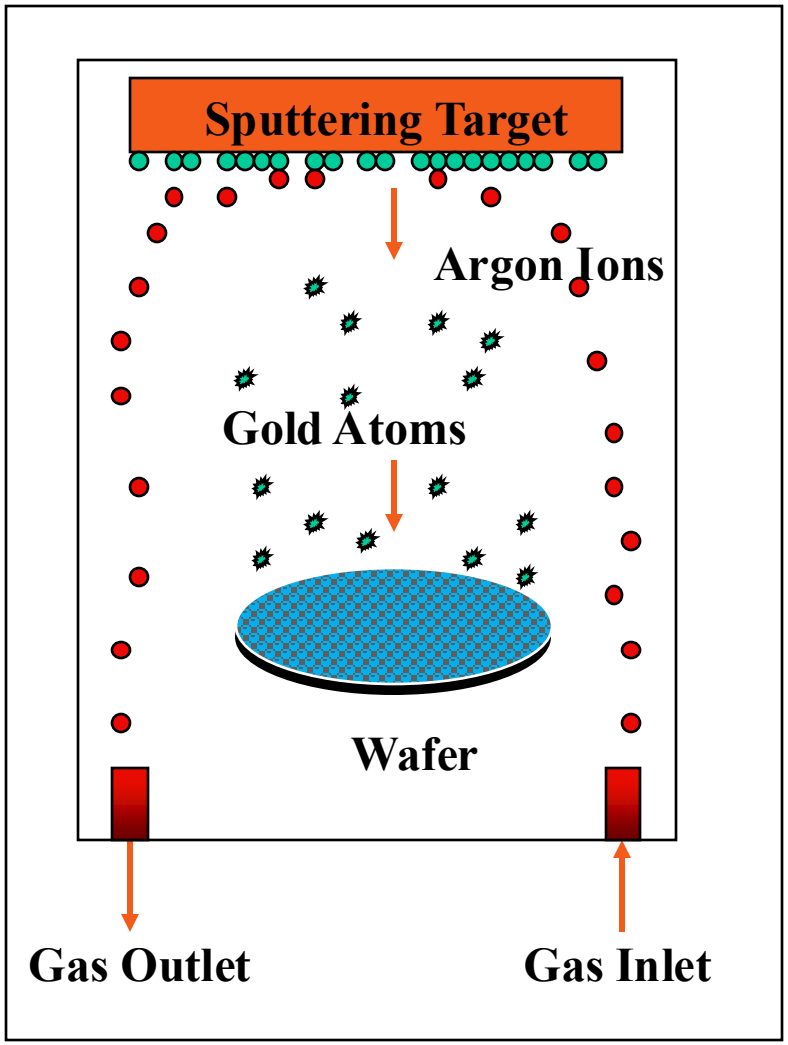


Trimmed Thin Film Precision Resistor



Au Sputter Deposition

- **Target is bombarded by plasma generated ions**
- **Gold plate is bombarded with ions dislodging gold atoms which migrate and settle onto the substrate.**



WATCH VIDEO

MRC Sputtering System

The Plating Process

Substrates are placed on a rack and lowered into a heated bath of plating solution. A current (usually a few hundred milliamps) is applied while the solution is agitated. Au is then plated out on the conductive areas to the desired thickness.

Thin Film Process Video

Electroplating Process Variables

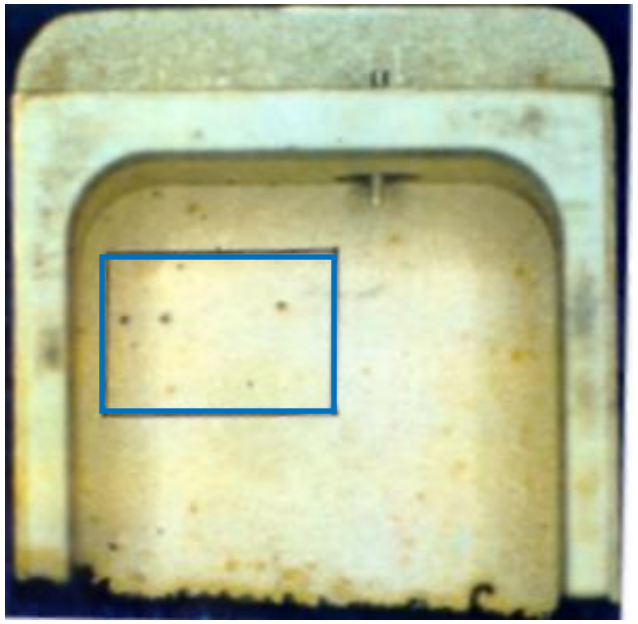
- Morphology and surface properties depend:
  - Current density to the plating tank
  - Bath impurity concentration
  - Power supply current waveform
  - Solution concentration
  - Bath temp and degree of agitation
  - Run area, plating rate, and time in bath

Defective Platings Cause Problems

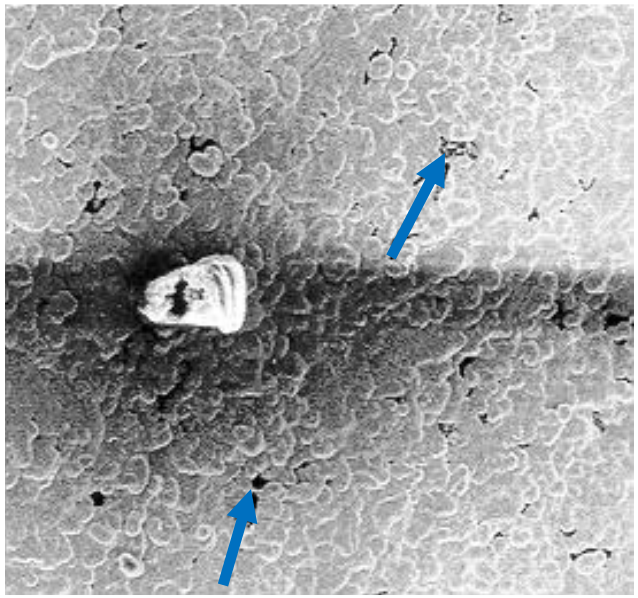
- The photo of the hybrid package on the following slide was identified during assembly and was defective due to improper plating……blisters were contaminants from the plating process
- The package was intended for use on a Space Program
- Failure Analysis found the gold plating to be porous and there were many particles on the surface that were oxides of Cu, Zn and/or Fe along with sodium, calcium and chlorine
- Bake out at 200C under vacuum caused some of the particles to “burst” on the surface and change color
- The cause and corrective action was to have the entire lot of packages stripped and re-plated

- Initial Kovar (FE-NI-Co alloy) Plating Spec (typical for a high rel package) was
  - 50 microinches of Ni Strike per QQ-N-290
  - 200-300 microinches of sulfamate nickel per AMS 2424B
  - 50-75 microinches gold per Mil-G-45204, Type III, Grade A

Plating Defects



Housing after 200°C for 2 hours



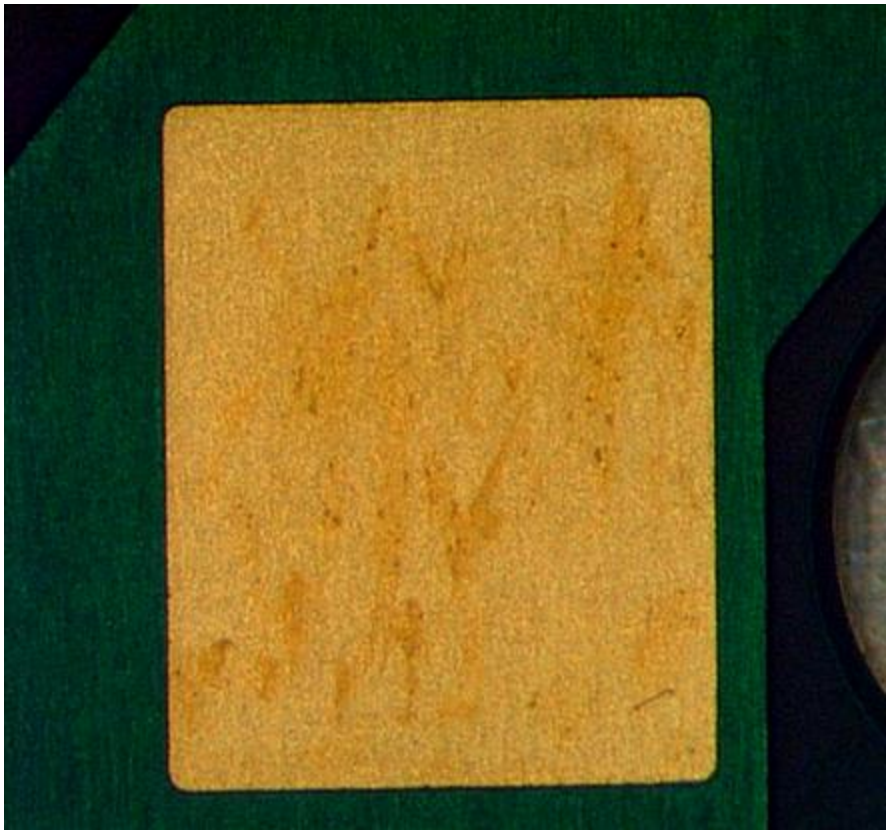
SEM photo (300 x) of crystalline particles and porosity. EDX spectra showed particles consisted of Ca, Cl, Fe, + O

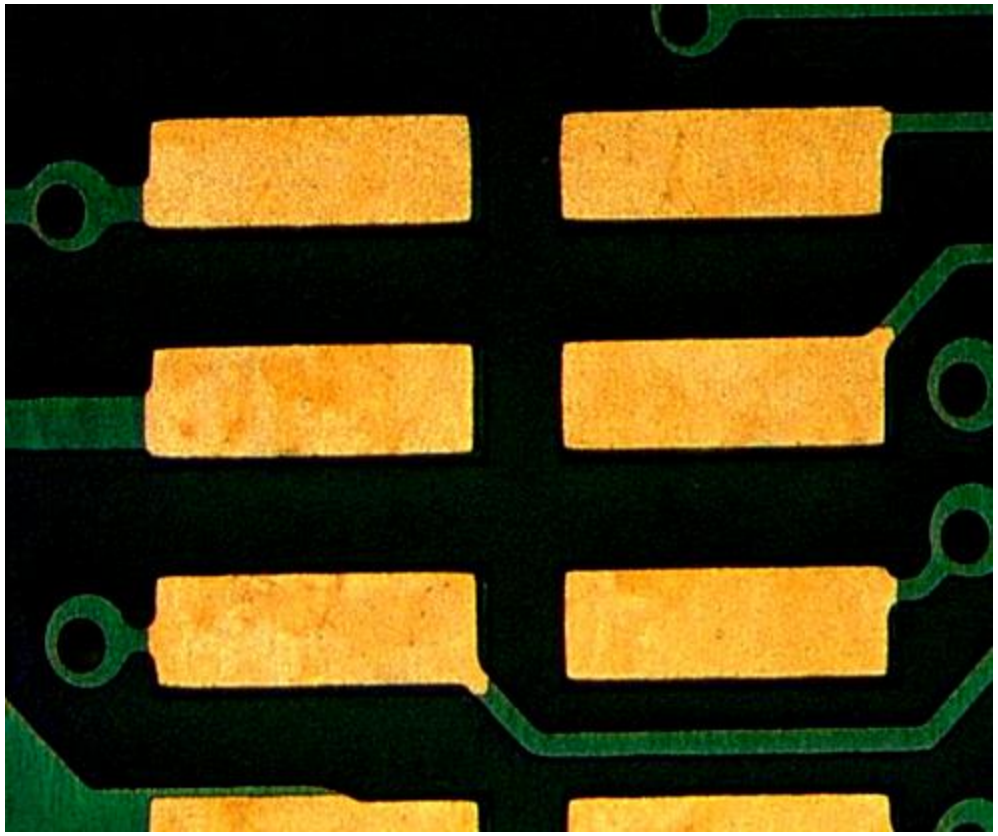
Wirebond Problems due to Poor Plating Processes

Following defects resulted from a poor a ENIG (Electroless Nickel Immersion Gold) Ref IPC 4552 plating process on FR-4 which was done incorrectly and caused a very serious wirebond problem. The 7 and 15 mil heavy aluminum wirebonds would not stick to the gold plated traces on the FR-4. All the circuit boards in stock had to be pulled and sent out for hydrogen plasma cleaning in order to remove the contamination left from the residual plating chemistries that were left on the surface.

Also shown are other common plating problems.

Contaminated FR-4 Traces

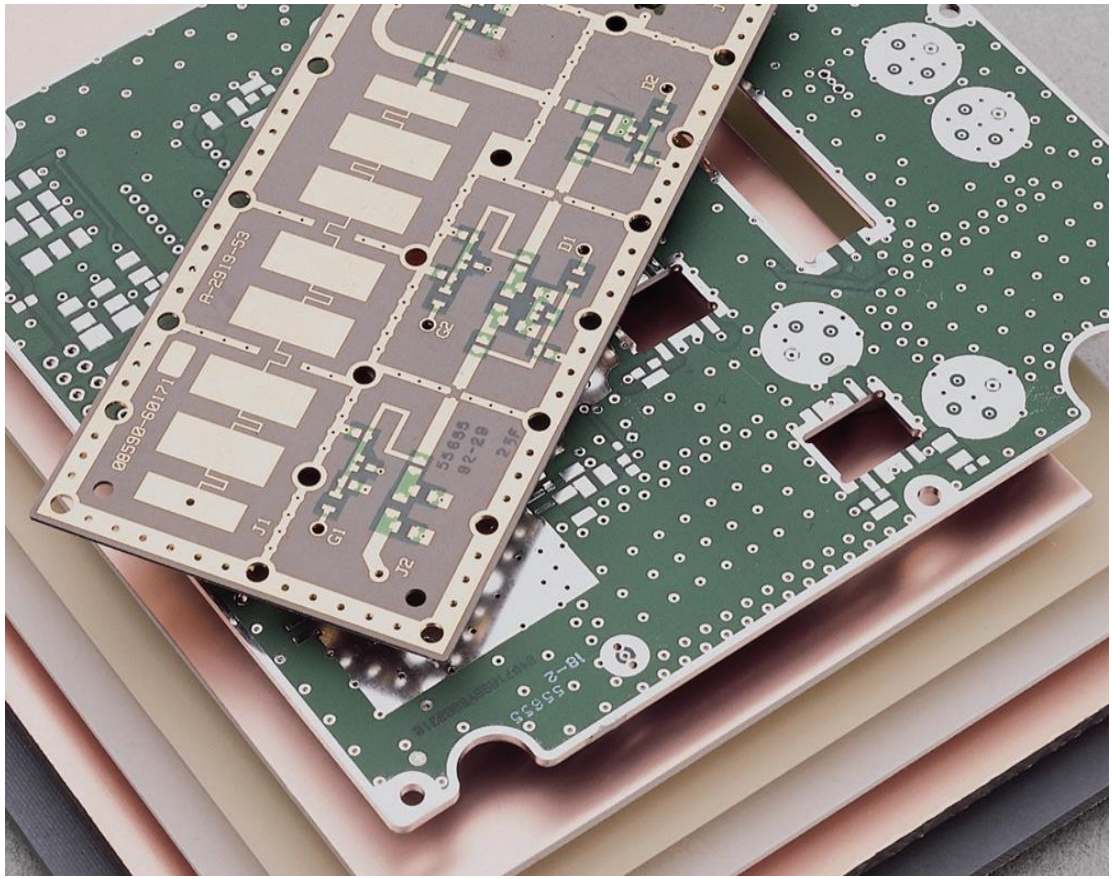




Orange-brownish stains due to improper cleaning at the supplier. PWBs with this type of contamination must be cleaned prior to wire bond and/or solder attach of power chips (40X)

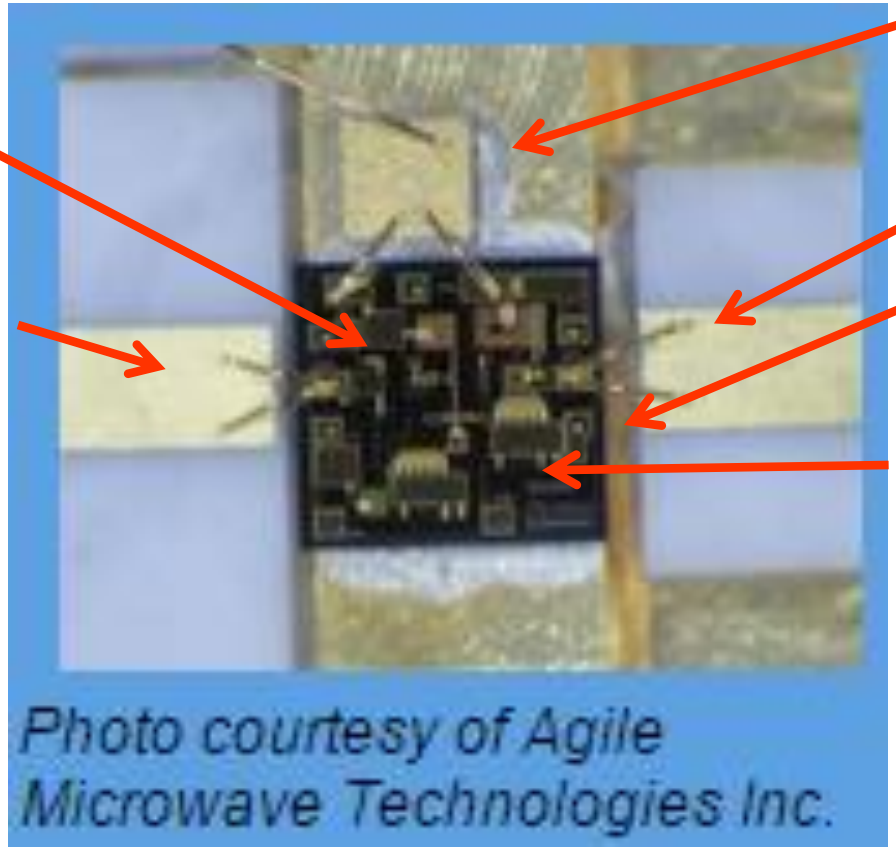
Duroid (PTFE) Boards

- Copper clad teflon boards with excellent RF properties
- Soft and flexible ..makes die bond and wirebond more of a challenge
- Rogers is a major supplier e.g. RT 5880
- RT 5880 glass fiber reinforced softens with heat



Epoxy
Component and Substrate Attach Materials /Process Fundamentals

MICROELECTRONIC PACKAGING



- Little "chips" …ICs, MMICs are placed into packages and then get connected with wirebonds or flipped over as in flip chips .
- These parts are then packaged in a cavity, or simply molded with epoxy in plastic packages. The idea is to protect the sensitive IC chips and little tiny wires that connect them to the outside world!.

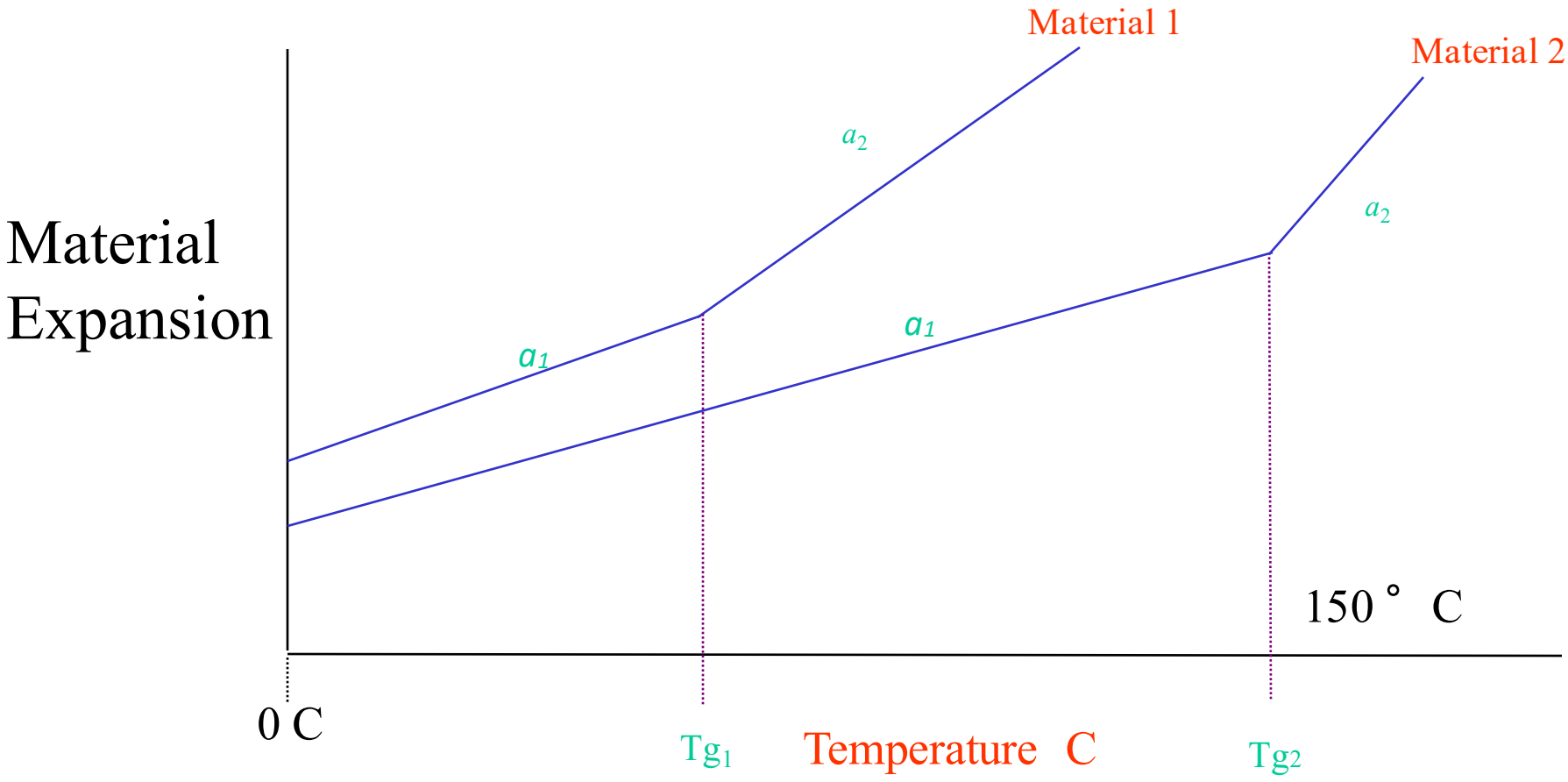
Physical Properties

- **Viscosity** is a measurement of how thick the epoxy is, it is the resistance to flow. In automated epoxy dispensing equipment the viscosity is very important to avoid problems such as tailing or epoxy runout. Sometime the dispensing tip and /or stage is heated to decrease the viscosity.
  - Viscosity measurements can vary widely depending on the type of viscometer used, measurement temperature and spindle size and speed
  - 25,000 cps at 10 rpm (23 C) is a typical viscosity number for a silver filled epoxy die attach material
- **Thixotropic index** is the viscosity ratio at two different speeds (typically 10:1). It is an indication of how the material's viscosity changes in response to a shear force. This is an important issue during high speed automatic dispensing processes. 2.5 - 5.0 is a typical thixotropic index value.
- **Work Life or pot life** the amount of time the uncured material remains fit for use in the intended application. Time it takes for the material to increase in viscosity by some percentage value

Physical Properties

- **T_g is the Glass Transition Temperature**. This is the temperature at which point the epoxy begins to soften, which may create problems during subsequent processes if this temperature is exceeded.
- **Coefficient of Thermal Expansion or CTE** defines the degree to which a material will change its shape/dimensions under the influence of temperature. Two values , above and below the Tg are reported. A typical epoxy CTE of 30 X 10^{-6} in/in/°C means that a one inch long sample of cured epoxy will expand approx. 30 millionths of an inch for every °C rise in temperature.
- **Modulus of Elasticity** is a general term describing the flexibility of an adhesive, a higher flexural modulus indicates a harder, stiffer material. The tensile modulus (also known as Young's modulus), is difficult to measure but often used in FEA analysis. 500,000 lbs./in^2 is a typical modulus of elasticity.
- **Thermal Conductivity** describes how well heat is transferred through the epoxy. Typical silver filled epoxies are less than 3 Watts/m °K
- **Volume Resistivity** describes the electrical conductivity of the material. 0.0002 Ω-cm for a silver filled epoxy is typical

Glass Transition Temperature T_G



Epotek H35-175MP Epoxy Data Sheet

Typical Properties: *(To be used as a guide only, not as a specification. Data below is not guaranteed. Different batches, conditions and applications yield differing results; Cure condition: 180°C/1 hour; * denotes test on lot acceptance basis)*

Physical Properties:	
*Color: Bright Silver	Weight Loss:
*Consistency: Smooth, Thixotropic Paste	* @ 200°C: 0.13%
*Viscosity (@ 10 RPM/23°C): 22,000 – 28,000 cPs	@ 250°C: 0.14%
Thixotropic Index: 4.0	@ 300°C: 0.28%
*Glass Transition Temp.(Tg): ≥ 100°C (Dynamic Cure 20—300°C /ISO 25 Min; Ramp -10—200°C @ 20°C/Min)	Operating Temp:
	Continuous: - 55°C to 200°C
Coefficient of Thermal Expansion (CTE):	Intermittent: - 55°C to 300°C
Below Tg: 31 x 10^{-6} in/in/°C	Storage Modulus @ 23°C: 1,106,623 psi
Above Tg: 97 x 10^{-6} in/in/°C	*Ions: Cl^- < 200 ppm
Shore D Hardness: 83	Na^+ < 50 ppm
Lap Shear Strength @ 23°C: > 2,000 psi	NH_4^+ 39 ppm
*Die Shear Strength @ 23°C: ≥ 10 Kg / 3,400 psi	K^+ < 50 ppm
Degradation Temp. (TGA): 372°C	*Particle Size: ≤ 20 Microns
Electrical Properties:	
*Volume Resistivity @ 23°C: ≤ 0.0005 Ohm-cm	
Thermal Properties:	
Thermal Conductivity: 1.46 W/mK	

- Certified to MIL-STD 883/Test Method 5011 –yields low levels of water extractable monovalent ions such as Chlorides.
- Passes NASA low outgassing standard ASTM E595 with proper cure - http://outgassing.nasa.gov/

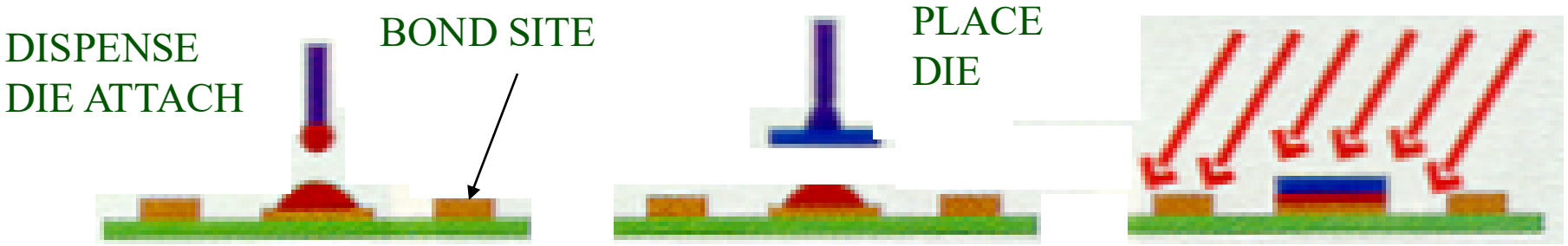
Epoxy Material &Process Issues

- Conductive vs. non-conductive
- Pot Life
- Rheology (the study of flow and material deformation)…viscosity (the resistance to flow)
- Cure Schedules..
- Ionic Contamination
- Electrical and thermal conductivity properties
- Reworkability
- Processing issues: Bleedout
- TM 5011 Certifications

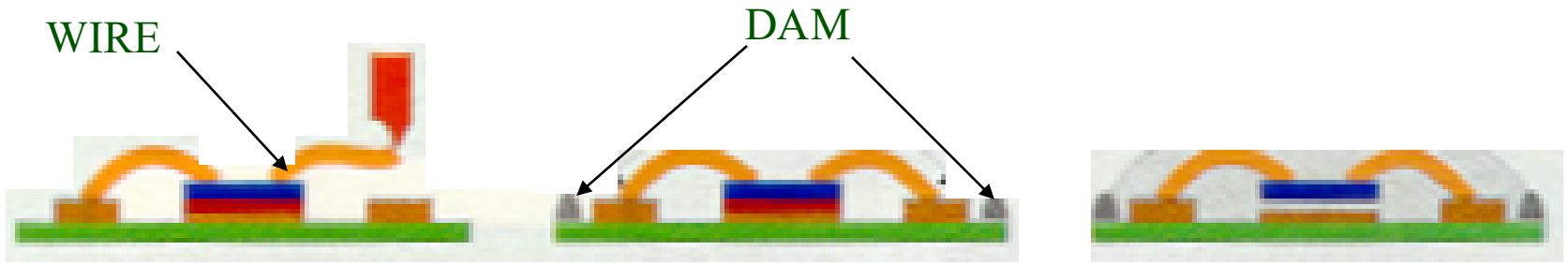
TM 5011 ….Evaluation and Acceptance Procedures for Polymeric Adhesives

- User and supplier responsibilities for certification and acceptance testing to assure clean/consistent material from lot to lot
- Viscosity and pot life checked and measured
- Shelf life…….12 months at -40C
- IR spectrum of uncured material supplied
- TGA analysis required to determine thermal stability
- Outgassed materials test <5000 ppm
- Ionic impurities tested Na, K, F, along with total ionic content
- Other tests; coefficient of linear expansion, thermal conductivity, volume resistivity, dielectric constant, bond strength and the sequential test environment

DCA Process Flow

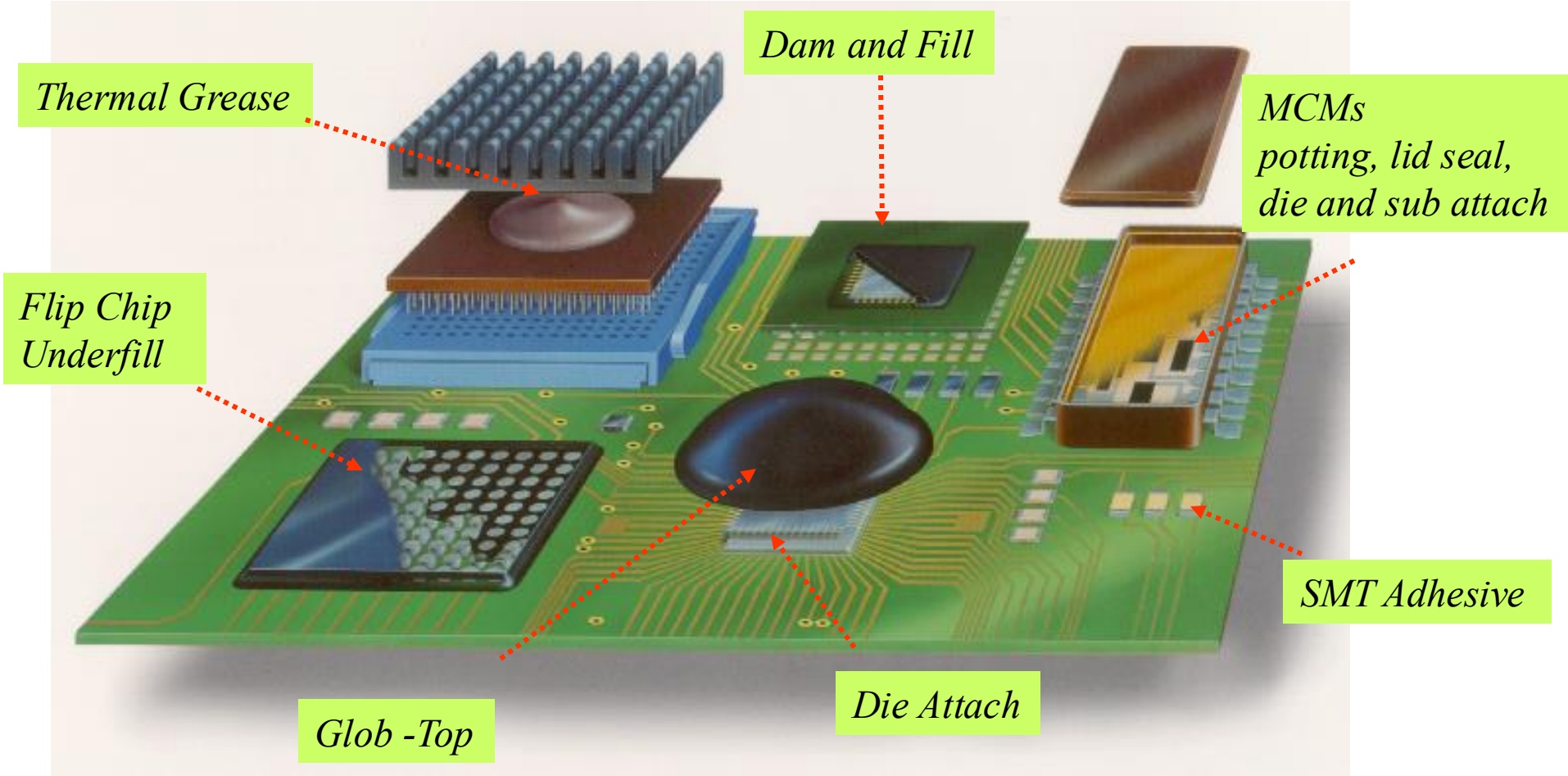


ADHESIVE PLACEMENT HEAT CURE



WIRE BOND DAM FORMATION ENCAPSULATE

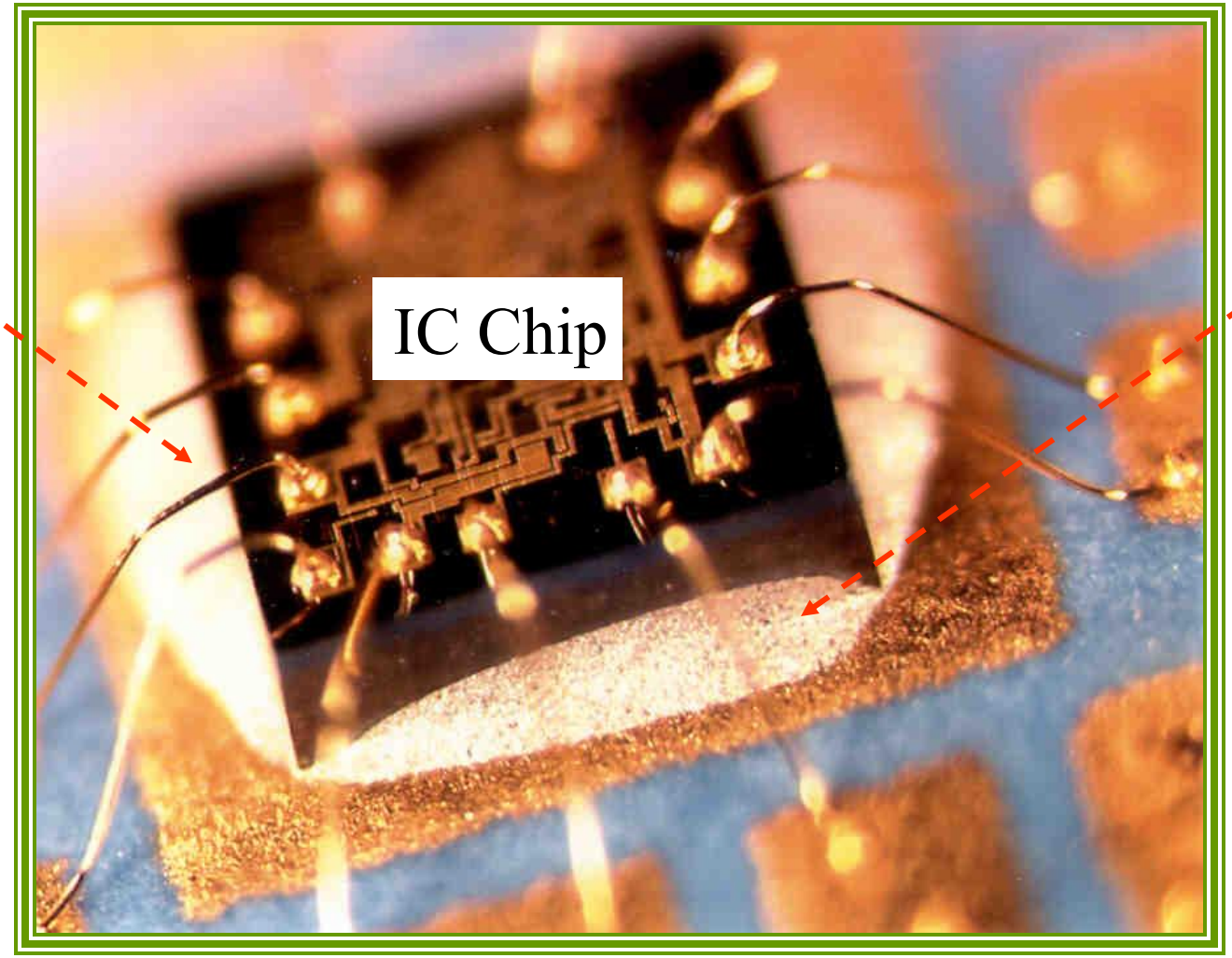
Critical Fluid Dispensing Technologies



Ref: Lord Corp Photo

ACCEPT

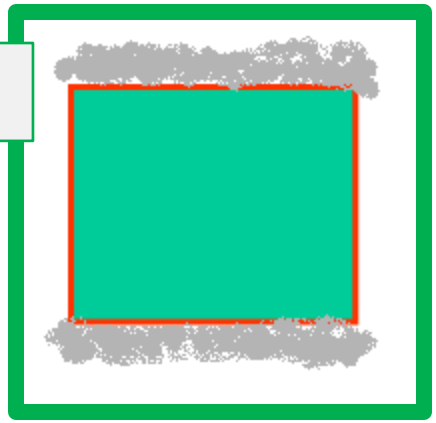
Epoxy Mount IC Chip 45°



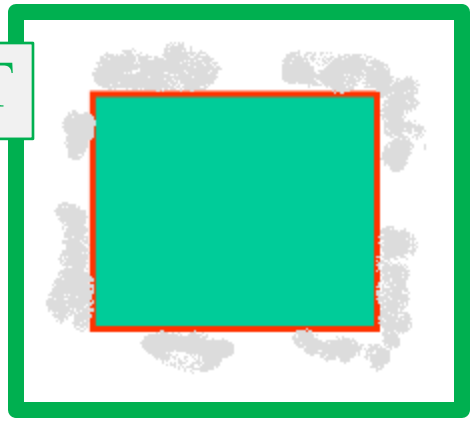
NOTES: Preferred condition.. good epoxy climb up the side wall of the IC chip (200X)

TM 2017 Element Attach Criteria
(Evidence of wetting or adhesive visible)

ACCEPT

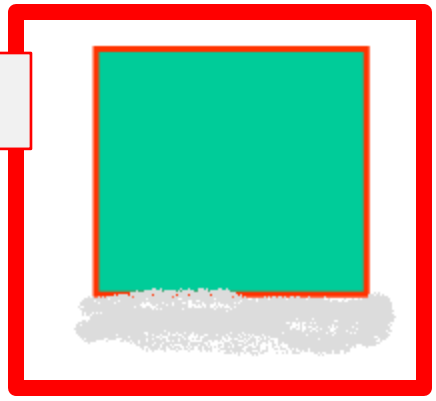


ACCEPT



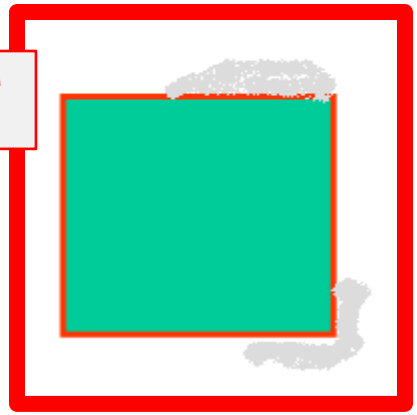
2 Complete Sides OR 50% of the Element Perimeter

REJECT



One side only

REJECT



Insufficient eutectic flow

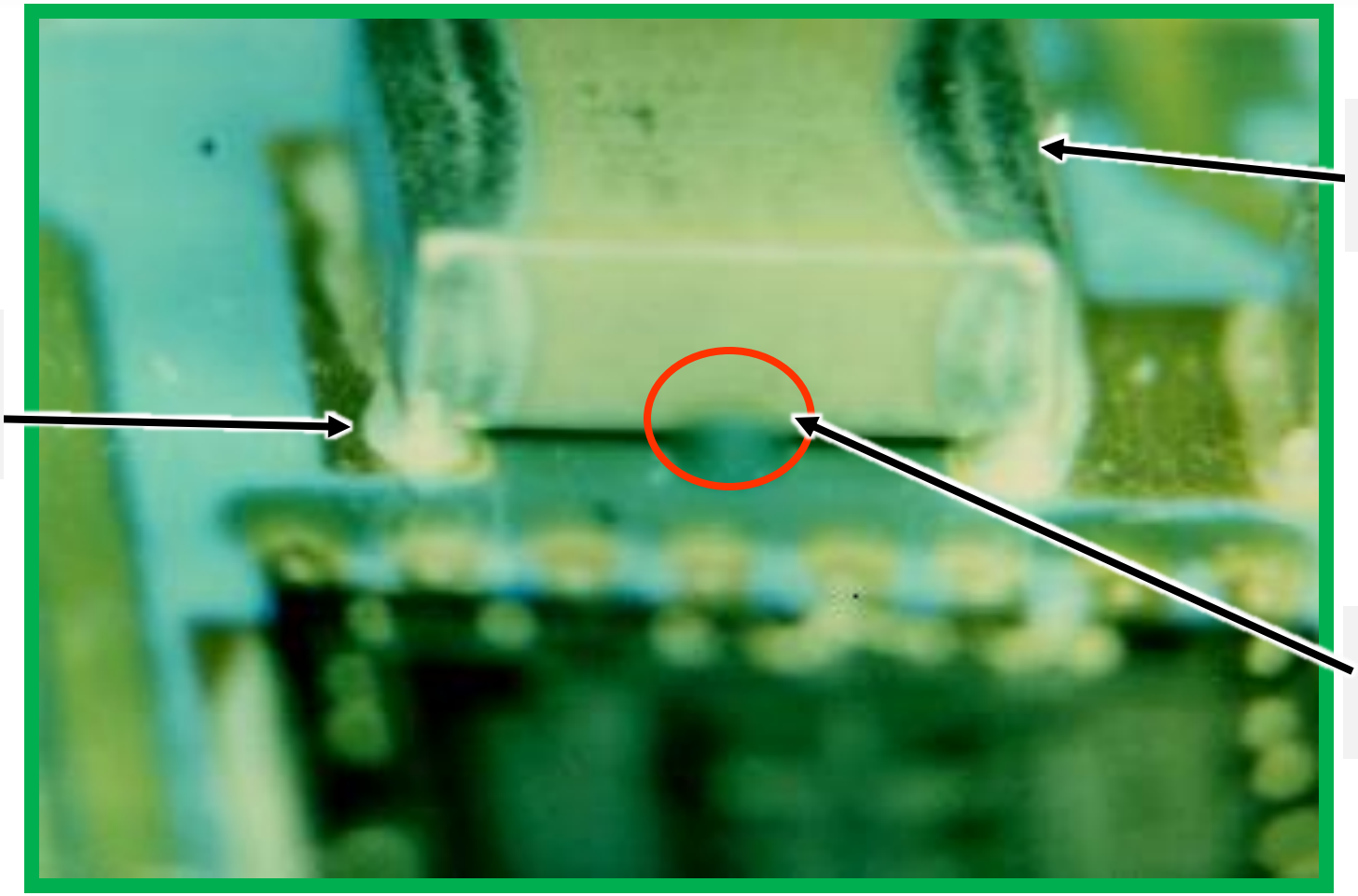
TM 2017 Para. 3.1.2.2.b

Things to Look for after Die Attach

- Surface flatness is very important
- Cleanliness of the bonding surface
  - Resin bleed..vacuum bake prior to die attach seems to help/control resin bleed…plasma clean may make matters worse
  - Residual epoxy, contaminated films from oven cure process etc..
  - Discolored platings or package pins
- Use caution when cleaning off wet epoxy prior to cure…if epoxy is not completely removed it will interfere with wirebonding
- During the epoxy auto dispensing sequence residual epoxy material is sometime transferred via the pick up collets to the chip topside, also stringing of the epoxy is common
- Auto wirebonder does not detect residual epoxy on surface
- Other forms of foreign material contamination (e.g. gel pack contamination, finger oils etc..)

Stake Bonded Chip Capacitor

ACCEPT

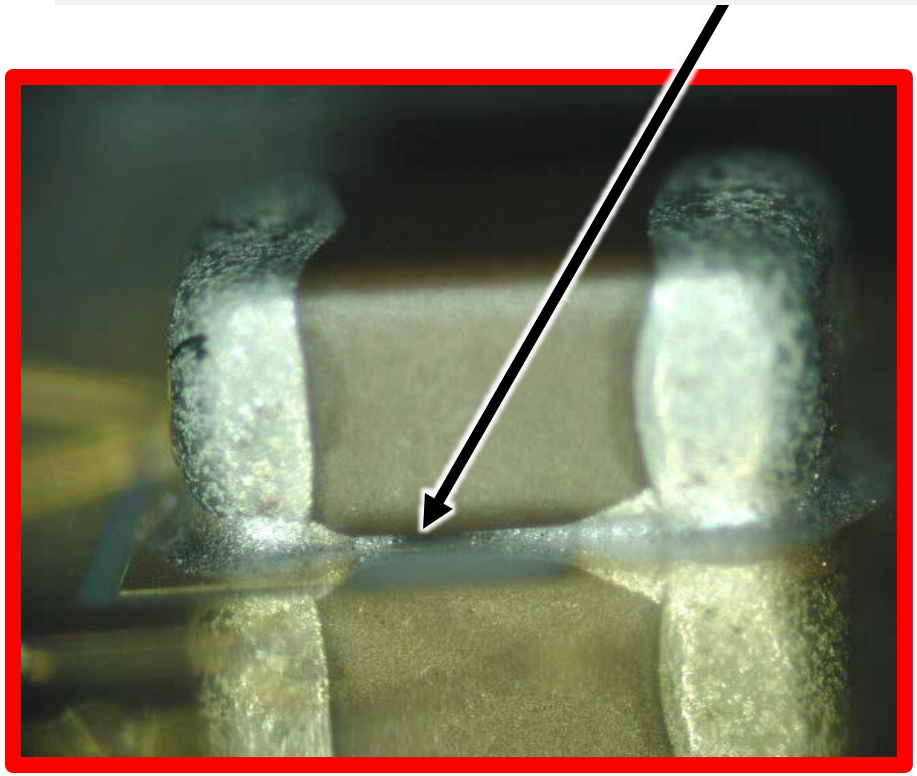


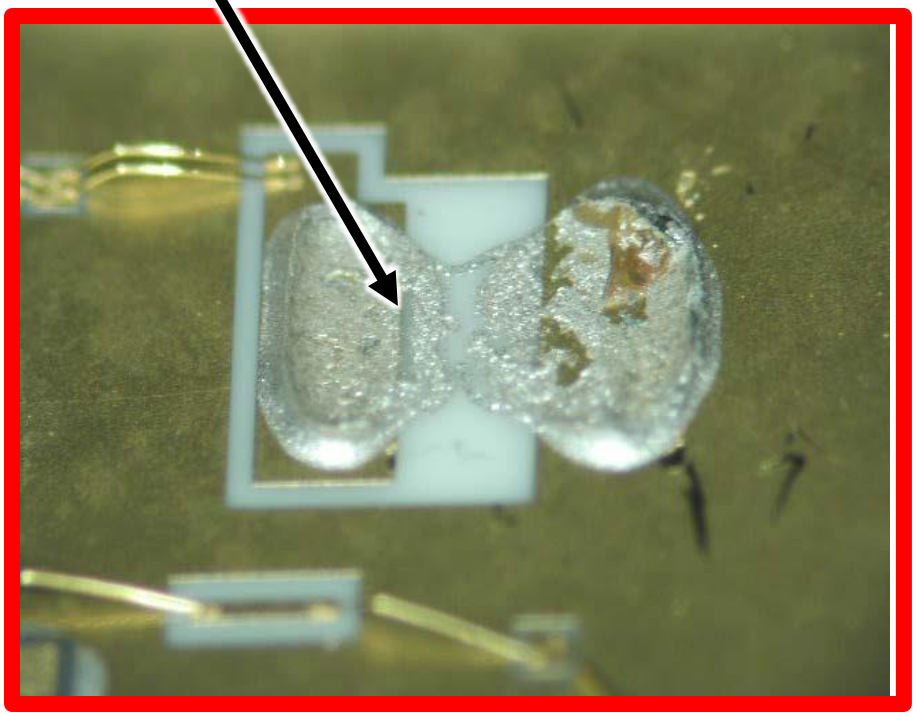
ACCEPT: Photo shows a large ceramic chip capacitor with non-conductive staking compound added to the body of the component to add strength and prevent a failure during centrifuge testing. Conductive silver epoxy is used on the end terminations. (12X)

Multilayer Ceramic Capacitor -Short

REJECT

Excess epoxy caused a short on underside of capacitor, verified after component removal as shown in picture on the right.

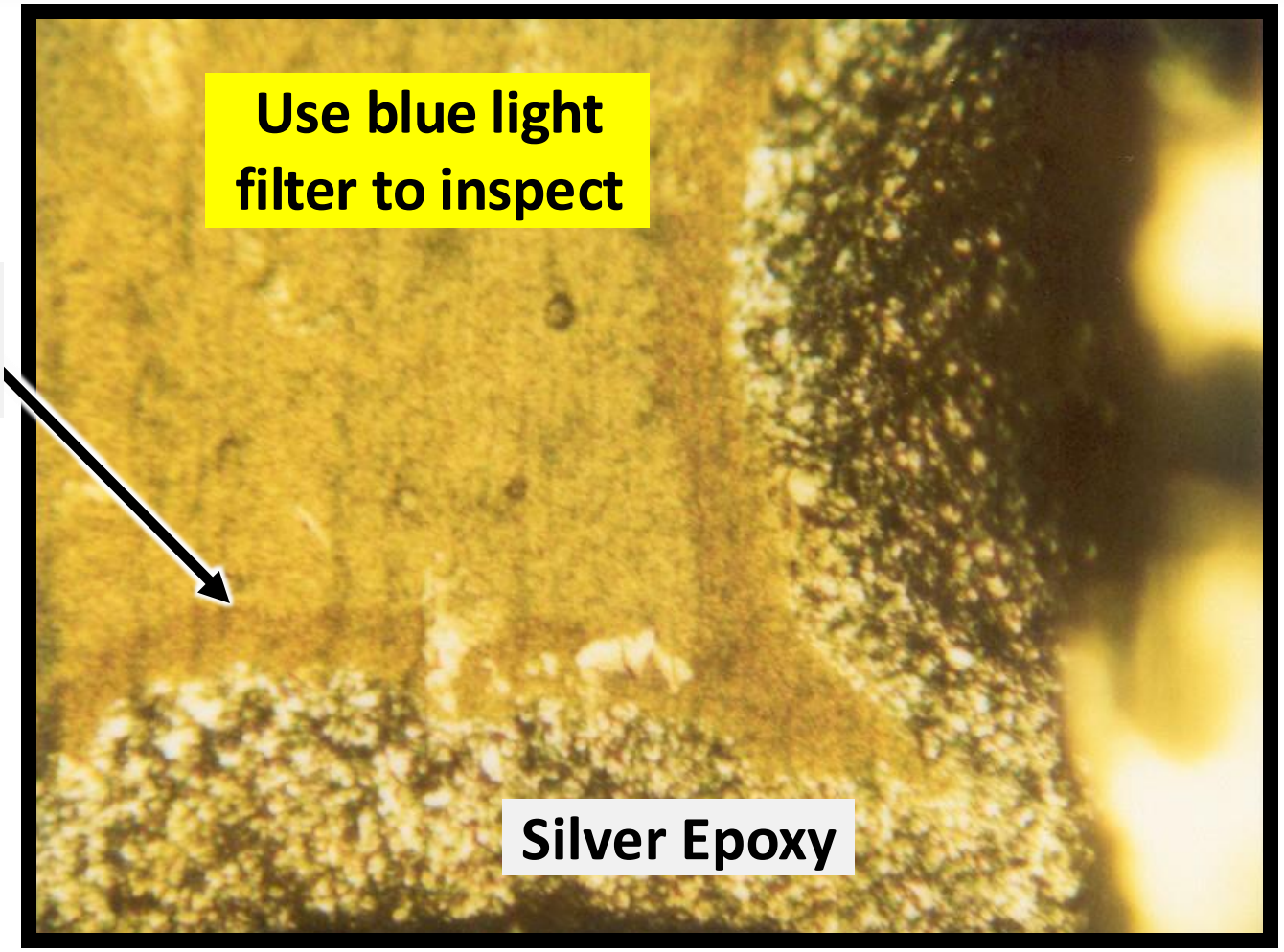




d. Evidence of conductive adhesive under the body of the element that reduces the spacing between attached metallization, or end terminations, whichever is smaller, by more than 50% as viewed from the side (this applies whether or not staking adhesive is used).

TM 2017 Para. 3.1.2.1.d

Epoxy Resin Bleed

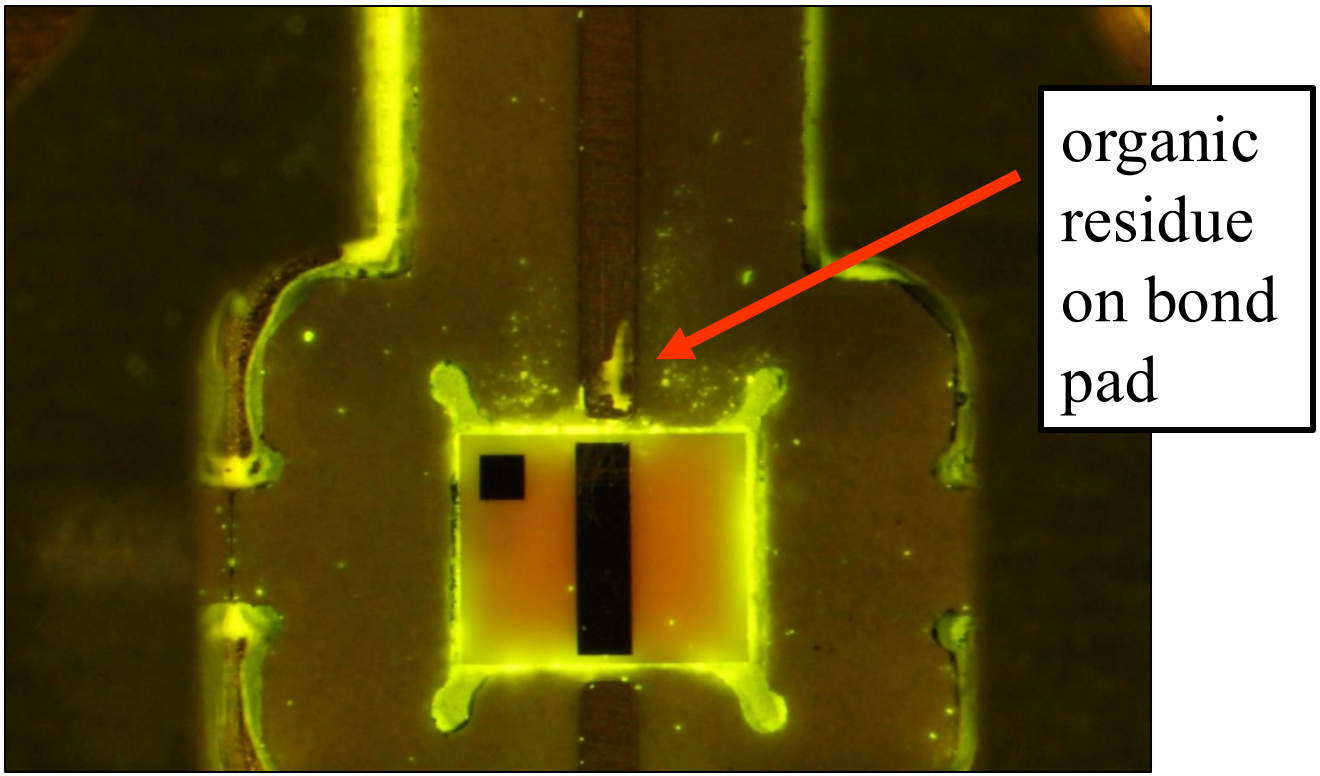


Do not wirebond within 5 mils of the silver epoxy or any resin that may bleed out from the epoxy. The discoloration shown above is resin bleed and is a common problem. A wirebond that happens to stick to the resin is a potential latent defect in the unit.

TM 2017 Para. 3.1.5.8.m

UV Blue Light Fluorescence Technique

NOTE: Criteria of 3.1.5.8 (m) can be excluded when the absence of material or residue within 1 mil of wire bond can be confirmed with ultraviolet, blue light fluorescing, or equivalent techniques.

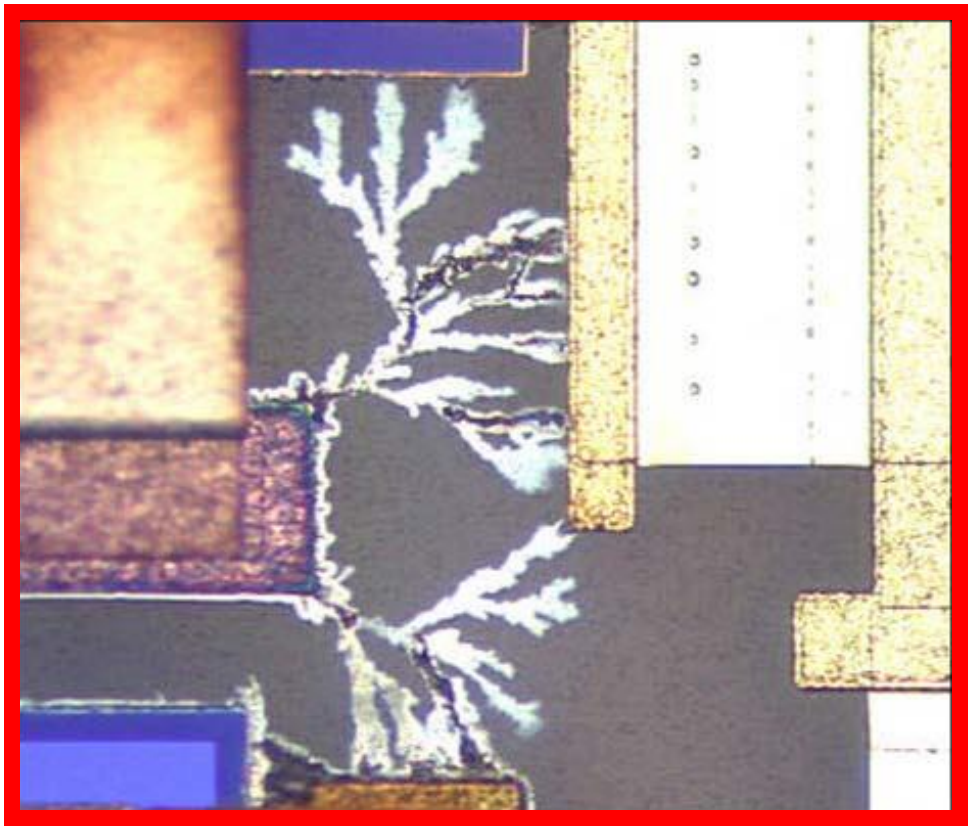


It is possible to readily visualize epoxy resins other organic contaminants on gold bond pads and surfaces with a 460nm blue LED illumination and a 515 nm long pass filter. These surface contaminants would otherwise not be visible under normal lighting conditions.

REF : "Visual Identification of Organic Residue on Microelectronic Components via In- Process Visible Light Fluorescence" Presented the CMSE conference in LA, CA 2018 by Tristan Baldwin BAE Systems Nashua, NH

Silver Dendrites Cause Short Circuits

REJECT

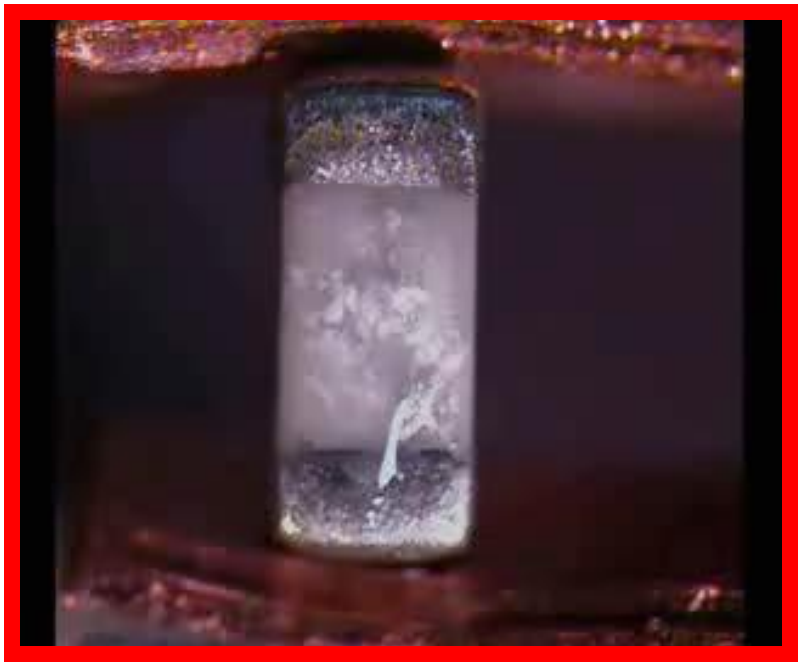


Ref: "Electrolytic Electro-migration of Metallic Material and Silver Filled Epoxy" IEEE Transactions on Reliability, Vol 44, No. 4, 1995 December.

SHOW DENDRITE VIDEO

TM 2017 Para. 3.1.2.1.g

Electrochemical Migration (ECM)



Dendrite formation is an ionic process which requires an electrolyte, bias voltage and time.

This capacitor exhibits some flux residue and alcohol (simulate moisture). It took only 2.5Vdc and 35 seconds for this dendrite to develop across the capacitor.

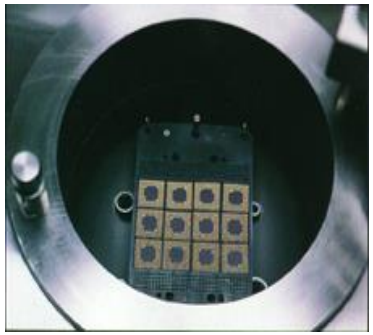
Solder Processing

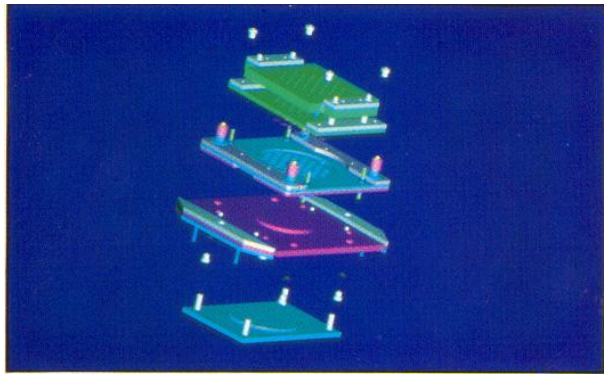
- Manual Process..Using a hot plate operator controls time and temperature
- Furnace ..Reflow in a belt furnace with clips or weighted fixtures for high volume production, belt speed, zone temps, and atmosphere critical
- Belt Reflow…Direct contact of substrate to belt belt speed and zone temp critical no atmosphere control
- Vapor Phase..Process profile controlled by regulating rate of descent & ascent into vapor, as well as dwell times
- Eutectic semiautomatic die attach with “scrubbing” to break up the oxides
  - Requires selective heating..heated collets, heated cover gas, IR added, heated work stage AuSi, AuGe
- Vacuum Soldering…Precise atmospheric control.. AuSn

Solder Processes

- Many solders are available for component attach
  - Electrically conductive only
  - Better for heat transfer…about ten times better than most epoxies
- The flux used in most soldering processes is a highly aggressive organic acid. When the ionic contamination mixes with moisture there are many well known reliability and manufacturing problems that result
- Design the product/process so all the flux assisted operations are performed before epoxy attach of sensitive ICs and thin film resistor networks
  - This allows for easy clean up of the flux residue without damage to the exposed metal and sensitive die structures like air bridges

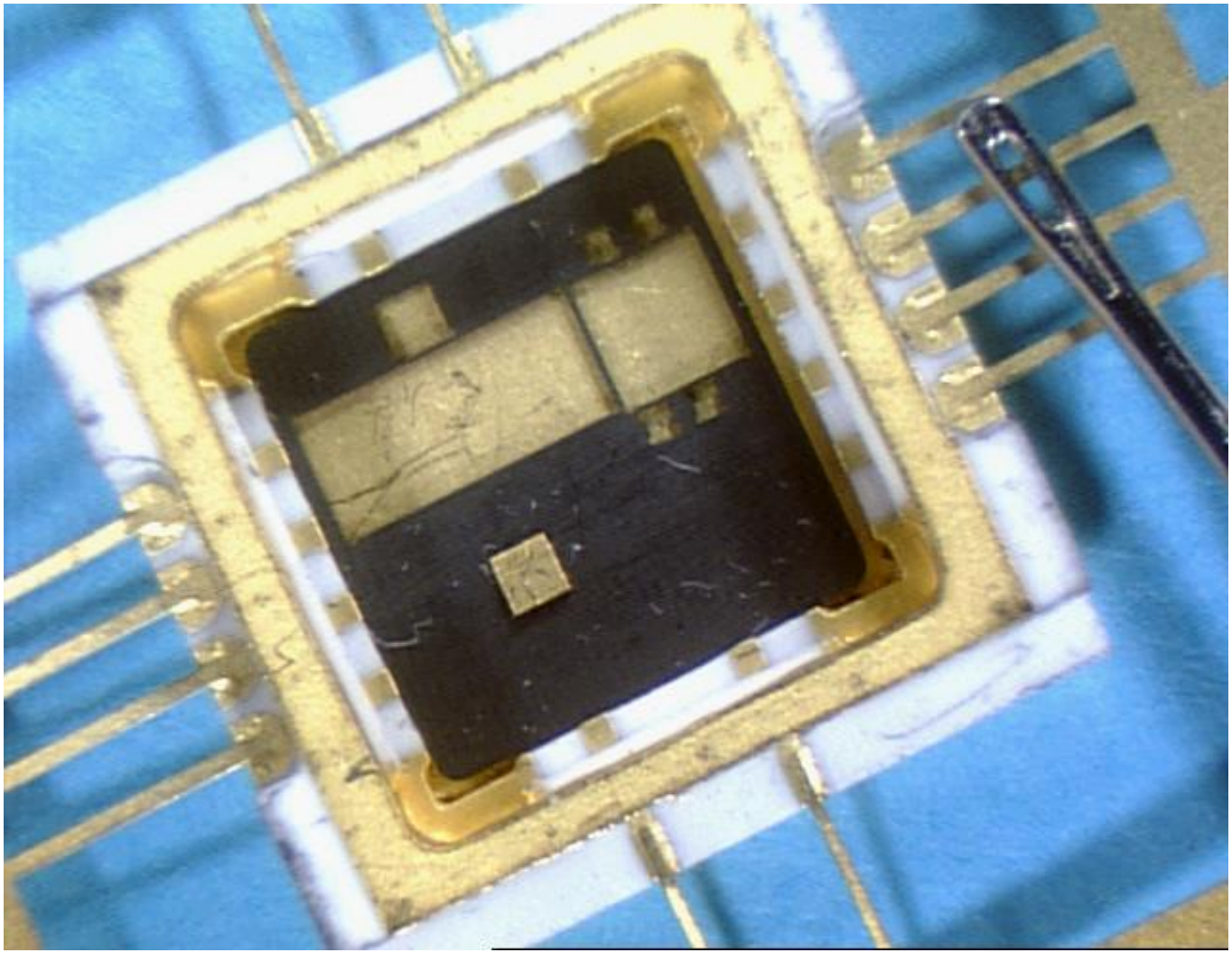
Vacuum Soldering Equipment





Ref SST

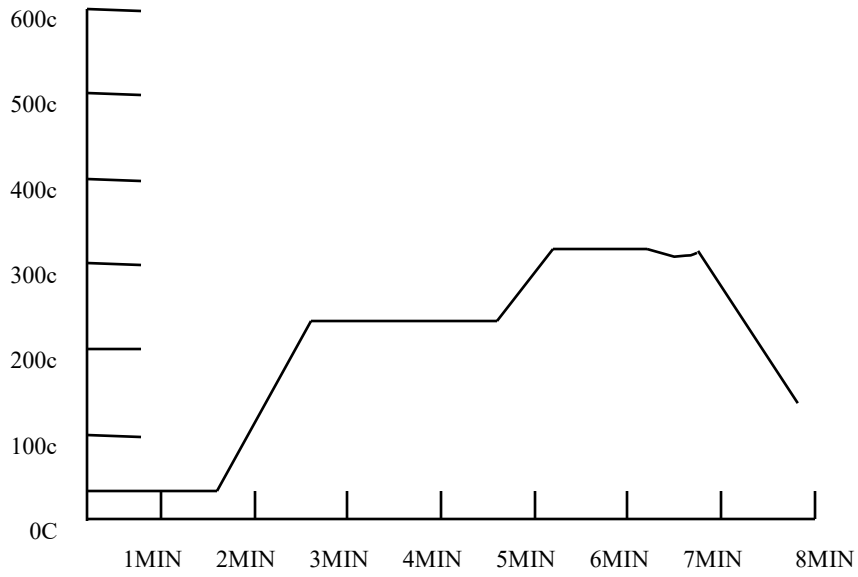
INSERT FITS WITHIN PACKAGE AND IS USED TO LOCATE COMPONENTS



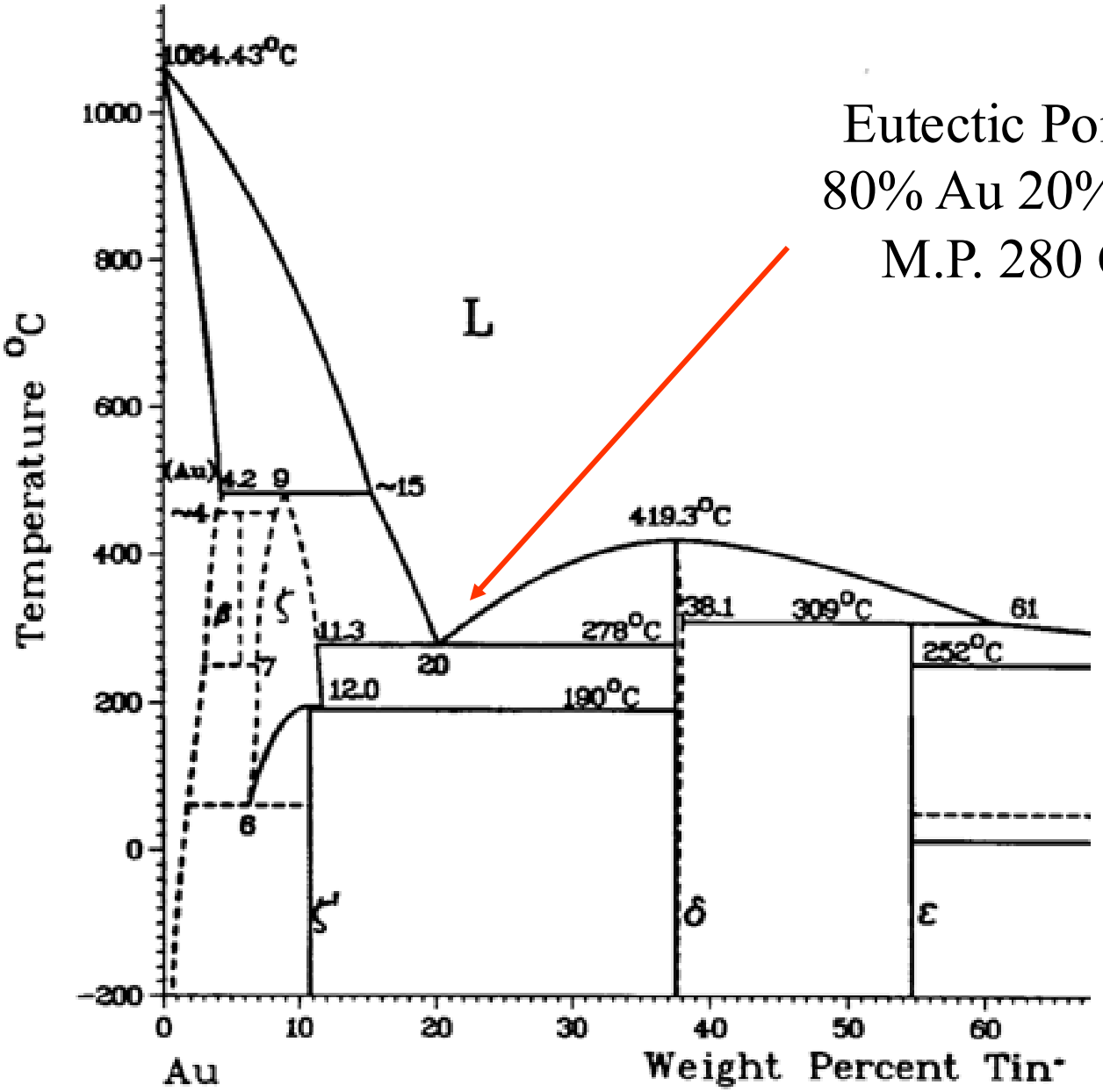
Ref: SST International

Vacuum Soldering

- Precise control of time, temp, vacuum and backfill conditions, fully programmable
- Resistive heating via graphite boats and piece part carriers
- AuSn Profile
  - 1st minute…cycle vacuum and N2 purge
  - 2 minutes of …240 C vacuum bake
  - at 4 min. mark introduce N2 for thermal reason
  - Peak to 325 C for seconds
  - Add N2 at 30 PSIG (to help with voiding)
  - and hold for one minute
  - Turn heater off and vent using an N2 purge



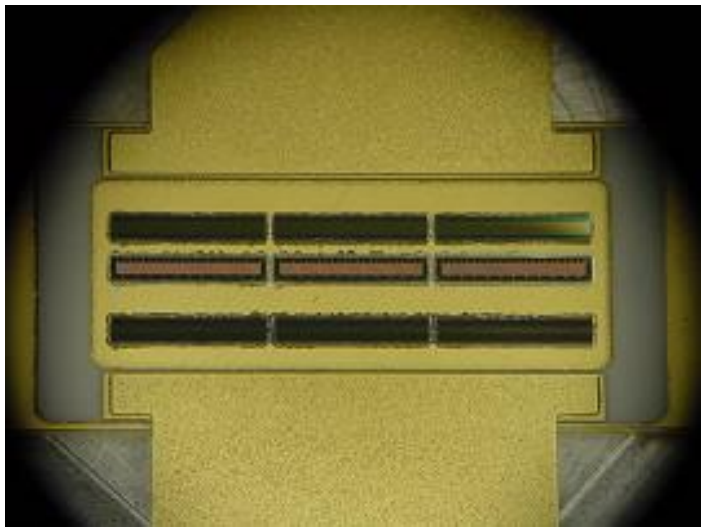
Au Sn Eutectic



Eutectic Point
80% Au 20% Sn
M.P. 280 C

Automatic Eutectic Die Bonding

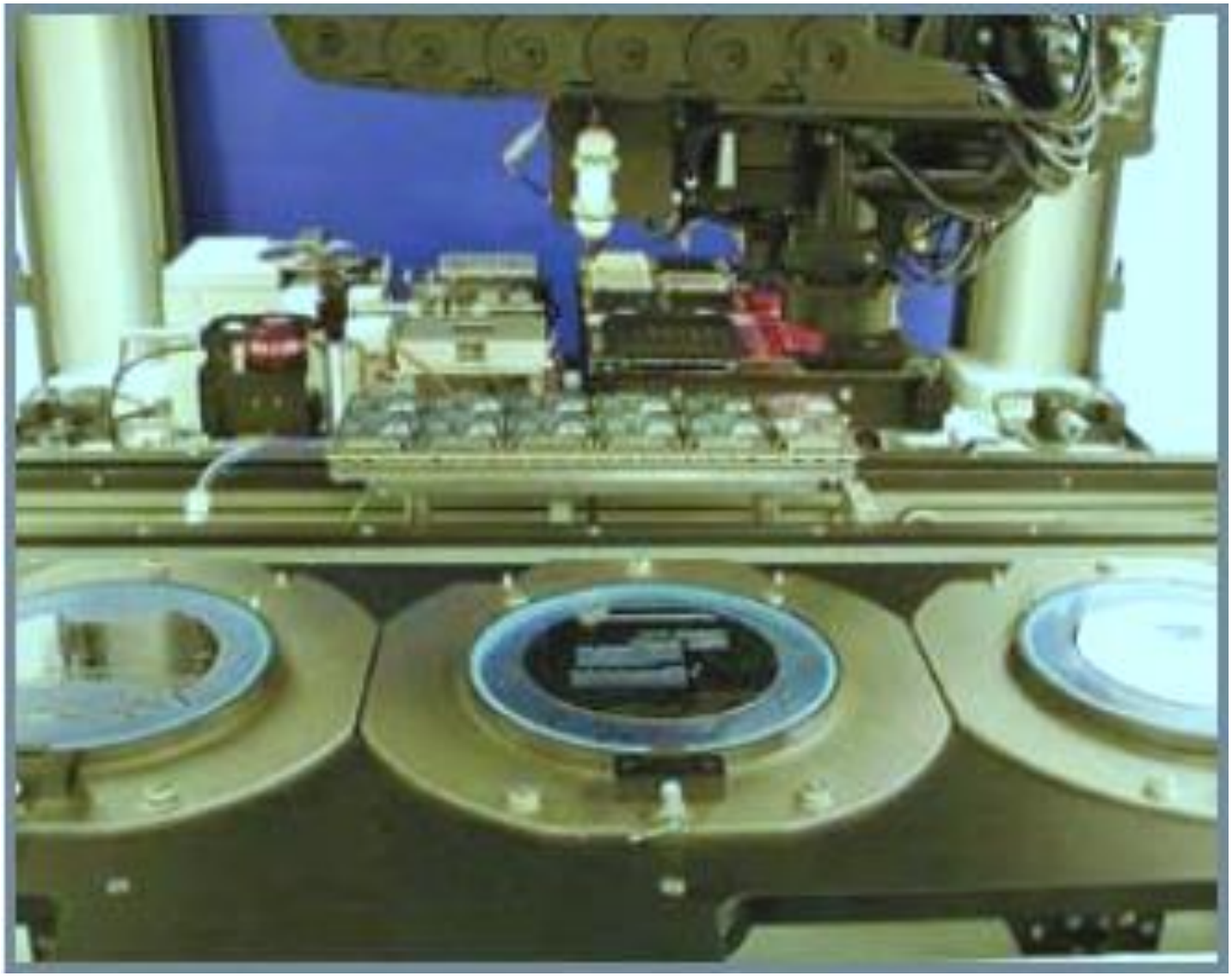
- Process Parameters:
  - Stage heat
  - Delay before scrub
  - Scrub time and amplitude (# of cycles)
  - Force..Very important!
  - Collet selection and sizing (i.e. two sided vs. 4 sided collets)
  - Inert gas flow over chip surface



AuSi eutectic attach of RF chips to header

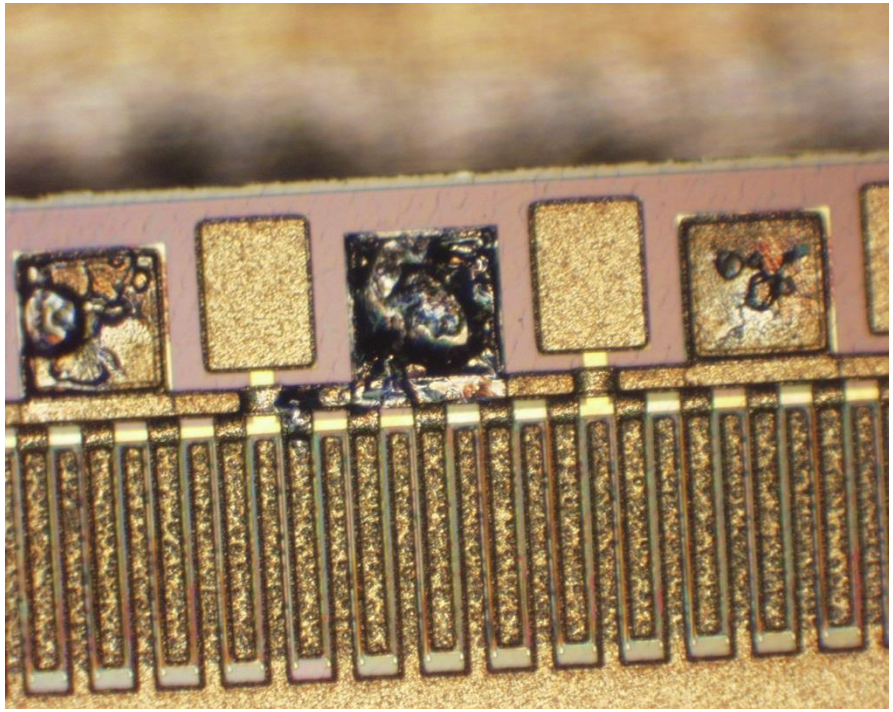
Photo Ref: Palomar website

Auto Pick Place and Scrub

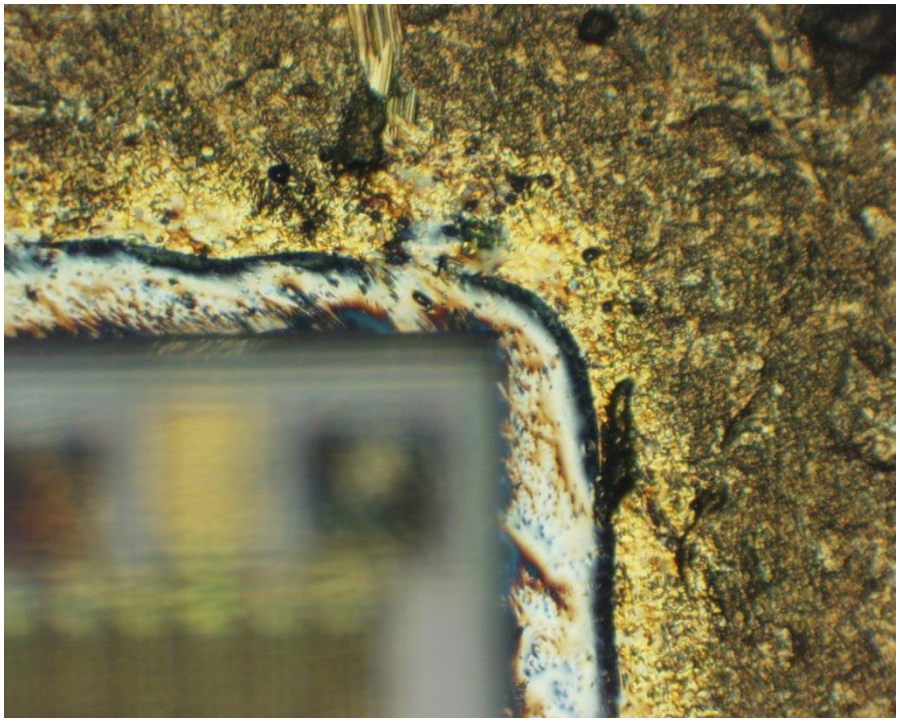


Palomar Pick and Place Eutectic Scrub VIDEO

Eutectic Solder Flow Patterns

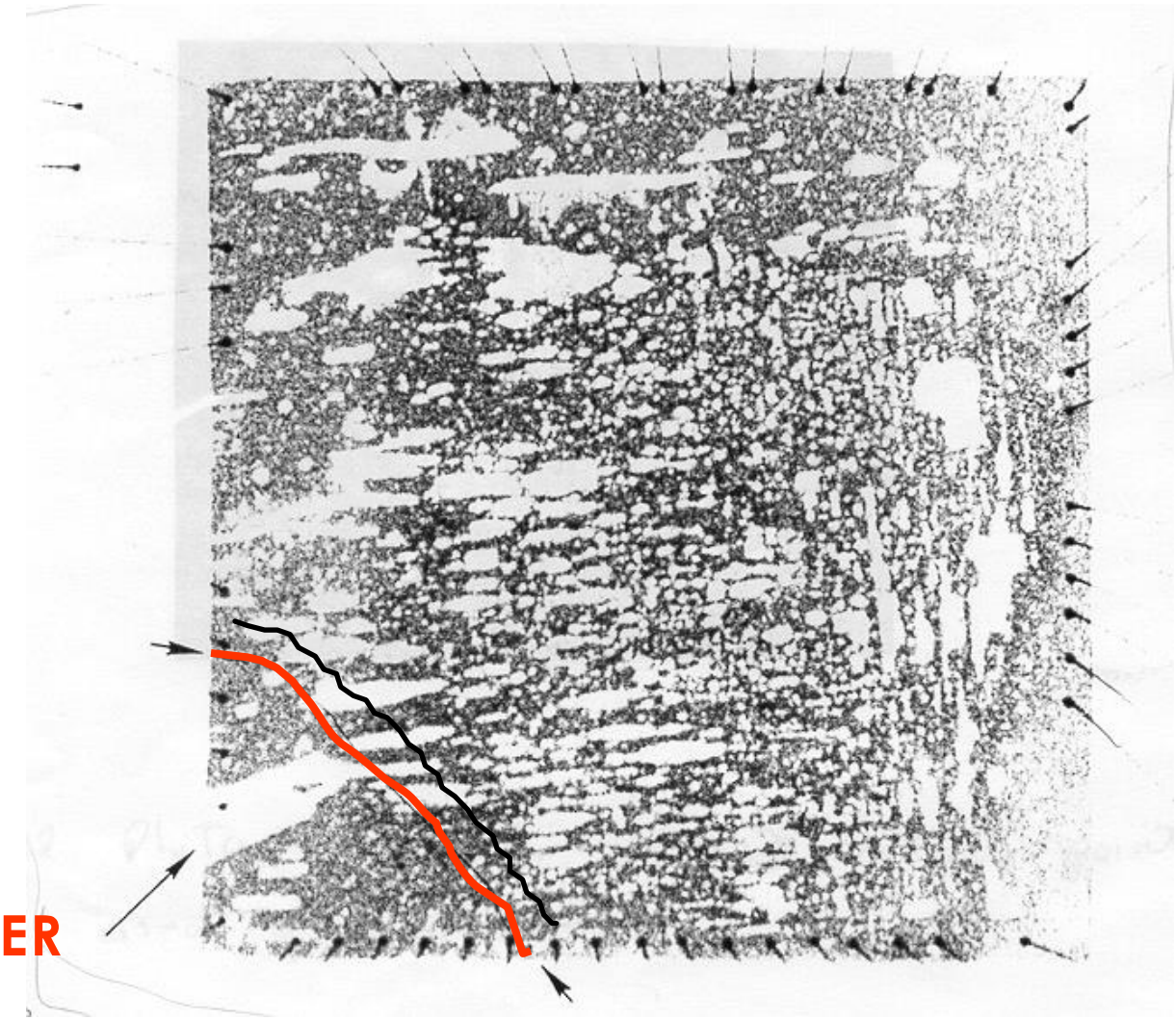


Excess Bulging at Vias

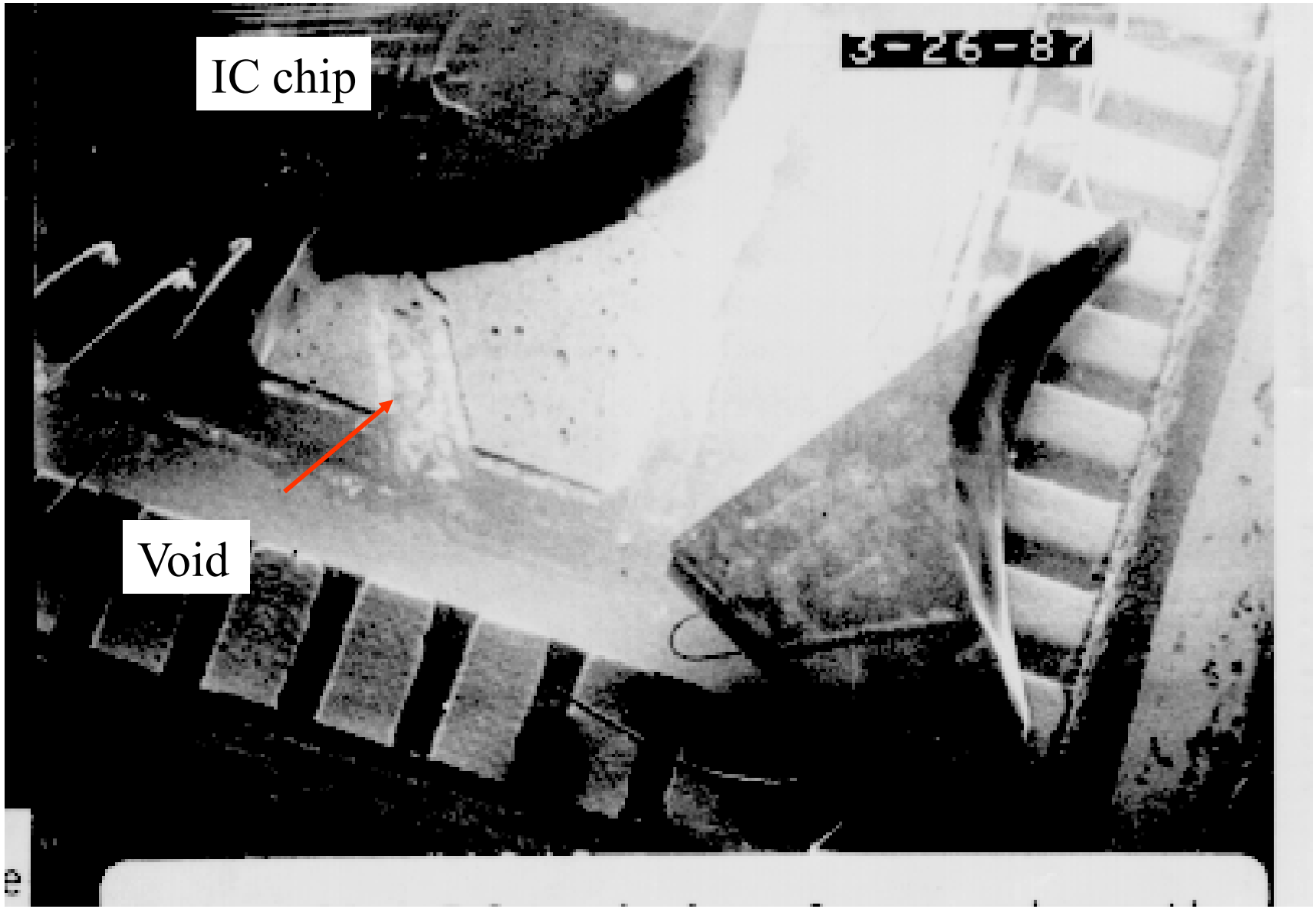


Nice flowout around base of Die

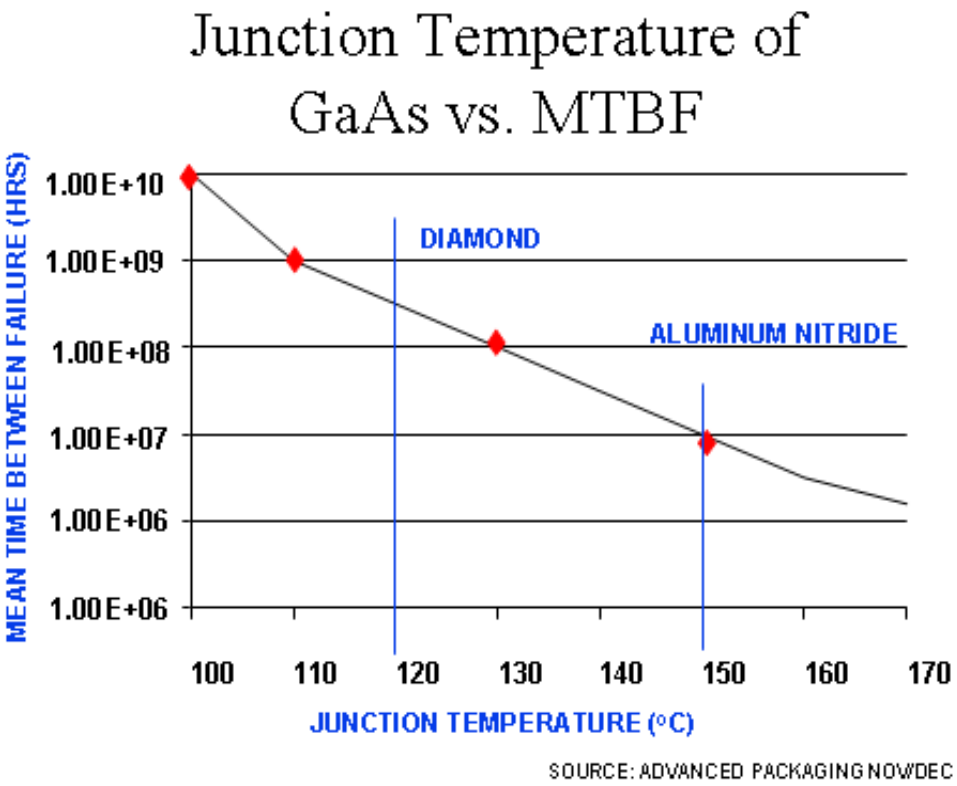
X-Ray of Die Attach (Au-Si)



Die Bond Failure

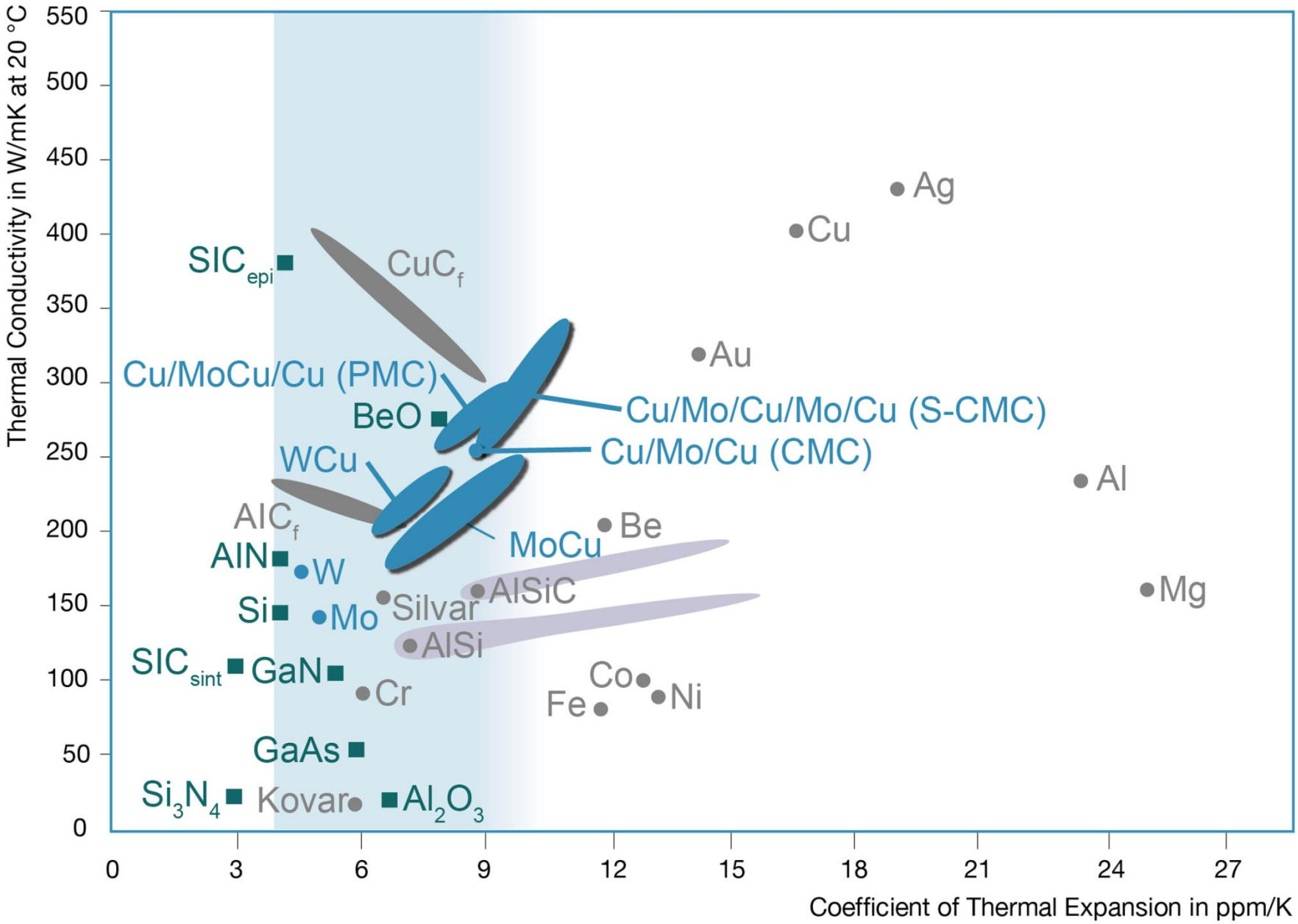


MTBF vs. Junction Temperature



- *There is a very strong and well known correlation between junction temp and expected lifetime of the device. The simplified chart above illustrates this point*
- *Heat in a hybrid is generated on the surface of the power semiconductors, MMIC channels, resistors , diodes etc….this heat must be managed and efficiently dissipated through package base. Computer thermal modeling is a way to characterize and trade off materials/package geometries in order to maximize heat transfer and minimize junction temps*

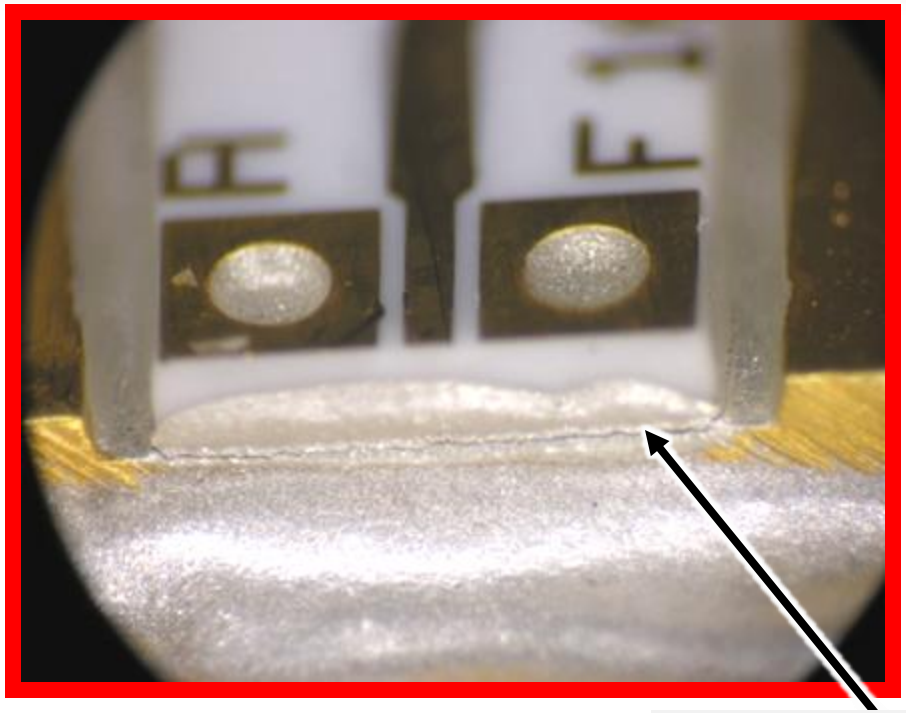
Thermal Conductivity vs CTE

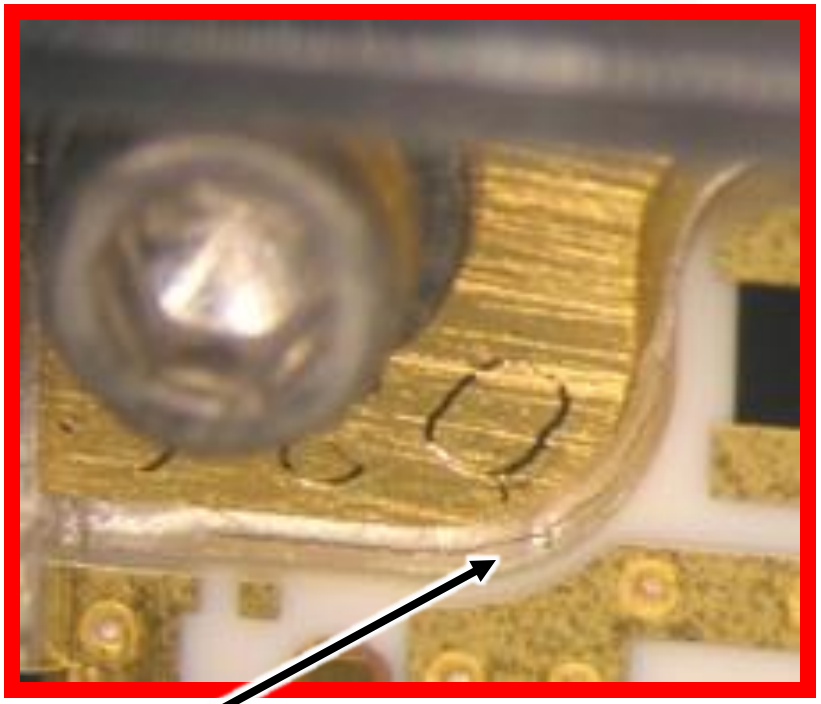


Ref: Plansee

Epoxy Cracks in Fillet

REJECT





Cracks in Silver Epoxy

A Crack is a line of of fracture that does not result in complete separation of a material. When evaluating mounting material, this separation is measurable in length, width and depth. It is not pullback of the fillet or shrinkage due to the curing process.

REJECT: Any crack in the surface of the attachment adhesive greater than 5.0 mils in length or 10 percent of the contact periphery.

Cleaning Processes

- UV ozone
- Solvent cleaning methods
- Plasma Cleaning
- Use caution with ultrasonic bath cleaning

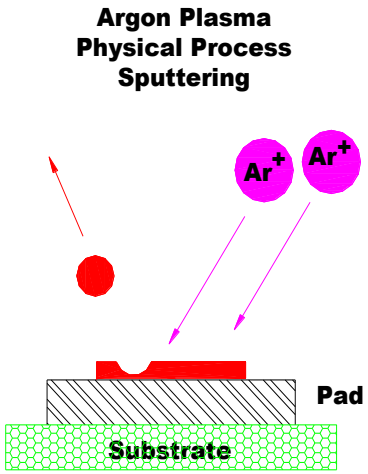
Plasma Cleaning

- Plasma is a partially ionized gas containing electrons, ions and other species at different levels of excitation
- Need vacuum and an RF energy source
- Ionized gas reacts with surface contaminants producing volatile by products CO, CO2, H20
- A widely used process prior to wirebonding

Physical Plasmas

Physical

- Sputtering - Argon Plasma
- Ar^+ Ion Attracted to (-) Electrode
- Operated at Lower Pressures - 50 to 300 mTorr
- Lower Pressure increases the Mean Free Path
- Impact Force Removes Contamination



Advantages

- Non-Chemical Reaction: No Oxidation
- Pure Substrate Remaining

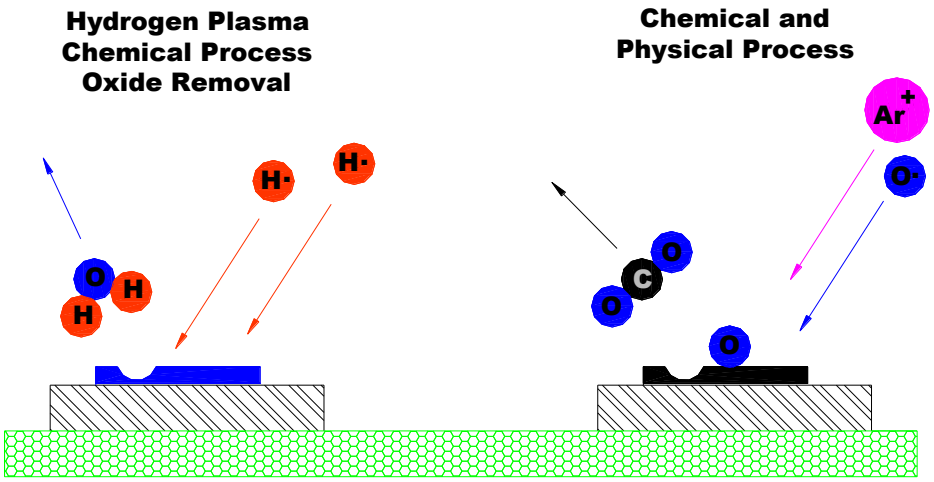
Disadvantages - Easy to Minimize

- Substrate Damage: Impact, and Overheating
- Poor Selectivity
- Low Etch Rate
- Contaminant Redeposition

Ref: L Wood March Plasma Systems

Chemical Plasmas

Plasma Generated Reactive
Chemical Species
Source Chemicals Include:
H_2, O_2, CO_2, N_2O, and CF_4
Ionized Source Chemical
Produces Reactive Species
Gas Phase Products Produced From
Reactions with Substrate Surface



Advantages
High Cleaning Speed
High Selectivity
Effective for Organic Contaminants

Disadvantages - **Oxides Can Be Produced**

Ref: L Wood March Plasma Systems

Plasma Cleaning

CHEMICAL REACTIONS (Oxygen Plasma)

Uses free radicals to chemically etch surface

$$O_2 + e \longrightarrow 2O + C_xH_y \longrightarrow CO_2 + CO + H_2O$$

PHYSICAL REACTIONS (Argon Plasma)

Heavy ions physically break weak organic bonds

$$Ar + e \longrightarrow Ar^+ + 2e^- \longrightarrow Ar^+ + C_xH_y$$

Wire Bonding Methods

Wirebond VIDEO

Thermocompression (T/C) Bonding

- Heat + pressure (300 C typical)
- First method ever used

Ultrasonic (U/S) Bonding

- A metallurgical cold weld is formed using pressure and ultrasonic energy (vibrations)

Thermosonic (T/S) Bonding

- Married U/S plus T/C (lower temps possible)
- Most popular method

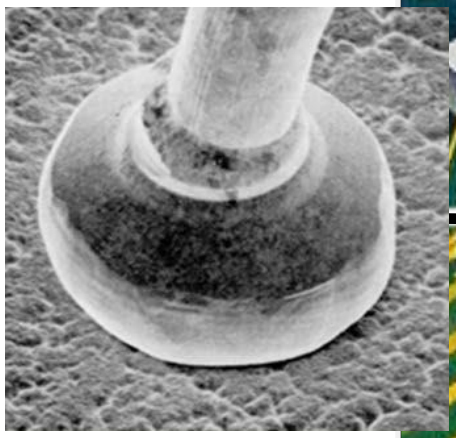
Terminology used in TM 2017 ….tailless, small vs large wire, etc.

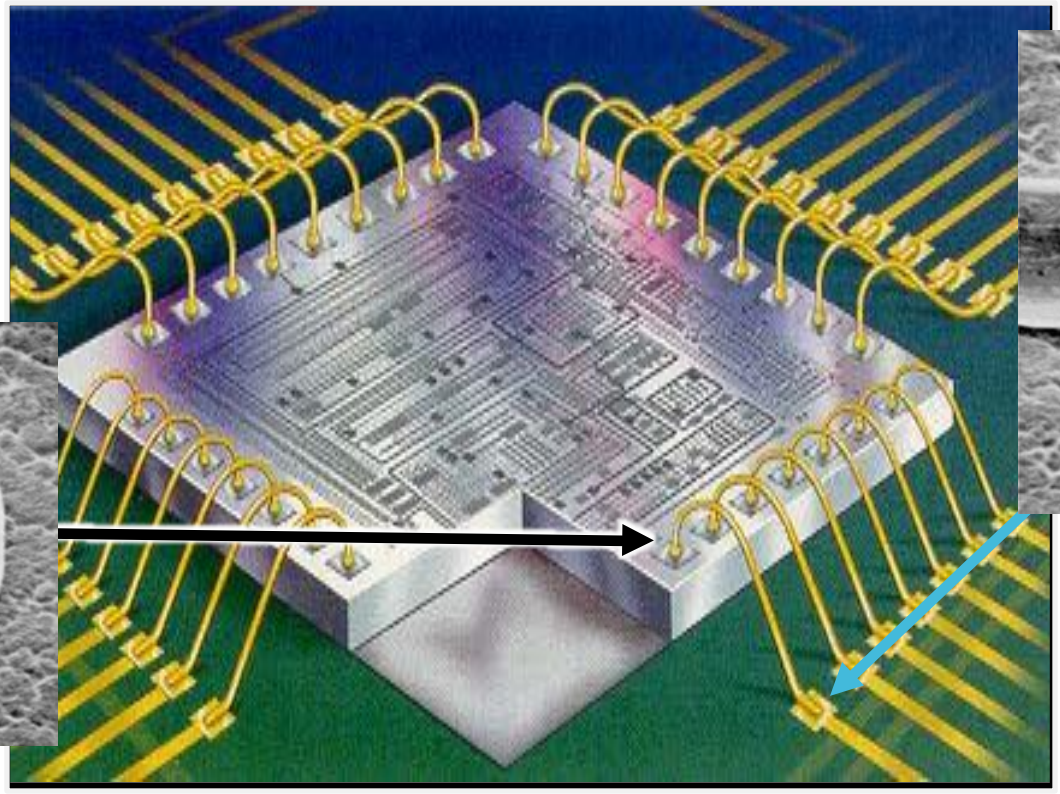
For more information on wirebond materials, processes and testing refer to the following textbook:

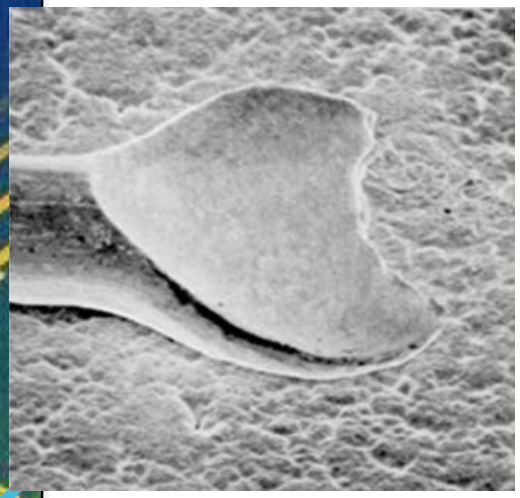
Harman, G. (2010). Wire Bonding in Microelectronics Materials, Processes, Reliability and Yield ; McGraw-Hill Third Edition

Thermosonic Gold Ball Bonding

Ball



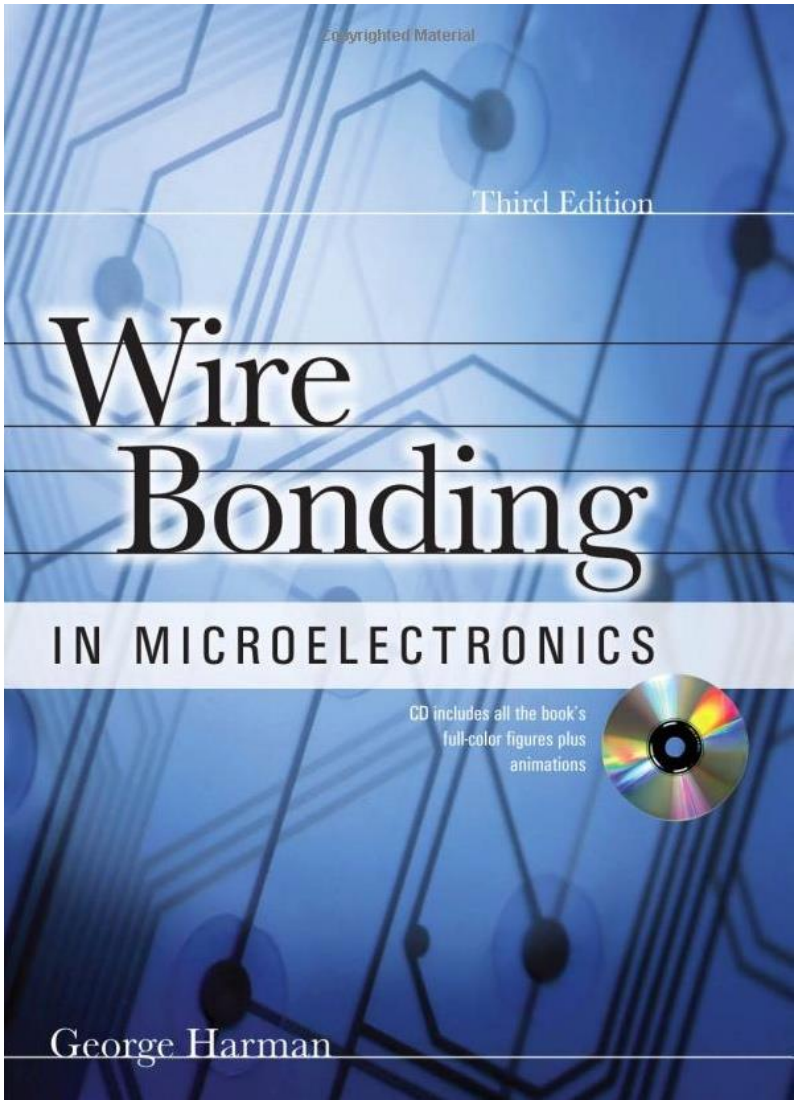




Stitch

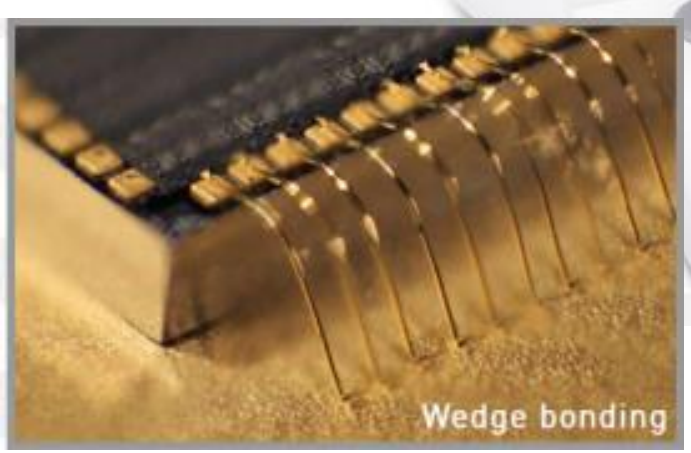
Most wires today are made with a ball bonder. Modern-day high-speed auto ball bonders can attach 20 wires per second. Whether placed manually or with an auto bonder TM 2017 has criteria focused on the deformation and placement accuracy of the ball and stitch (aka tailless) as shown in the following slides. Wirebond inspection is performed at 30X-60X.

George Harman's Book



3rd Addition Available 2009

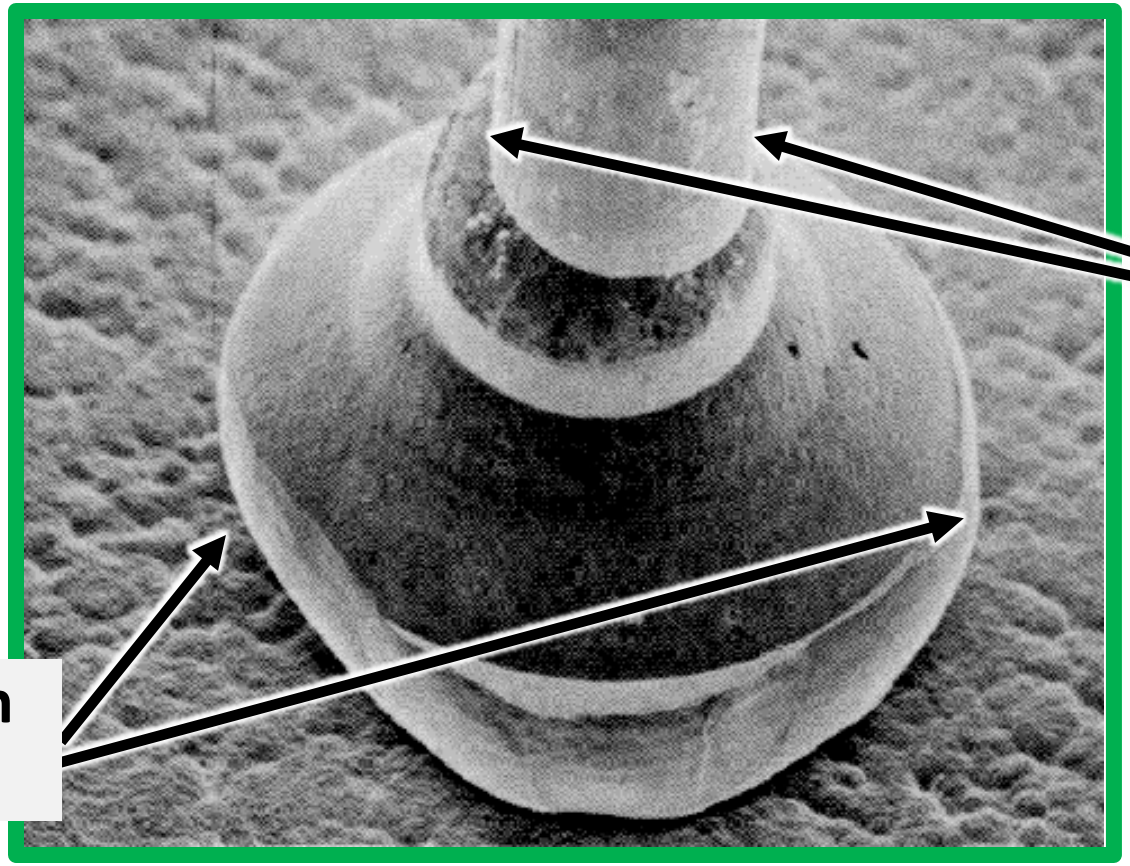
TPT Ball/Wedge Bonder



REF: http://www.tpt-wirebonder.com/uploads/

Gold Ball Squash Guideline

ACCEPT

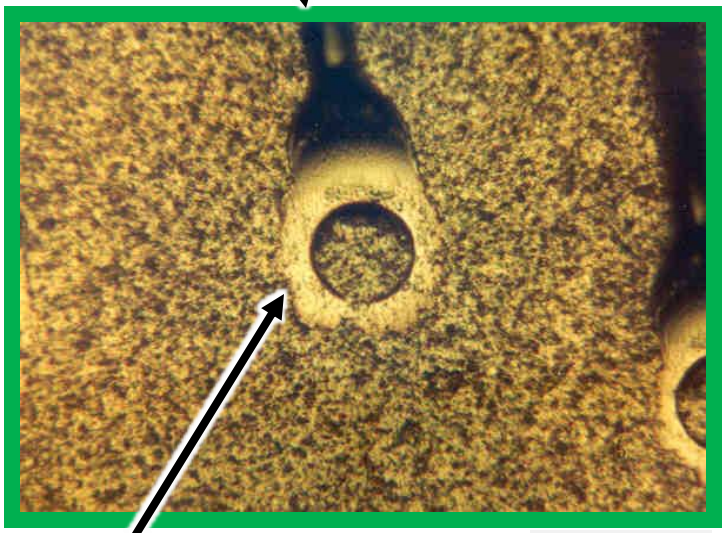


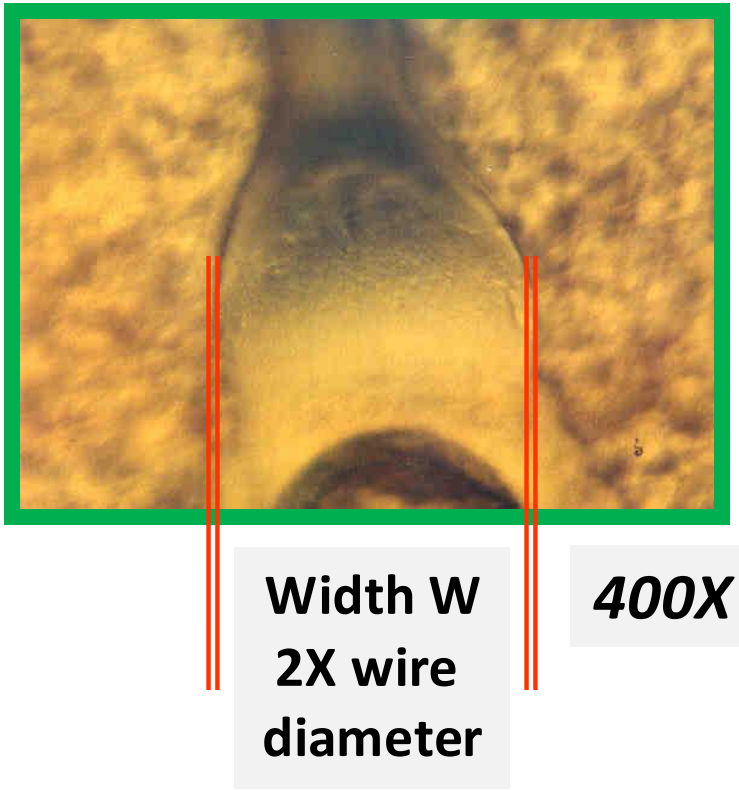
SEM photo showing a nicely deformed ball with a typical squash out of 2 to 3 times the wire diameter. Squash out may be much less for fine pitch applications using bottleneck capillaries. MIL-SPEC requires ball size to be greater than 2X and less than 5X the wire diameter.

TM 2017 Para. 3.1.5.1.a

Gold Crescent Bond

ACCEPT

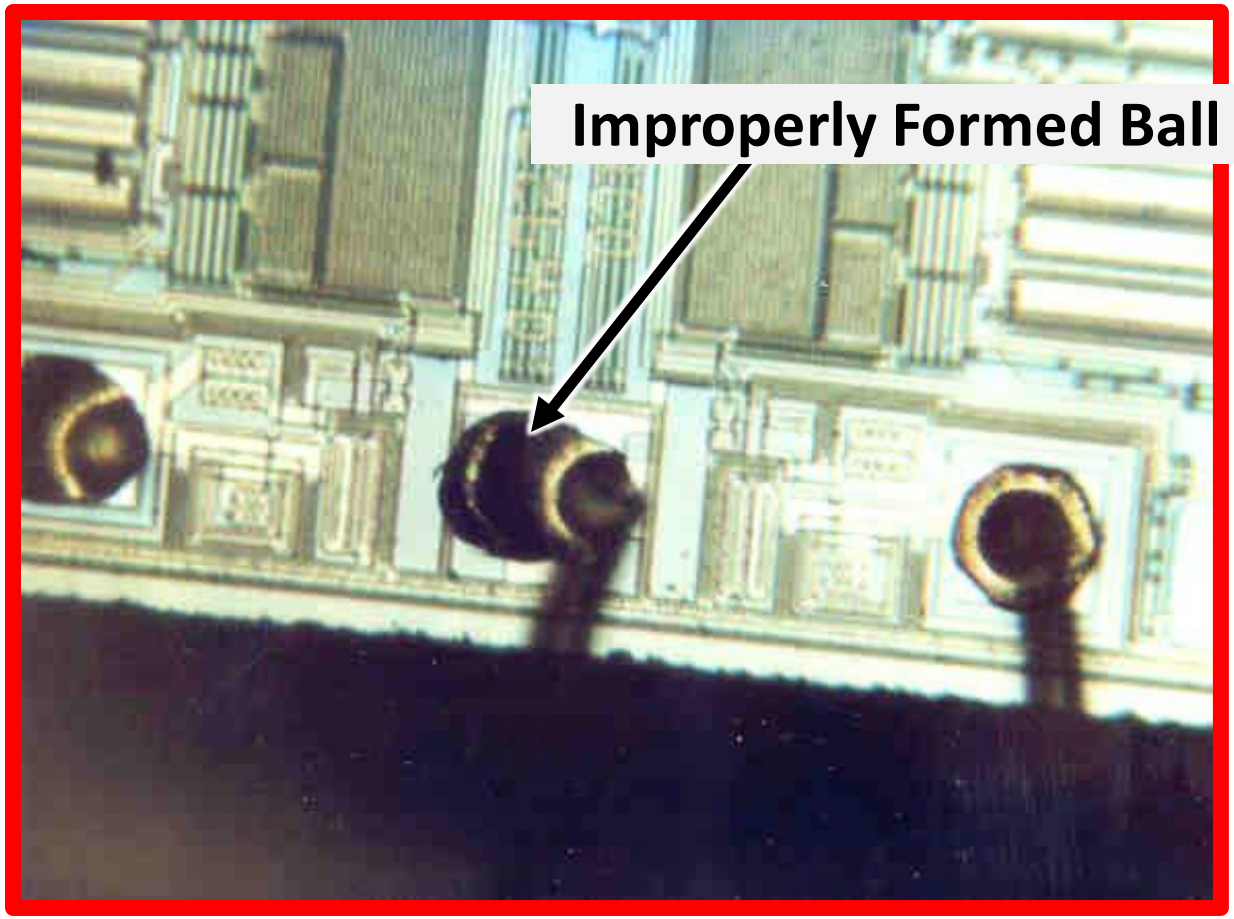




Preferred condition, view of a nicely formed 1 mil gold crescent or tailless bond, same bond at two different magnifications. Seeing a circular tool mark indicates the tool hit flat onto the surface.

Golf Clubs

REJECT



Bond impact was outside the perimeter of the ball. This improperly formed ball could possibly fail in a customer application because the IC chip may have been damaged during the bond process as the ceramic tip impacted the die surface. Ball bonds where the wire exit is not completely within the periphery of the ball is cause for reject.

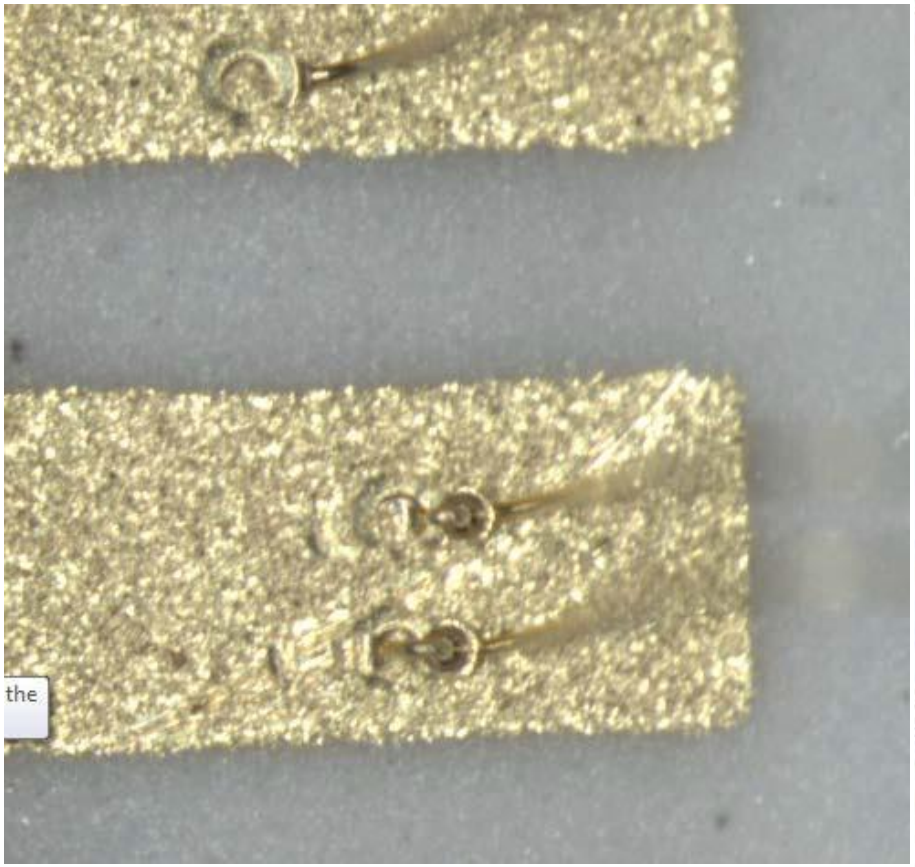
TM 2017 Para. 3.1.5.1.b

Wire Bonding to Thick Film

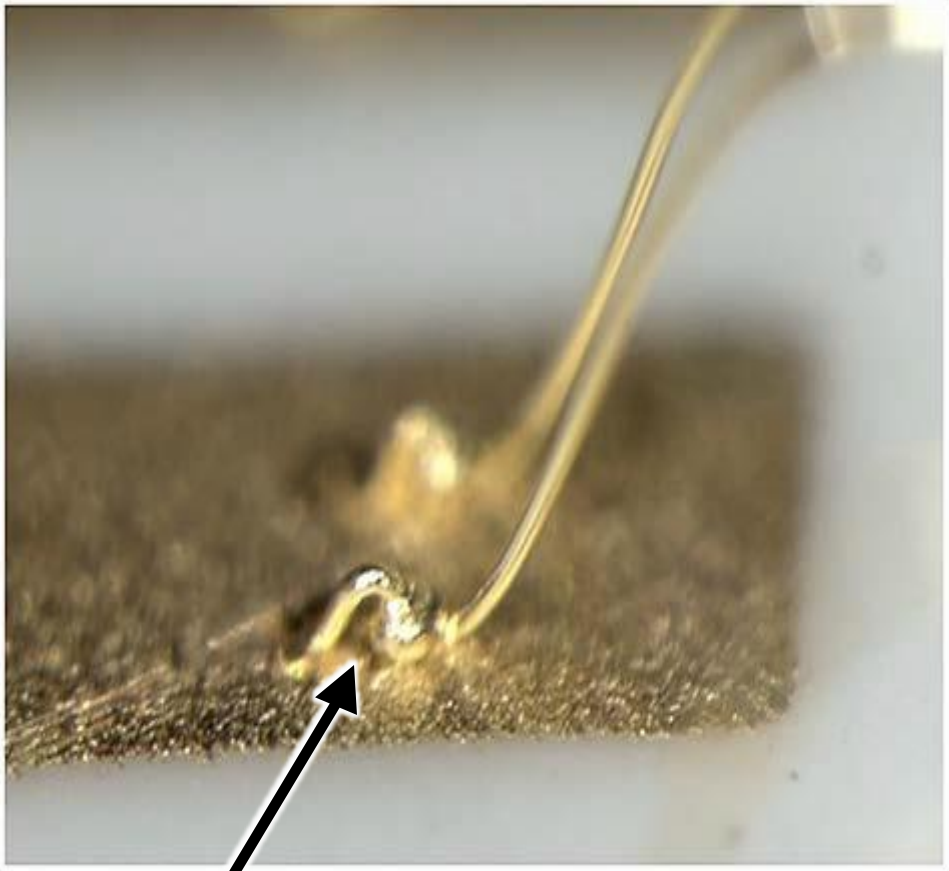
Thick film is often rough and has a saddle in the middle of the metal run. Security bonds at crescent on thick film is common.

Security Bonds (Ball on Crescent)

(aka Compound bonds, Tack bonds or Reinforcement Bonds)



Top View

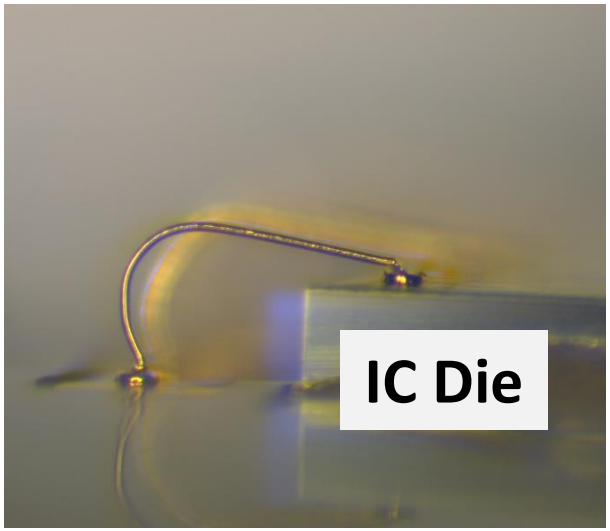


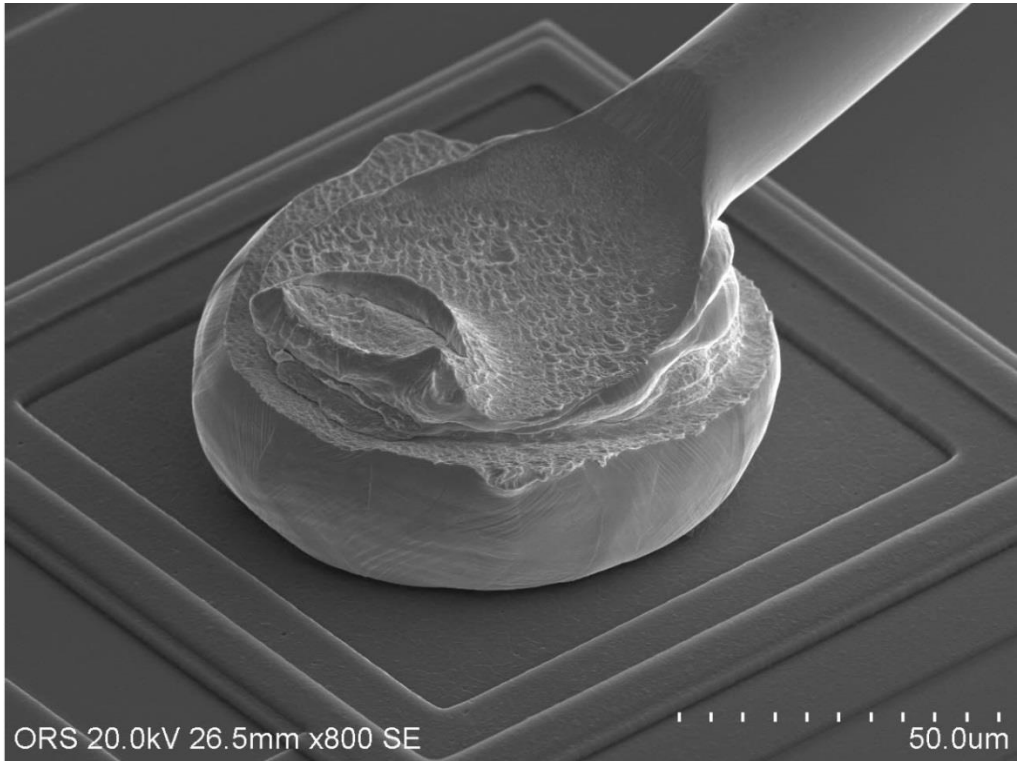
Side View

Compound bonds must be monometallic, meaning gold on gold. The ball must be centered up on the stitch so 75% of the crescent bond is secured. This security bond was made with a manual ball bonder. Tack bonds from an auto machine produce just the ball on stitch.

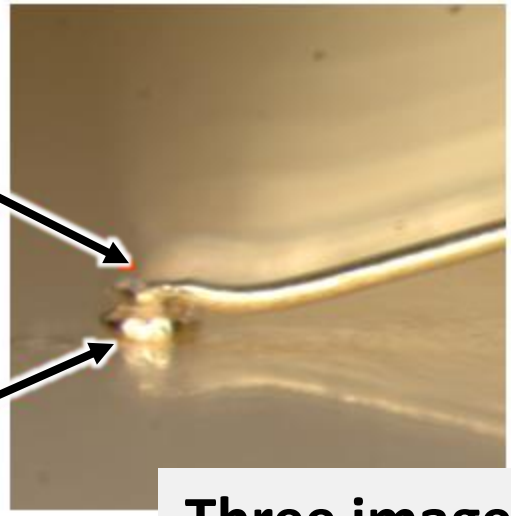
TM 2017 Para. 3.1.5.4

SOSB Stand Off Stitch Bond





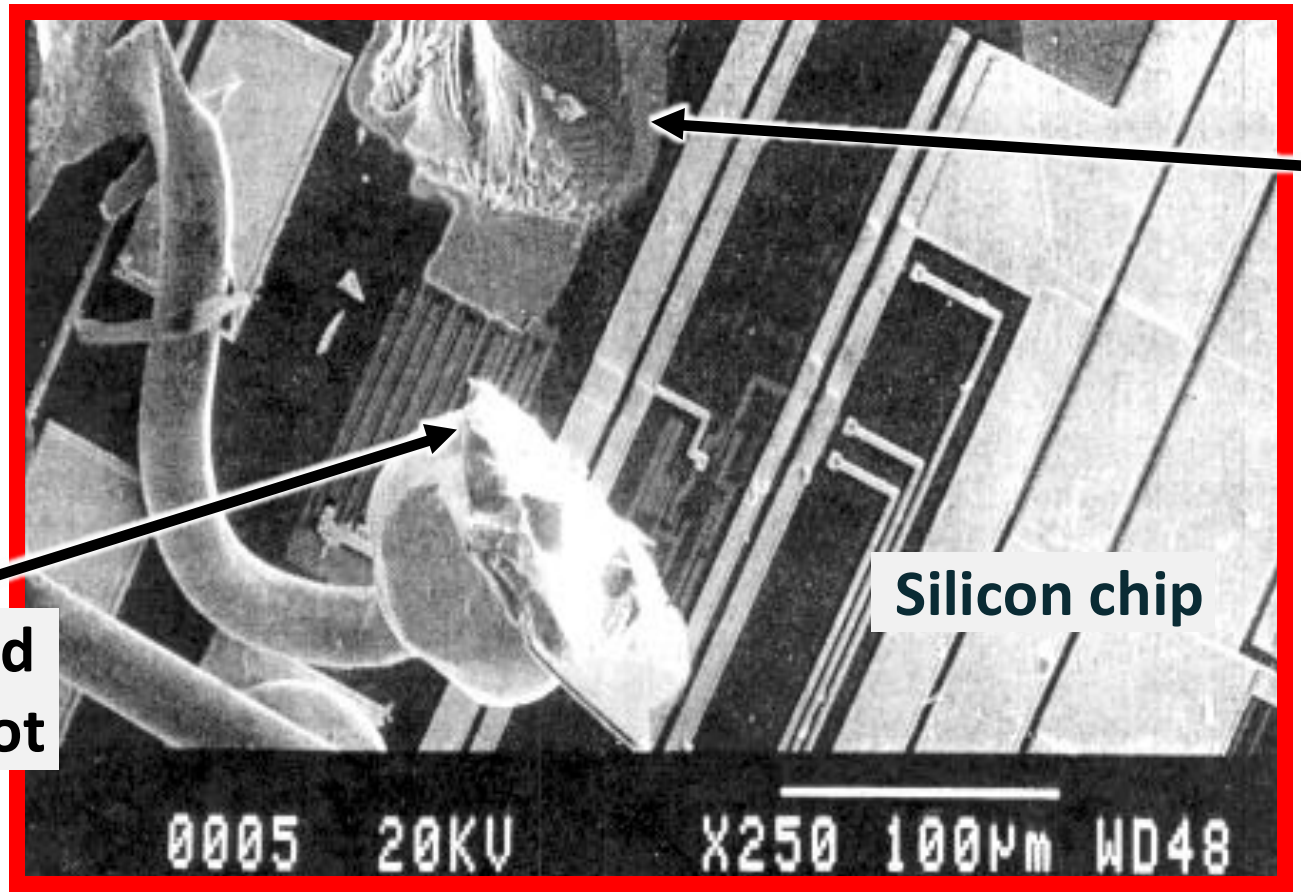
SEM Image of crescent on ball



Three images showing a SOSB type bond which in TM 2017 is considered a compound bond.

Gross Die Cratering

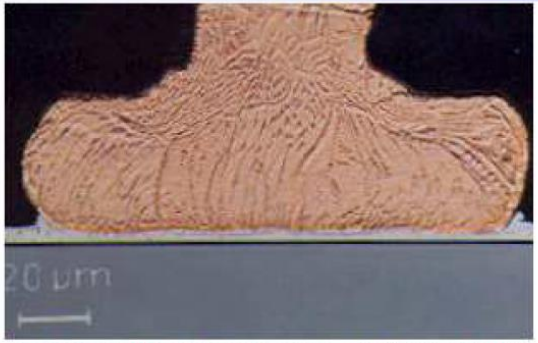
REJECT



SEM photo showing gross cratering. Optical inspection may reveal small perimeter cracking around the ball indicating the potential for cratering. MMICs and next generation GaN chips and modern day ICs are prone to cratering for a variety of reasons.

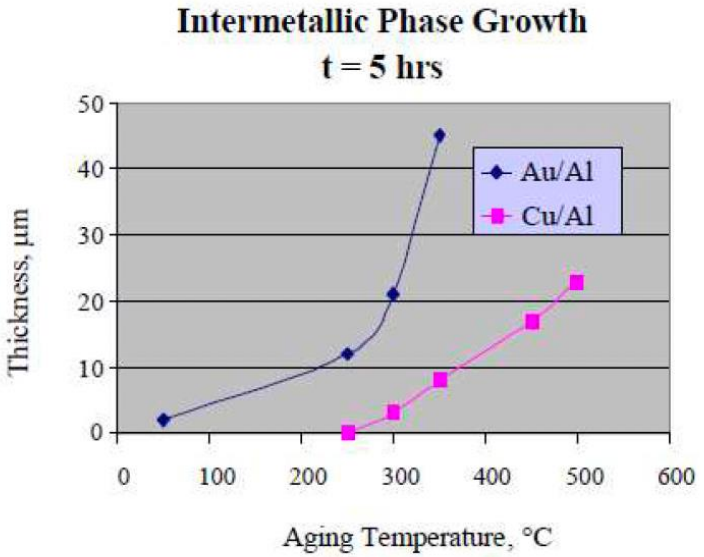
Cu Wire Bonding is Cheaper

Cu-Al Intermetallic Growth



Intermetallic Penetration - AlSi-Cu Bond
(aged 800 hours at 180°C)

Intermetallic Penetration - AlSi-Au Bond
(aged 200 hours at 200°C)



Process SOLUTIONS CONSULTING, INC.

Lee Levine

Bottom Side of Au Ball Bond

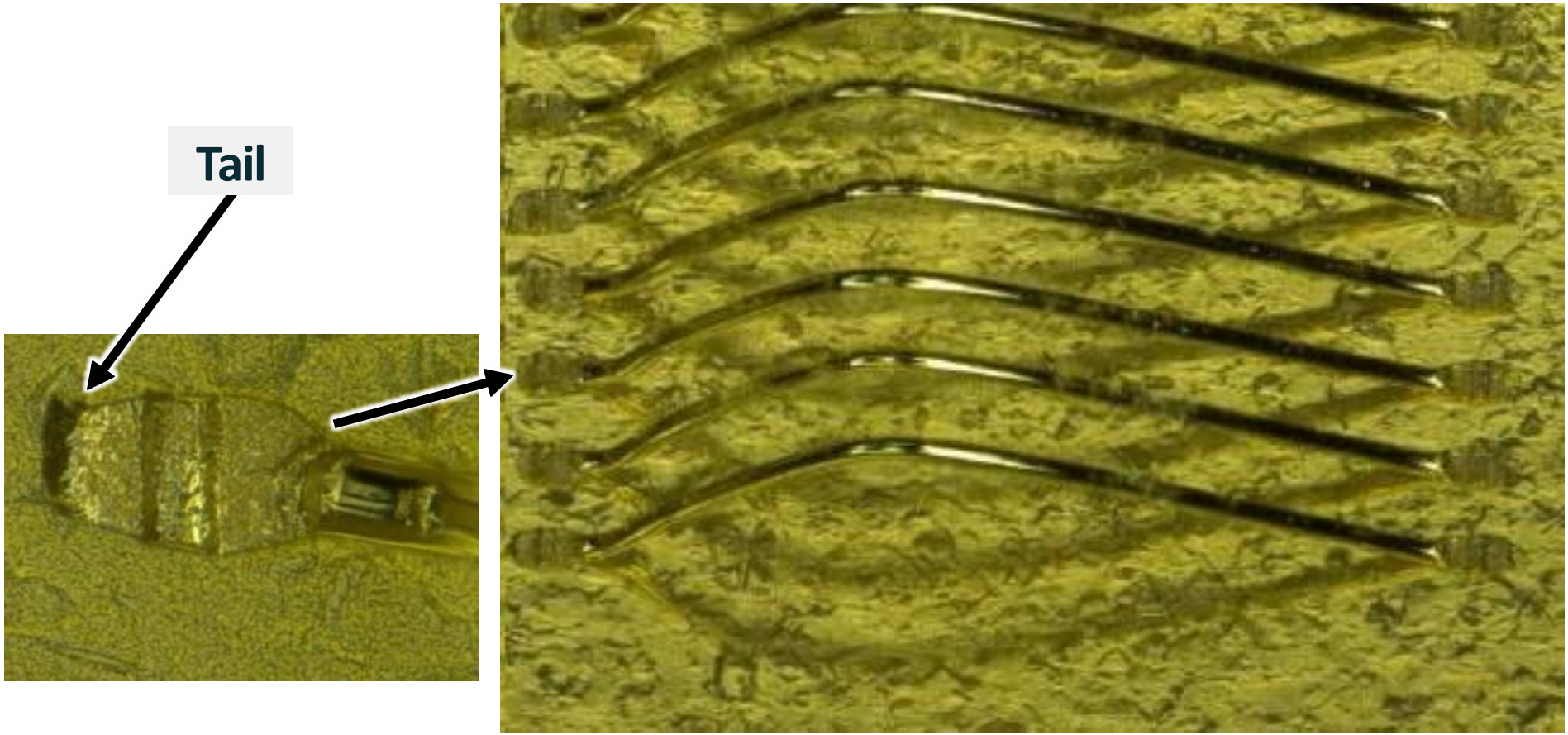
Intermettallic formation under the ball is critical

Result of KOH-Etching of Al Pad from under Au Bond, Revealing Intermetallics (related to amount of welding)

- It is very important to measure IMC coverage during qualification, every process change and periodically during production
- A common requirement is 80% IMC coverage in Au ball bonding
- Use of pixel counting techniques/software takes time to achieve repeatability but is worth the effort
- Copper IMC is much thinner initially and impossible to distinguish
- Standardized bake tests to "GROW" Cu IMC prior to measurement are recommended

Process SOLUTIONS CONSULTING, INC.

Gold Wedge Bonds



Wedge bonds are typically made using gold or aluminum wire. Although sometimes hard to see first bond has a small tail. The above is 1 mil gold wire wedge bonds were made with a cross groove tool. The bond imprint is the reverse image of the tool used to form the bond.

Aluminum Wedge Bonds

ACCEPT

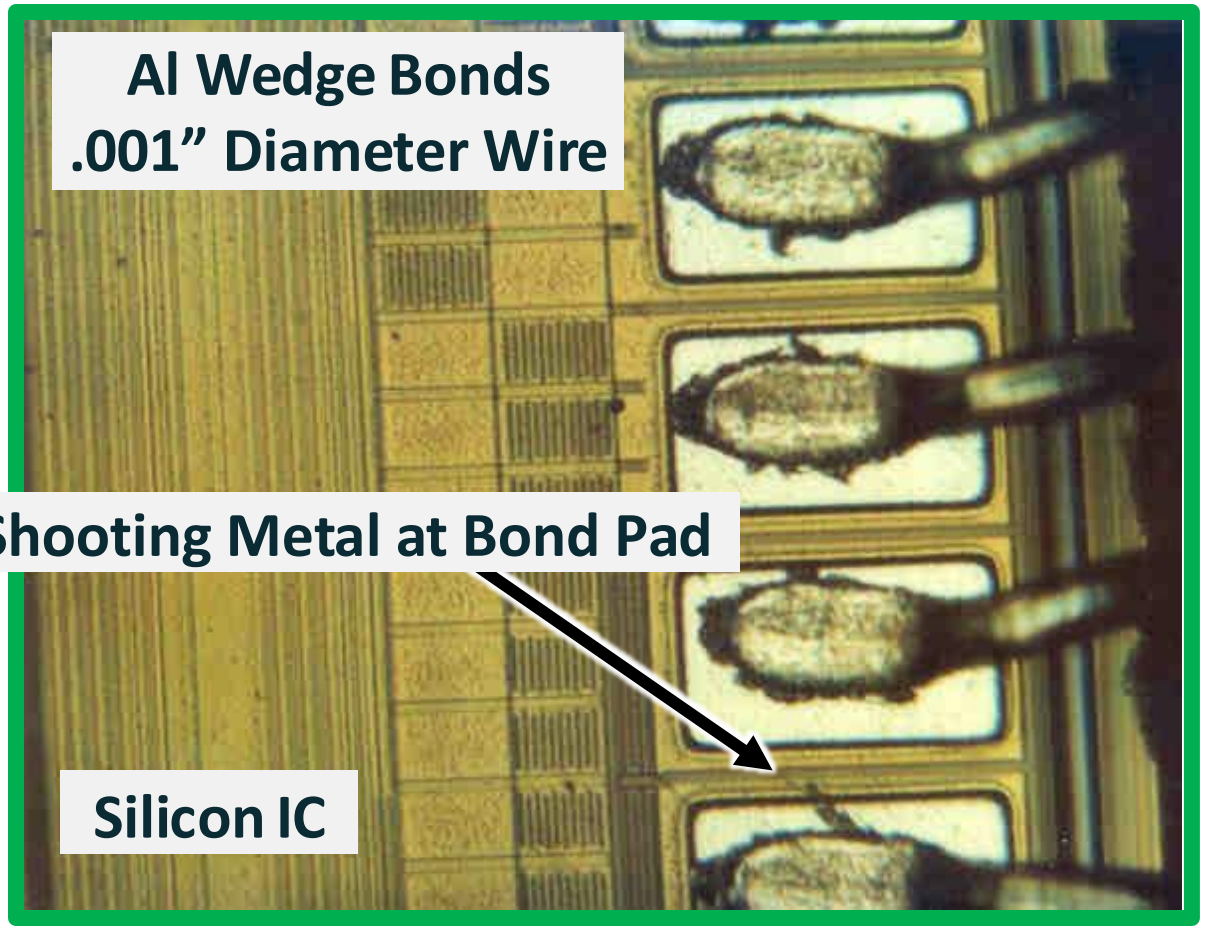
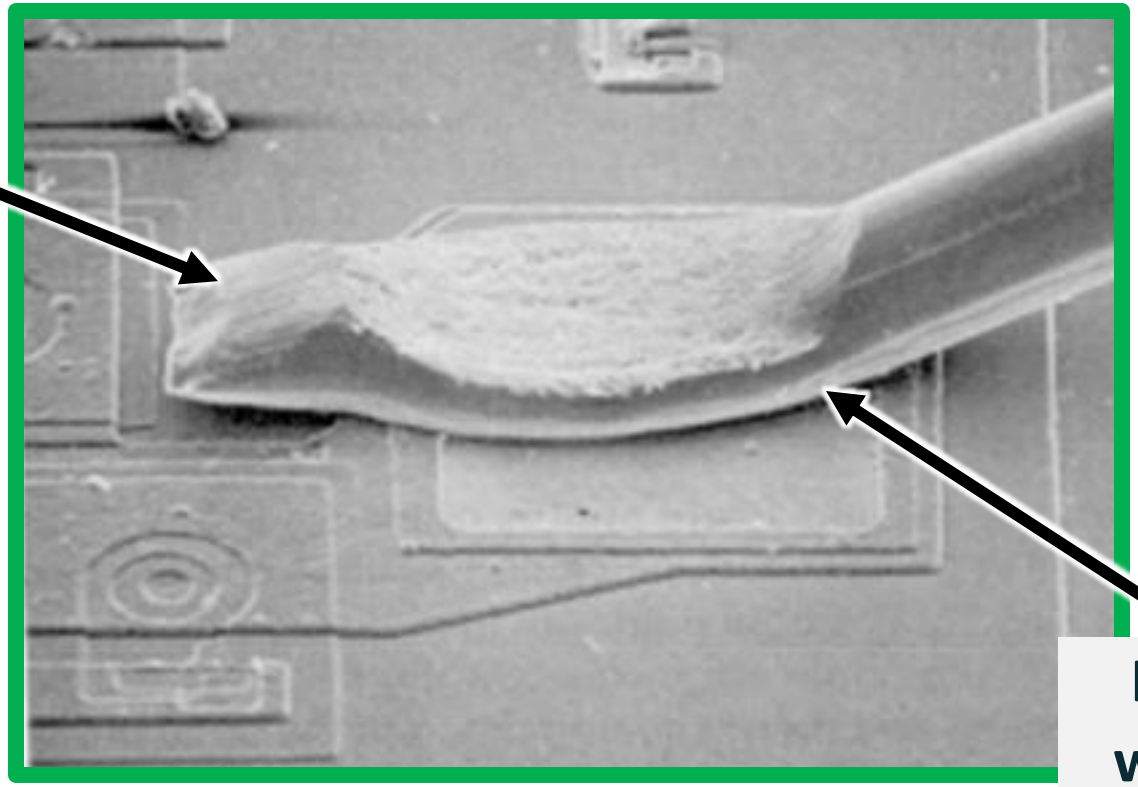


Photo shows nicely formed wedge bonds made with an automatic wirebonder, formed within the boundary of the aluminum bond pad. (200X)

Typical Wedge Bond

ACCEPT

Tail of the wedge bond



Heel of the wedge bond

Bond tails must show a clear “line of separation” between other conductive metal run. The short tail shown above on left side extends out over and an area protected by the glassivation on the IC surface. The wire deformation looks about right, 1.2 to 1.5X is a good nominal squash factor on a wedge bond. Arrow points to critical heel area, which in this case looks good.

Cracked-Lifted Heel (Gold Wedge)

REJECT

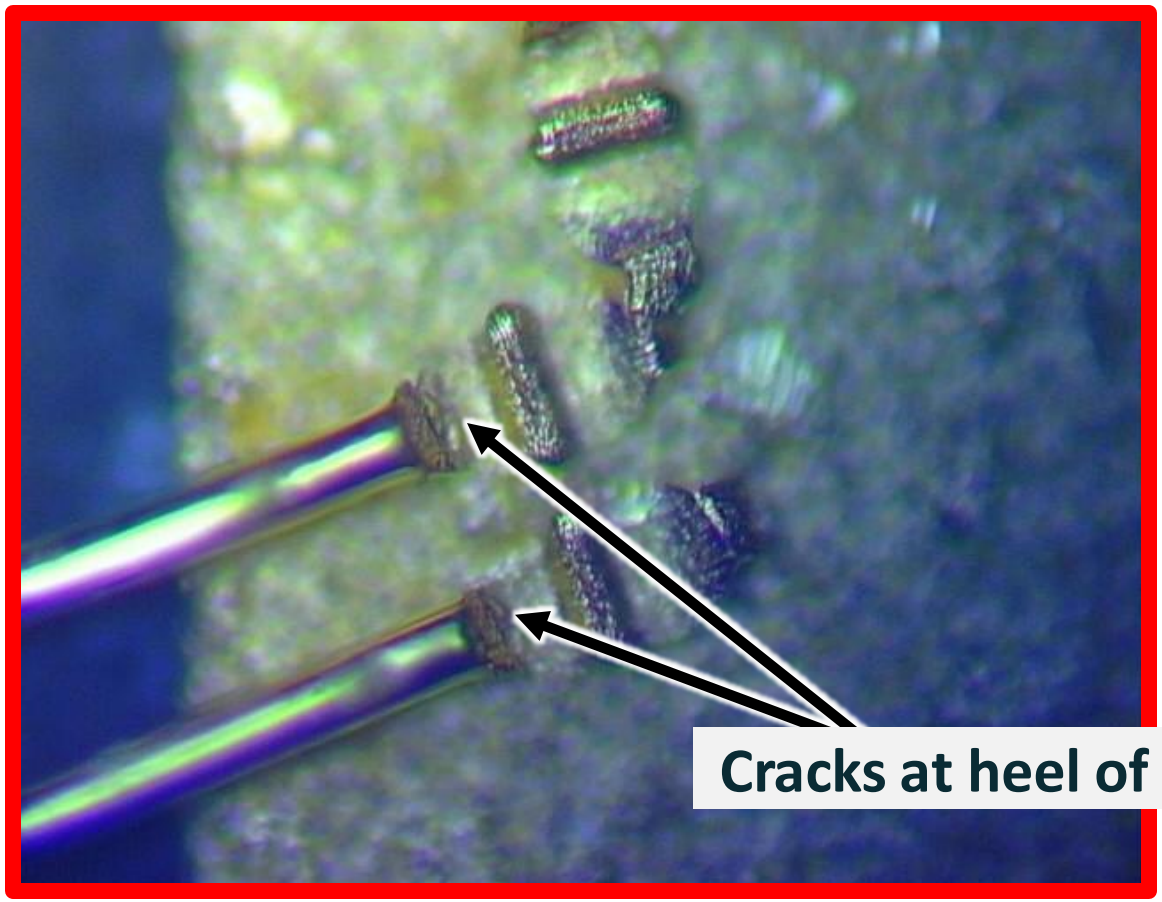
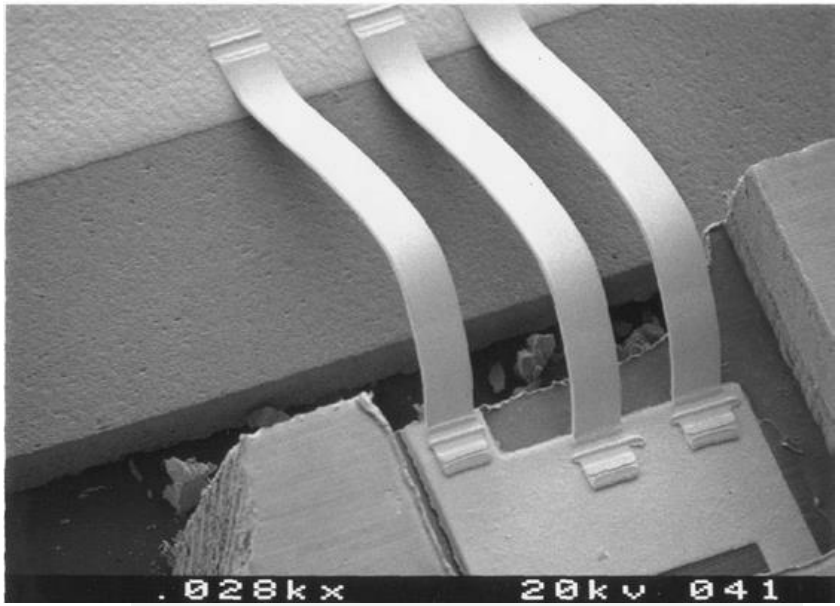


Photo shows evidence of cracked/lifted bonds, probably due to excessive power/force setting on the wire bonder. Heel cracks are a common problem and difficult to spot. Higher magnification is often needed to see the cracks. Excessive wire squash is a good indication heel cracks are present.

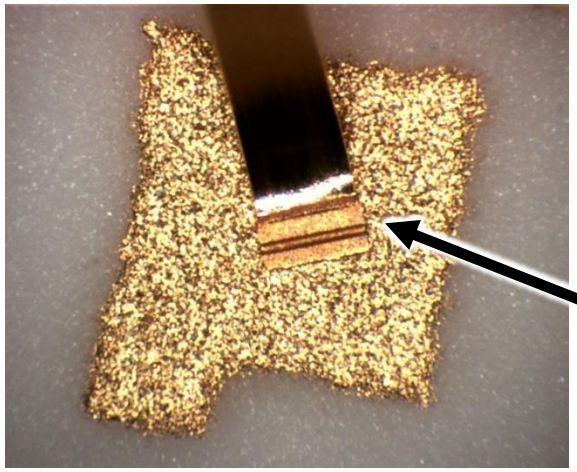
TM 2017 Para. 3.1.5.8.o

Ribbon Bonding

MMIC to MMIC ribbon



SEM image of ribbon

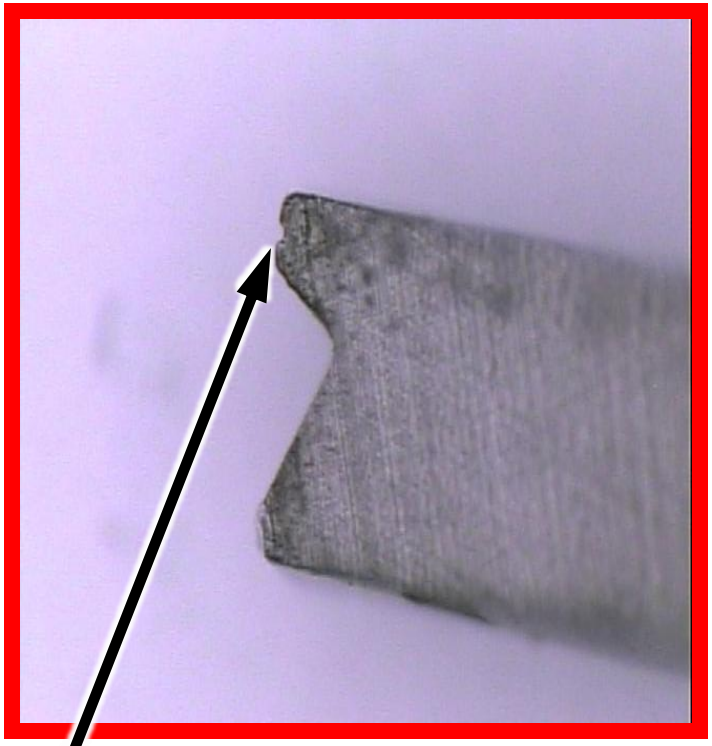


Ribbon bond on thick film substrate

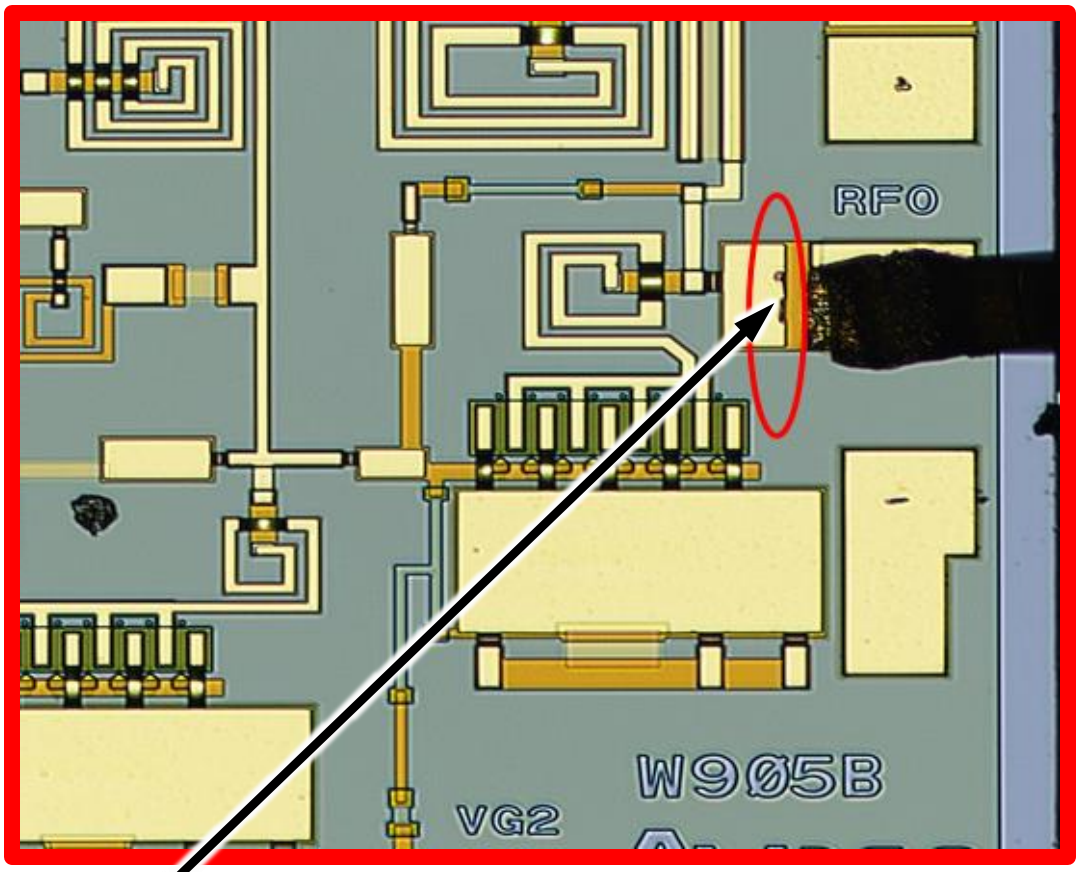
Gold ribbon bonding is an extension of wedge bonding. Different tools are needed and the gold ribbon comes in a variety of widths and thickness. e.g. 3 X .5 mil ribbon is common, especially in the microwave industry.

Ribbon Tool Damage on MMIC

REJECT

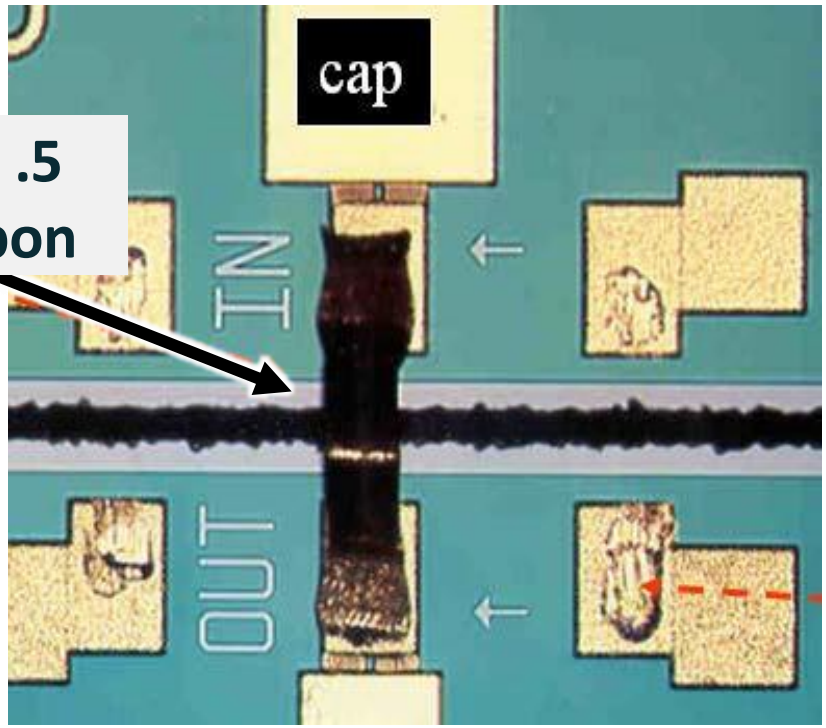


Side view of 3 mil ribbon tool with cross groove



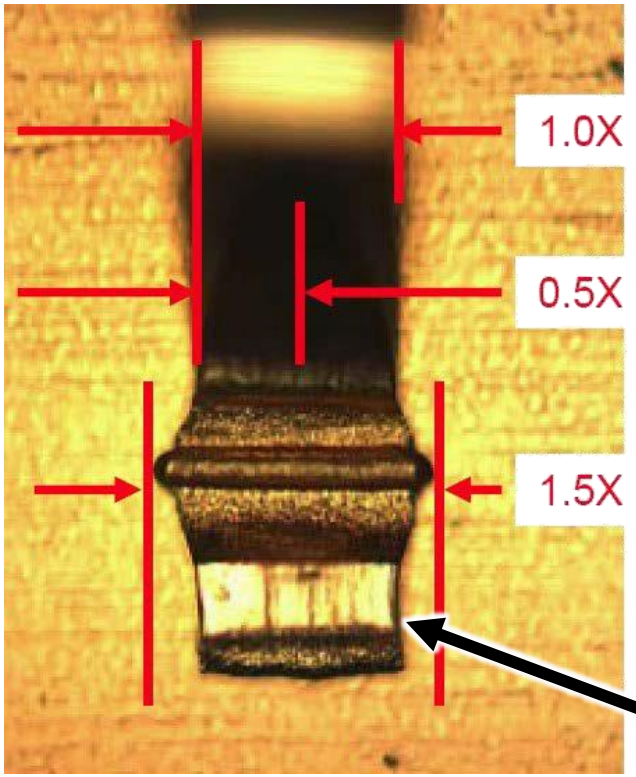
Tool from Ribbon Bonder Damages Nearby Capacitor

Gold Ribbon Criteria



3 X .5 ribbon

MMIC to MMIC ribbon



Tail of ribbon

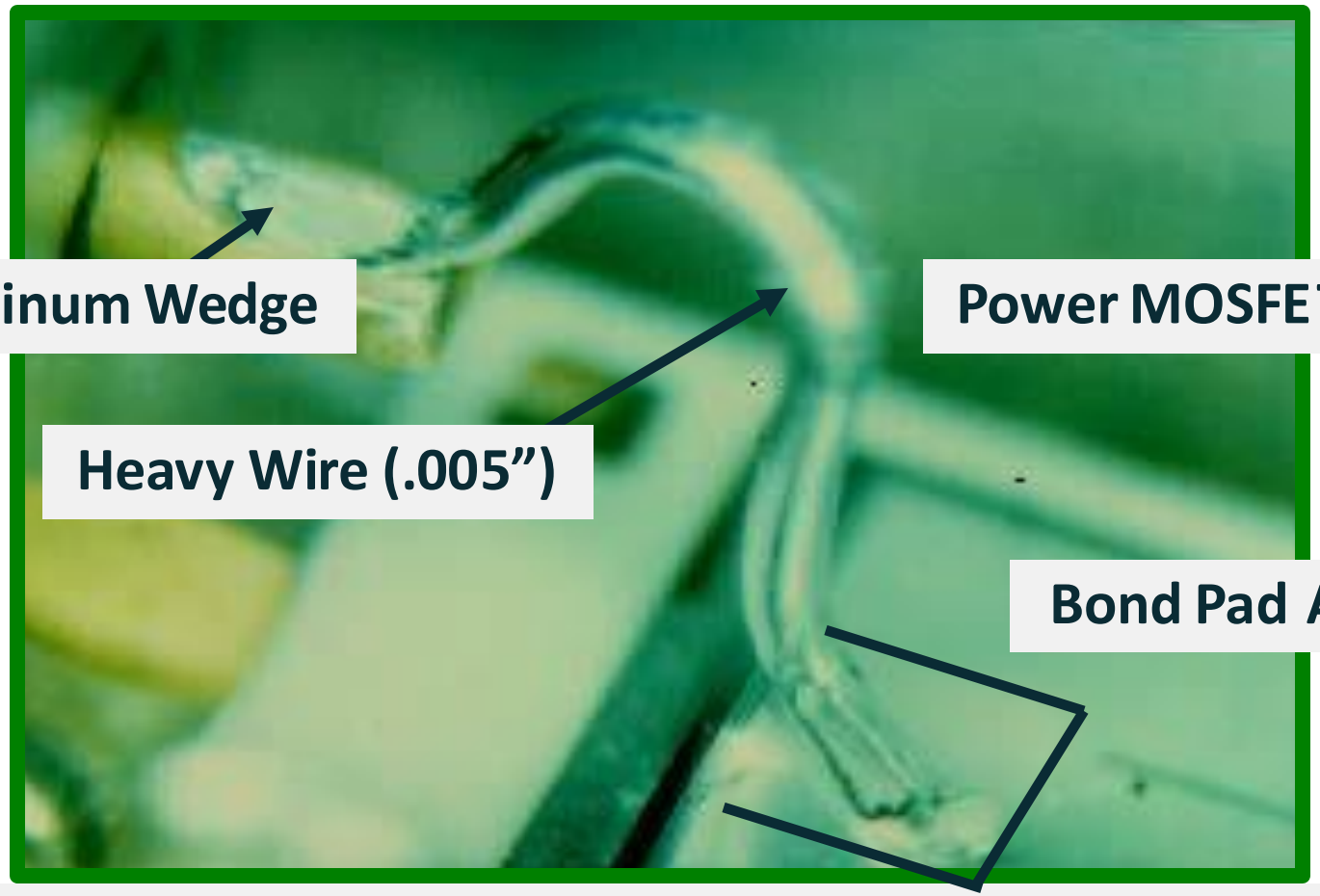
In TM 2017 the squash out on a ribbon is not specifically addressed but 1.5X is a good upper limit (as shown above). Inspect to assure there are no cracks or tears at the heel or junction of the ribbon. Ribbon tails should be less than one ribbon width or 10 mils and 100% weld impression across width of ribbon.

TM 2017 Para. 3.1.5.7.f

Heavy Gage Wirebond

(Aluminum wire greater than 4 mils diameter)

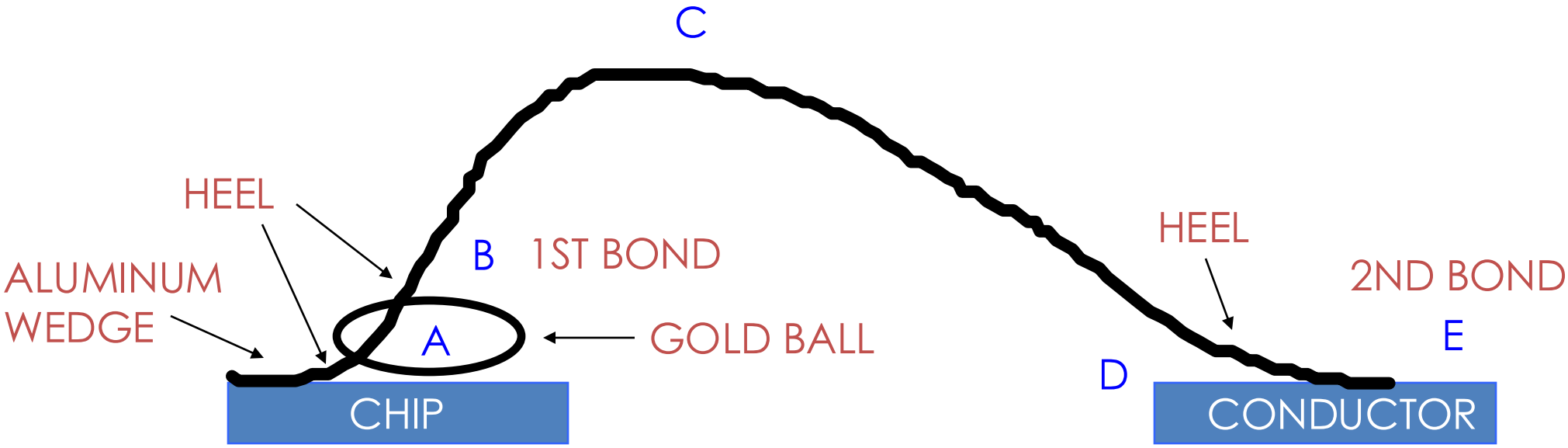
ACCEPT



Heavy gage aluminum wire used to connect a power pin to a power semiconductor device. Heavy wire is used for high current applications. The bonds look different due to the V-groove style tool that is often employed (100X)

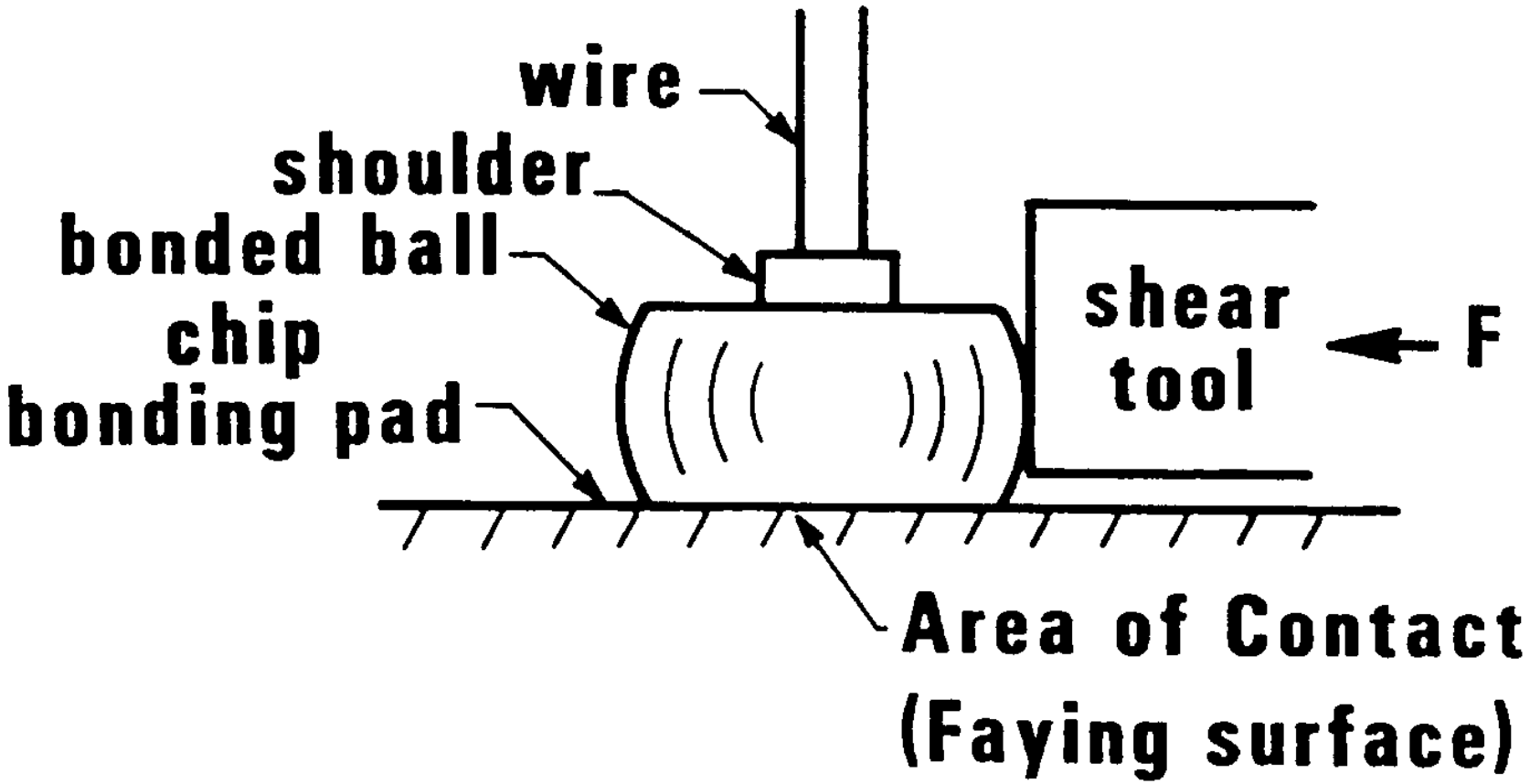
TM 2017 Para. 3.1.5.3.b

Wire Bond Failure Modes



A. FIRST BOND LIFTS COMPLETELY FROM CONDUCTOR
B. WIRE BREAKS AT FIRST BOND HEEL
C. WIRE BREAKS BETWEEN HEELS
D. WIRE BREAKS AT SECOND BOND HEEL
E. SECOND BOND LIFTS COMPLETELY FROM CONDUCTOR

Ball Bond Shear Test



Ref ASTM F 1269-89

Hybrid Low Mag Inspect (10 to 60X)

Stereo Zoom Microscope

TM 2017 Spec Review

Inspect for die attach, wire and ribbon bond, F/M and assembly related defects. Must be able to handle and freely rotate the part under the microscope.

Use finger cots or gloves and follow ESD safe handling procedures .

A formal “Pre Cap”, sometimes in the presence of the customer is the last and most important visual inspection step prior to hermetic seal. No further process steps are allowed after the final inspection.

TM 2010 High Mag Inspection

For Class H Hybrid use Condition B in TM 2010

(75X to 150X) for ICs

Up to 1,000X for some GaAs MMICs

TABLE I. GaAs microwave device high magnification requirements.

Feature Dimensions	Magnification range
> 5 microns	75 - 150x
1 - 5 microns	150 - 400x
< 1 micron	400 - 1000x

What is Hermeticity?

- The dictionary definition of the term "hermetic" means a seal that is gas tight or impervious to gas flow. In the context of microelectronics it implies an airtight seal that will keep moisture and other harmful gases from penetrating the sealed package.
- Metals, ceramics and glasses are the materials used to form the hermetic seal and prevent water vapor from accumulating inside the package.
- A properly made hermetic seal with a sufficiently low leak rate can keep a package dry and moisture free for many years
- Per the mil specs epoxies cannot be used to create a hermetic seal, moisture will slowly penetrate through the epoxy seal and into the package. Some polymeric materials are better than others in terms of moisture permeability, and an epoxy sealed package may pass leak test.
- However, in time all epoxies will allow moisture into the cavity. The problem becomes one of moisture diffusion ala….Ficks' 1st and 2nd law of diffusion ..TM 1014 does not apply!

What it's Not

- Per the mil specs epoxies cannot be used to create a hermetic seal, moisture will slowly penetrate through any epoxy or polymeric seal and into the package. Some polymeric materials are better than others in terms of moisture permeability, and an epoxy sealed package may pass leak test, but that doesn't make it hermetic!
- In time all epoxies will allow moisture into the cavity. The problem becomes one of moisture diffusion ala….Ficks' 1st and 2nd law of diffusion ..TM 1014 does not fully apply!
- What about plastic cavity packages that are advertised as "hermetic" because they pass TM 1014 ?

Why does a Package need to be Hermetic?

- If liquid droplets form on the surface of an IC or MEMS device, the water (H_2O) combined with ionic contamination along with a bias can adversely affect the device..namely
  - Chemical corrosion …especially the exposed aluminum wires or Al bond pads
  - Leakage across pins
  - "Stiction" on a MEMS device
  - Early wearout of moving parts within the MEMS
  - Performance issues in vacuum packed MEMS
  - Changes in dielectric constant on waveguides used in RF MEMS
  - Protection from particles and outside contamination
  - Ag and Au dendritic growth
  - Damage to the doped layers on a silicon chip if the surface passivation isn't good enough
- Moisture droplets can form as the package is cooled below the dew point within the package or if frost has formed on the chip and the package is then warmed

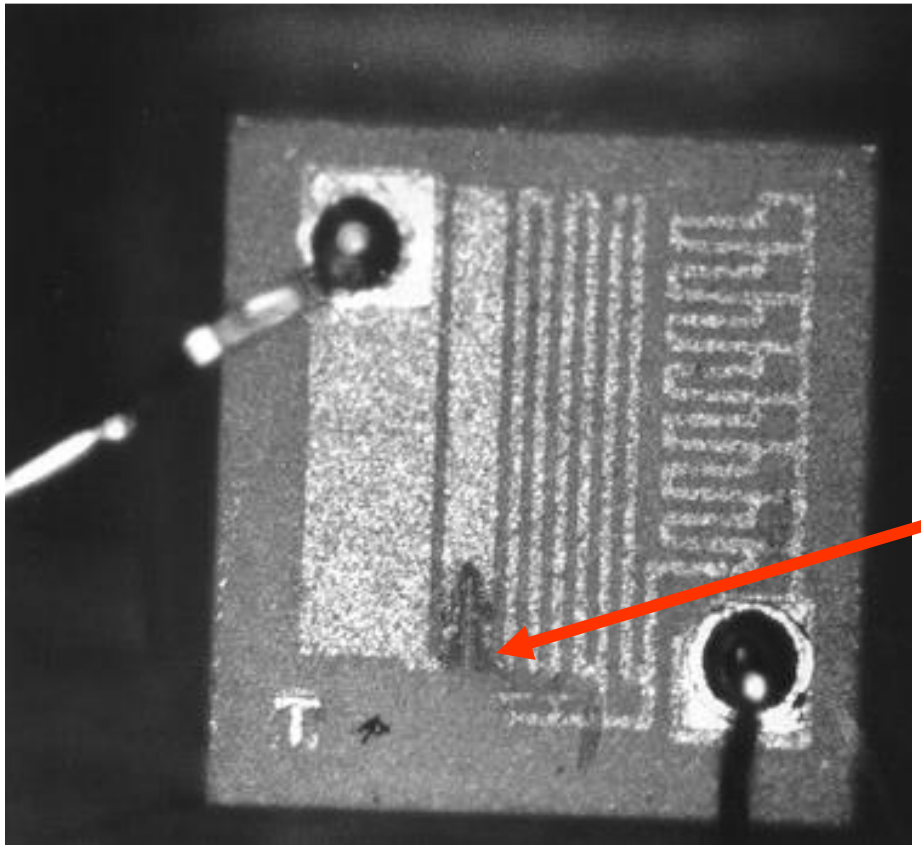
Moisture in Electronic Packages

MOISTURE IS A BAD ACTOR

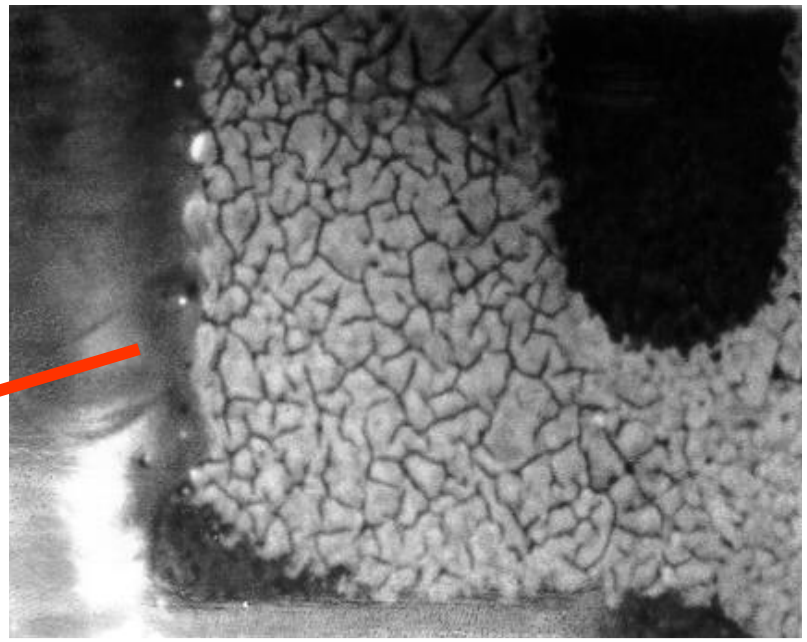
- Water adsorbed on the inside surface of the package and components
- Moisture absorbed in the organic materials (e.g. epoxies can absorb .1-.4 % moisture by weight and polyimides 1-3%)*
- Evolved moisture released as a reaction product of materials undergoing thermal degradation
- Moisture present in the sealing chamber
- Water vapor leaking into the package
- Oxygen and hydrogen inside the packaging reacting to form water..some metals such as nickel can act as a catalyst
- Moisture trapped in the package platings that is released

*Ref: MCM Handbook, Garrou and Turlik p. 7.28

Corrosion Failures on a Chip Resistor



Area of Corrosion



HUMAN SNEEZE VIDEO

(Enlarged View 3000X Backscatter SEM Image)

Optical photo of a NiCr Unpassivated chip resistor(100 x)

Aluminum Corrosion Reaction

- Halogens + Moisture + Metals that differ widely in the electrochemical series potentials

$$Al(OH)_3 + CL^- \longrightarrow Al(OH)_2 + OH^-$$

$$Al + 4CL^- \longrightarrow Al(CL)_4^- + 3e^-$$

$$2AlCL_4^- + 6H_2O \longrightarrow 2Al(OH)_3 + 6H^+ + 8CL^-$$

(The chlorine ion is liberated and available to continue the corrosion process…..this is bad news and the reason why just minute amounts of ionic contamination can cause failures downstream)

Hermeticity Design Considerations

- ***Susceptibility of the component to moisture and other harmful gases***
  - Remember Au doesn't corrode and most active areas on chip have pretty good passivation these days. Packaging materials hydrophobic vs. Hydrophilic?
  - Keeping moisture out means keeping moisture and other harmful gases like hydrogen in
- ***Expected end use Environment and Service Life***
  - Do the parts run hot? Do they run continuously? What are the temp extremes and T/C cycling environment? How often will the device pass through the dew point? How many layers of moisture will form? Will the moisture have an effect on the device performance electrical specs?
- ***Cost Considerations***
  - Hermetic parts cost more to build and test
  - Silicones, LCPs and other "near hermetic" or novel non hermetic approaches may allow for suitable moisture protection at a greatly reduced cost.
  - However: Part costs must be measured relative to the cost of system failure!!

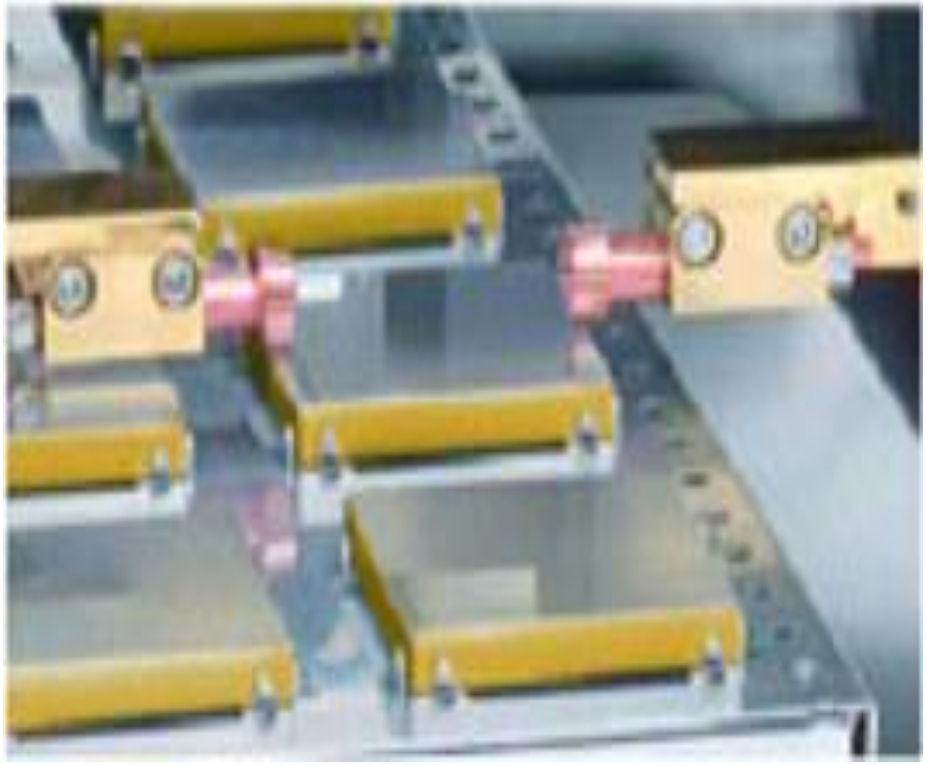
Hermetic Packaging Processes

- MEMS Packaging at the Wafer Level
- Seam Sealing or Brazing
  - I^2R heating melts platings or solder preform
- Laser Welding
  - A true welding process, deeper weld penetration
- Solder seal
  - Furnace reflow
  - Vacuum sealing
- Projection Welding

Seam Sealing

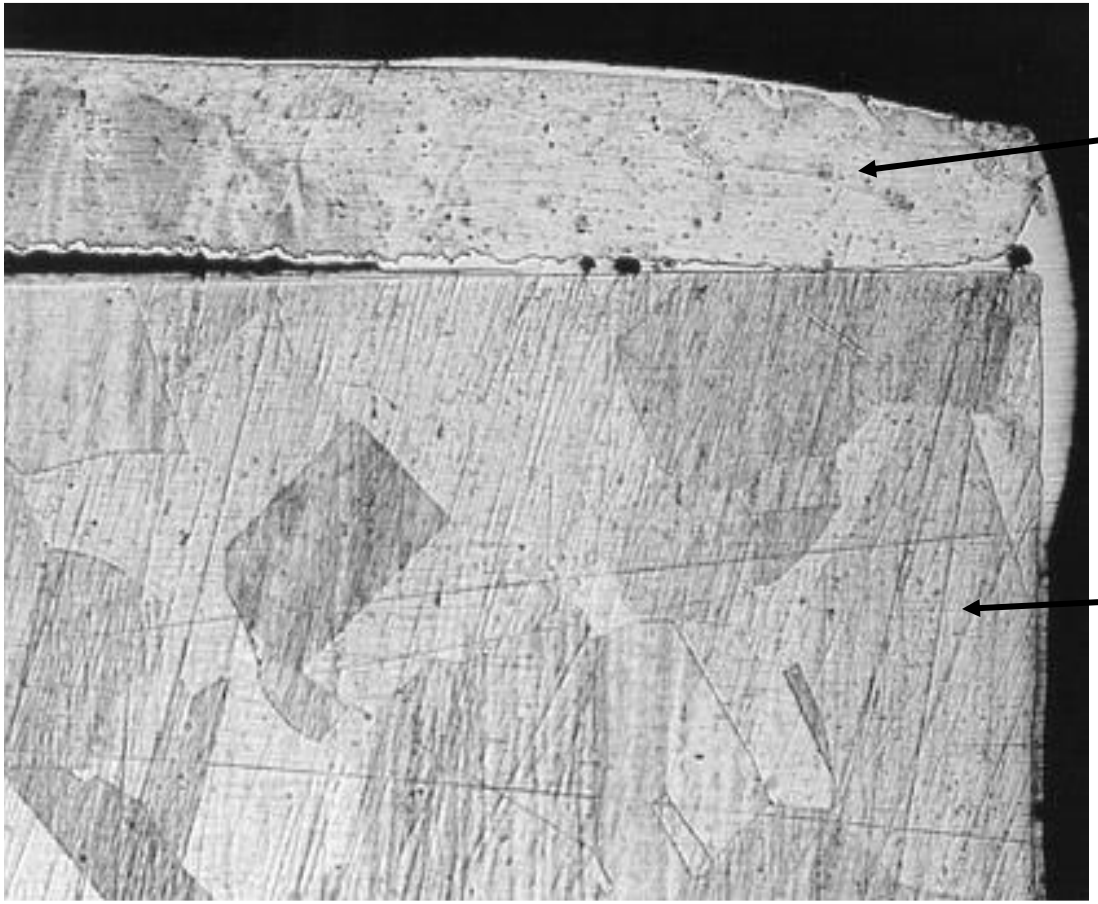
- Electrodes rolling on the seal frame provide localized heating to melt the platings or solder preform
- Key is to provide a seal with a minimum of energy input to prevent excessive grain growth and overheating of the package
- Heating at the lid to package interface can vary from 200 to 1500 C depending on :
  - Speed of rollers
  - Intensity, duration and timing of the power pulses
  - Resistivity of the materials (e.g. can't seam weld aluminum)

Electrode “Rollers” Contacting the Top of Package



Ref: SSEC website

Cross Section Lid to Package Interface

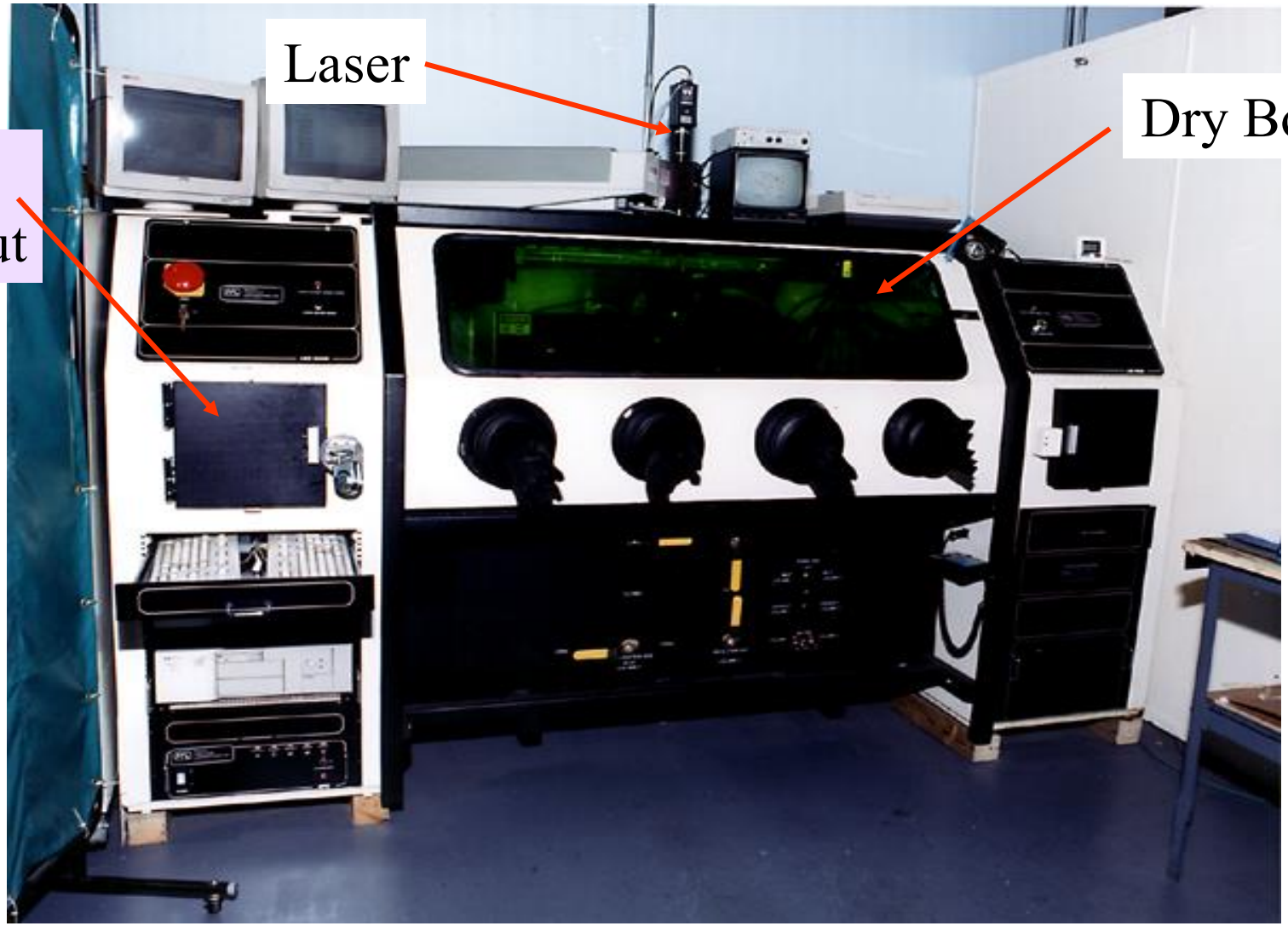


CROSS SECTION (156 X)

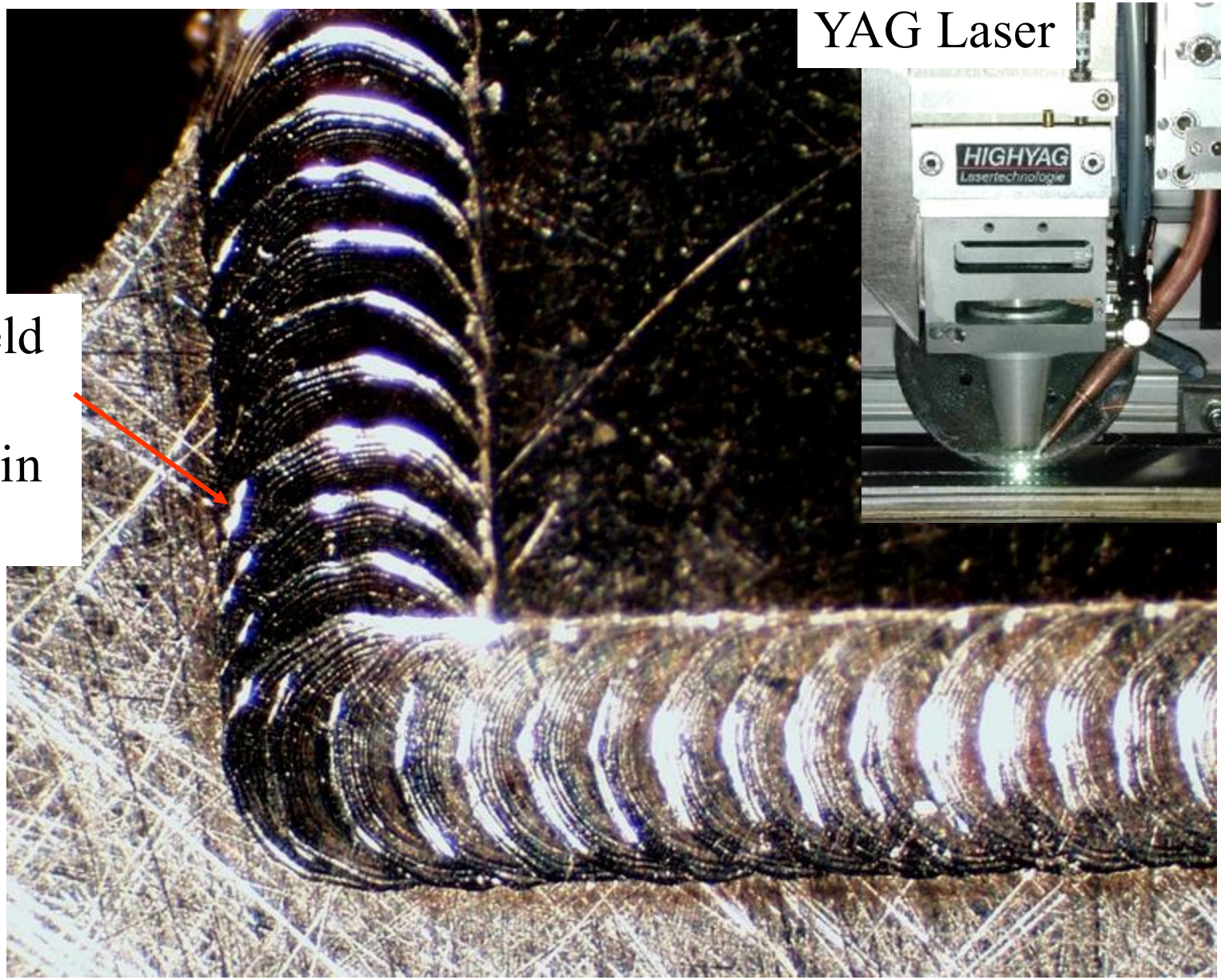
Laser Sealing

- 400 Watt Nd:YAG Laser
- Laser energy is absorbed in localized area and heat is conducted through the weld typical weld penetrations 10 to 60 mils
- Al 4047 cover (contains 12 % silicon) to Al 6061 housing typical. Si needed to improve the ductility of the joint.
- Metals with high S or P usually avoided
- Different joints possible
  - Butt, Lap and Fillet

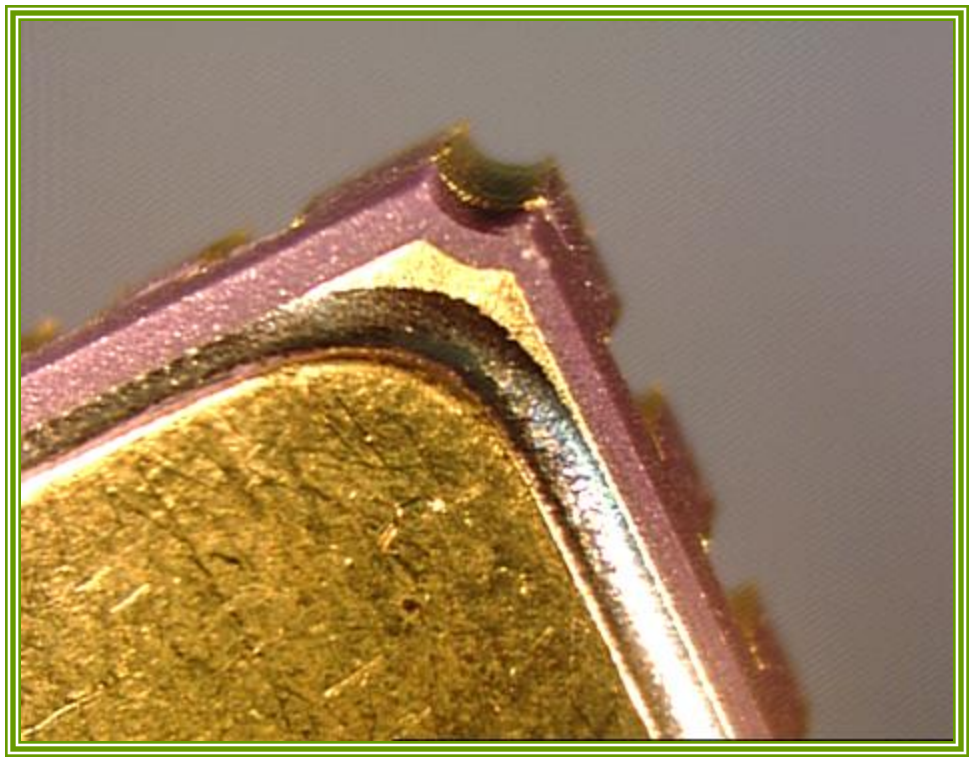
Laser Sealer Setup

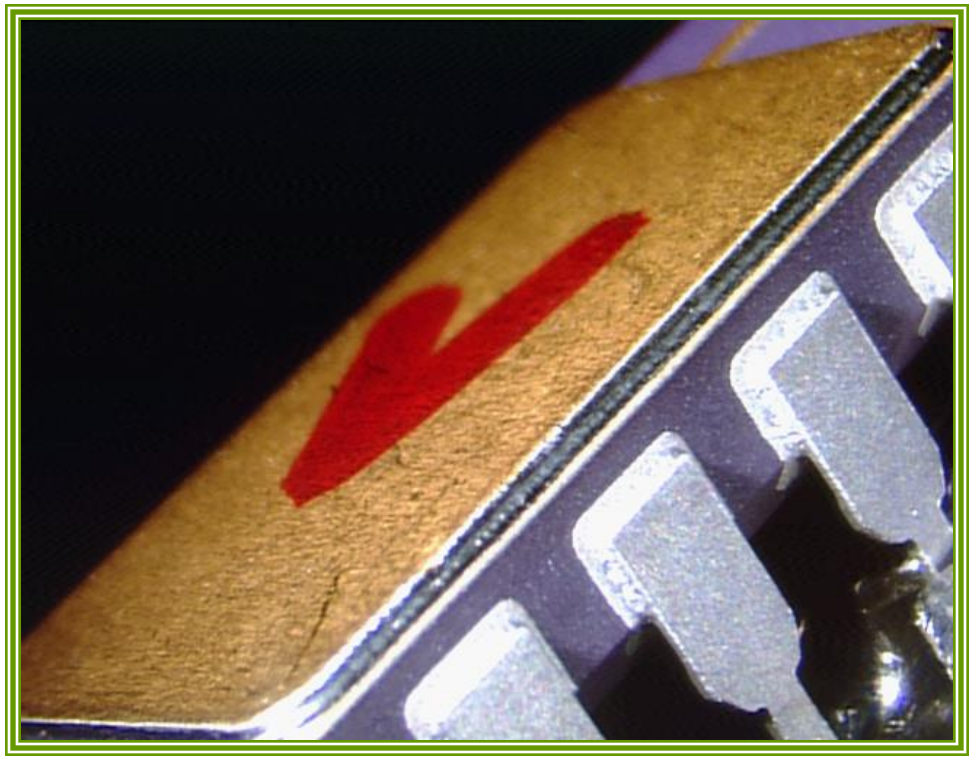


Laser Weld – Top View



Au/Sn Solder Seal of Lid to Package





NOTES: Accept..Photo on the left is a corner view of a nice solder fillet, no voids, no pinholes, nice even fillet. Photo to the right is a side view of a Au/Sn solder braze of lid to package. Both packages were done in a vacuum furnace (inert atmosphere).

Ref. Scientific Sealing Technologies

Impulse Welder in a Glove Box

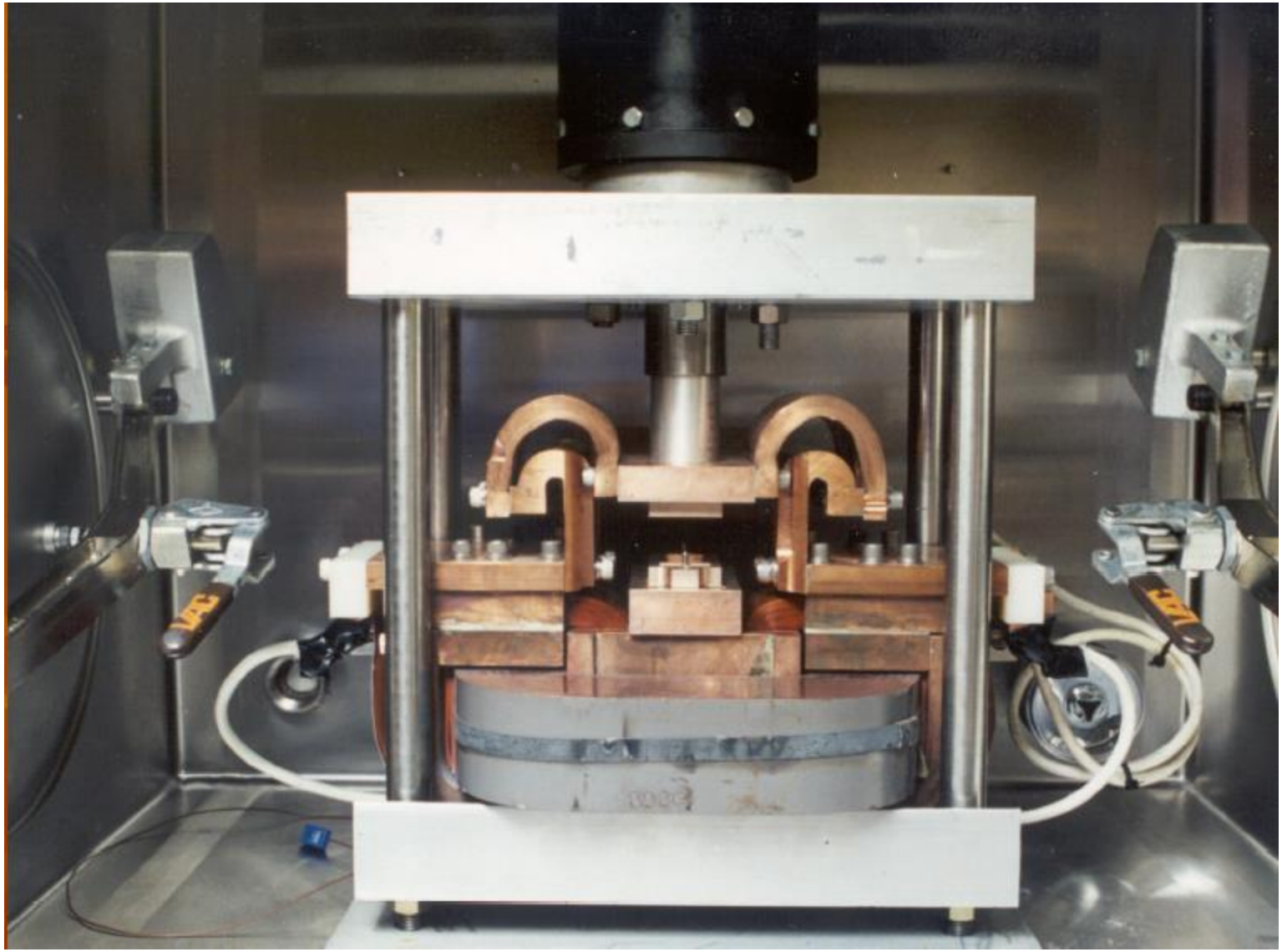


Photo Courtesy of Tom Salzer

Hermeticity Testing per MIL-STD-883 Test Methods

Seal (TM 1014)

Designed to determine the integrity of a hermetically sealed device

Fine and Gross test leak methods defined

Internal Gas Analysis (TM 1018)

Identifies gases internal to a hermetically sealed cavity also known as RGA

These two tests are closely tied together!

Seal Testing per 883 TM1014

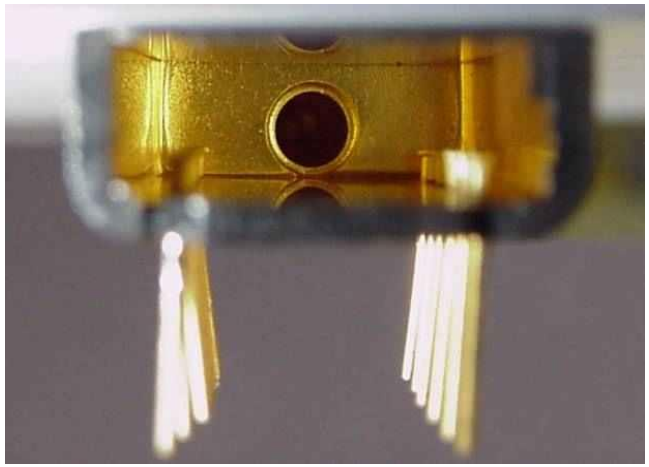
- Helium tracer gas testing
  - Fixed and flexible methods A1,A2 Open Can A4
  - A5 Combined He/O2 dry gross leak, and, He fine leak (per A1 or A2) by mass spectrometry
- Radioisotope fine leak radioactive tracer gas (Kr-85)
  - Condition B1,B2,Combo B1/B2 and Wet gross leak
  - Thermal Leak test at elevated temps
- Gross Leak Testing
  - Bubble Test, Dye Penetrant, Weight Gain Method, C3 Vapor
- Optical Leak Testing…Lid deflection
  - C4 Gross, C4/C5 Gross Fine combo
- Cumulative Helium Leak Detection (CHLD)

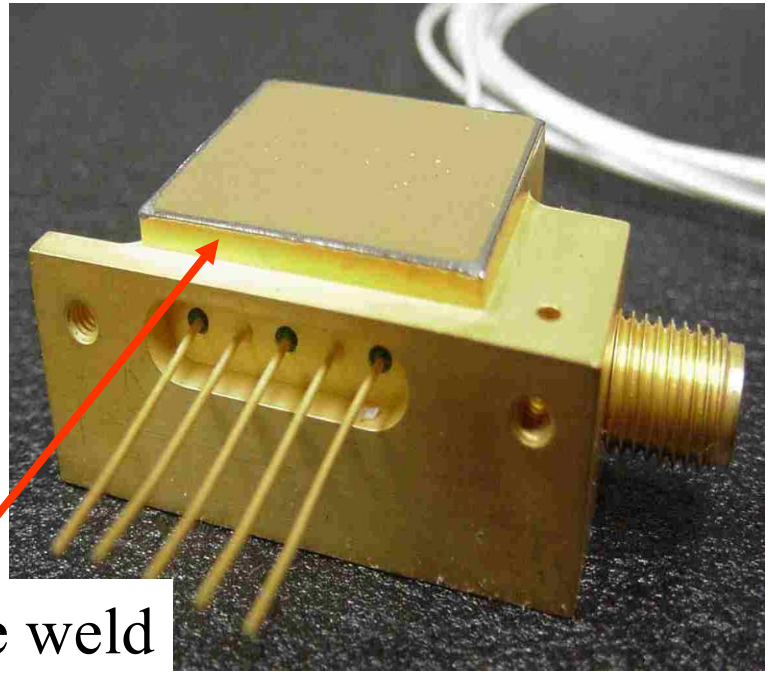
Examples of what Hermeticity Testing Detects

- Cracks or holes in sealing glass to case or glass to pin
- Cracks or holes in multilayer packages
- Inadequate welds in metal cans
- Header glass eyelet cracks
- Incomplete sealing or microcracks in brazed alloys such as Au/Sn
- Non wetting issues in solder seals

- ***But does not detect moisture slowly diffusing through a polymeric material…..which is why the mil specs don't allow one to fix a seal using epoxy***

Sources of Leaks in Packages

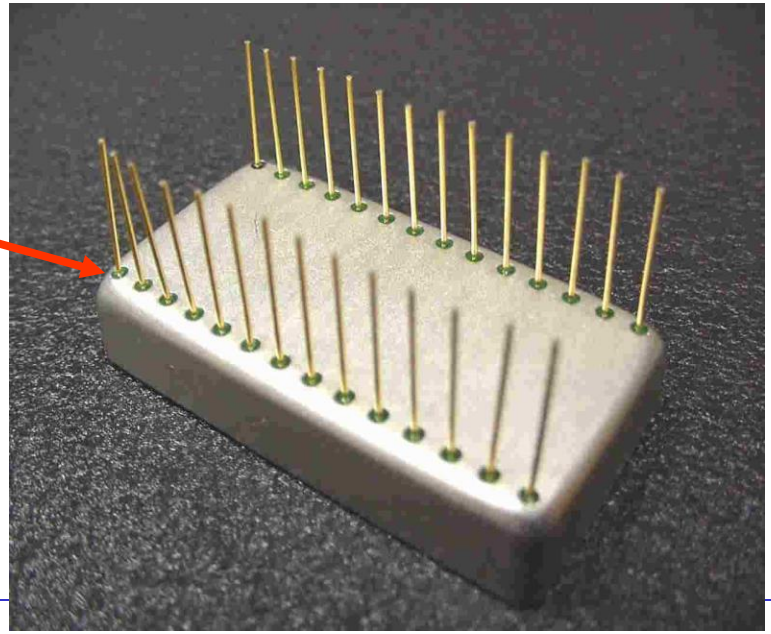




Along the weld

At the glass to metal feedtrough

Or through a defect
in the package itself



Basic Mil Spec Hermeticity Requirement

TABLE VII. Test limits for all fine leak methods. 1/ 2/

Internal Free Volume of package (cm^3)	L Failure Criteria atm-cm^3/sec (air) Hybrid Classes B and H, and Monolithic Classes B, S, Q and V	L Failure Criteria atm-cm^3/sec (air) Hybrid Classes S and K only
≤ 0.05	$5 X10^{-8}$	$1 X 10^{-9}$
>0.05 - ≤ 0.4	$1 X 10^{-7}$	$5 X 10^{-9}$
> 0.4	$1 X 10^{-6}$	$1 X 10^{-8}$

- *Note: the spec is defined in terms of an air leak which is related to but not the same as the measured helium leak rate.*

Helium Fine Leak Test Equipment

Helium bombing tank

Helium Mass Spectrometer

Source: Bid Service Varian Leak Detector

Howl and Mann Equation (ref. handout)

- During a fine leak test helium is initially forced into the package under “bomb” conditions for a specified amount of time/pressure, the amount of helium entering the package will depend on the size of the leak path.
- After “bomb” the package is inserted into the leak detector and the amount of helium escaping is measured..the amount that escapes again depends upon the size of the leak and the partial pressure of the tracer gas helium inside the package (a function of internal package volume)
- The mathematical relationship that relates this physical phenomenon is known as the Howl and Mann equation
- This equation is the basis of the “flexible” method
- Flexible method is now required per latest release of 1014, no longer can use the Table (unless specifically required by contract)

https://store.tjgreenllc.com/product-category/white-papers/

Howl and Mann Equation

$$R_1 = \frac{LP_E}{P_O}\left(\frac{M_A}{M}\right)^{\frac{1}{2}} \left\{1 - e^{-\left[\frac{LT_1}{VP_0}\left(\frac{M_A}{M}\right)^{\frac{1}{2}}\right]}\right\} e^{-\left[\frac{LT_2}{VP_0}\left(\frac{M_A}{M}\right)^{\frac{1}{2}}\right]}$$

Where:

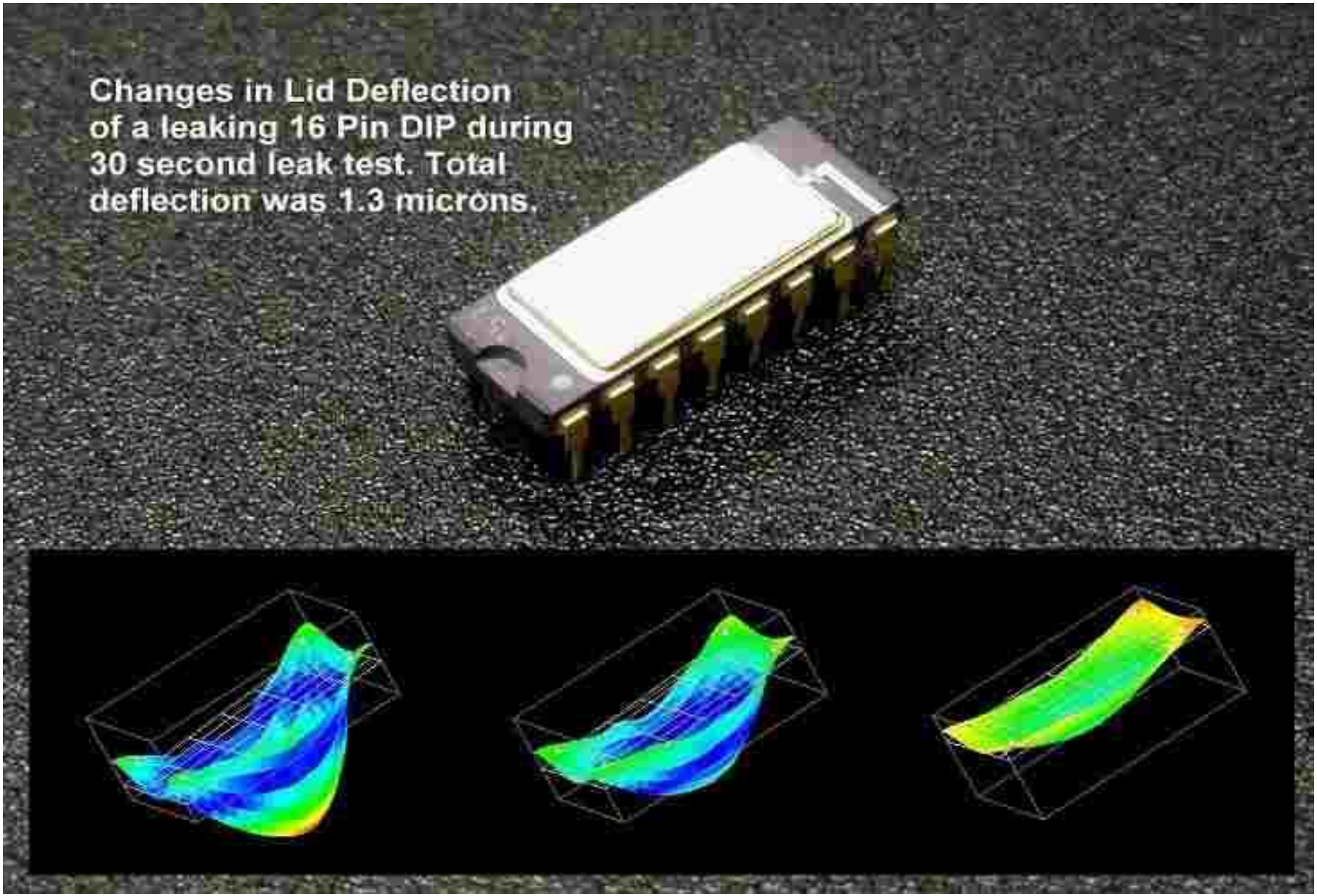
- R_1 = The measured leak rate of tracer gas (He) through the leak in atm cc/s He.
- L = The equivalent standard leak rate in atm cc/s air.
- P_E = The pressure of exposure in atmospheres absolute.
- P_O = The atmospheric pressure in atmospheres absolute. (1)
- M_A = The molecular weight of air in grams. (28.7)
- M = The molecular weight of the tracer gas (Helium) in grams. (4)
- t_1 = The time of exposure to P_E in seconds.
- t_2 = The dwell time between release of pressure and leak detection, in seconds.
- V = The internal volume of the device package cavity in cubic centimeters.

Refer to page 8 in Practical Guide for further explanation

HSHLD® Model 310 High Sensitivity Helium Leak Detector

(Condition A5) Combined Dry Gross/Fine Leak Detector

https://www.orslabs.com/test-equipment/



Ref: John Newman NorCom Systems

Radioisotope Fine Leak Test

- TM 1014 Test Condition B
- Tracer gas is a mixture of dry nitrogen and krypton-85
- Similar to helium fine leak testing…… parts are pressurized or soaked in tracer gas then the number of counts per second is measured and converted to a value Q_s atm/cc/s Kr
  - Qs limits specified in Table III of TM 1014 for 3 different volume ranges
  - Max 1 hour dwell
  - Surface sorption characteristics of the parts must be addressed
- Federal regulations limit the amount of krypton 85 that can be released into the atmosphere 3.1 Residual Krypton

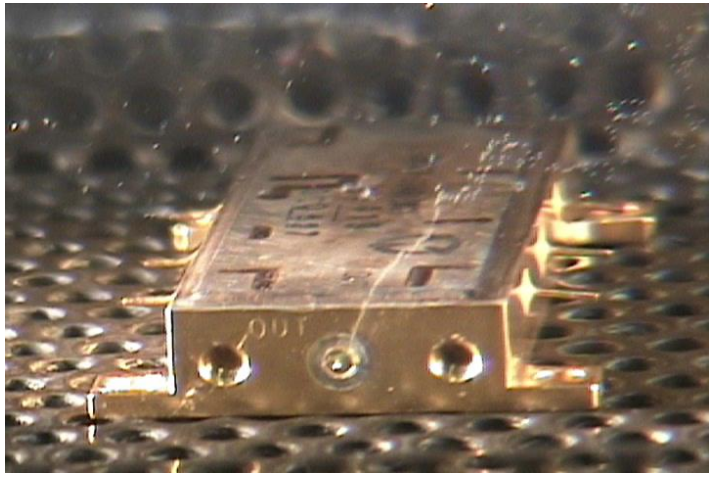
Kr-85 Condition B Pressurization Tank

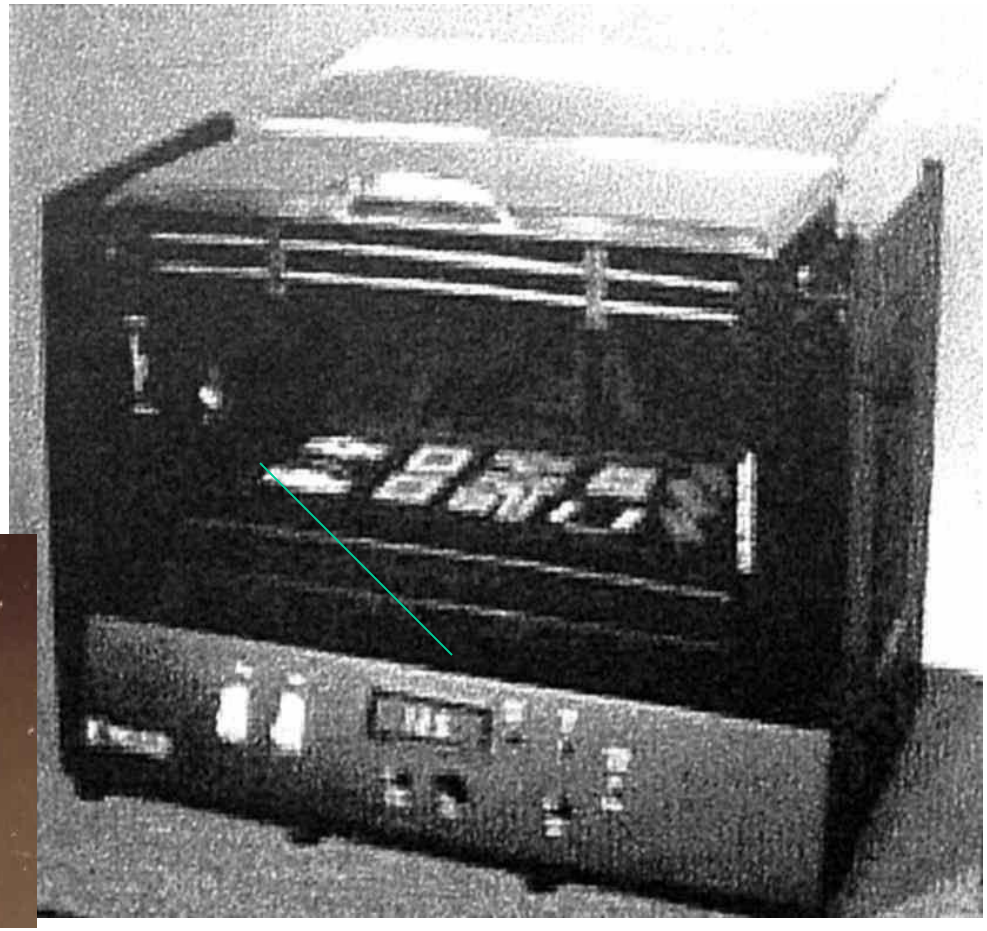
THE BUBBLE TEST

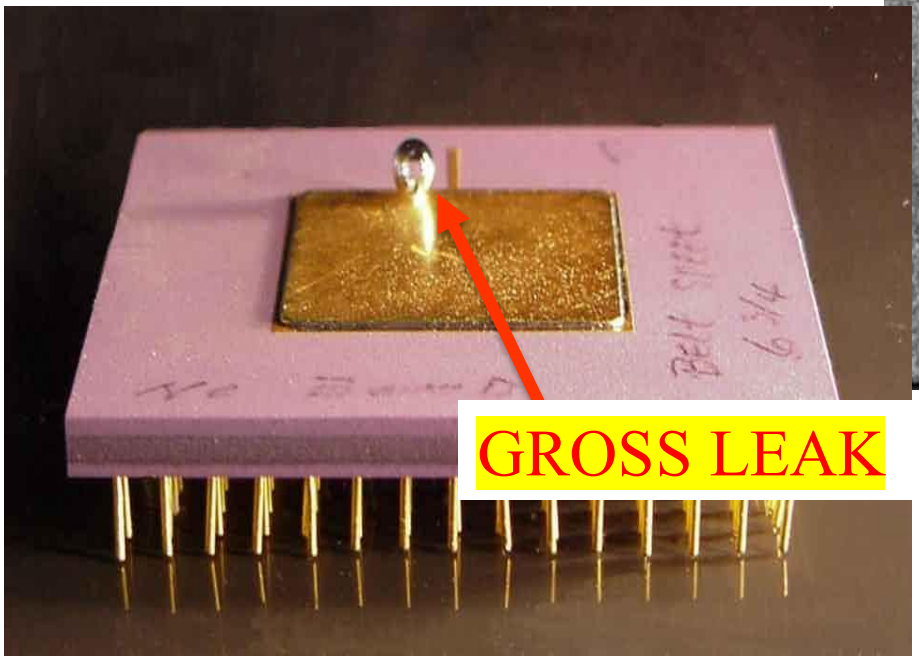
Test condition C, Perfluorocarbon gross leak.

- The test is traditionally used in conjunction conventional fine leak testing. Because during the fine leak testing there is a possibility all the helium will leak out of the package or be sucked down during the pump down cycle before running the test..resulting in a false reading
  - Always do fine leak before gross leak
  - He fine leak testing combined with bubble testing may still miss leakers in the 10^{-05} to 10^{-04} according to RADC Report
- Bubble Test
  - A fluorocarbon (detector fluid) is forced into the package under specified time and pressure conditions and has a boiling point of around 90C. The package is then placed in a liquid bath that boils at 125 C. If you see a couple of big bubbles or a stream of smaller bubbles then it's a leaker!
  - A qualitative test that is somewhat subjective and prone to operator error, especially when you have a lot of parts in the basket
  - Potential Shortages ..3M memo and environmental concerns

Gross Leak Bubble Tester





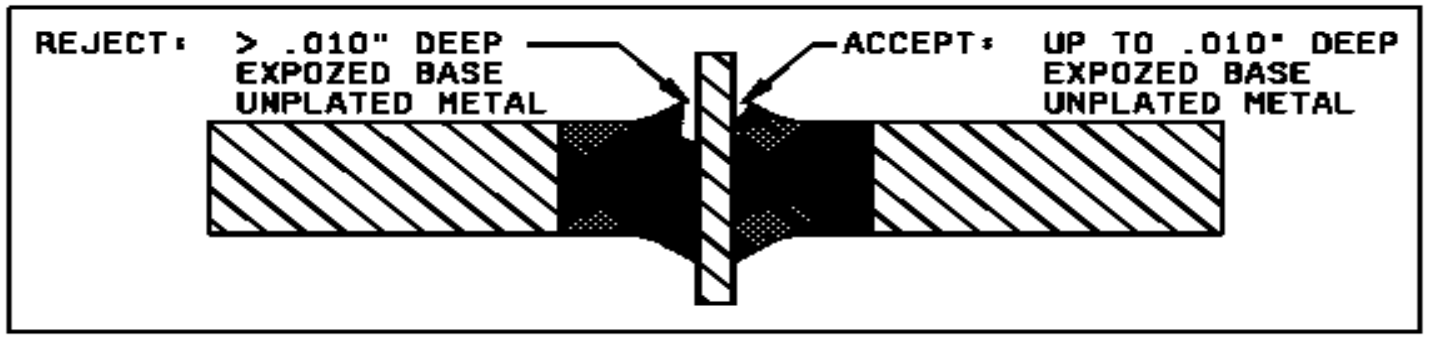


Bubble Video

External Visual Inspection

- Typically performed after test and screen just prior to pack and ship Mil-883 TM2009
- Defines inspection criteria for package markings, workmanship, glass to metal seals, platings, solder on leads etc…
- Major controversy over glass to metal seals
  - good cracks vs bad cracks and their relationship to hermeticity failures (guess what there is none !)
  - exposed base metal
- Can't inspect for fine leaks
- Per the Mil Specs you can't improve a seal and make it hermetic by adding epoxy. Even though a leaker can be made to pass by adding epoxy it's still not an effective seal against moisture penetration. However, If a part does pass leak test and the seals appear cracked some companies will add epoxy to strengthen the lead and prevent further cracking.

Crack Glass Seal Criteria per TM 2009



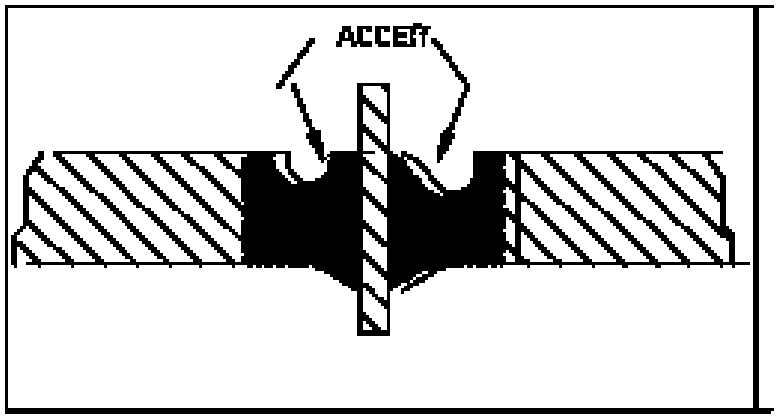


FIGURE 2009-7a. Surface bubbles.

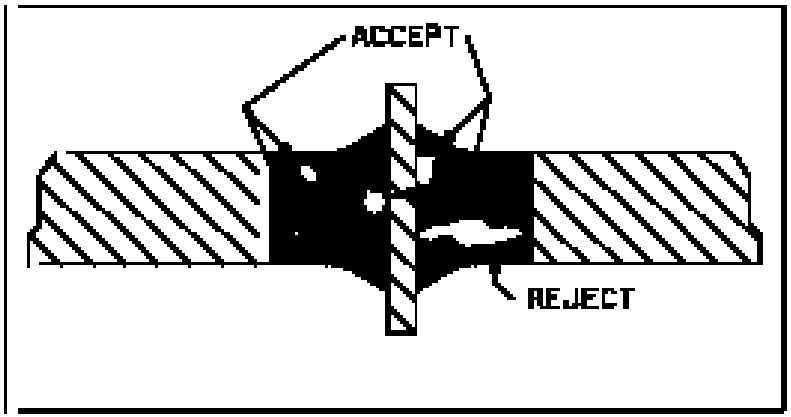


FIGURE 2009-7b. Subsurface bubbles.

Crack Glass Seal Criteria per TM 2009

FIGURE 2009-3. Crazed glass surface.

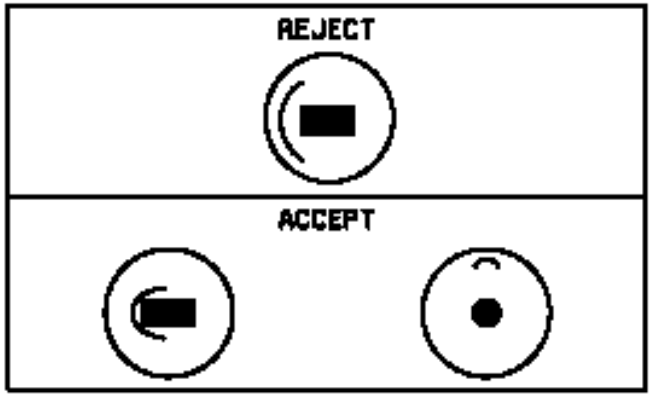


FIGURE 2009-4. Circumferential cracks.

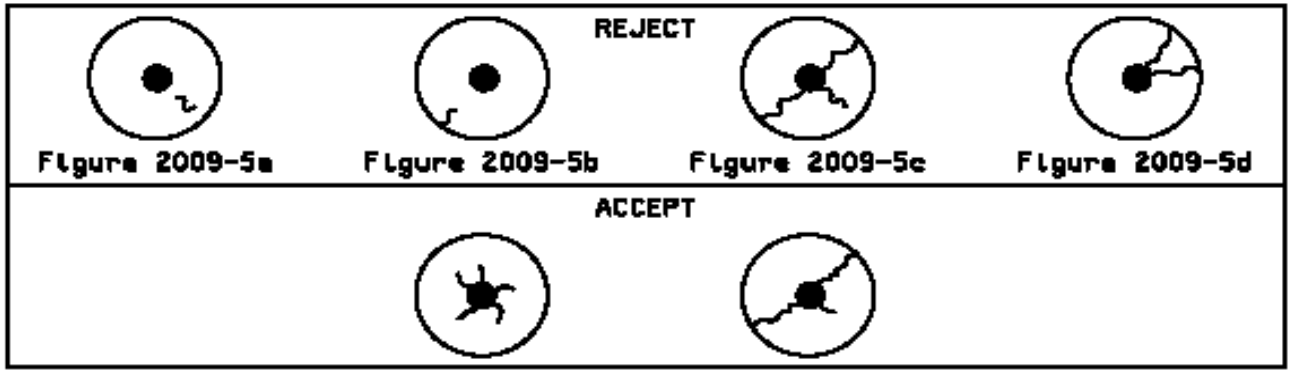
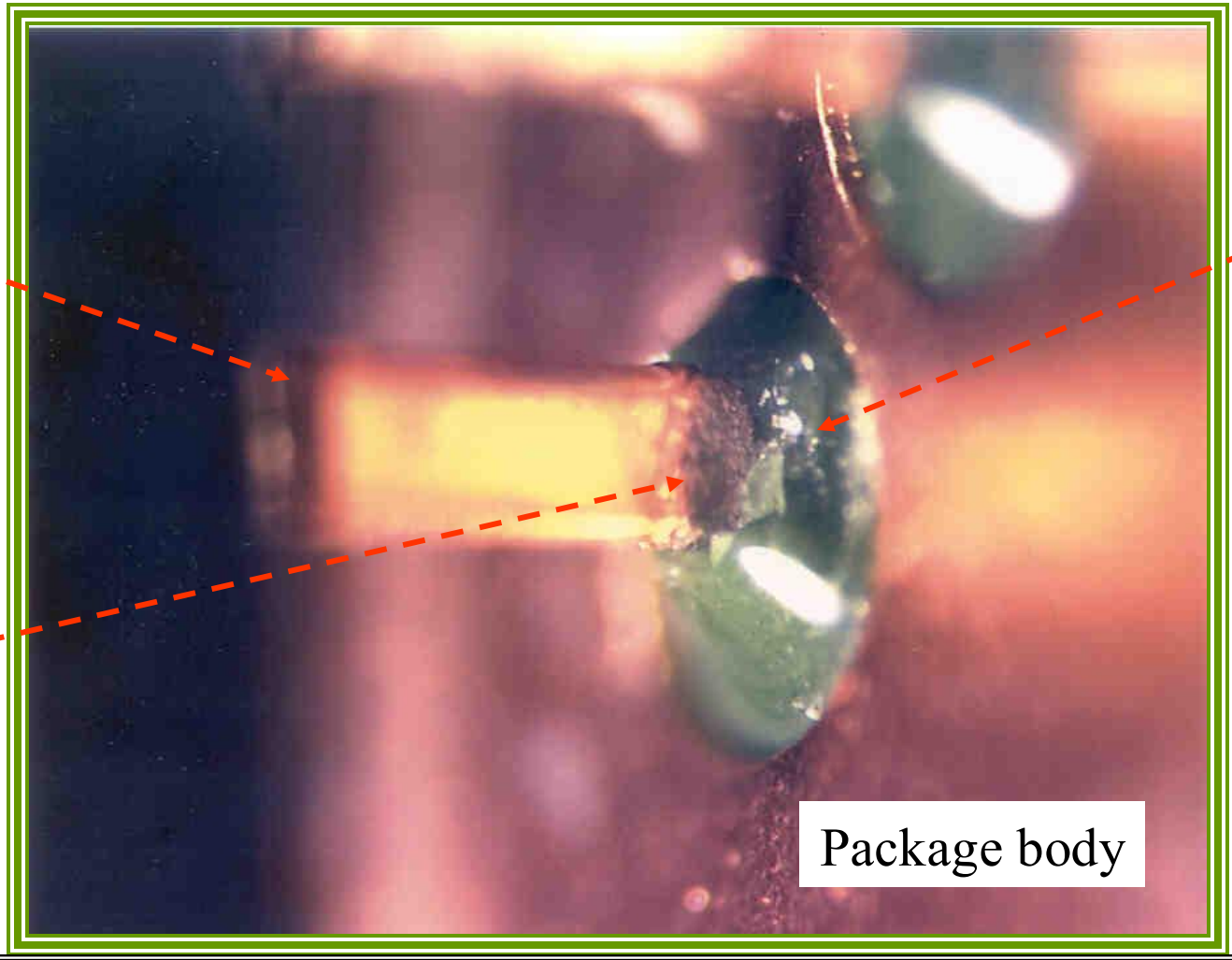


FIGURE 2009-5. Radial Cracks.

REJECT

Chipout in Glass to Metal Seals



NOTES:Reject.. A significant chipout in the glass to metal seal which exposes the base Kovar metal on the lead. (100X)

JEDEC Standard No 9C Sample Criteria

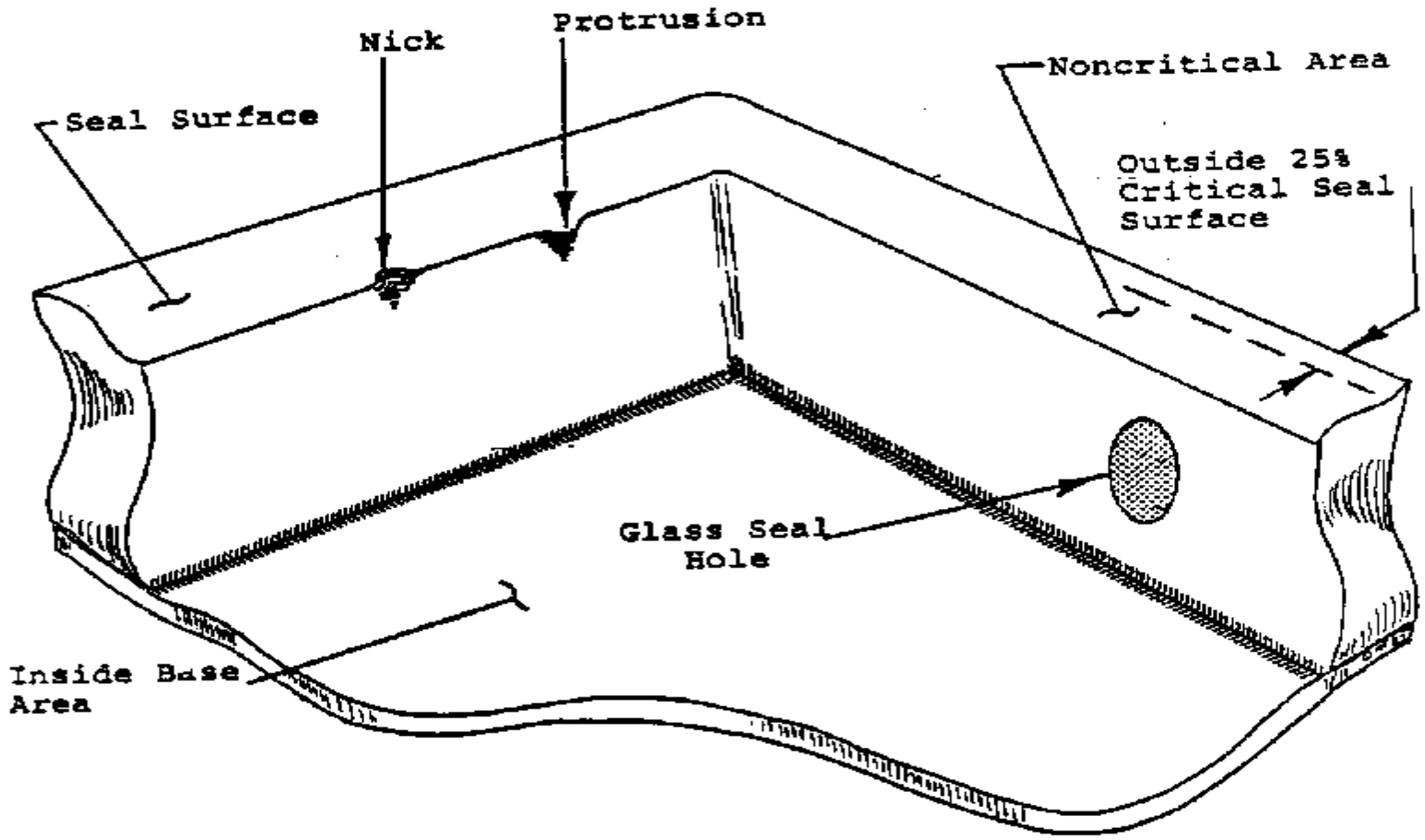
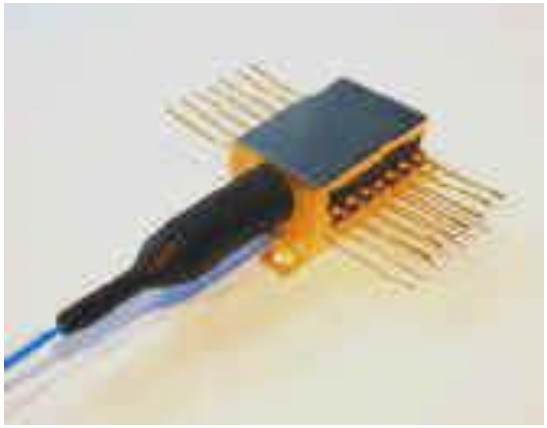


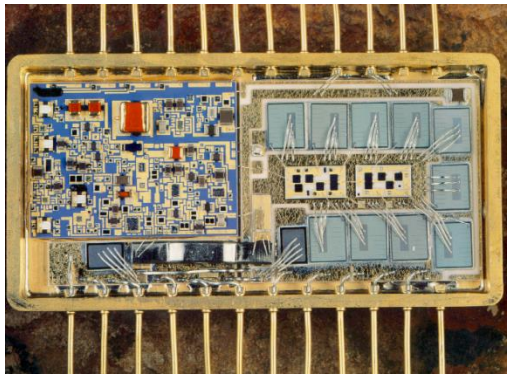
FIGURE 34

CASE SURFACE CONDITIONS

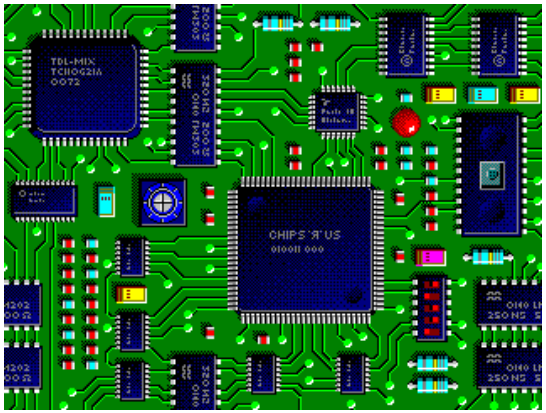
Hermetic (Cavity)



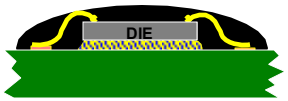
Made from glasses, metals and ceramics



Non-Hermetic (Plastic)



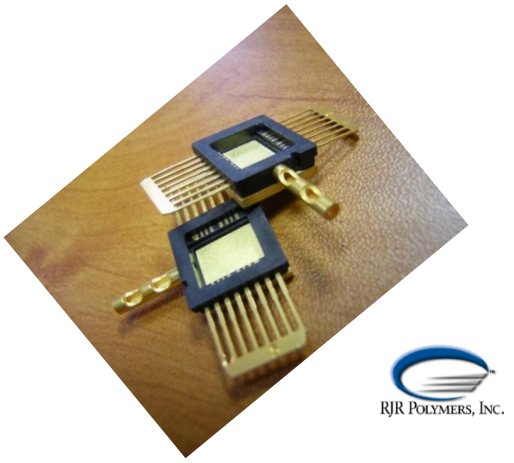
Commercial COTS BGA's, CSPs…



Overmolded

Underfilled

"Near Hermetic" (Cavity)



Cavity's made from polymeric materials

Ref : J. Roman

Does a Part Need to be Hermetic?

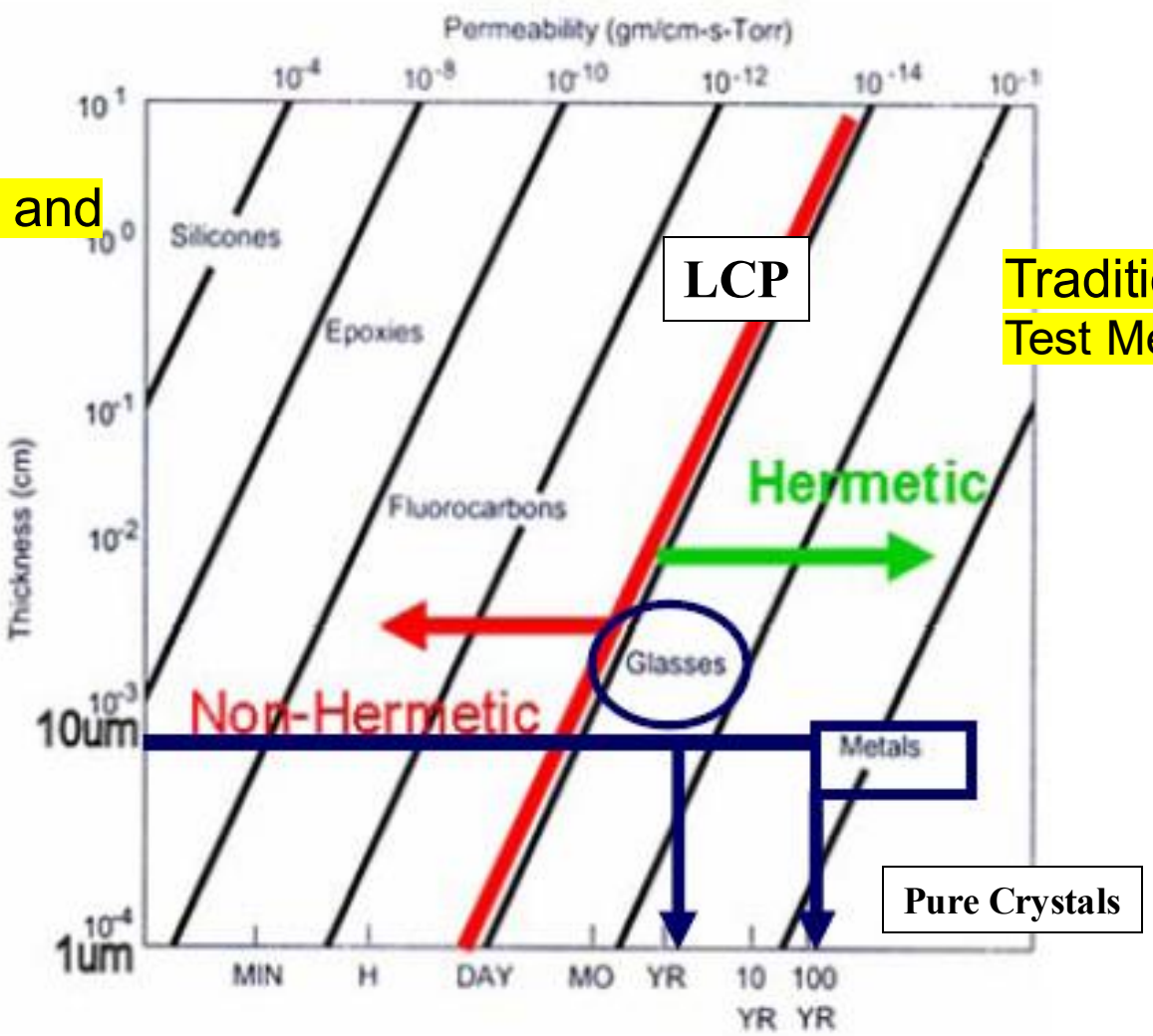
For most Space, high rel military, medical and telecommunications and MEMS Hermeticity is still a requirement but…

- Non hermetic parts cost a lot less..an important consideration for many systems
- For years the automobile industry has assembled microelectronic devices, potted with silicones and snapped on a plastic lids ..these components are exposed to severe environments and generally last close to the advertised warranty period (unless you're the unlucky guy's who's electronic engine control craps out at 102,000 miles!)
- AF Reliability without Hermeticity Program and other efforts to impart the same reliability without the cost of seal/leak test/RGA etc…
- Parts intended for use in Space… Do they need to be hermetic? Hermetic seals protect the parts only while on this planet, Space is a near perfect vacuum
- Moisture inside a hermetic part is often the result of outgassing of the epoxies or the moisture was sealed in from the start
- Some polymer sealed hybrids have lasted 23 to 27 years working successfully in an in controlled military fighter aircraft environment*
- "Non-hermetic" breathable packages may be a better choice for some applications

* D. Dylis and G.H. Ebel "Long Term Package Integrity in a Military Environment" ISTFA 1994

Permeability as a Function of Material Thickness

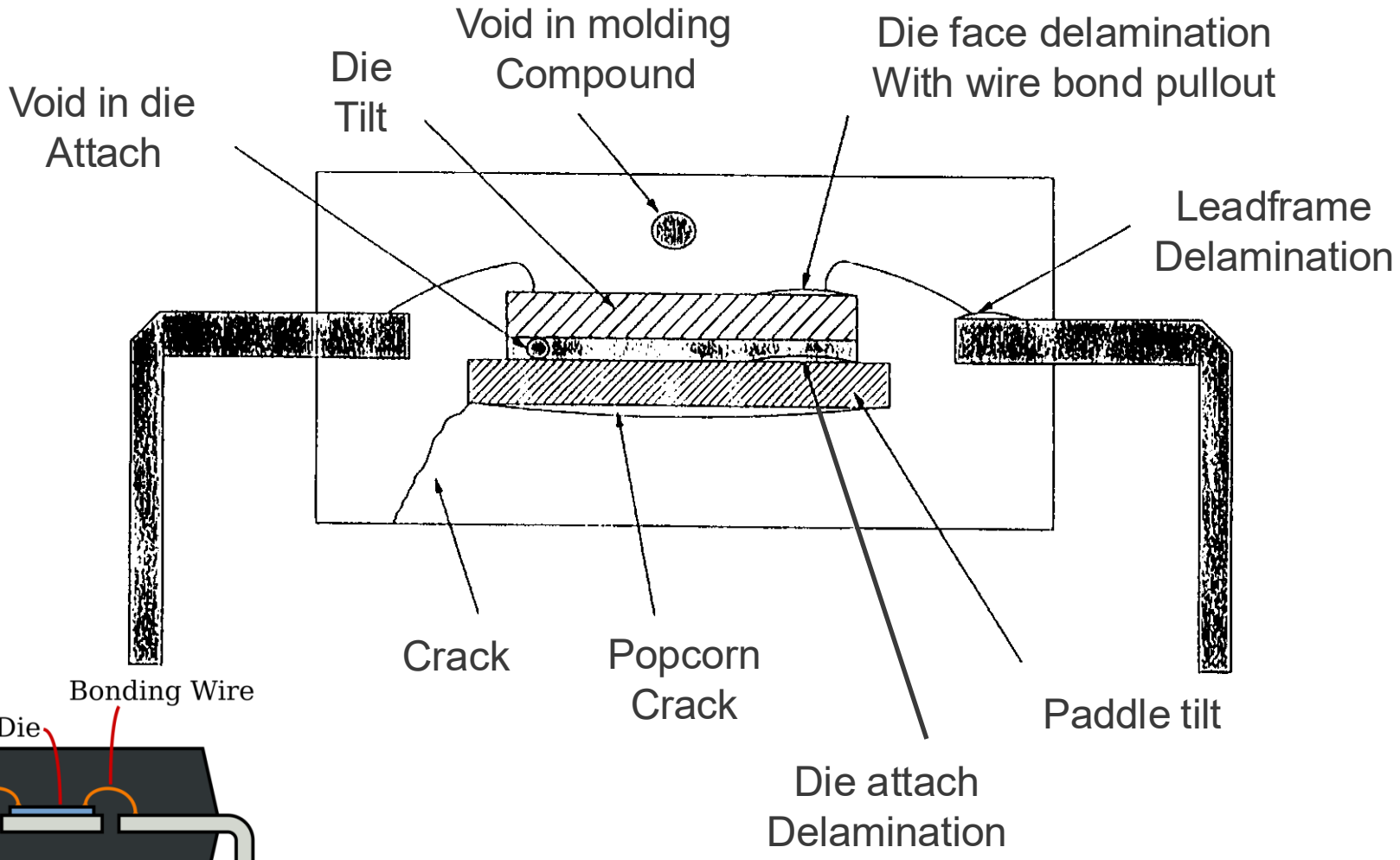
Industry /JEDEC and ??????
Specs Apply

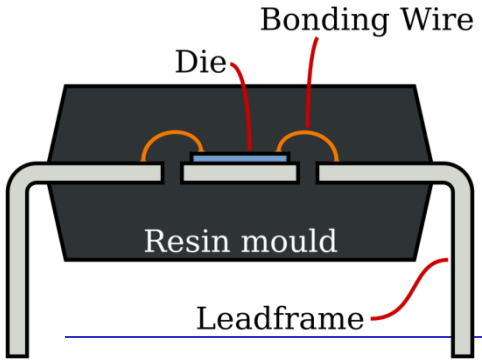


Traditional MIL SPECS
Test Methods Apply

Calculated time for moisture to permeate various materials (to 50% of exterior humidity) in one defined geometry. The red line indicating the transition between hermetic and non-hermetic is somewhat arbitrary.

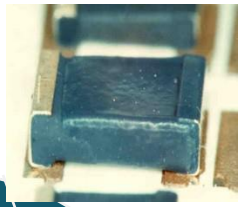
Typical IC Plastic Packaging Defects





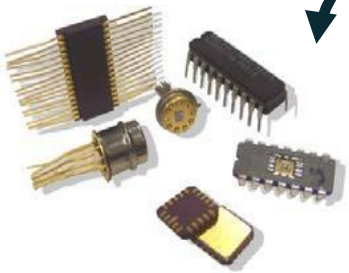
Applicable Mil Specs for Non-Hermetics

access specs here: https://landandmaritimeapps.dla.mil/programs/milspec/DocSearch.aspx



Monolithics

MIL-PRF-38534 Appx B
Class Y for Space



PWBs per IPC specs

Hybrids

MIL-PRF-38534 Appx D

Discrete
Semiconductors

Review JEDEC Task Groups for non-hermetic technology

MIL-PRF-19500R
Appendix J

Minnowbrook Moisture in Microelectronics

October 7-10, 2025

University of Syracuse Conference Center
Adirondack Mountains, New York

Minnowbrook Microelectronics

A forested retreat at the University of Syracuse Conference Center in the Adirondack Mountains of New York where engineers, scientists and technologists meet to explore solutions to the deleterious effects of moisture in microelectronics. Minnowbrook is quite different from the typical technical conference. It utilizes a casual workshop format where questions and discussions often take longer than presentations. Its an educational experience that makes a difference.

https://www.tjgreenllc.com/wp-content/uploads/Minnowbrook2025-About.pdf

THE END

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