Introduction to Electronics Failure Analysis

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Summary of presentation

What is Failure Analysis?

- **What do you do for work?**
  - Forensics for electronics, detective work, kind of like CSI Miami
  - “So you work on computers and stuff?”
  - Not exactly! We are investigating electrical failures in Rockets, Satellites, Defense Systems, Aircraft, Medical Equipment, Vehicle Safety, Power Plants. High reliability applications!

What is Failure Analysis?

- The general flow starts with, obviously, a FAILURE
- Engineering determines a malfunction, troubleshoots the failure to a specific component/area of the PCBA
- Two choices:
  - Desolder the component, throw it in the trash and replace to regain circuit functionality and call it good
    - Cheap, fast, easy
  - Perform component-level failure analysis to determine root cause of failure to prevent reoccurrence
    - Expensive, slow, difficult

Why do we perform it?

- There are many reasons, and as a 3rd party lab with different customers from different sectors, we've seen every reason.
- Safety
- Reputation
- Liability
- Contractual Requirements
- Curiosity
- Money

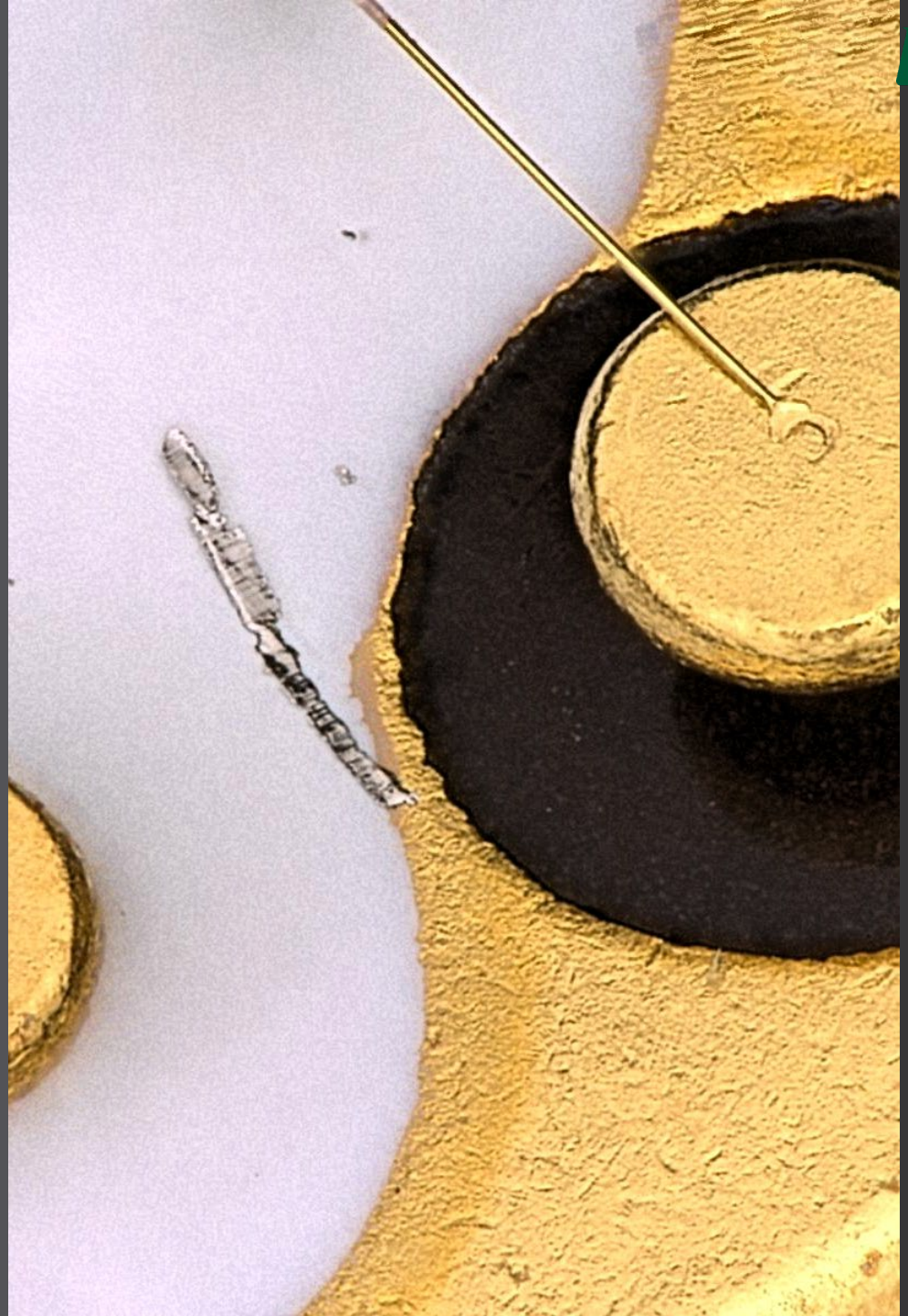
What is the purpose for this seminar?

- Education, understanding what to look for when performing failure analysis and/or requesting failure analysis
- Turnover
  - Retiring, let-go, new careers
  - Leaves the next generation of analysts lacking in experience, and experience is a big part of failure analysis.

What is the purpose for this seminar?

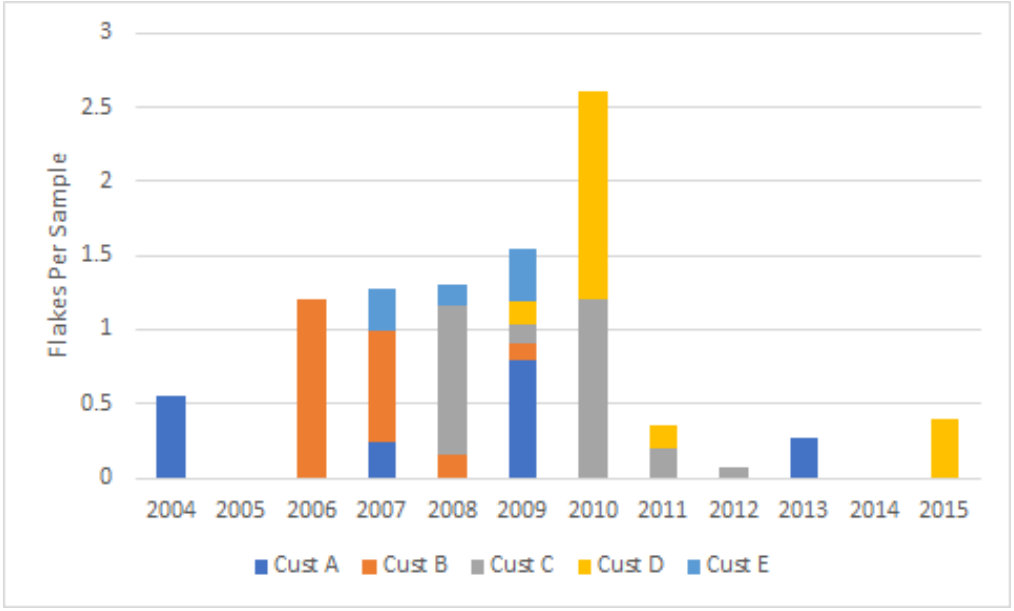
- In this presentation I will provide a very broad overview of failure analysis
- It is intended to familiarize you with the overall FA process and make you aware of common challenges faced
  - In-depth, component specific analysis would take days/weeks to present
- Training and refresher courses help to share knowledge with the newer generation of analysts
- Prevent history from repeating itself!

Nickel Flakes?



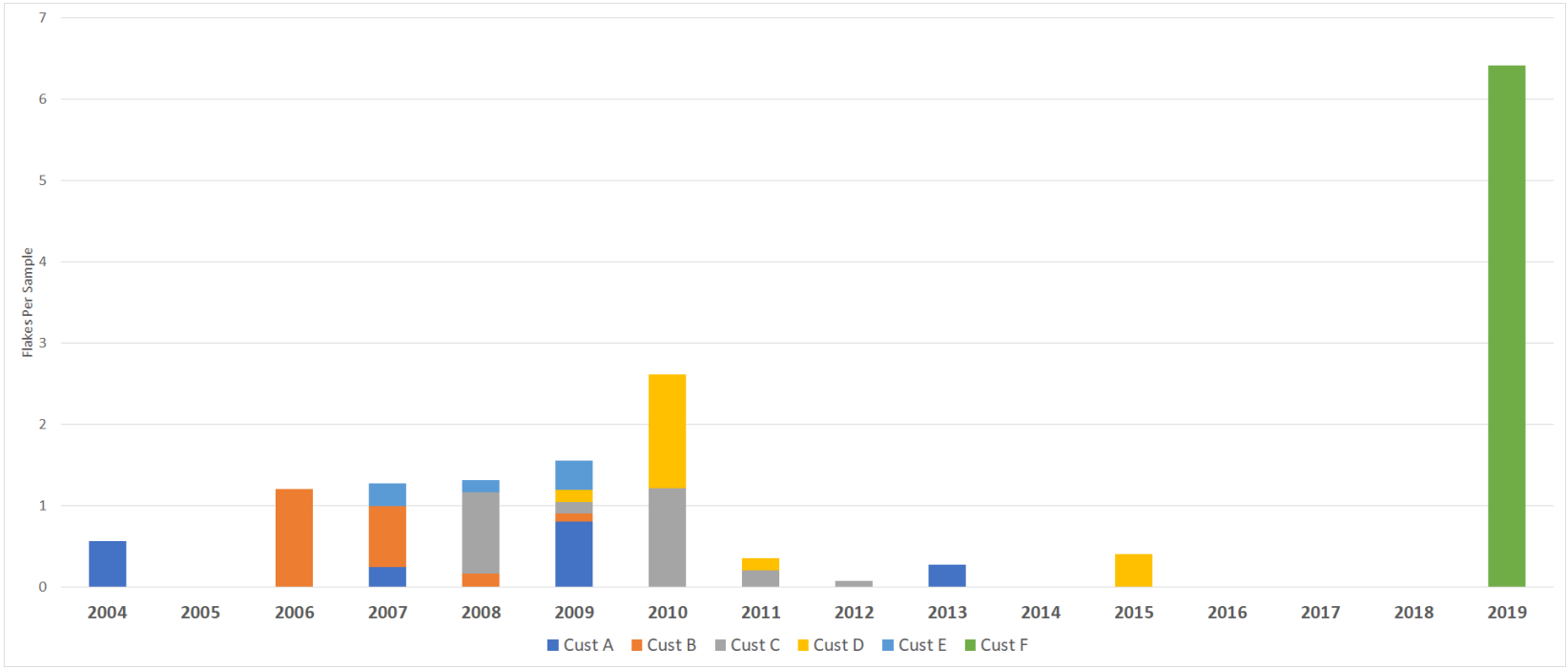
Nickel Flakes?

- We perform nickel flake inspection routinely
- Big push in late 2000s
- Gidep alerts for components with nickel flakes going back to 1969
- After 2010 much fewer nickel flake inspections and/or nickel flakes found in components
- Had manufacturers solved the nickel flake problem?



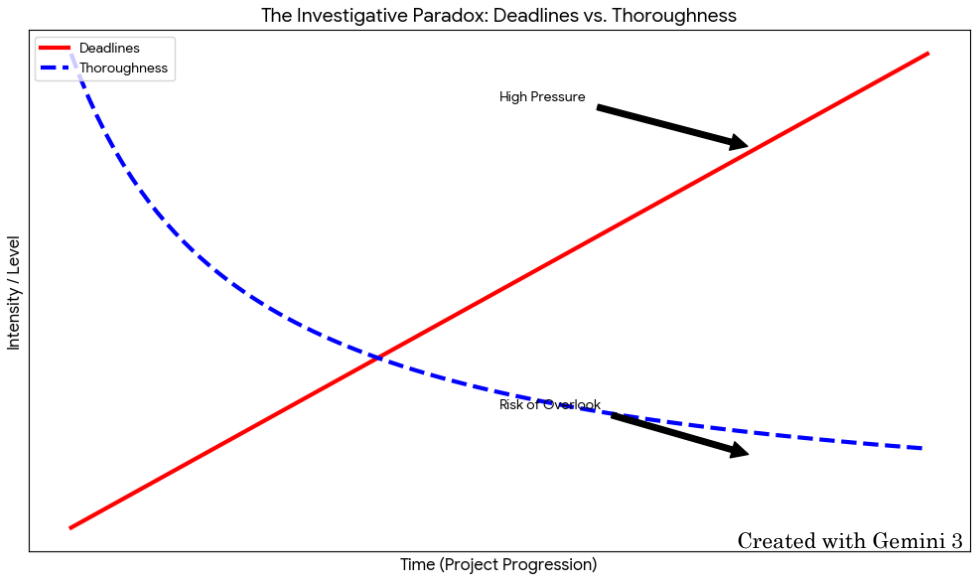
Nickel Flakes?

- No, there was a resurgence in nickel flakes and inspection in 2019 following yet another failure caused by nickel flakes!



Trends in Failure Analysis

- Evolution of component design and complexity
- More FRBs
- For 3rd party analysts, more instances where the only point of contact is a buyer
- Deadlines, deadlines, deadlines!



FA Lab Setup

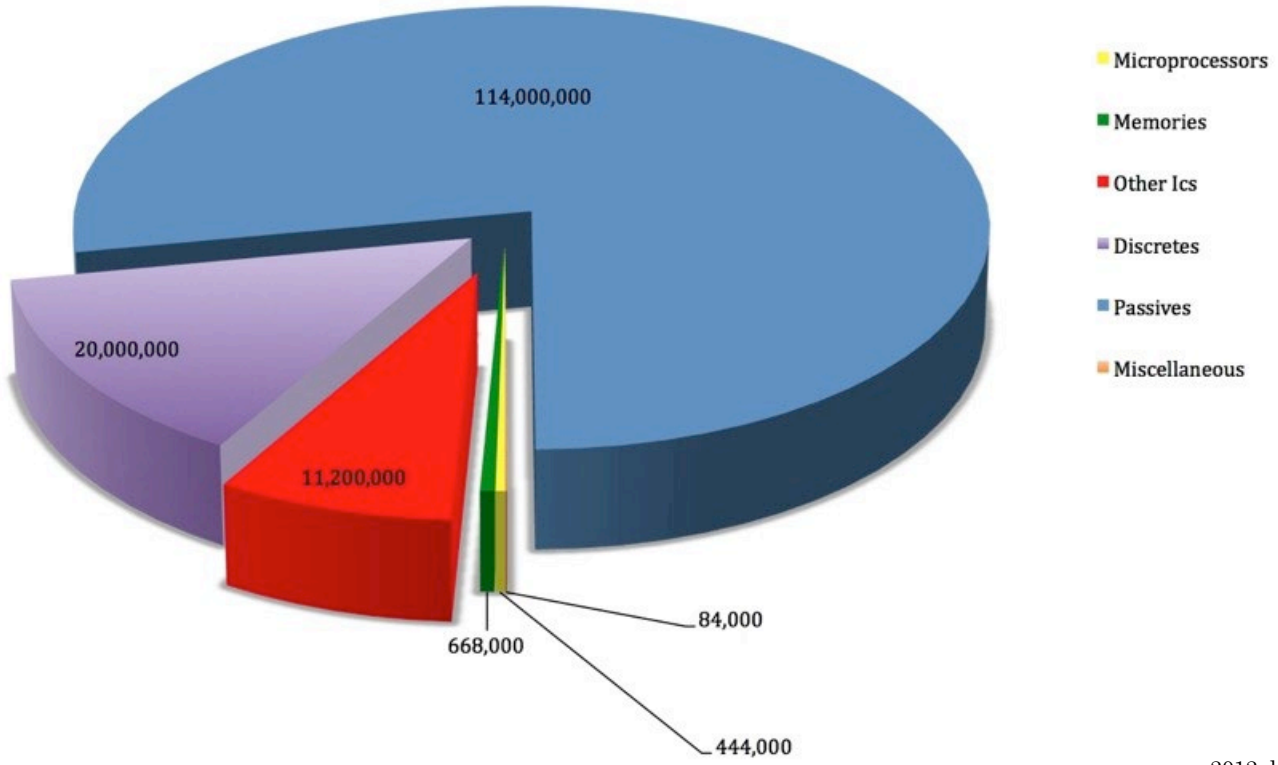
Created with Gemini 3

FA Lab Setup

- What do you need to start failure analysis?
- Personnel
  - Not just anyone, you need people who are curious and determined to “get to the bottom” of the failure analysis.
- Equipment
  - The multi-million dollar equipment showcased at failure analysis conferences or other shows is nothing short of remarkable.
  - BUT, this equipment is not required for the majority of failure analysis, and is more aimed at microprocessor or memory device analysis, especially at the fabrication level.

FA Lab Setup

- This pie-chart shows a representative part distribution for a space-level program.
  - While microprocessors and memory chips are vital components, that do experience failures, the supporting circuitry is arguably just as vital, and just as prone to failure.



2012 data

FA Lab Setup

- Some of you may be part of an existing lab, or trying to set up a lab, here's what you need:
- **Low magnification documentation**
  - Cell phone camera
  - Macro photography stand and lighting
  - This pictures matter for future reference

FA Lab Setup

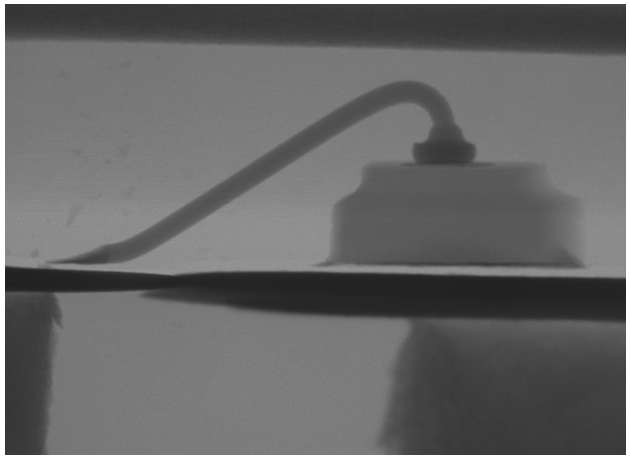
- **High magnification inspection/documentation**
  - Stereoscope with in-line digital camera that can interface with computer/tablet/cell phone
  - Compound microscopes with digital camera
    - Understanding lighting and polarization
  - Digital microscope systems (Leica, Zeiss, Keyence)

Image from Keyence

FA Lab Setup

- **Radiographic inspection/documentation**
  - What is it, why is it so important?
  - It's X-Rays, just like when you go to the dentist or the doctor
  - Non-destructive (mostly)
  - Allows internal inspection for packaging damage/defects, or other abnormalities

Image from yxlon



FA Lab Setup

- **Radiographic inspection/documentation**
  - Provides an as-received record of the condition of the component, especially with CT
  - Can be accomplished with basic film X-Ray, where you set the sample up, expose it, and then can examine the resulting image. Less expensive, much older tech
  - Real-time X-Ray is much more preferred and common in the industry. Allows manipulation of the component while inspecting in real time, and is quick and easy to use.
  - Computed tomography (CT) can be an addon for real-time X-Ray systems. Allows 3d rendering and virtual cross sectioning of the component. More expensive, less common, can take a very long time depending on the many factors. Provides excellent documentation of the condition of modules and PCBAs

Computed Tomography (CT)

The client reported an intermittent circuit and their engineering team isolated it to a suspected via. CT inspection found that a drill bit had broken off in the via, resulting in normal operation at first.

FA Lab Setup

- **Scanning Acoustic Microscopy (SAM), sometimes referred to as C-SAM**
- Also allows non-destructive analysis
- Damage can result in package delamination/fracturing
- Packaging defects, contamination ingress paths
- Not always applicable, but worth using if you have one available. Otherwise, it is recommended to sub this work out until workload warrants purchase

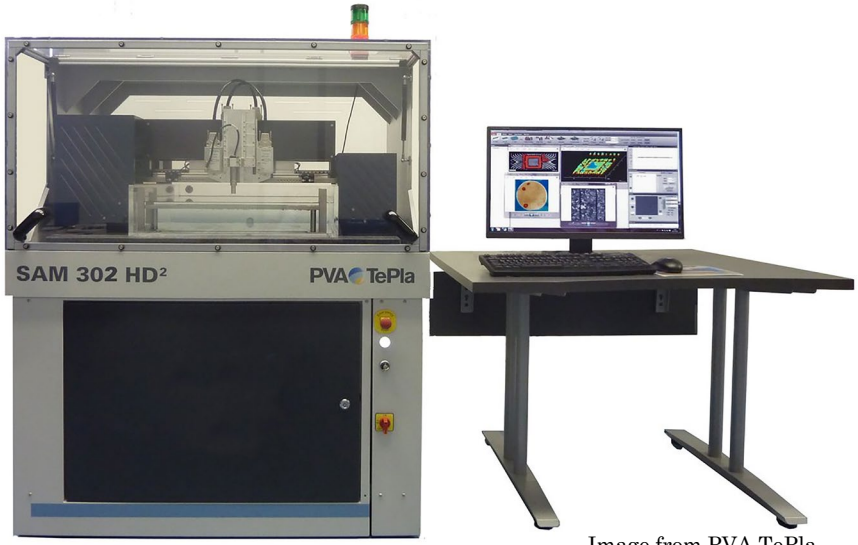


Image from PVA TePla

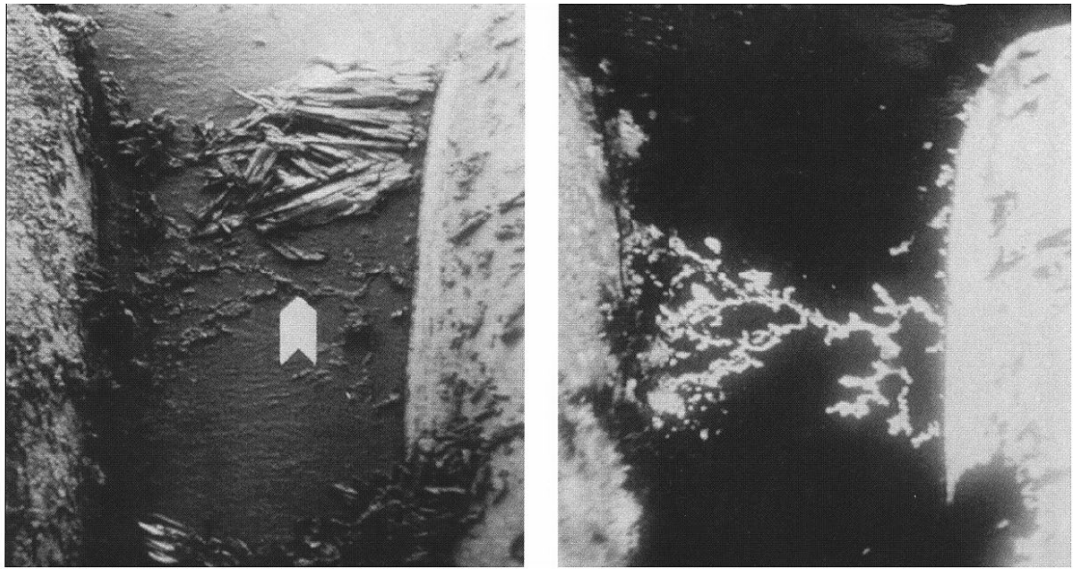
FA Lab Setup

- **Scanning Electron Microscope (SEM) with elemental analysis capabilities, e.g. Energy Dispersive Spectroscopy (EDS)**
  - Sometimes called EDX or "EDAX"
- Likely the most expensive "must have" piece of equipment
- The SEM allows for very high magnification inspection and documentation of materials, but it also provides a lot more information than just a super-high-magnification microscope.

Image from Thermofisher.com

FA Lab Setup

- **Scanning Electron Microscope (SEM)**
- How does it work?
- Instead of light to image the sample, like a standard microscope, it uses an electron beam
- The electron beam interacts with the sample and, for the sake of this discussion, emits secondary electrons (SE), backscattered electrons (BSE) and X-rays. We use all of these!



Secondary emission image on the left, backscatter image on the right

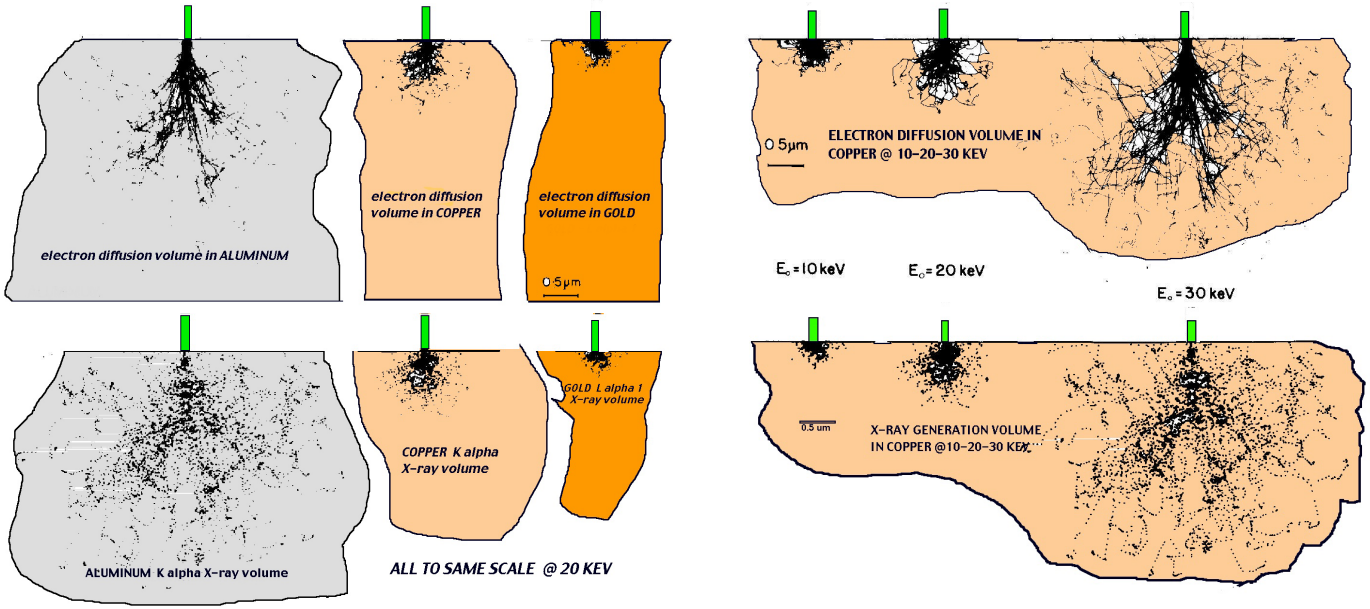
FA Lab Setup

- **Scanning Electron Microscope (SEM)**
- Machine setup and alignment is critical for SEM use.
- Machine operation will be manufacturer specific. Training is recommended to get the most from your machine.
- You may be limited on access depending on your company's policies, so do whatever you can to get them to buy your own personal SEM!

- **Sample prep!**
- The SEM will cause insulators to build up a charge, and when image a charged material it will become distorted, and you will also find erroneous EDS results.
- Charging can be mitigated by proper sample prep **OR** proper SEM setup.
  - "Normal" SEM setup uses 5-20KV beam voltage, which will likely charge insulators you may be interested in analyzing.
  - It's recommended to start at lower voltages, e.g. 1.5-2KV – The cost here is that you lose signal, image quality, and EDS analysis capabilities.
  - Sample prep, to put it simply, electrically grounds the sample which keeps the charge from occurring.
    - Typically this is accomplished with a conductive coating: gold and palladium, or a colloidal carbon paint. – **You will likely need a coater!**

FA Lab Setup

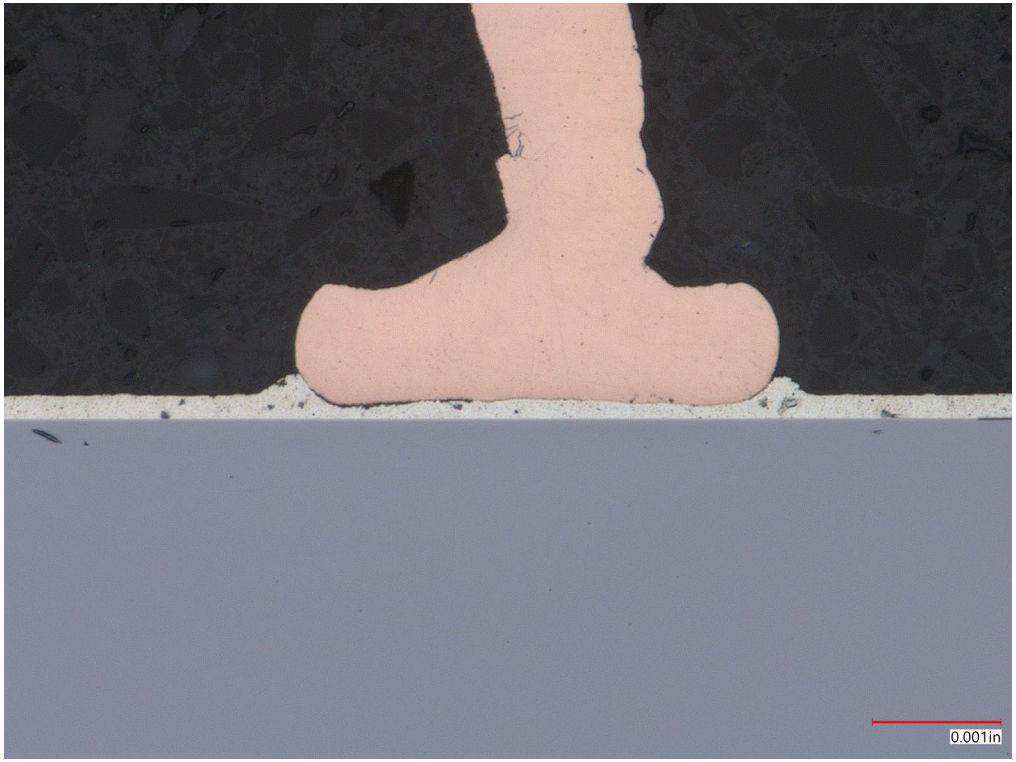
- **Scanning Electron Microscope (SEM)**
- Beam voltage is one of the most important parameters for sample analysis.



Images showing electron diffusion in various materials and at different beam voltages. Note that the material density also plays a role.

FA Lab Setup

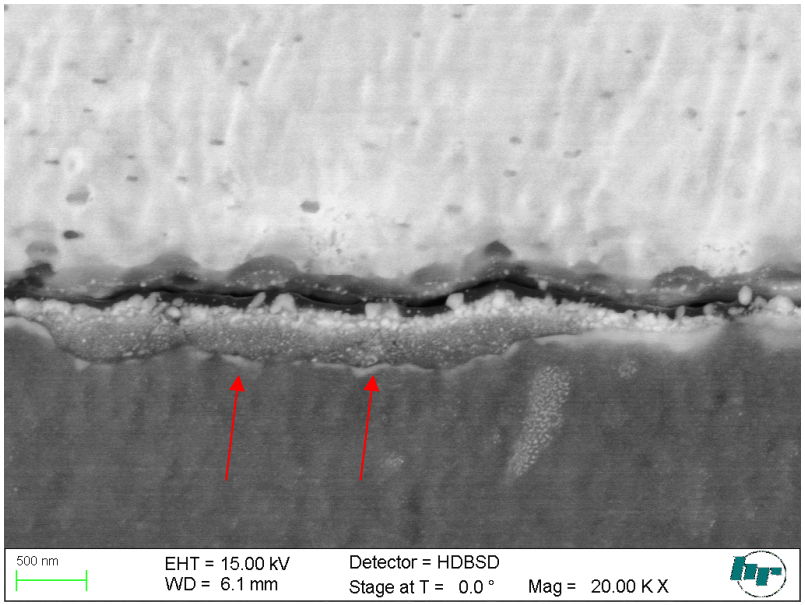
- **Scanning Electron Microscope (SEM)**

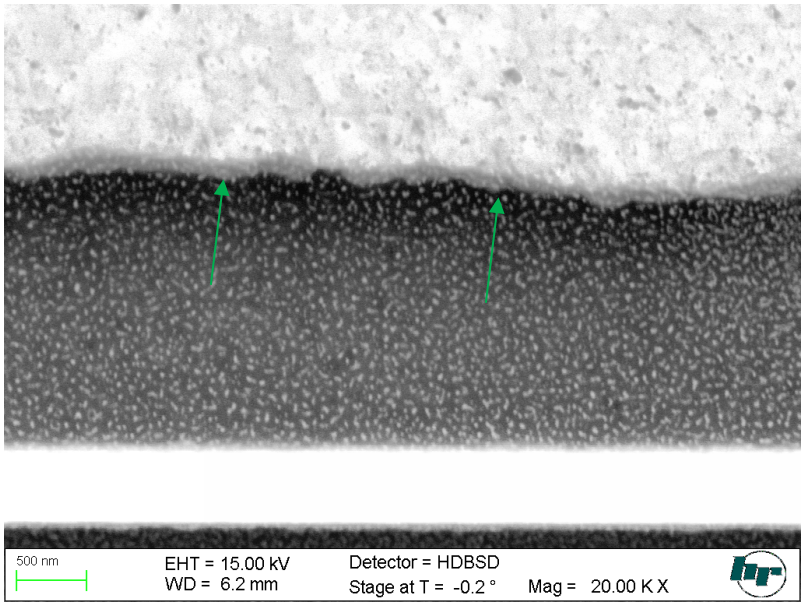


Optical image of a cross sectioned diode that failed with high V_F. This was due to a bond lift/fracture, but what caused that?

FA Lab Setup

- **Scanning Electron Microscope (SEM)**





Not only does the SEM allow for higher magnification inspection (these images are at **20,000x**), but using alternate modes like Backscatter Electron Detection provides better differentiation of materials. In this case, we can see poor intermetallic formation in the failed device when compared to a "known good".

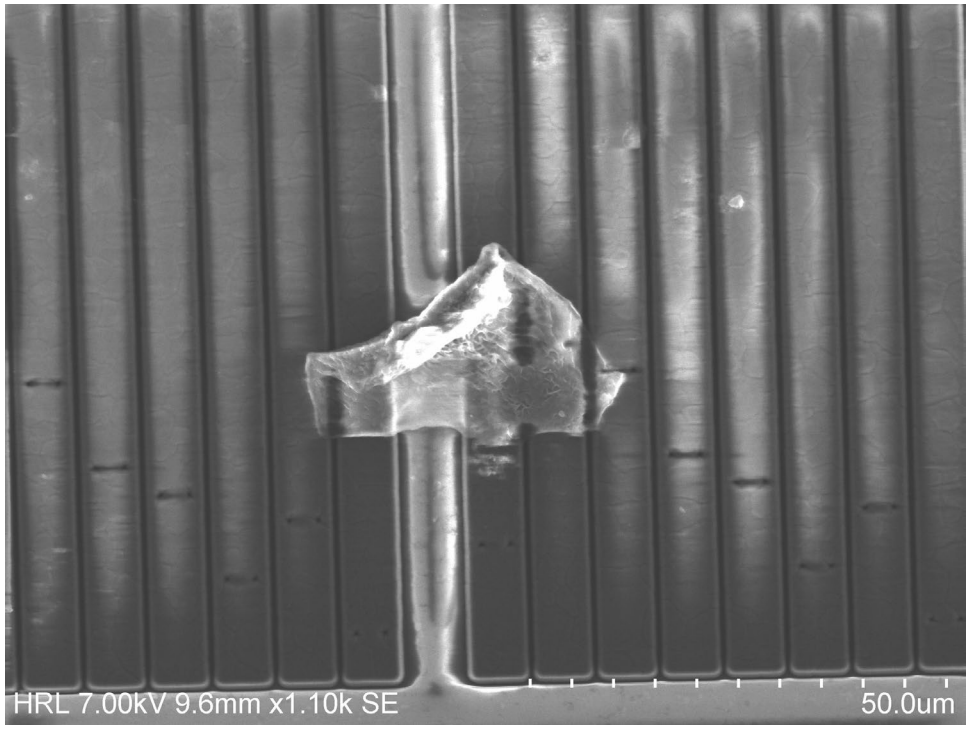
FA Lab Setup

- **Energy Dispersive Spectroscopy (EDS)**
- Elemental analysis is a **significant** part of FA.
- Material compositions, contamination, corrosion byproduct
- It's a must have in the FA lab

- Recommendations for EDS are similar to SEM imaging.
- Signal strength, beam voltage, important parameters to be aware of.
  - Signal strength results from a combination of beam voltage, beam alignment, probe current, aperture selection, sample characteristics/preparation and working distance. These can be machine specific!
  - Signal strength directly correlates to "counts" in EDS, which is the rate of data acquisition when acquiring a spectrum.
  - Too much signal can cause inaccurate results, as more material is being analyzed than intended. Most equipment has a sweet spot.
- Beam voltage will determine "how deep" you are collecting data.
  - In bulk materials, depth isn't a huge concern, but if analyzing surface contamination/residues it's an important consideration

FA Lab Setup

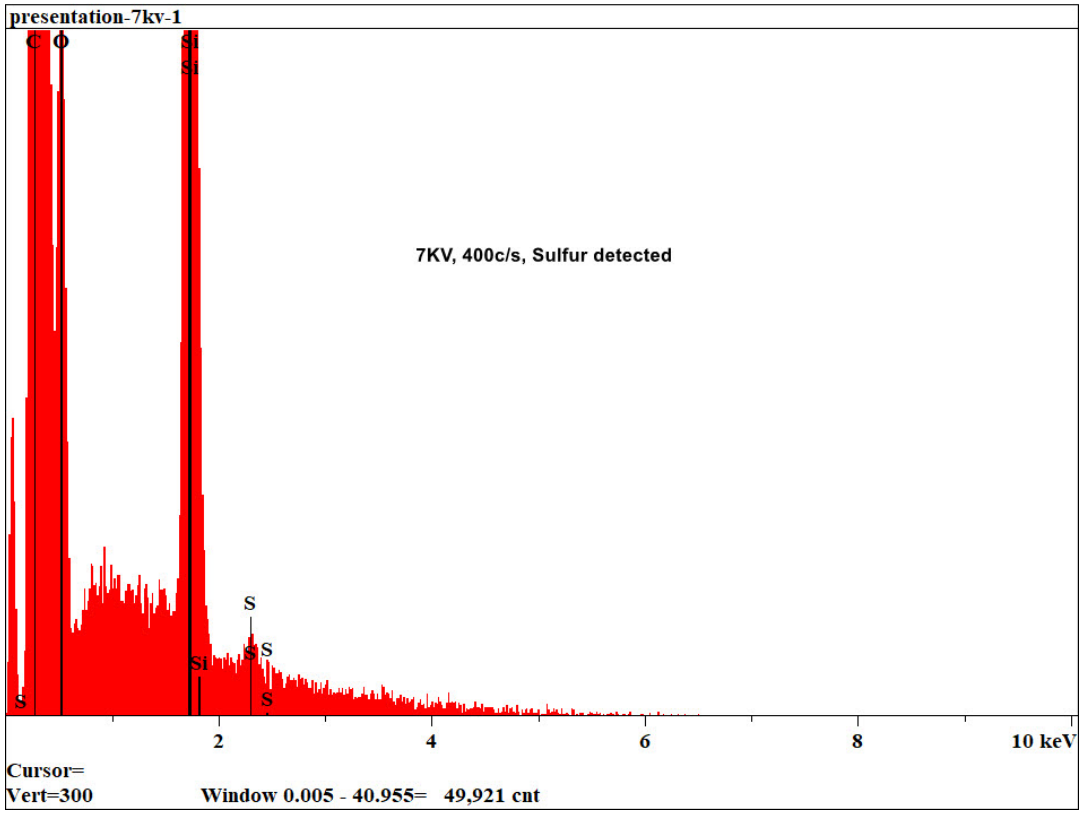
- **Energy Dispersive Spectroscopy (EDS)**



SEM image of a particle on the surface of a memory chip.

FA Lab Setup

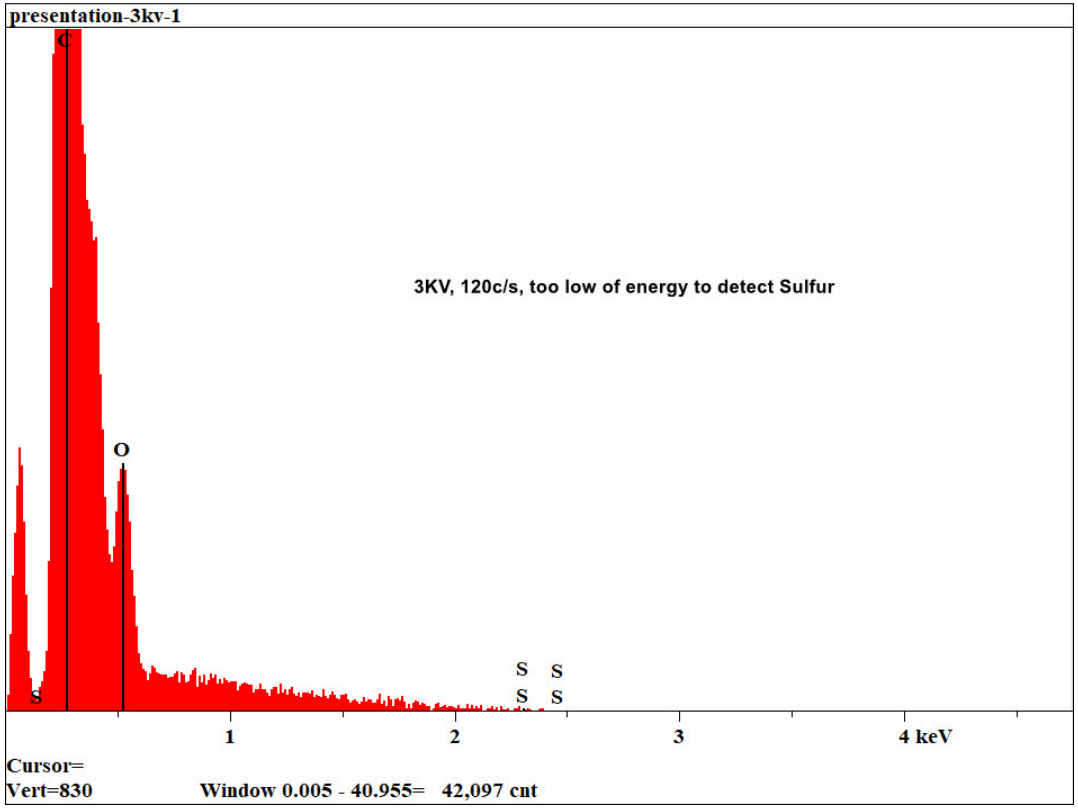
- **Energy Dispersive Spectroscopy (EDS)**



7KV, good beam voltage for identifying contaminants like Sulfur (S) and Chlorine (Cl), 2 minutes to acquire 50,000 samples.

FA Lab Setup

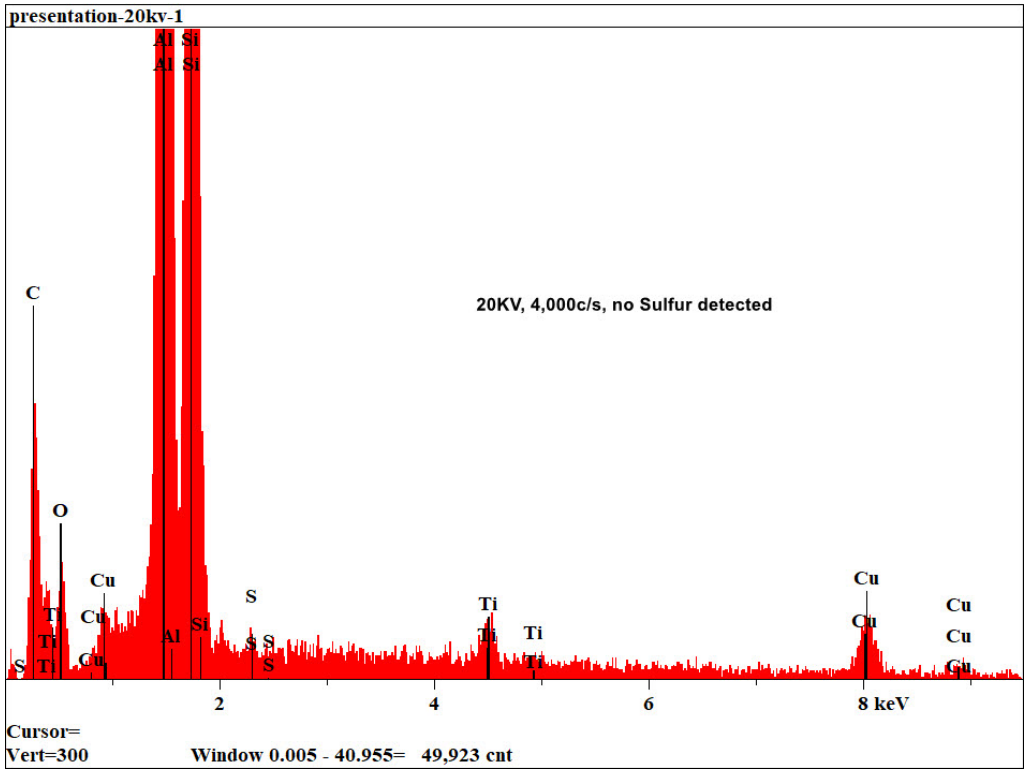
- **Energy Dispersive Spectroscopy (EDS)**



3KV, too low of voltage for detecting things at higher excitation voltages. 7 minutes to acquire 50,000 samples.

FA Lab Setup

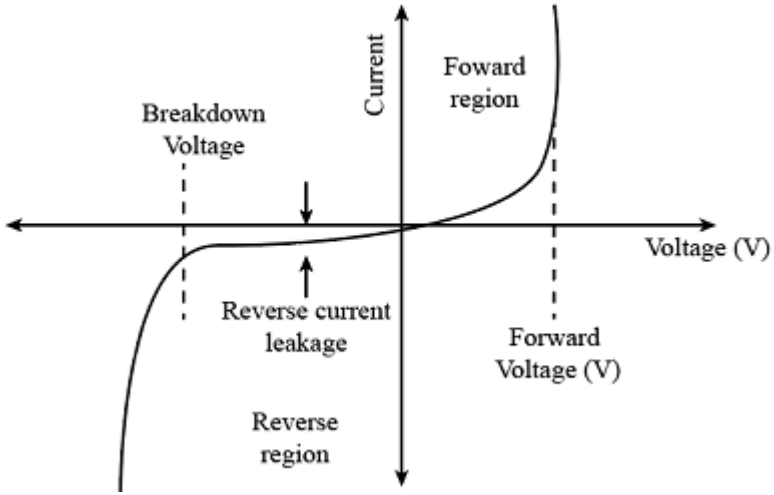
- **Energy Dispersive Spectroscopy (EDS)**



20KV, too high of penetration. “Blasts” through the particle and Sulfur doesn’t show up, but we can see deep into the die metallization, aluminum, on titanium-tungsten, on copper.

FA Lab Setup

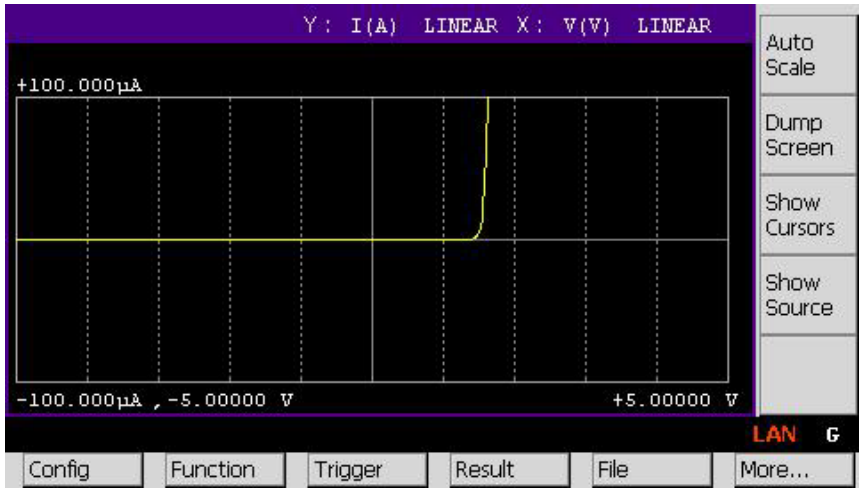
- **Electrical test equipment**
  - This can vary depending on your product. If you are testing mostly RF components, your test lab will look a bit different than a lab that handles legacy products, older tech.
  - **Every lab should have an old, analog curve tracer**. My experience is with a Tektronix 576, introduced in 1969, produced until 1990!

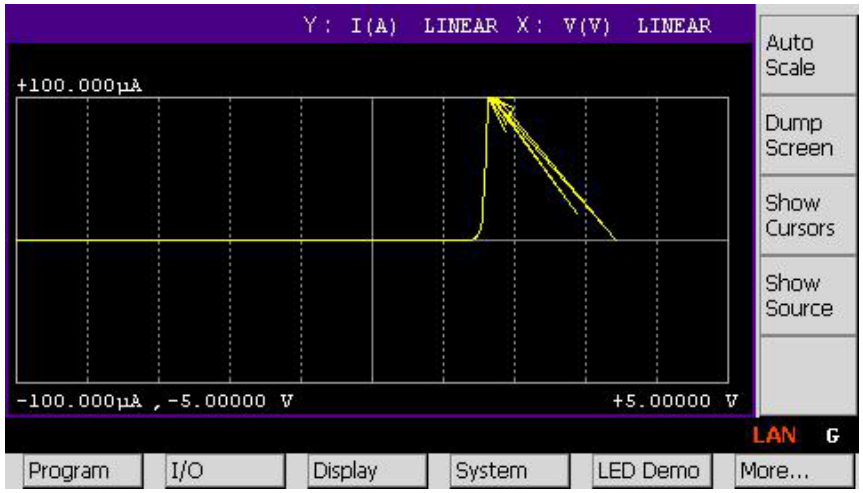


FA Lab Setup

- **Tektronix 576 Curve Tracer**
  - High power. Up to 1600V, or up to 20A, steady state or with pulsing.
  - Allows manual control of limits and safe power application to components.
  - Remember, you cannot test a failed device like you would a non-failed device. You can't test a degraded diode at the manufacturer's specified 10A forward current. You need control.
  - 60hz display gives you a more "real time" reading which is valuable when testing over temperature, or testing other intermittent conditions. Digital options, in my experience, are not as fast.
  - Cheap - $500 on ebay, or $3k-$4k refurbished.

FA Lab Setup



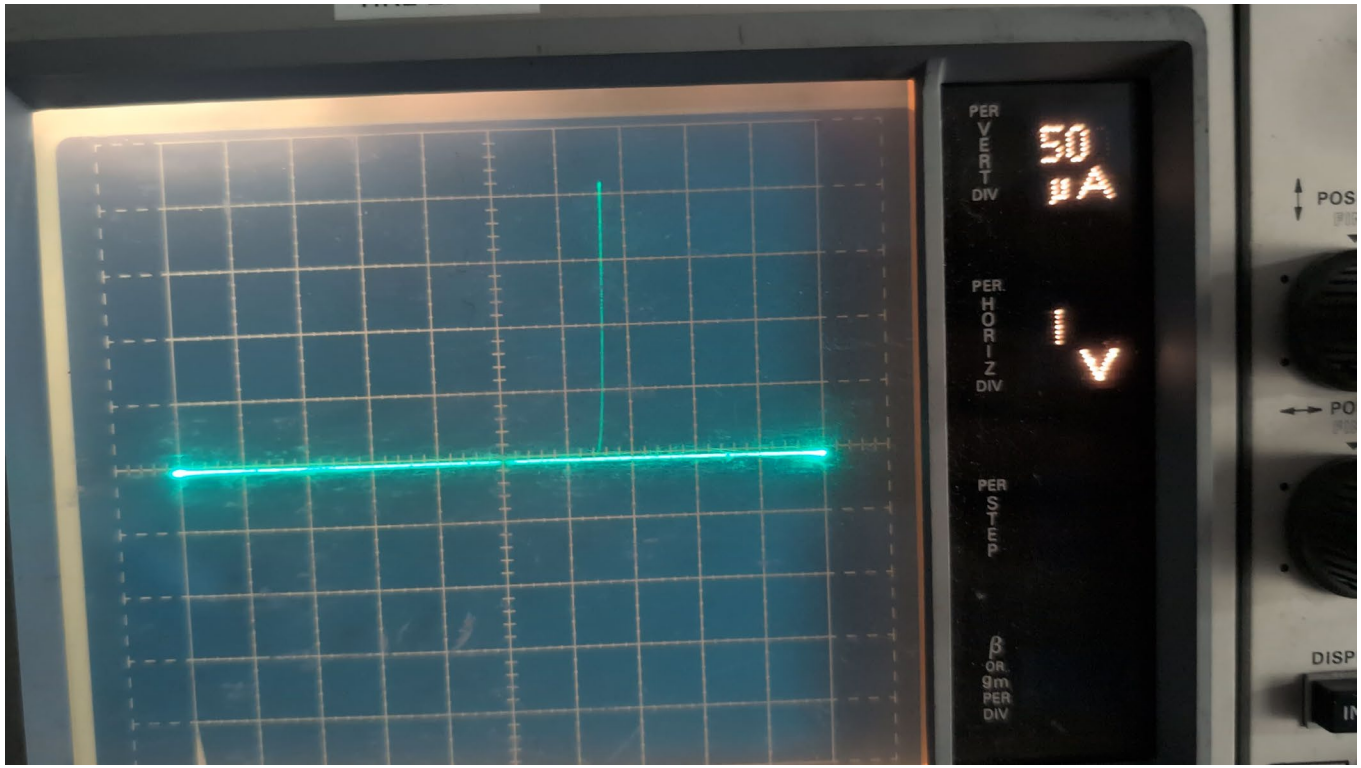


These images show two different I/V curves with a digital sweep of an LED with an intermittent bond wire.

Note that depending on the state of the LED it can appear good (top), while the bottom image shows an intermittent connection.

If you only test once with this equipment, you might miss it.

FA Lab Setup



Video of a 576 curve tracer of the same LED showing the intermittency in “real-time” (60hz).

FA Lab Setup

- **Electrical test equipment**
  - Curve tracer downsides: OLD. Very hard and expensive to keep calibrated, hard to repair and keep running. Best used as a "reference only" instrument, requiring validation with calibrated equipment
  - Alternatives: There are newer digital curve trace systems over a very wide range of prices and capabilities, from a couple hundred dollars up to nearly $100k.
    - Most of these have power limitations when compared to the older curve tracer.
    - Less intuitive
    - We had to purchase several 210V, 3A source/measure units (SMUs) and a 1000V unit to satisfy our testing needs. This also allows networking the equipment to perform more complex testing.
    - This equipment has many perks as well, and compliments the old curve tracer perfectly.

FA Lab Setup

Image from Keysight

Image from Tektronix

- **Electrical test equipment**
  - Other testing needs include DMMs, benchtop power supplies, LCR meters, Insulation Resistance/DWV/Hipot testers, oscilloscopes – standard electronics test equipment

FA Lab Setup

- **Particle Impact Noise Detection (PIND)**
- Similar to hermetic seal testing, this is recommended on most samples with a cavity, but only when the act of vibrating the component will not result in information loss (fractured wires after vibration can lose all distinguishing markings on fracture face, for example).
- Fast and east method to test for any particles within the cavity, such as welding material, fractured bond wires, FOD. Detected materials can be extracted with "particle capture" method.
- This can be subbed out to other labs if you lack the availability.

FA Lab Setup

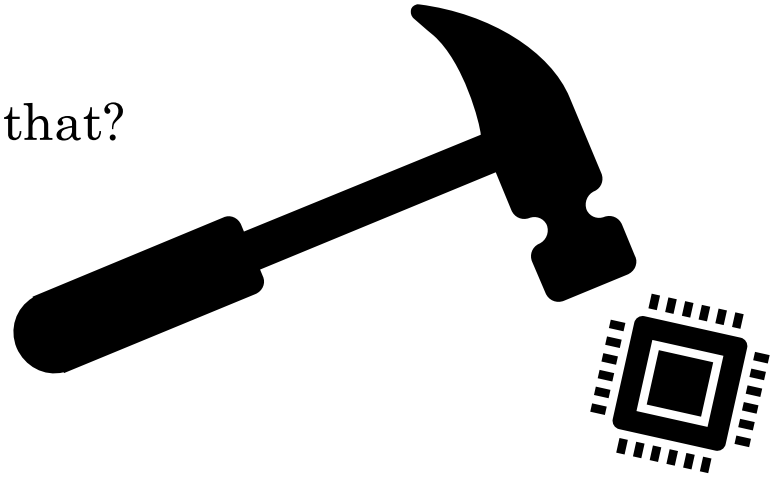
- **Hermetic Seal Testing**
- Hermetic seal integrity can be an important part of failure analysis, and in most instances it is recommended to test the seal regardless of the failure mode.
- There are several laboratories that can perform this testing and it is recommended to sub this work out.
- Drawbacks: Can be slow, faster methods such as Kr-85 require radioactive materials, gross leak failure can result in fluorocarbon ingress (check)

FA Lab Setup

- **Internal Gas Analysis (IGA)/Residual Gas Analysis (RGA)**
- This testing requires milling a small hole in the component packaging, typically the lid.
- Elemental analysis of the contents of the cavity is performed.
- This can tell you if the cavity contained high levels of oxygen or moisture, or other gasses, and is useful when any sort of contamination or outgassing is suspected.
- **This is a destructive test** and can result in severe damage to the internal components of the device.

FA Lab Setup

- **Destructive analysis**
  - If the previous testing was equivalent to crime scene investigation, this part is like the autopsy.
  - Depending on the findings of the non-destructive analysis, you will likely need to proceed to one or more of the following:
  - Disassembly
  - Delid
  - Decapsulation
  - Cross Section
- What do we need for that?



FA Lab Setup

- Disassembly
  - Basic tool set
  - Cutting tools such as Dremel or wafering saw
  - Hot air guns
  - Solder rework stations

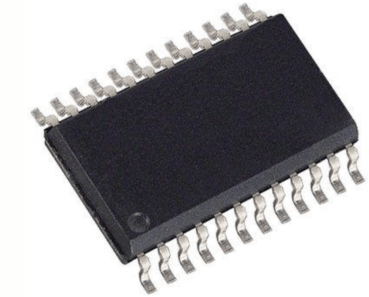
- Delid
  - Grinding/polishing tools – preferably metallurgical cross sectioning wheels
  - Razor blade/ophthalmic scalpels
  - Knifed-edged vise

FA Lab Setup

- Decapsulation
- What is it?
  - Removing the packaging/potting material to allow inspection of the internal structures; wires, die, capacitor, etc.
- Mechanical decapsulation
    - Not recommended but can be necessary in cases where contamination is suspected
    - Heating often helps soften the potting materials or adhesives
    - Some labs will simply place the device in an oven and heat until potting ashes away or can be picked away
    - Will induce substantial damage to interconnects, e.g. wires and attach materials and will likely damage the semiconductor itself

FA Lab Setup

- Decapsulation
- Chemical decapsulation and chemical delayering/deprocessing
  - Requires extremely harsh chemicals
    - Can be challenging to acquire and use depending on company and location
  - Relatively low cost
  - HNO_3, H_2SO_4, HF, HCl, H_2O_2, NMP, CU7, SU100 acids/solvents cover the majority of decapsulation/deprocessing chemical need
  - Requires a fume hood and appropriate PPE, hot plate, beakers, petri dishes, watch glasses, good tweezers
  - Decapsulation can be subbed out, but there is risk of residues continuing to react after the decapsulation process which may corrode metals with time.



FA Lab Setup

- Decapsulation
  - Laser Ablation
    - Pre-cavitation of components is recommended prior to chemical decapsulation.
    - Costly investment at first, but a very valuable piece of equipment.
    - Repeatable, fast, can create “recipes” for components
    - RISKY IF NOT CAREFUL. “One more pass” is your cue to stop!
  - Pre-cavitation can also be achieved using a Dremel tool or milling station, though it has it’s own risks and can be less repeatable.
  - Useful for uncovering test points to isolate failures in potted components
  - Laser ablation can be subbed out.

FA Lab Setup

- Laser Ablation

FA Lab Setup

- Cross Section
- What is it? – Lapping/polishing into a component to allow a cross-section examination of various materials and interfaces.
  - Die attach, wire fractures, die metallization defects/construction, packaging damage
- What do you need?
  - A metallurgical polishing wheel with various coarseness of lapping papers
  - Polishing compounds
  - Metallurgical microscope (metallograph) – preferred, not needed
  - Experience – There can be a lot of induced damage/artifacts during this process, and it requires experience to know what is real
- Can be subbed out

FA Lab Setup

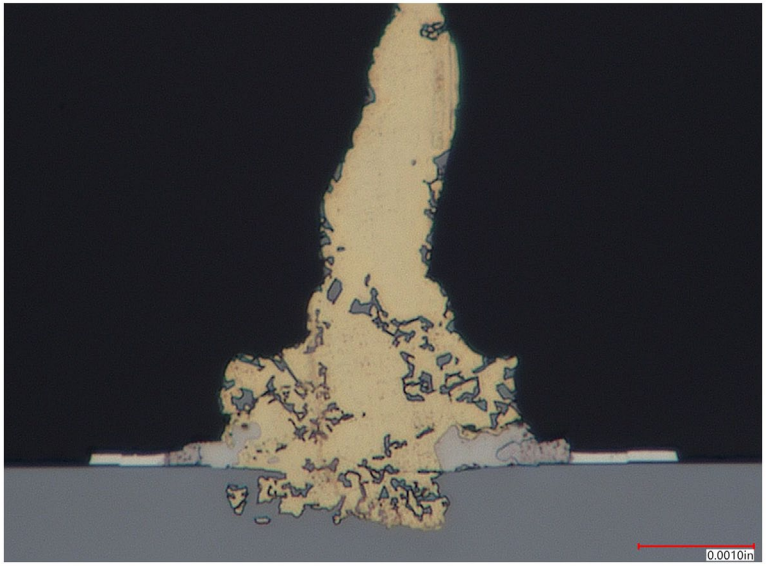
- Cross Section

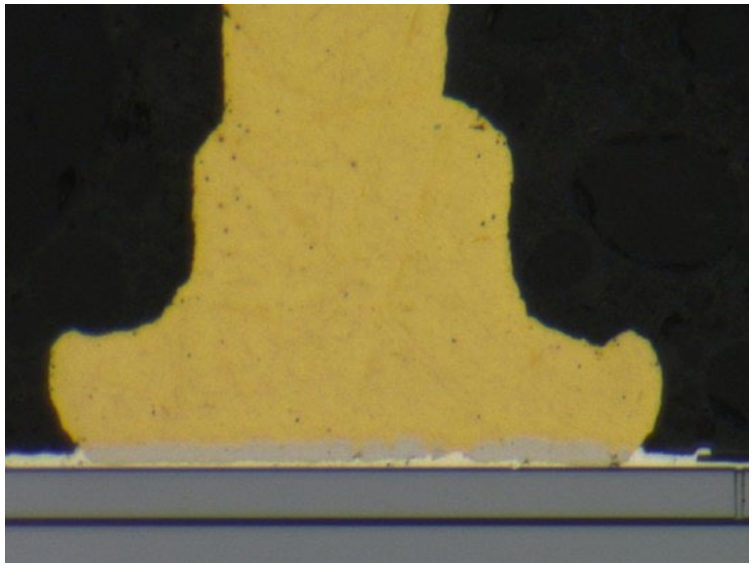
Image from Allied.com

Image from Buehler.com

FA Lab Setup

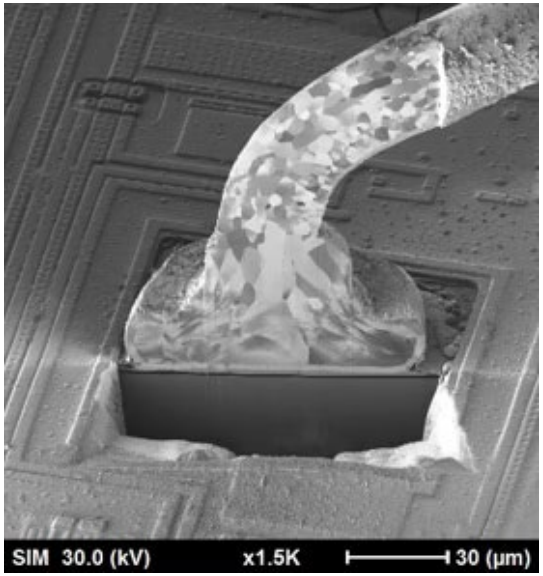
- Cross Section

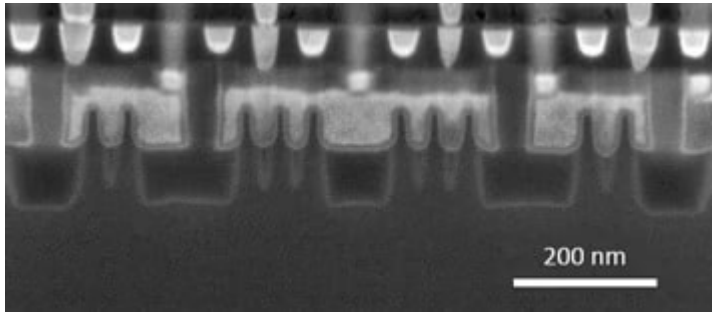




FA Lab Setup

- Focused Ion Beam (FIB)
  - High precision
  - High cost
  - Small area of cross section, useful for examining extremely small features that would otherwise be difficult to cross section by hand

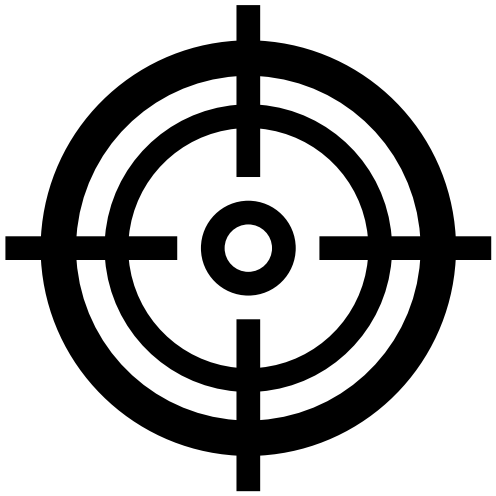




Images from Hitachi.com

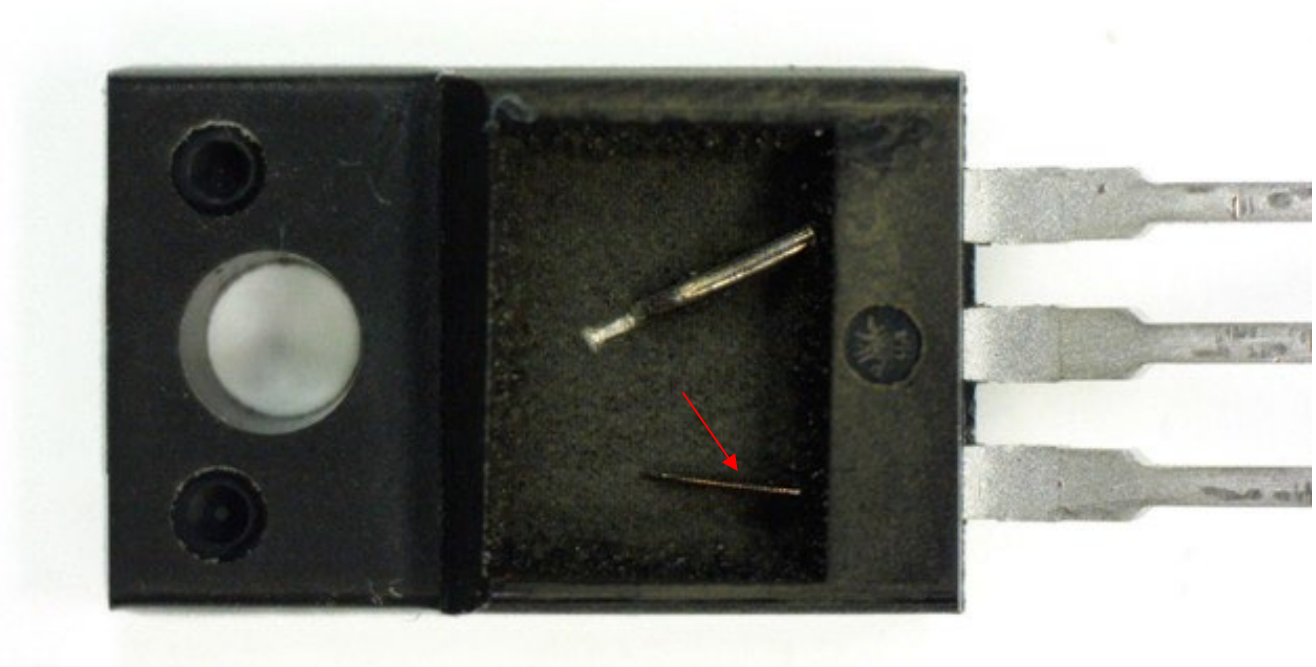
FA Lab Setup

- **<u>Failure Localization and Isolation</u>**
- What do you do when you can't find anything wrong after decapsulation?
- It depends. What was the failure?
- For open circuits, failure isolation must be considered throughout the process.
- For example, if an open circuit is present in a microcircuit, it may be advisable to uncover the suspect bond wire with laser ablation to allow probing the wire directly, isolating the failure to the lead frame or the die bond.



FA Lab Setup

- **Failure Localization and Isolation**



The gate of this FET tested as an open circuit, Scanning Acoustic Microscopy (SAM) found delamination at the gate lead frame in the bonded area. We can use laser ablation to access the gate wire, allowing us to probe the wire to the lead frame. This will completely change our analysis path moving forward.

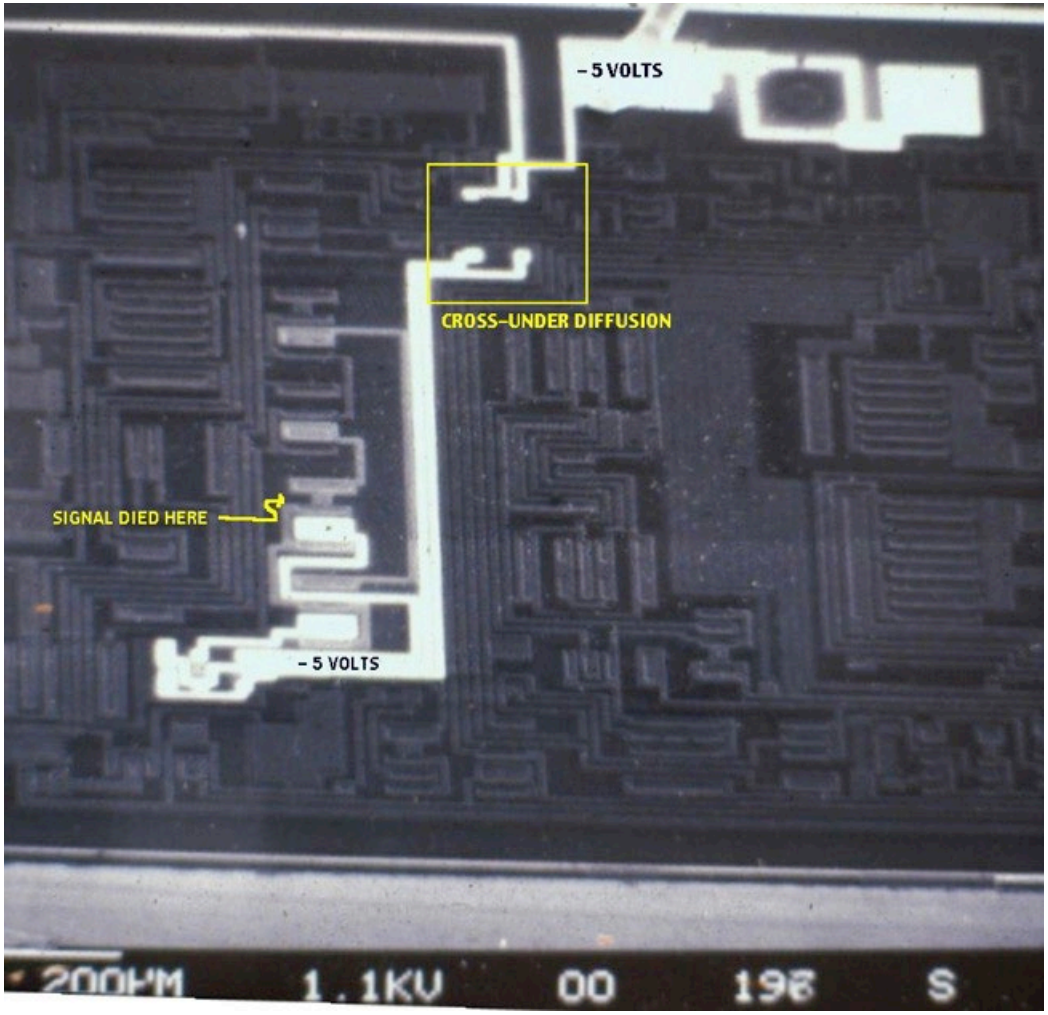
FA Lab Setup

- **Failure Localization and Isolation**
- Open circuits in die metallization can be isolated using a SEM technique called “voltage contrast”
  - This technique requires electrical access to the DUT while in the SEM chamber, and connectors in the ports of the SEM. This can be challenging depending on the SEM and if the modification is allowable.
- Other methods include IR and Photoemission microscopy and comparison to a control sample. Active transistor structures will emit heat/photons, and if a transistor is not active it may indicate the open circuit is in the related circuitry.

Voltage Contrast

Notice the "LOW" 1.1 kV beam voltage needed to achieve voltage contrast on this sample - it has also been tilted

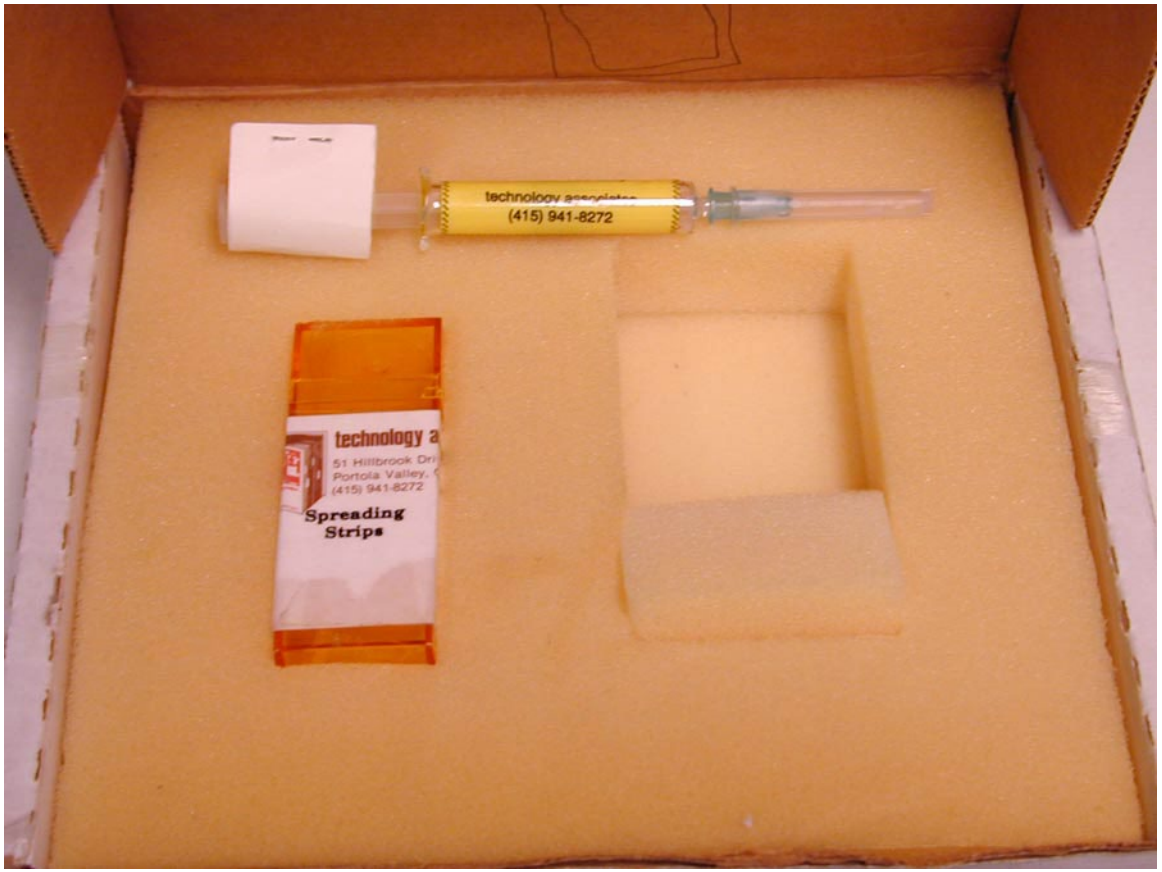
.



FA Lab Setup

- **Failure Localization and Isolation**
- What about shorted or resistive/degraded circuits?
- The least expensive and easiest method is liquid crystal hot spot detection.
- It may be difficult to find the liquid crystal.

LIQUID CRYSTAL HOT SPOT DETECTION



LIQUID CRYSTAL HOT SPOT DETECTION

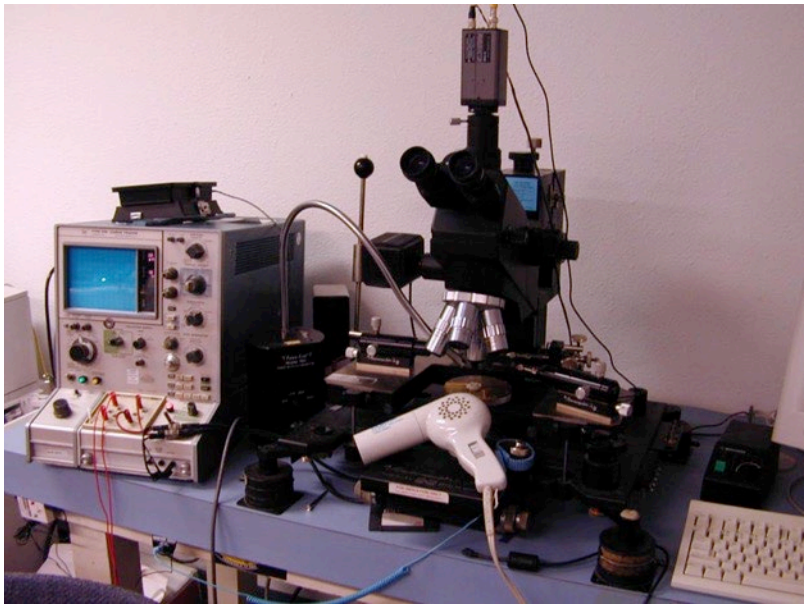
- Inexpensive - approximately $100 for a kit containing 2 syringes. One of the most cost effective techniques a failure analyst can use.
- Fast - rapidly locates short circuit/leakage sites.
- Simple - requires little practice to become proficient.
- Non-Destructive - allows location of leakage sites without removing metallization or glassivation.
- Minimal support equipment needed - a probe station with a polarizing microscope, a curve tracer and a heat source. Most of which are already present in a failure analysis lab.

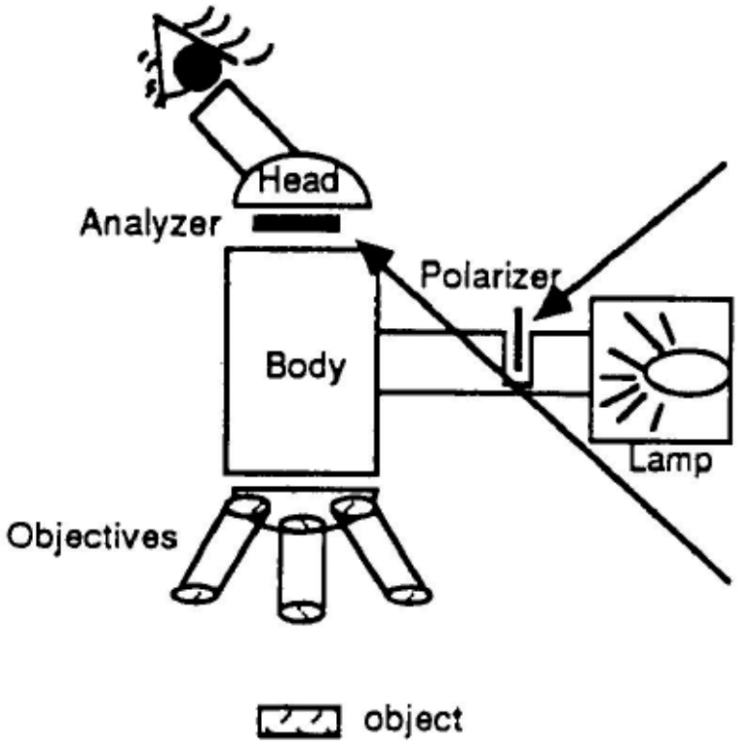
SUPPORT EQUIPMENT (recommended by manufacturer)

- Metallurgical microscope with polarizing filters and long working distance objectives.
- Collimated IR lamp with a continuously variable power source or,
- Precisely controlled socket heater
- Curve tracer (Tektronix 576 or 577)
- Power switching module
- Stereo microscope
- Ultrasonic cleaner

SUPPORT EQUIPMENT (used by Hi-Rel Labs)

- Probe Station with metallurgical microscope with polarizing filters.
- Curve tracer (Tektronix 576)
- Hair dryer - 1500 watt





One polarizing filter is inserted into the filter holder slide in front of the illuminator. The other filter should be inserted in the viewing path just above the microscope body. Remove the head, place the filter above the lens and rotate the filter for the darkest image. The first filter can then be rotated to adjust for the best imaging of the liquid crystal.

LIQUID CRYSTAL

The chemistry of liquid crystal is complex, however, an in-depth understanding of the chemical properties is not required to effectively use them.

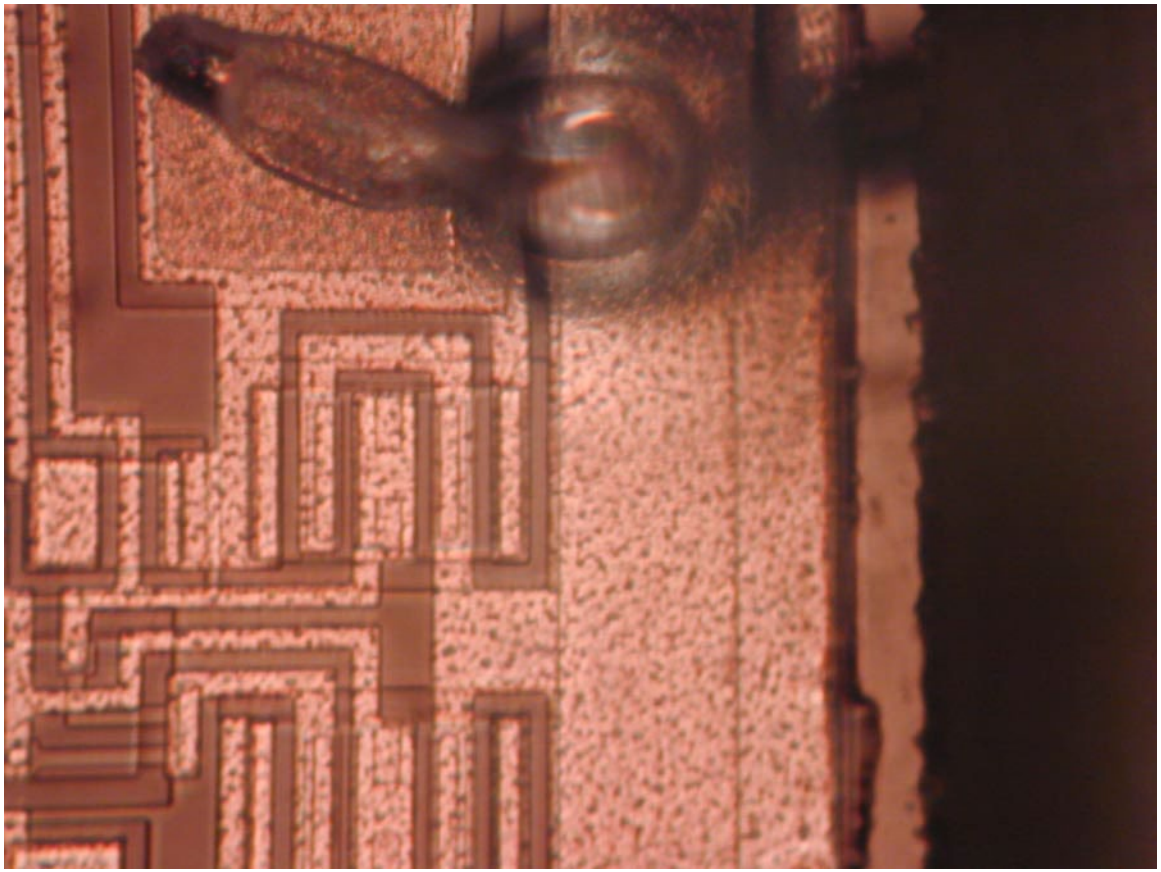
Most materials have one temperature which separates the liquid and solid states. Liquid crystal materials have one or more intermediate phases between liquid and crystalline states.

PHASES

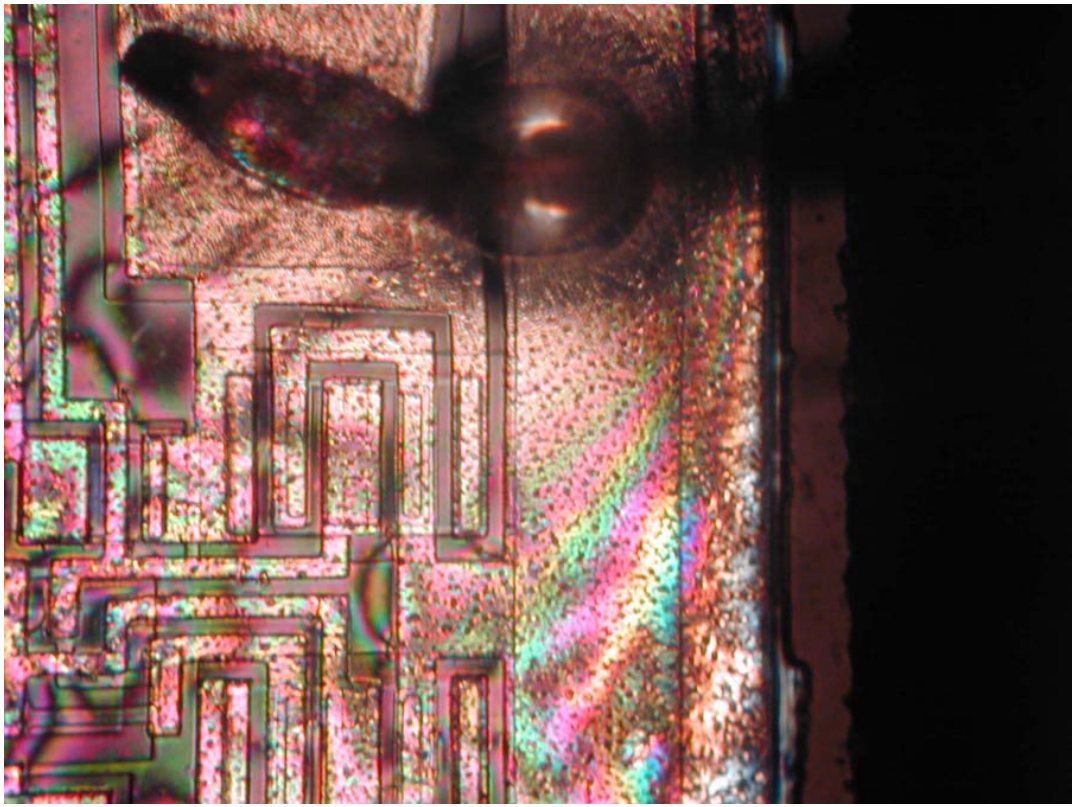
Isotropic phase	(liquid)
Nematic phase	(liquid crystal
Smectic phase	phases)
Crystalline phase	(solid)

The region near the isotropic to nematic transition is used for hot spot detection. The temperature at which the crystal changes between these states is referred to as the clearing point. For type A liquid crystal this temperature is 29 degrees C. Type B has a clearing point of 83.5 degrees and type C is 107 degrees.

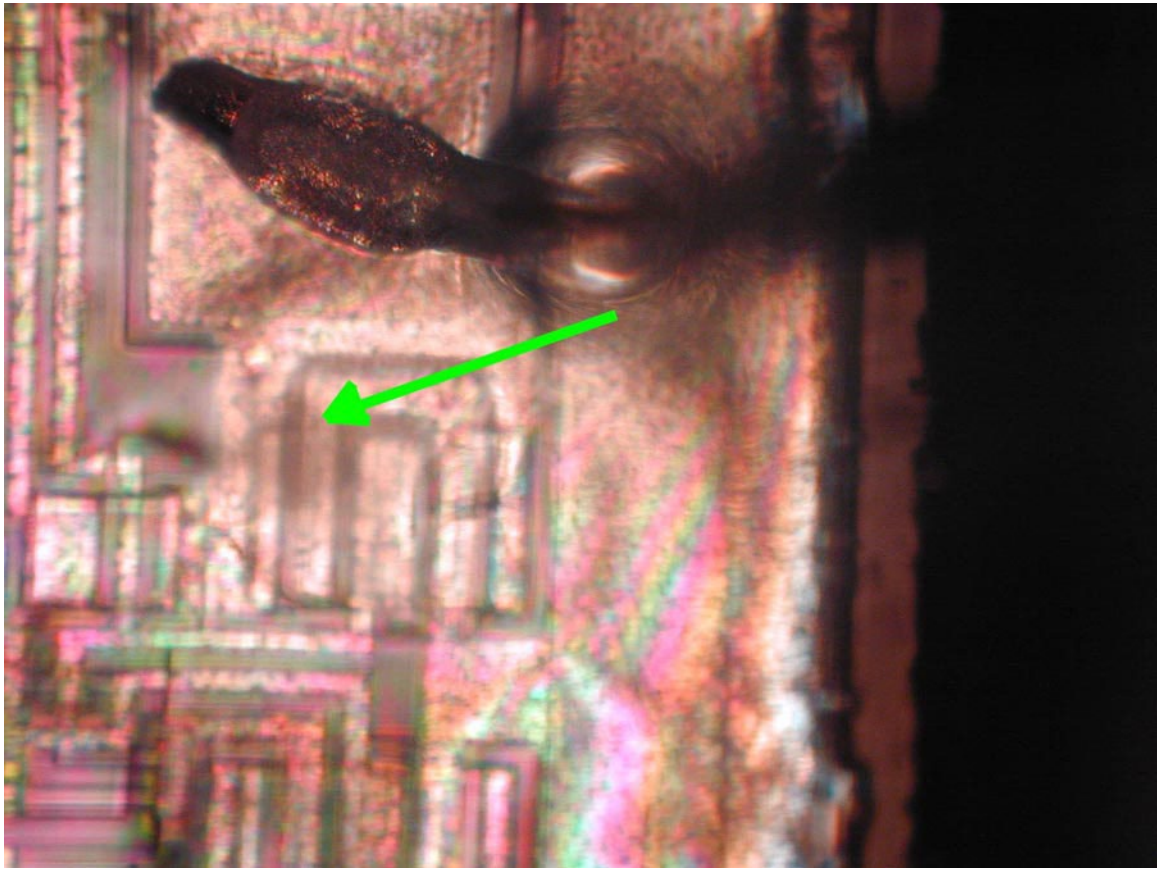
In the isotropic phase (above the clearing point) the long, threadlike liquid crystal molecules are randomly oriented. The film appears clear when viewed through bright field illumination. With polarizing filters the film appears dark.



In the nematic phase the crystal molecules assume an alignment parallel to each other. If the liquid crystal film is of the proper thickness for hot spot detection, the surface will have a distinctly mottled, rainbow colored appearance when viewed through polarized filters. The liquid crystal can also be affected by electrical fields in this phase as well as changes in temperature.



Clearing point - This is the transition between the two phases. For type A it is at 29 degrees C and is very abrupt. This temperature is optimal for most applications because it is near room temperature. Thus very little heat is required to increase the temperature of the small volume of crystal from one phase to the other. The arrow indicates the leakage site.



USING LIQUID CRYSTAL

- SAMPLE PREPARATION

  Have an appropriate sample - Liquid crystal utilizes the heating effect generated by current passing through a leakage site and must be viewed under a metallurgical microscope. (bright field)

  The device to be tested must be delidded/depotted and clean to allow the crystal to wet to the surface.

  Provisions for electrical connections to the affected pins.

USING LIQUID CRYSTAL

- APPLYING THE CRYSTAL

  Depending on the size of the area to be covered the crystal can be applied directly from the syringe or transferred to the die using the "spreading strips". If a large area is to be covered, depress the plunger on the syringe until a drop is formed at the tip. Then carefully allow the drop to contact the die, NOT THE TIP OF THE NEEDLE. The spreading strips can then be used to distribute the crystal evenly and absorb any excess. If only a small amount is needed, a drop can be placed on the spreading strip then smeared directly on the die surface. The proper thickness should exhibit a rainbow colored, mottled appearance when viewed under the polarized microscope.

APPLYING POWER

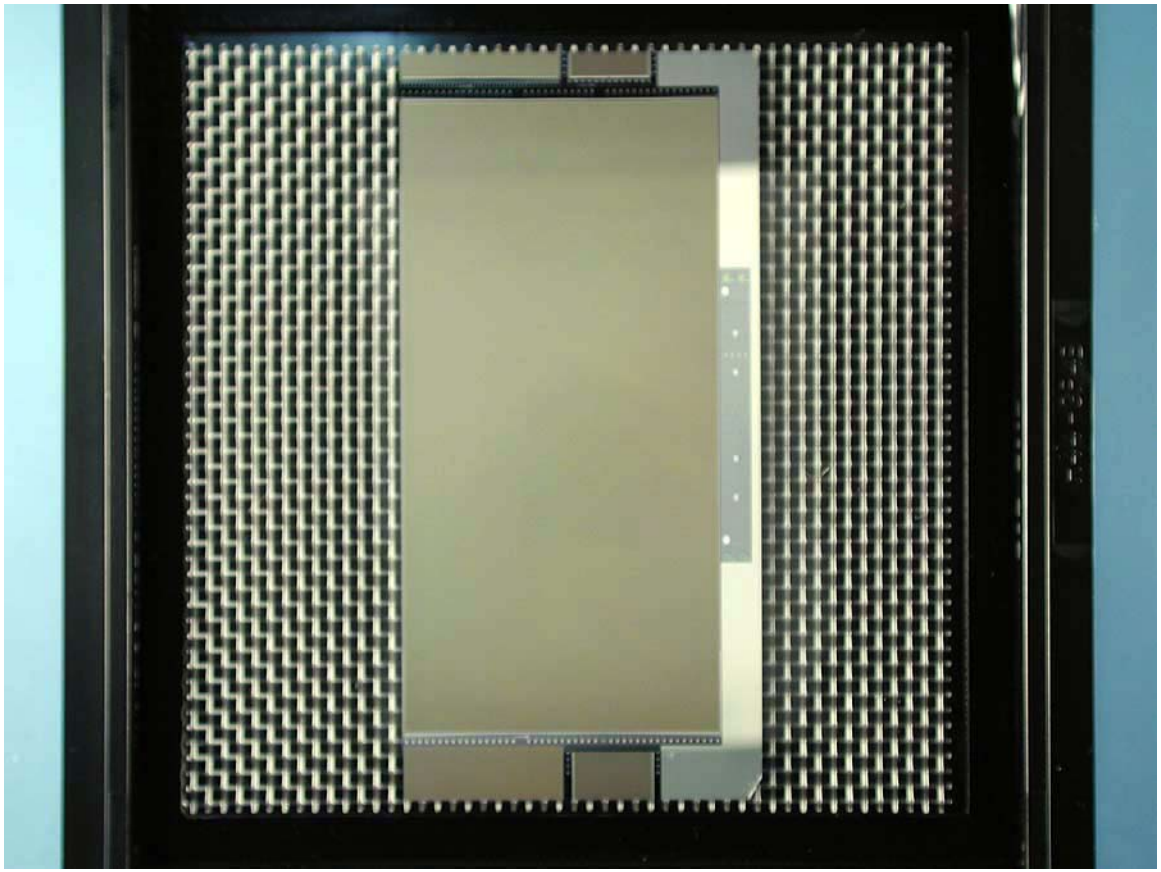
Power can be applied to the affected pins using any power supply. The curve tracer, such as the Tektronix 576, is the best choice due to its flexibility. Connections can be made using probes or the device leads depending on the sample. If possible probe the device away from the suspect area.

It is generally best to use the curve tracer in the DC mode in the polarity most affected by the leakage current.

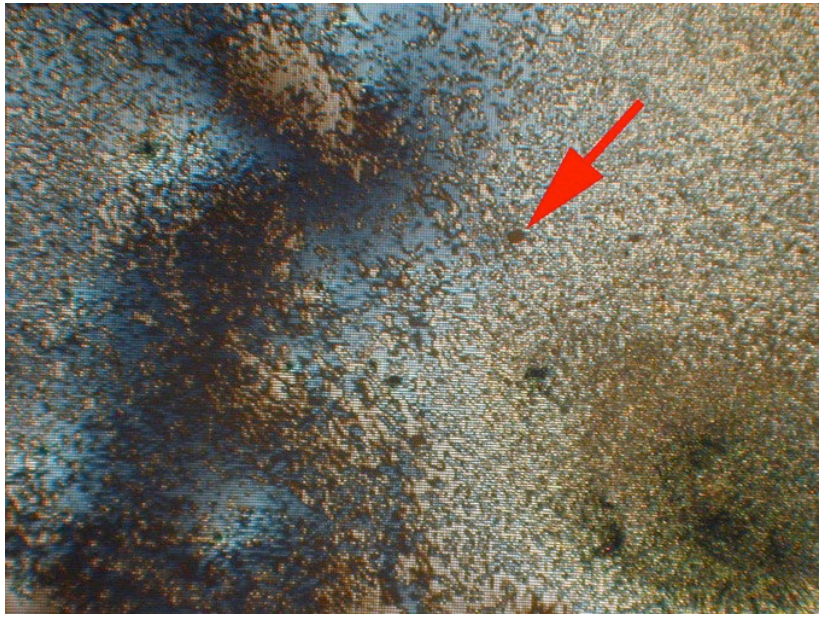
The device should then be heated to near the clearing point. This reduces the amount of power required to detect the leakage site. At this point power can be applied and gradually increased until a change in the appearance of the crystal is noted. Switching or pulsing the applied power will aid in the location of the leakage site.

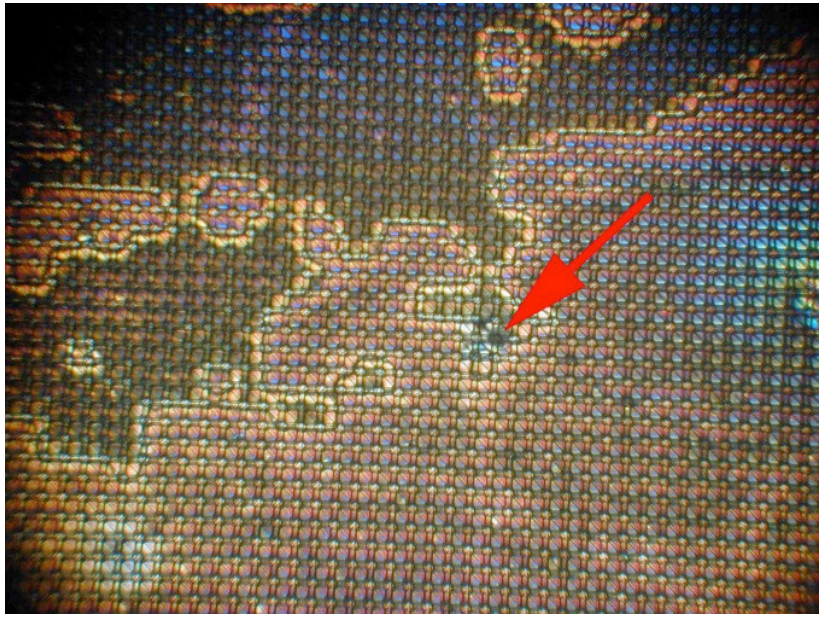
EXAMPLE 1

LARGE CCD DEVICE WITH A SHORT CIRCUIT AND NO VISIBLE DAMAGE

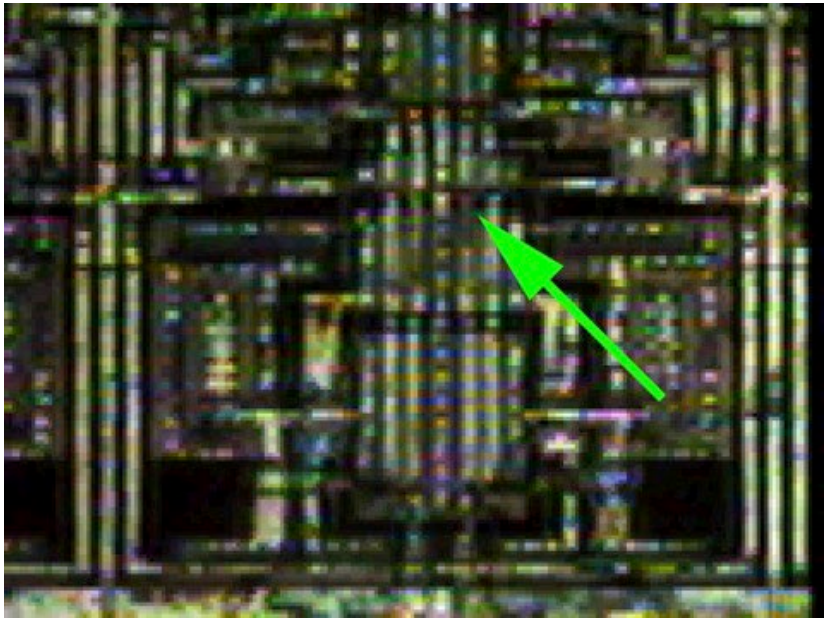


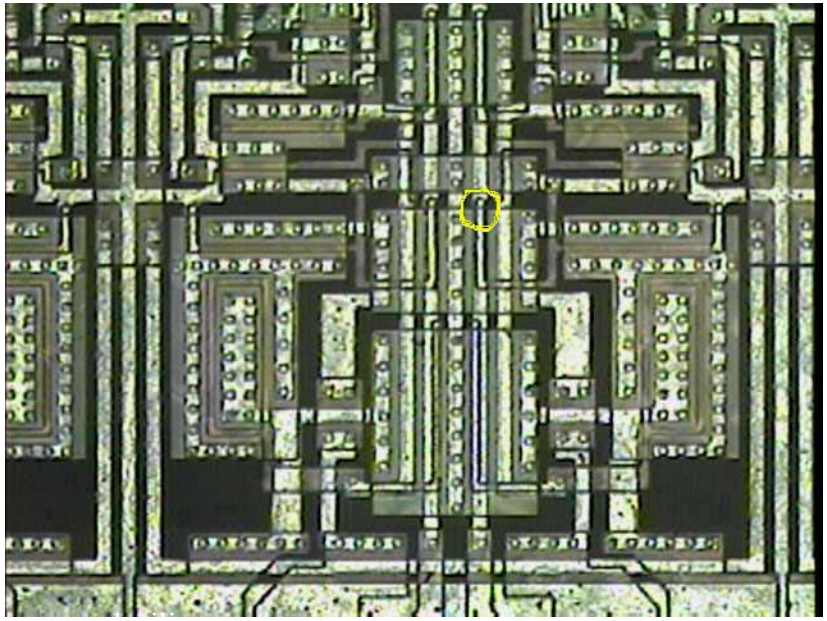
LIQUID CRYSTAL IS USED TO LOCATE THE LEAKAGE SITE.





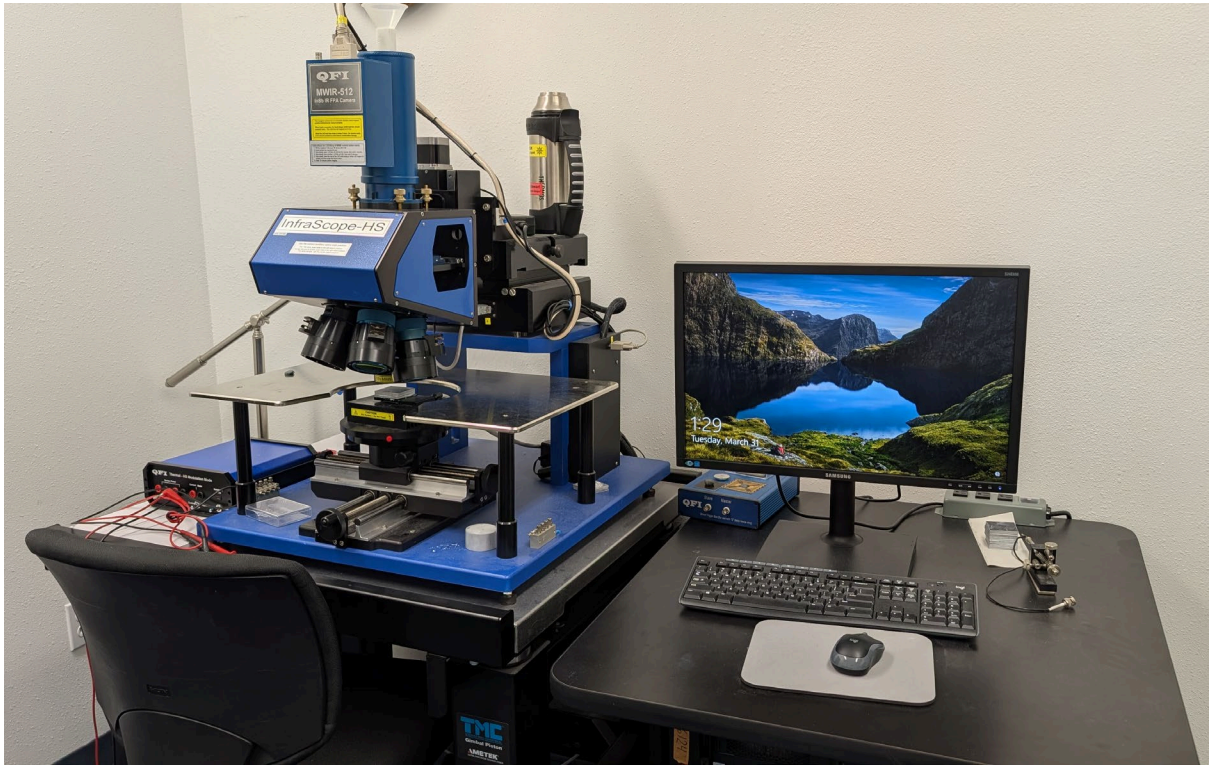
EXAMPLE 2
Liquid crystal locates a leakage site on a silicon on sapphire die.
Subsequent cross-sectioning find a defect in the oxide over the step.





FA Lab Setup

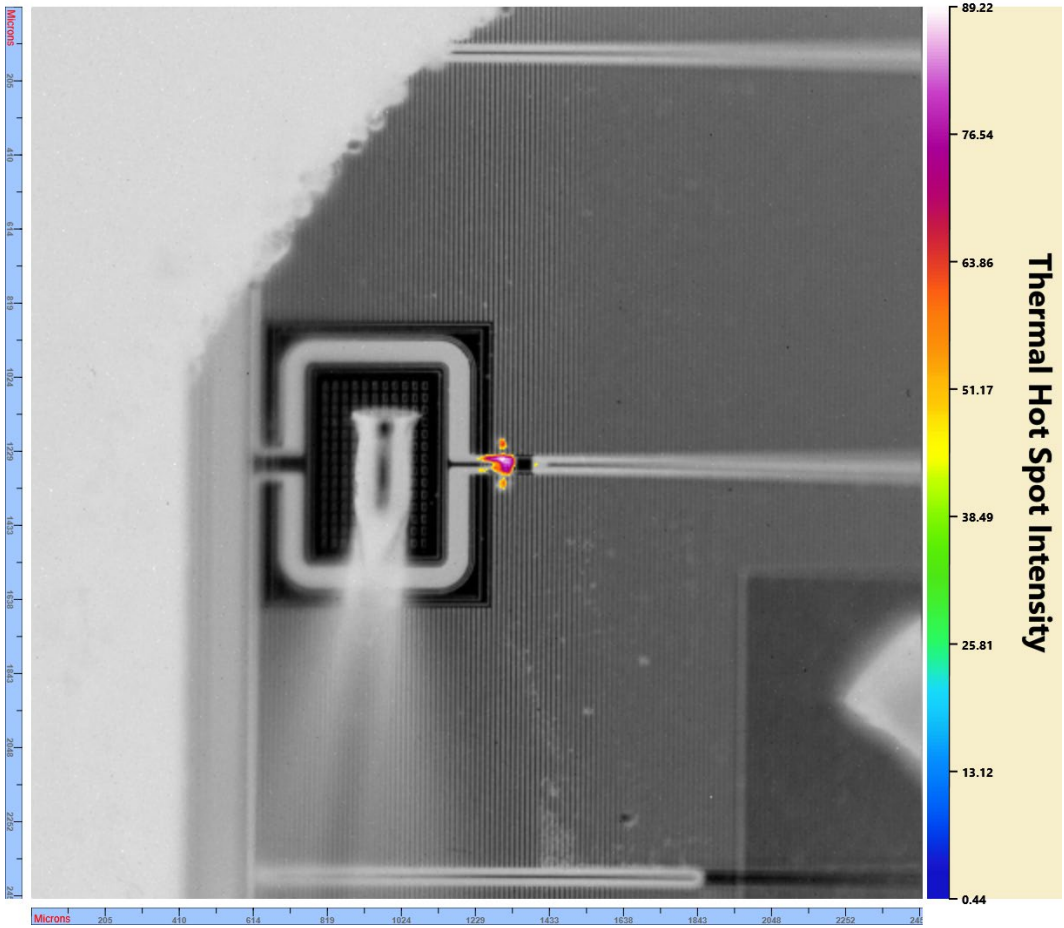
- Liquid crystal hot spot detection alternatives/upgrades:
- **Infrared Hot Spot Detection**



FA Lab Setup

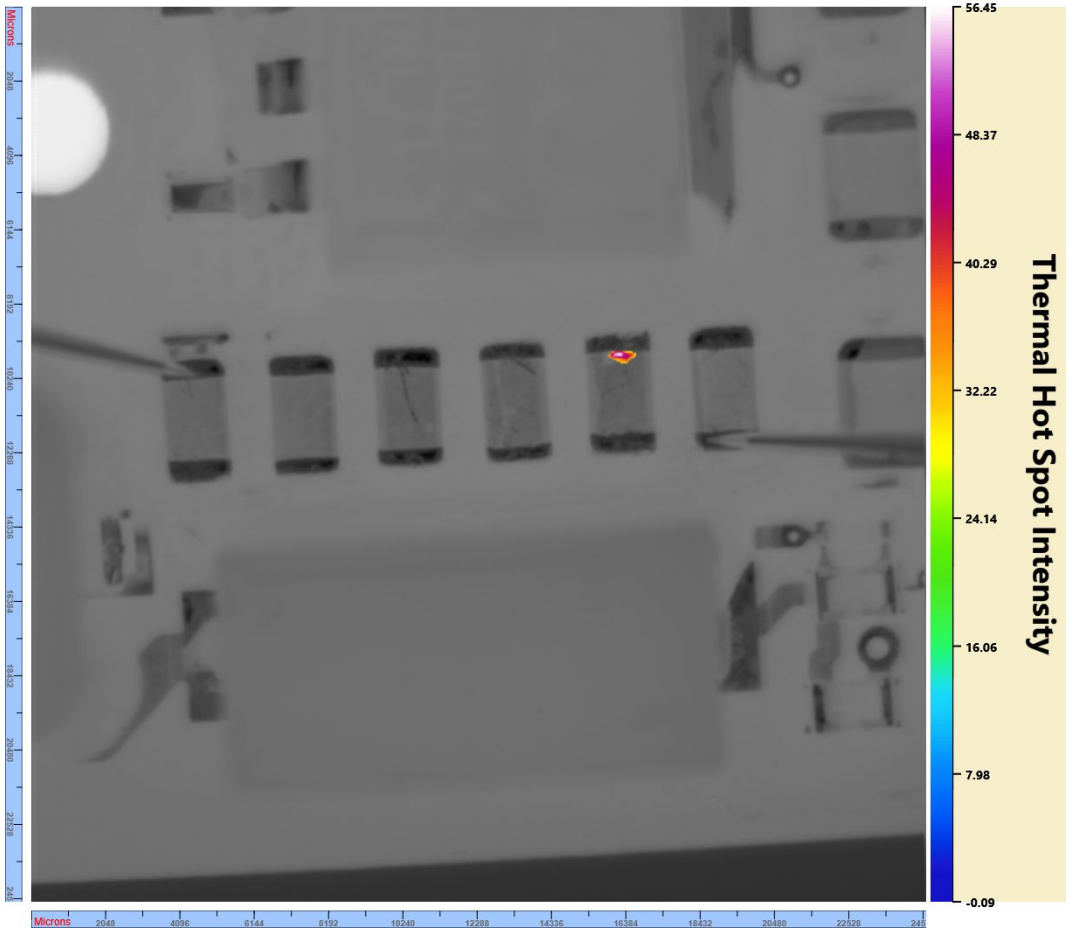
- **Infrared Hot Spot Detection**
- How is that better than liquid crystal hot spot detection?
- Much more sensitive. Liquid crystal requires ~10mW of dissipated power while IR requires ~1mW (rough estimates)
- Lock-in thermography modulates power applied to the fault, providing good SNR and detectability
- Useful in MORE instances. Board level, cross section, uneven surfaces like transformers, etc.
- Challenge: Heat dissipating materials like thick die metallization can make it difficult to pinpoint the failure site.

FA Lab Setup



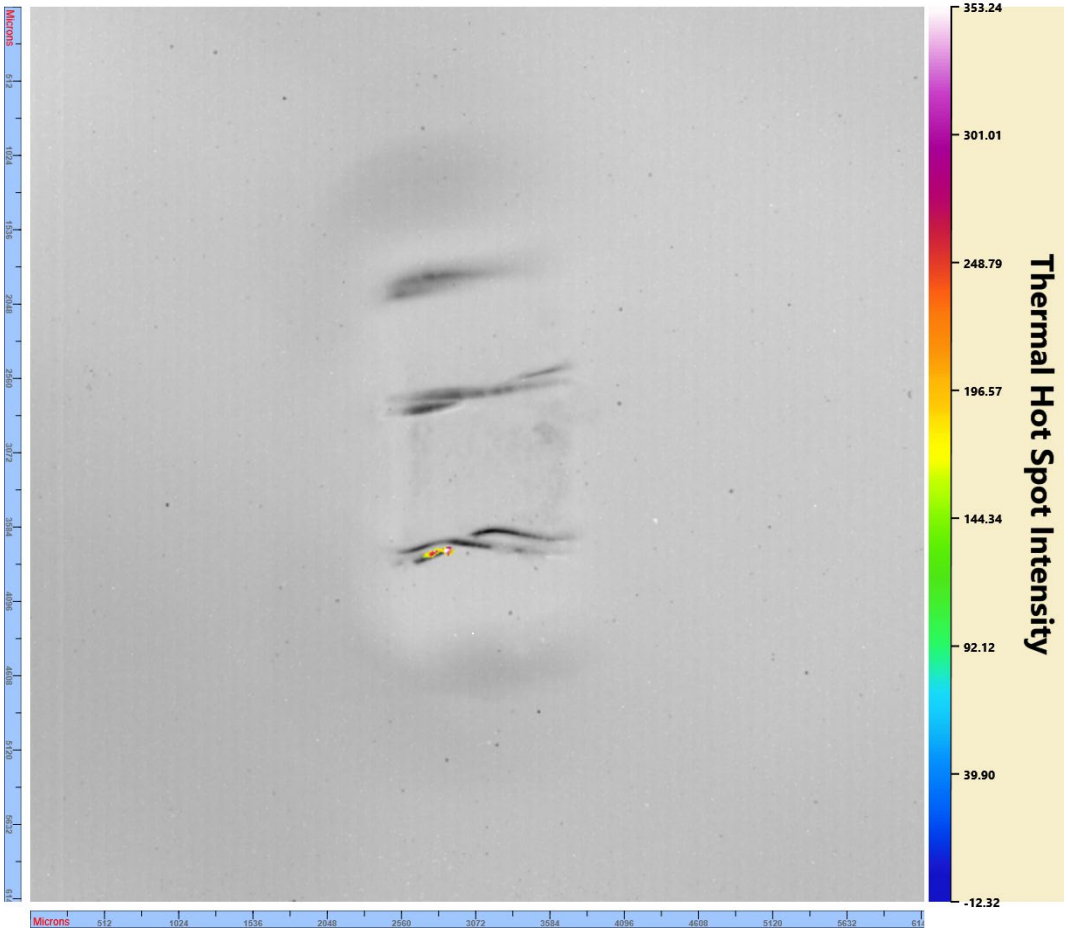
IR hot spot detection used to localize the short circuited gate-source of a transistor.

FA Lab Setup



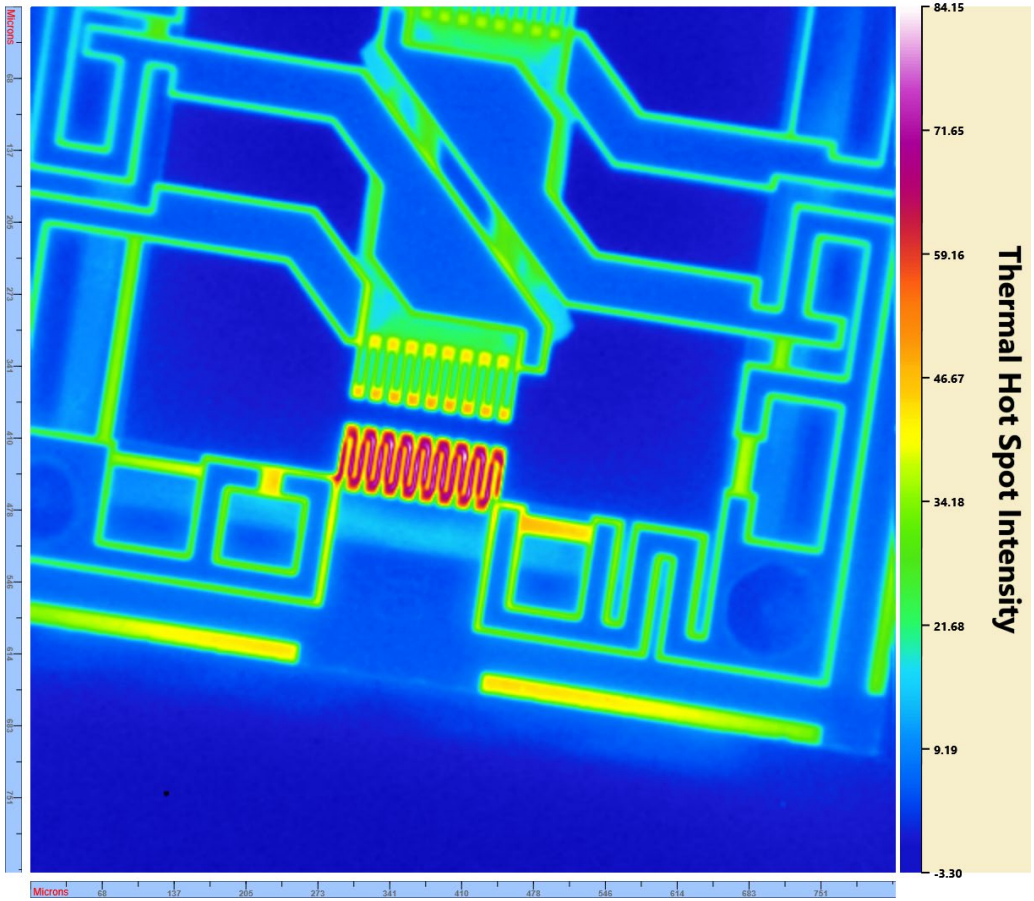
IR hot spot detection used to determine which capacitor in bank had failed.

FA Lab Setup



IR hot spot detection used to determine where two windings had shorted in a transformer.

FA Lab Setup



IR hot spot detection used image the current uniformity in a thin-film resistor. This is a great lab upgrade!

Terminology

- **FA** – Failure Analysis
- **DPA** – Destructive Physical Analysis, though it sounds similar, it implies a different type of testing that is more in-line with screening, where components are destructively analyzed to ensure they meet MIL-STD requirements
- **DUT** – Device Under Test, used to refer to the component being tested or analyzed
- **EOS** – Electrical OverStress, a failure mechanism typically including over-voltage, overcurrent, or other electrically induced phenomena
- **ESD** – ElectroStatic Discharge, a failure mechanism due to static charge buildup, can include Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM)
- **MLCC** – Multi-Layer Ceramic Capacitor, a common style of chip capacitor.

Terminology

- **SMT/SMD** – Surface Mount Technology or Surface Mount Device, a style of packaging that allows surface mounting rather than through-hole design, smaller form factor generally
- **SAM** – Scanning Acoustic Microscopy, a pseudo non-destructive method to examine components/packaging for delamination, voiding, cracking or other abnormalities
- **SEM** – Scanning Electron Microscope, a high power microscope to allow better inspection as well as elemental analysis with Energy Dispersive Spectroscopy (EDS)
- **Failure Mode** – the manner in which the component failed
- **Failure Mechanism** – the cause for the failure
- **Damage vs Defect** – "Defect" is a loaded word in this industry and implies a latent issue that negatively impacts reliability, where "Damage", or "failure site" implies that some external mechanism resulted in failure

The Failure Analysis Process

Overview of the Failure Analysis Process

- Component history
  - In some industries component details are not available, but in others a comprehensive history can be obtained. Details such as test conditions, environment, and time to failure can strengthen a failure analysis.
- Inspect and document
  - It may seem inconsequential, but the condition of the component and electrical connection in-circuit can be related to the failure. It is good practice to inspect and document the suspected component(s) prior to rework or any destructive electrical testing, e.g. removal of the component from the circuit or aggressive probing of the solder joints.

Overview of the Failure Analysis Process

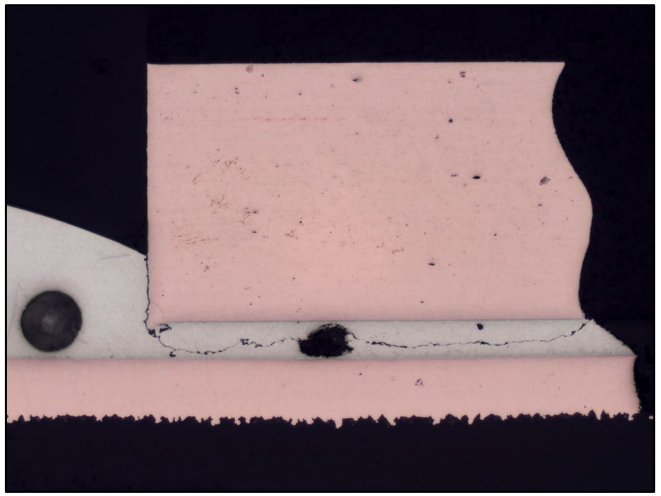
- Collect as much data non-destructively as possible
  - In failure analysis, the sample size is typically very small and because of this it is imperative to gather as much information as possible in a non-destructive manner. This includes thorough external examination, radiographic inspection, low-power electrical testing and failure characterization, and other techniques such as hermeticity testing and scanning acoustic microscopy when applicable.
- Keep an open mind
  - It is easy for biases to affect the failure analysis methodology. Things like the outcome of other analyses of similar components, or preconceptions based on data/history can result in an approach to the analysis that is focused on a set outcome. Many different mechanisms can result in the same type of electrical failure.

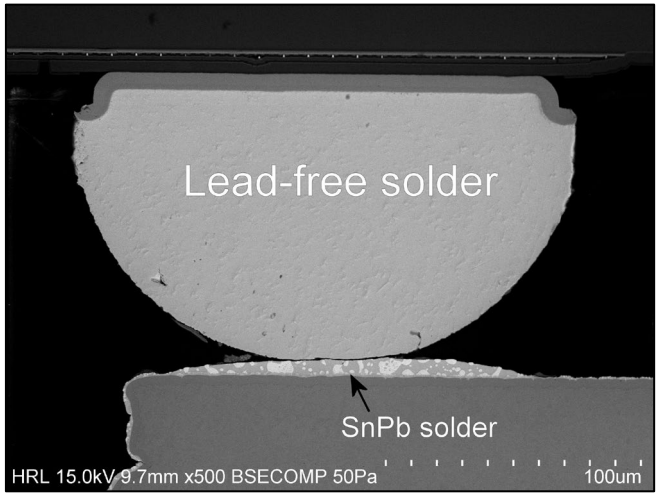
Board-Level Failures

Board-level failure mechanisms are a common cause of failure for every electrical component and must always be considered.

Board-Level Failures

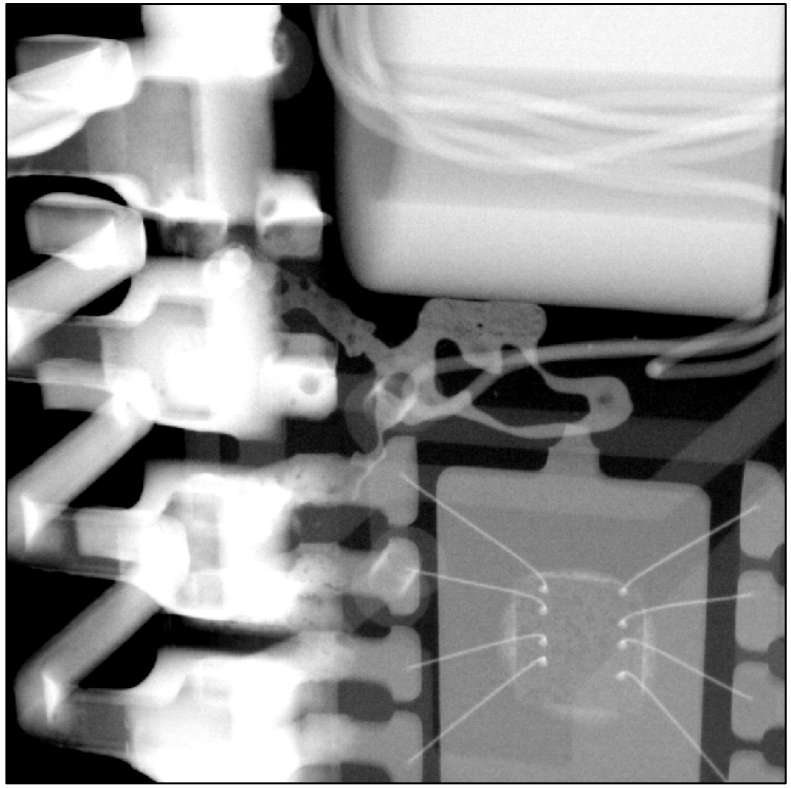
- Disconnected solder joints
  - Mechanical stresses
  - Non-wetting
  - Head-on-pillow
  - Each of these defects can be masked by solder reflow during component removal.





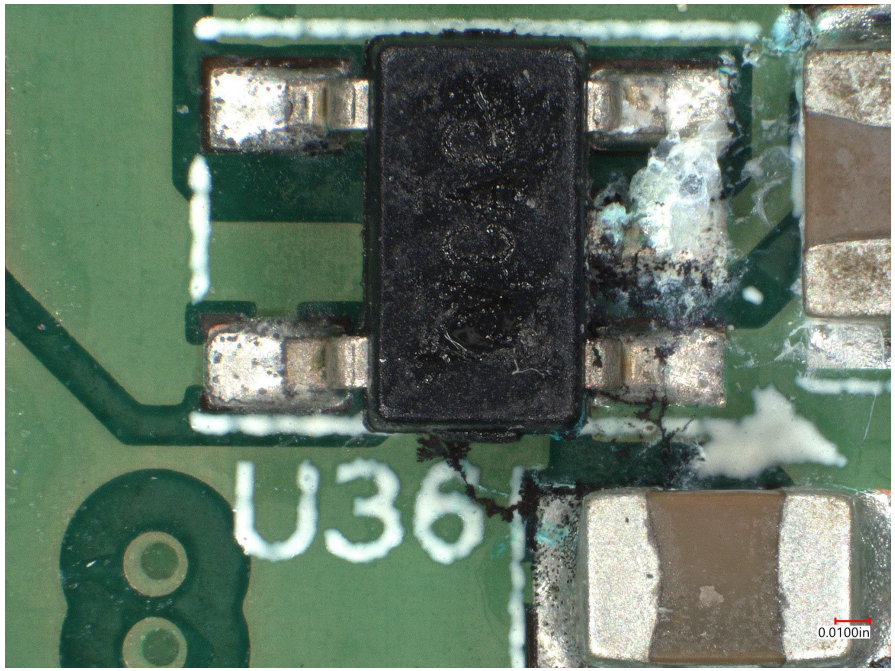
Board-Level Failures

- Reflowed solder
  - Incorrect solder compositions used
  - Incorrect solder reflow profiles
  - Hand soldering
  - Can be hidden beneath components
  - Can also be cleared with solder reflow during component removal



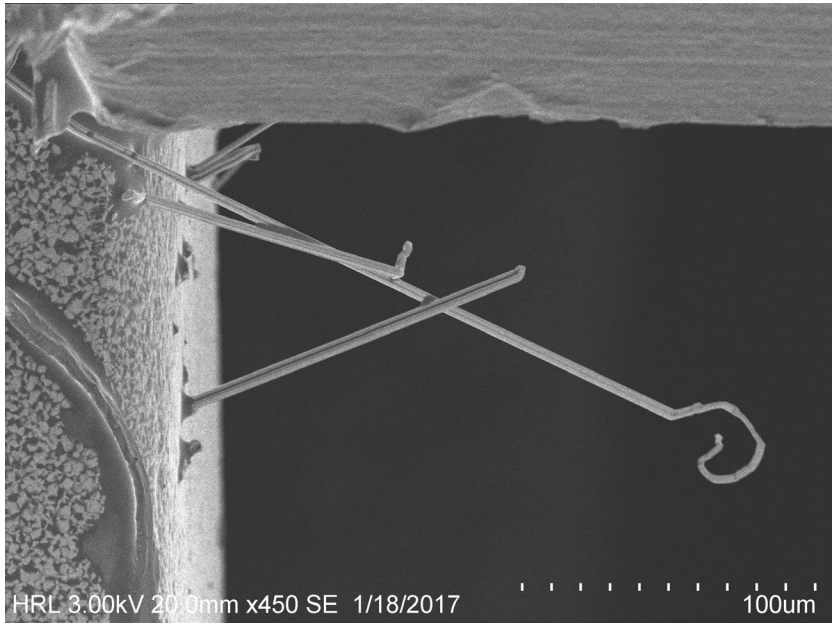
Board-Level Failures

- Dendrites/corrosion
  - Can occur in corrosive environments or due to improper board cleaning processes.
  - Typically results in resistive current leakage paths or open circuiting of metal traces
  - Can form beneath components



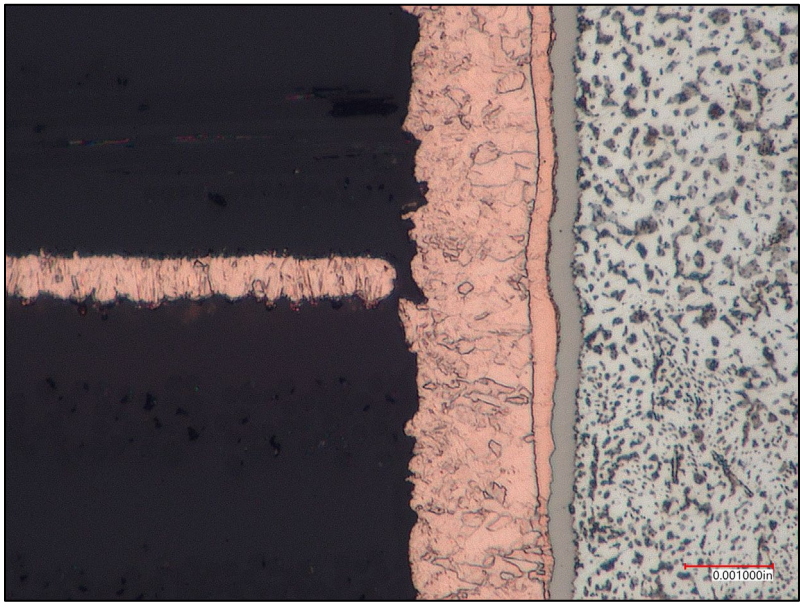
Board-Level Failures

- Tin Whiskers
  - Occur when pure tin plating is used, which is becoming increasingly more rare.
  - Can conduct high current for their size, but can also fuse open, resulting in a “self-heal”.
  - Can grow to surprising lengths.



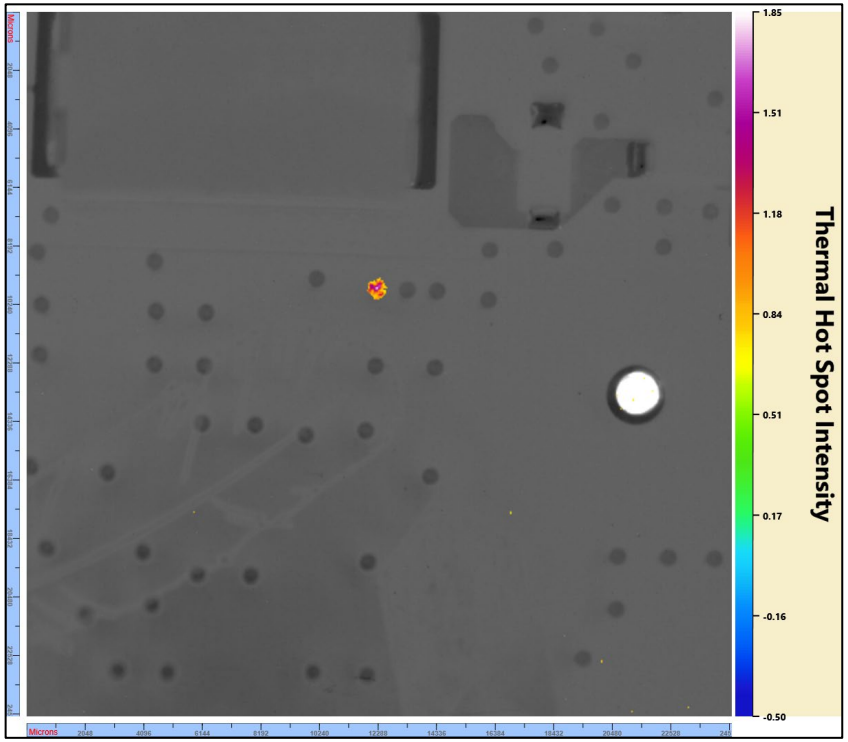
Board-Level Failures

- Internal PCBA failures
  - Board layer delamination
  - Over-etching of vias/through-holes
  - Conductive anodic filament (CAF)
  - Fracturing of board layers due to mechanical stresses
  - Masking/etching defects in metallization layers



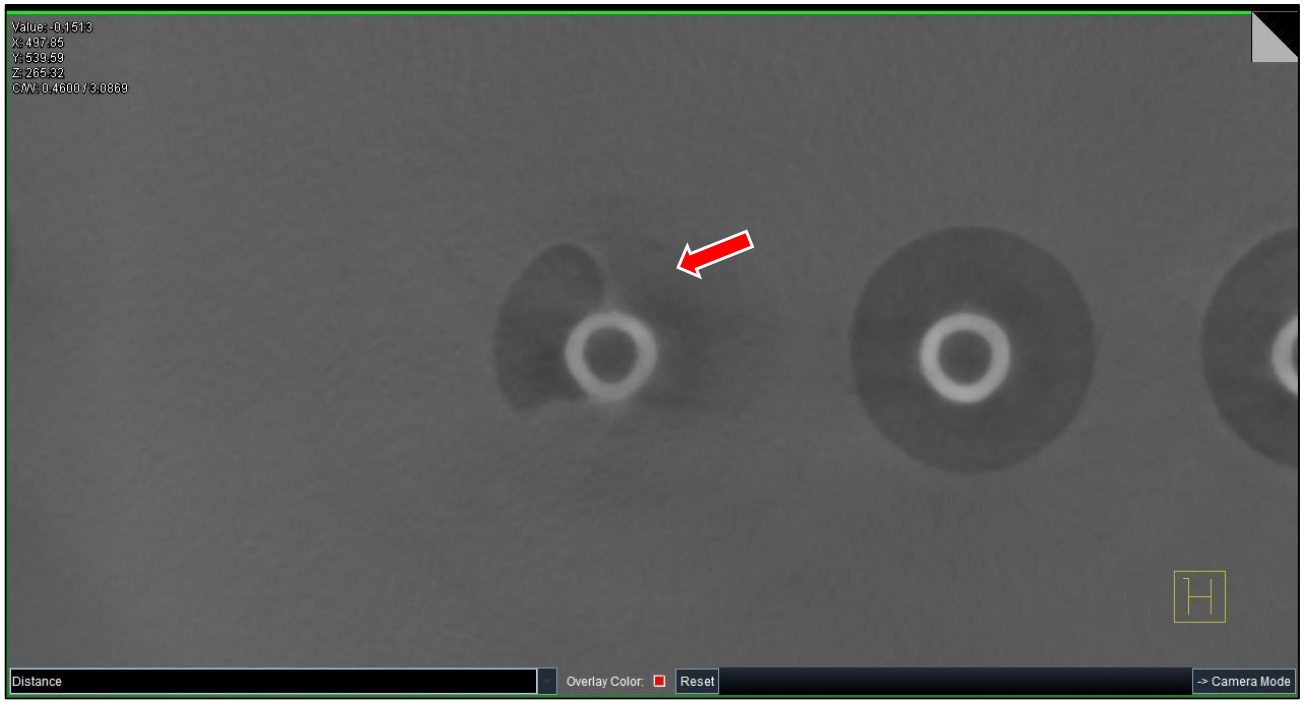
Board-Level Failure – Example

- A CCA exhibited a 4mΩ short circuit between two nodes.
- Customer-level testing isolated failure to two suspect planes.
- Infrared hot spot detection was performed and localized the failure to a single via, which was connected to the suspected planes.



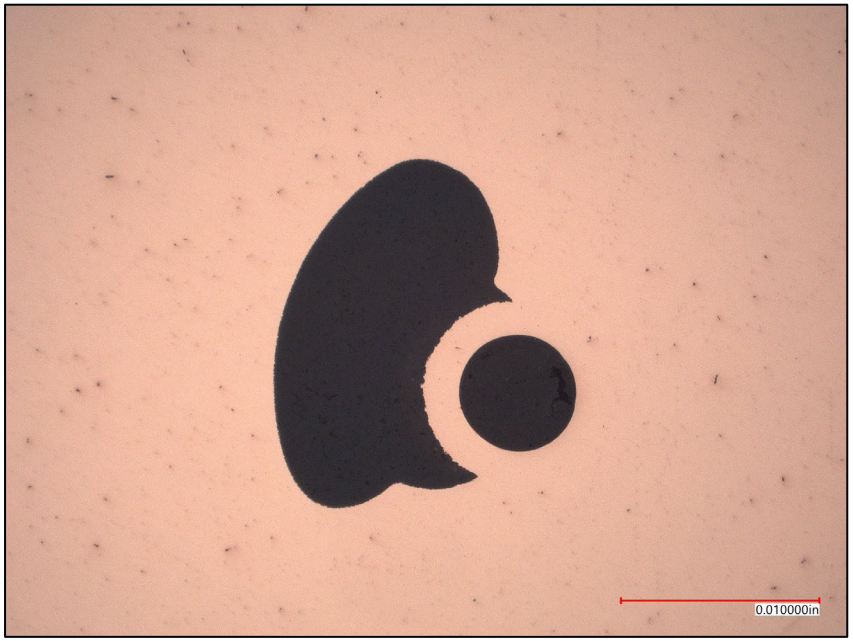
Board-Level Failure – Example

- 2D, real-time radiographic inspection was performed on the CCA in an attempt to identify any defects, but due to board density it was inconclusive.
- Laminography was then performed to “slice” through the layers of the board until the defect was identified.



Board-Level Failure – Example

- Metallurgical cross section was performed to verify and determine cause of failure; a copper metallization etching defect.



Resistors

Resistor failures are generally due to connection issues, electrical overstress or corrosion from their operating environment.

Resistors

Construction

- More than just a zig-zag symbol on a schematic
- The analyst must consider **all** interfaces in the construction of a resistor when examining for an open circuit or increased resistance.
- Short circuits or decreased resistance always involves some type of material "bridging" the resistor element, creating a low resistance parallel path.

Resistors

Construction – Thick Film Resistor

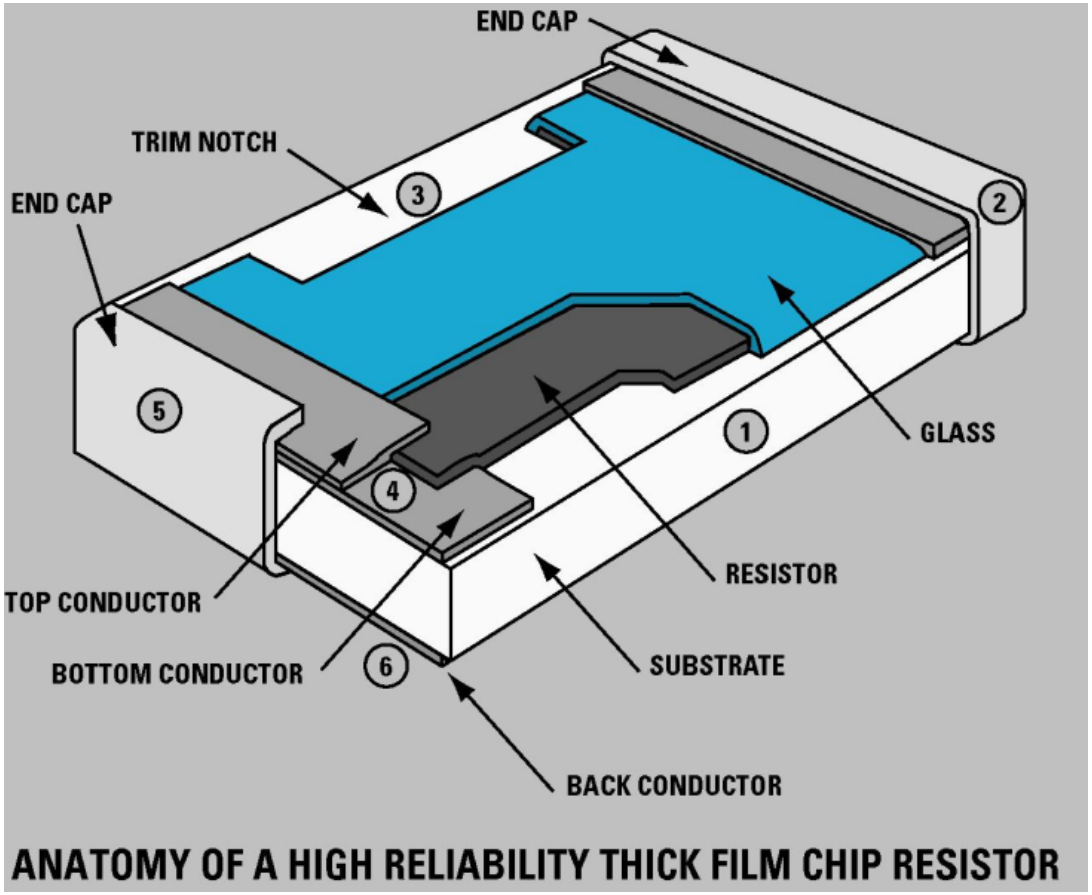


Image from globalspec.com

Resistors

Construction – Thin Film Resistor

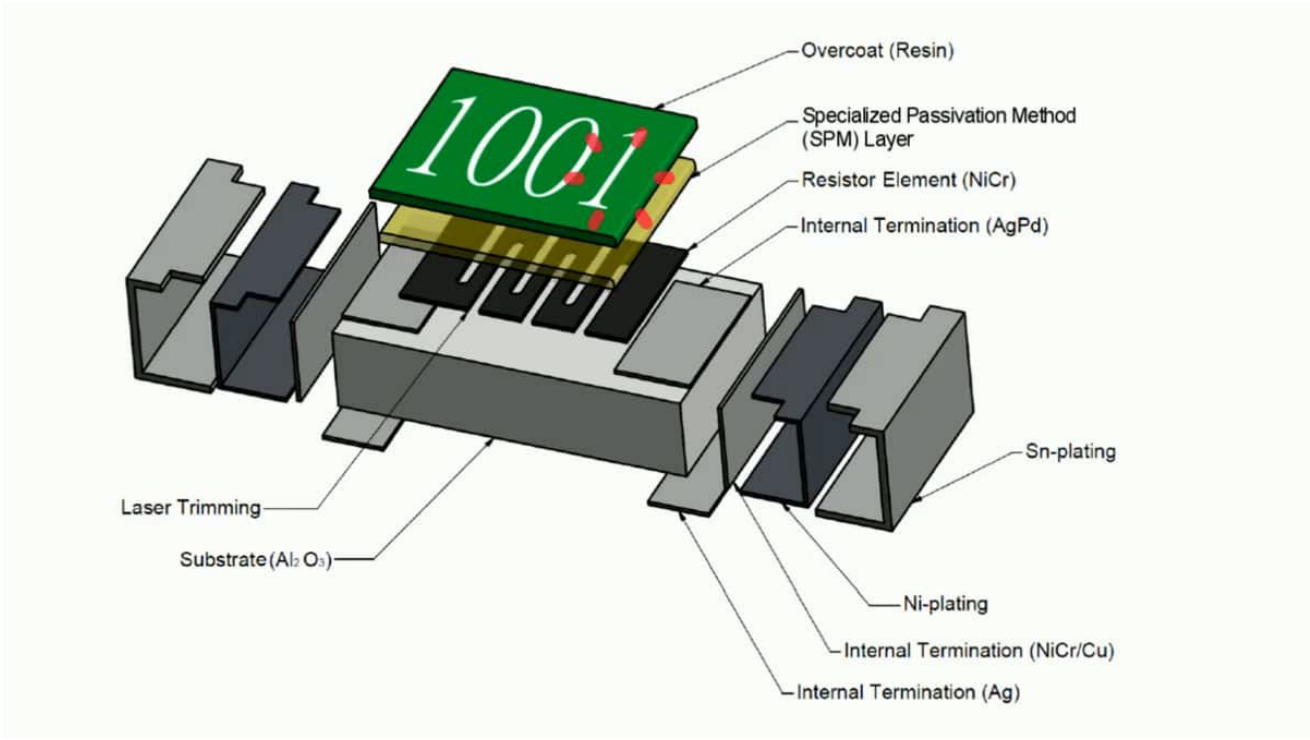


Image from Vishay.com

Resistors

Construction – Wire Wound Resistor

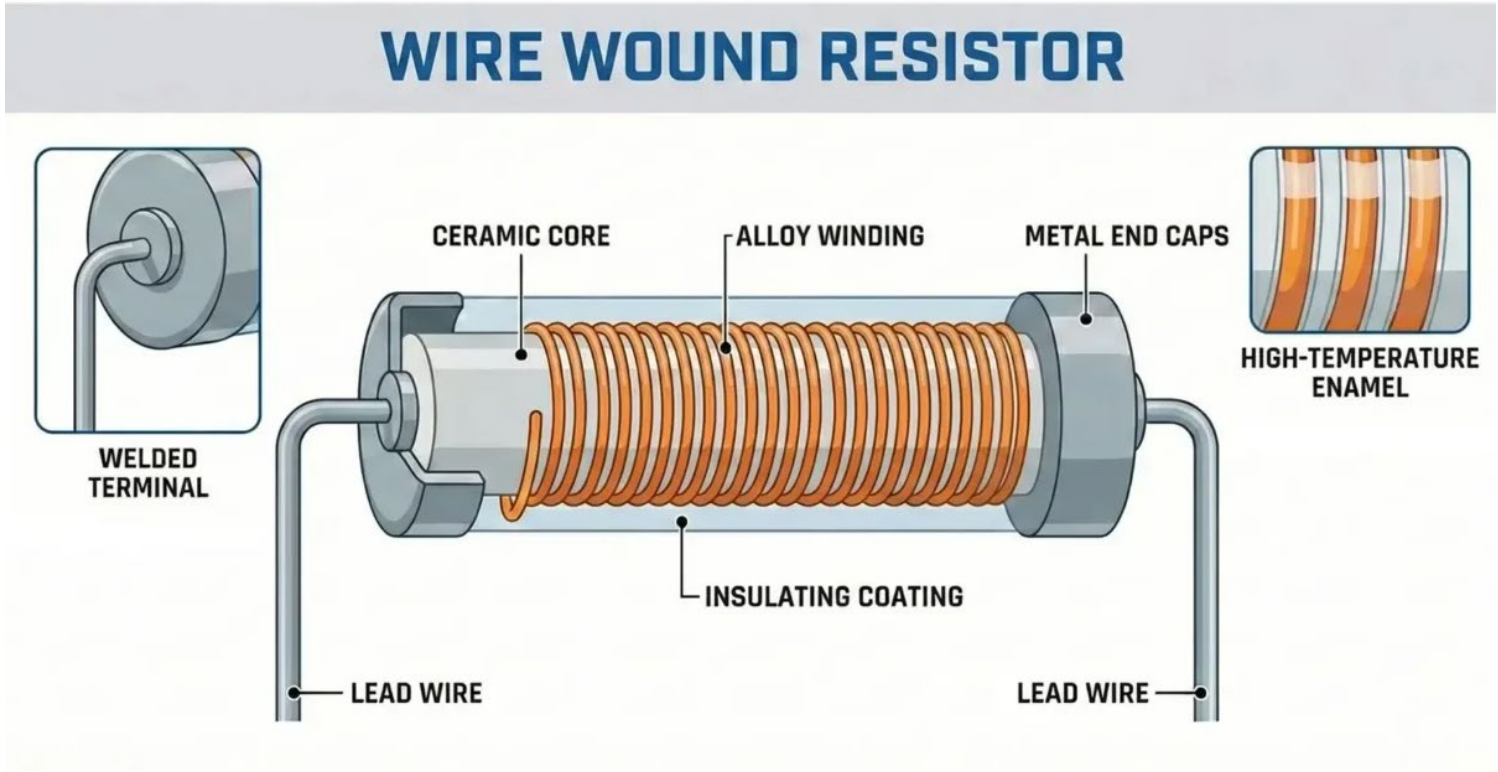


Image from hacktronic.com

Resistors

Construction – Integrated Resistor

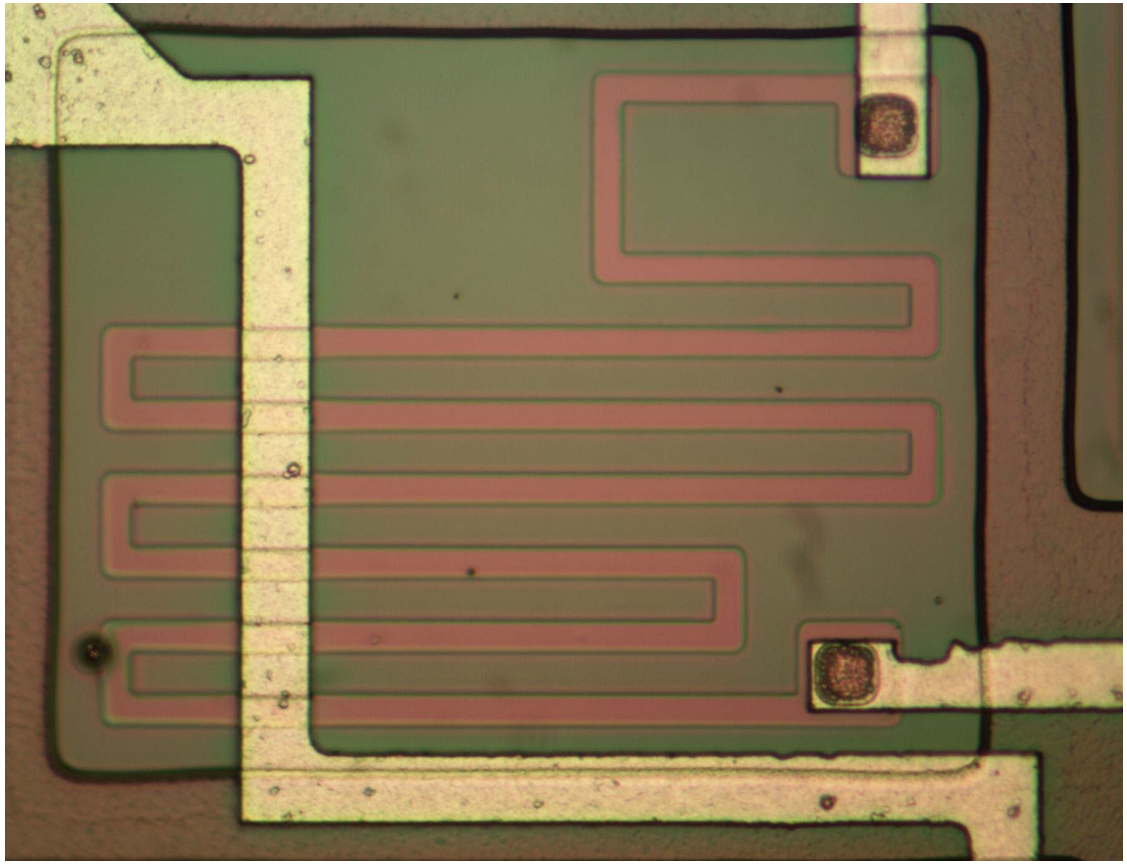
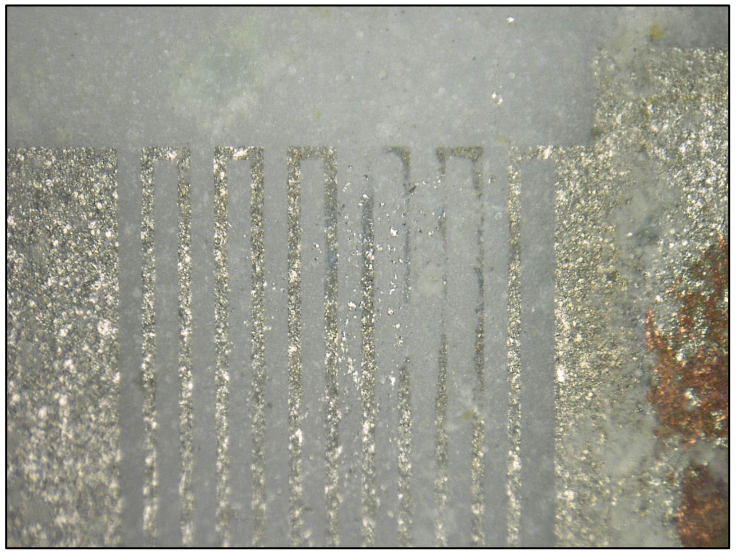
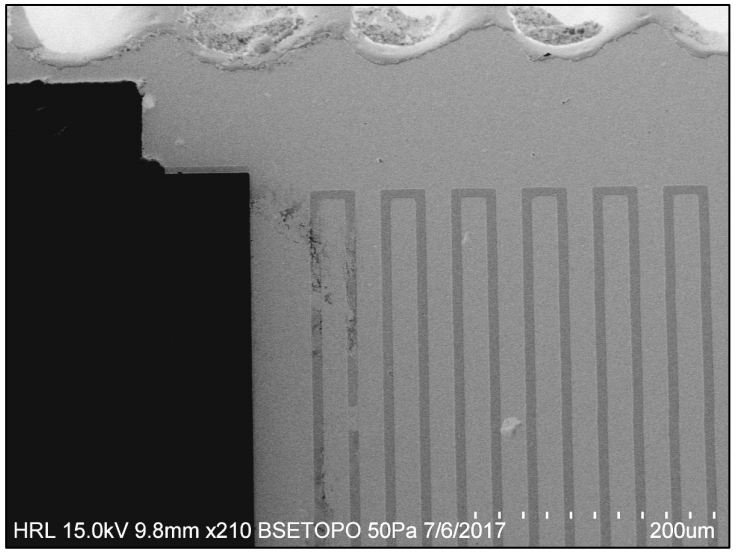


Image from static.righto.com

Resistors

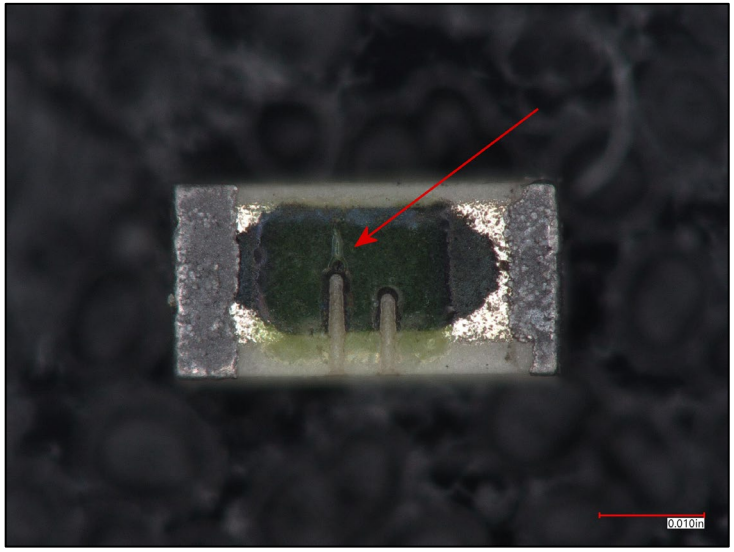
- Corrosion
  - Corrosion is a common failure mechanism for every style of resistor.
  - Can affect resistor element or interconnect metallization.
  - Generally attributed to packaging/seal issues.
  - Can be due to moisture or ionic contamination

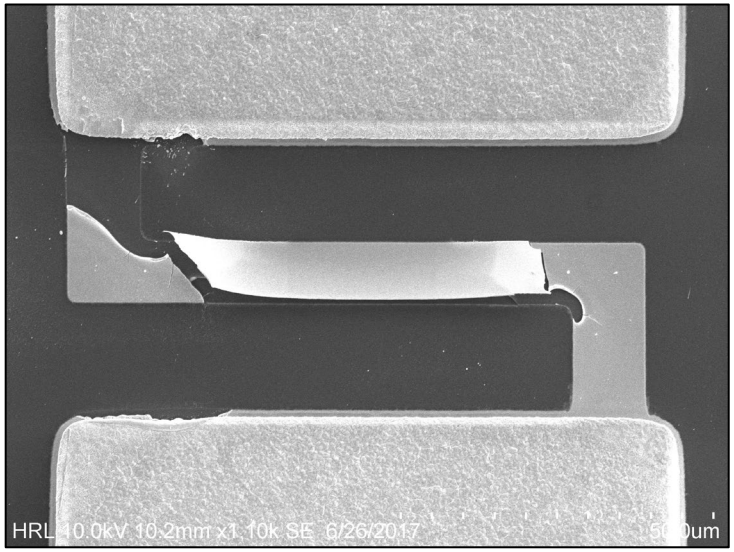




Resistors

- Electrical Overstress
  - Electrical overstress is a broad term, but typically refers to failure due to excessive current or high voltage conditions.
  - The location of the failure within the device, the severity of the damage, and associated circuitry can determine more specific information related to the failure





Capacitors

Multi-layer ceramic capacitors are often damaged by mechanical overstress, while tantalum capacitors are susceptible to damage from surge currents and moisture absorption.

Capacitors

Construction – Basic Design

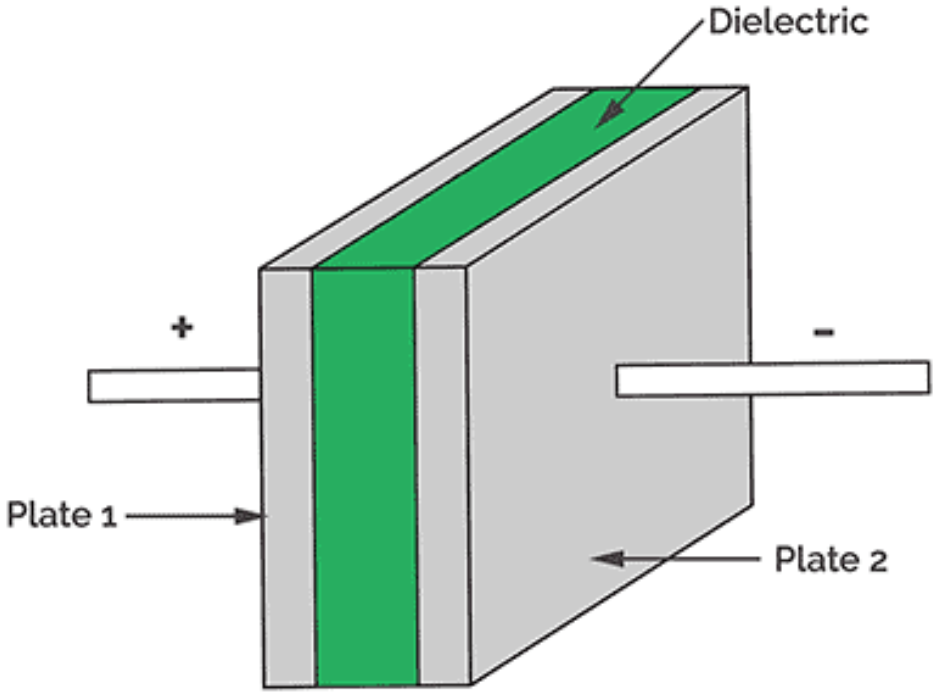


Image from codrey.com

Capacitors

Construction – MLCCs

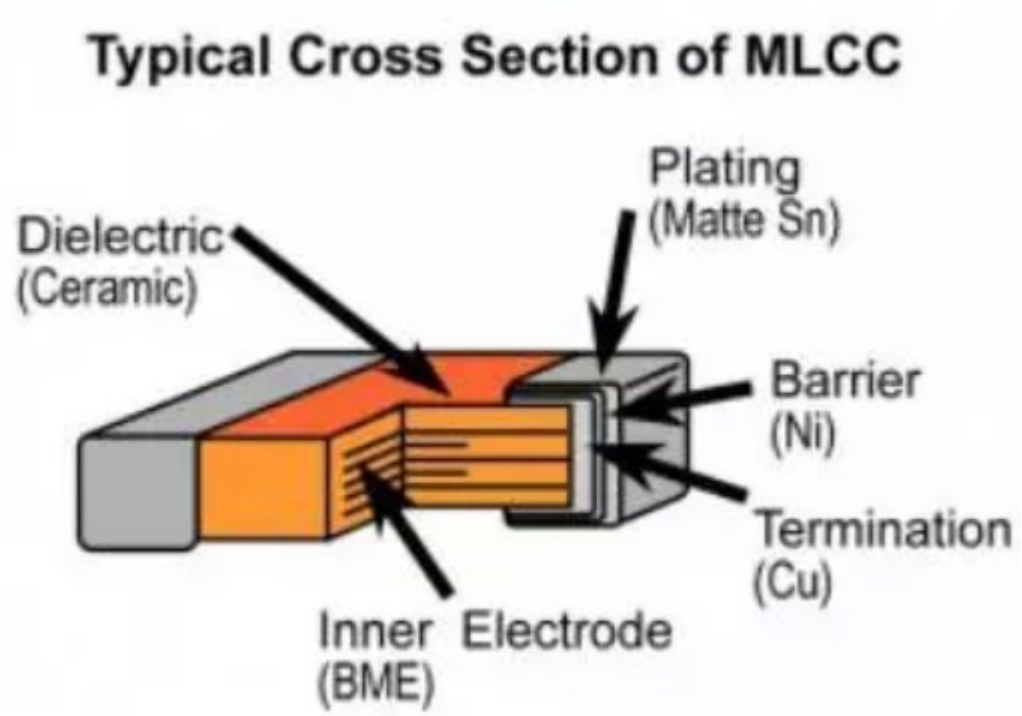
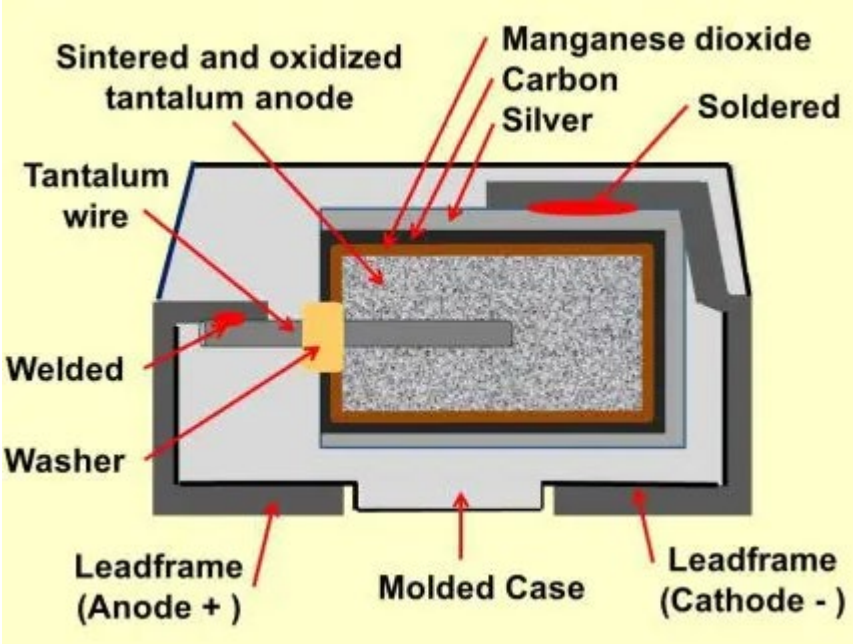


Image from samaterials.com

Capacitors

Construction – Tantalum



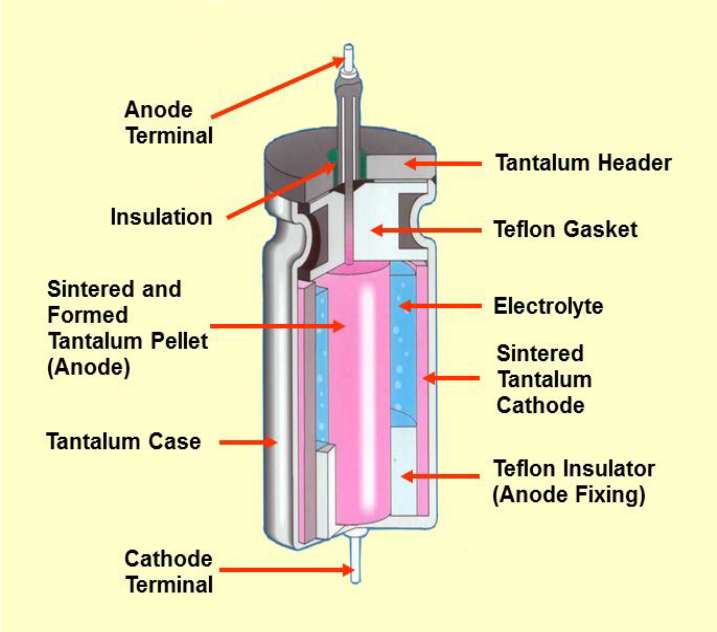
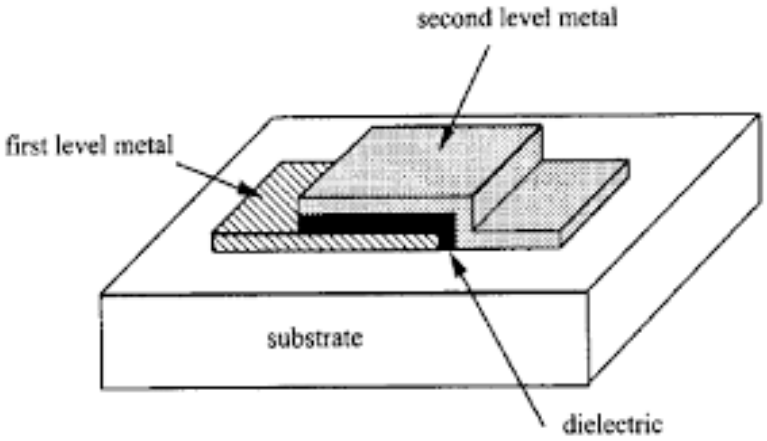
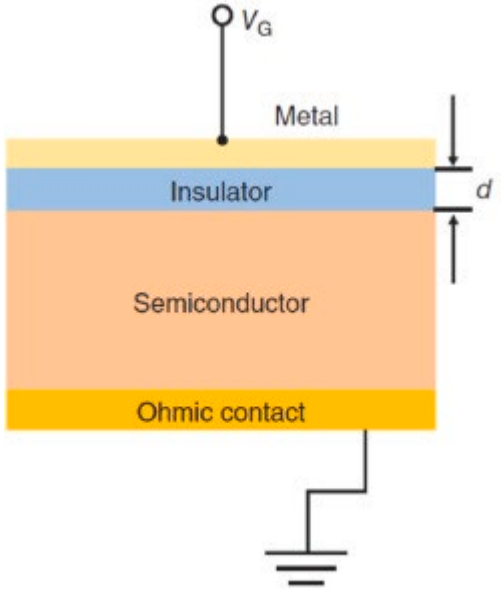


Image from designworldonline.com

Capacitors

Construction – Integrated Capacitors





(a)

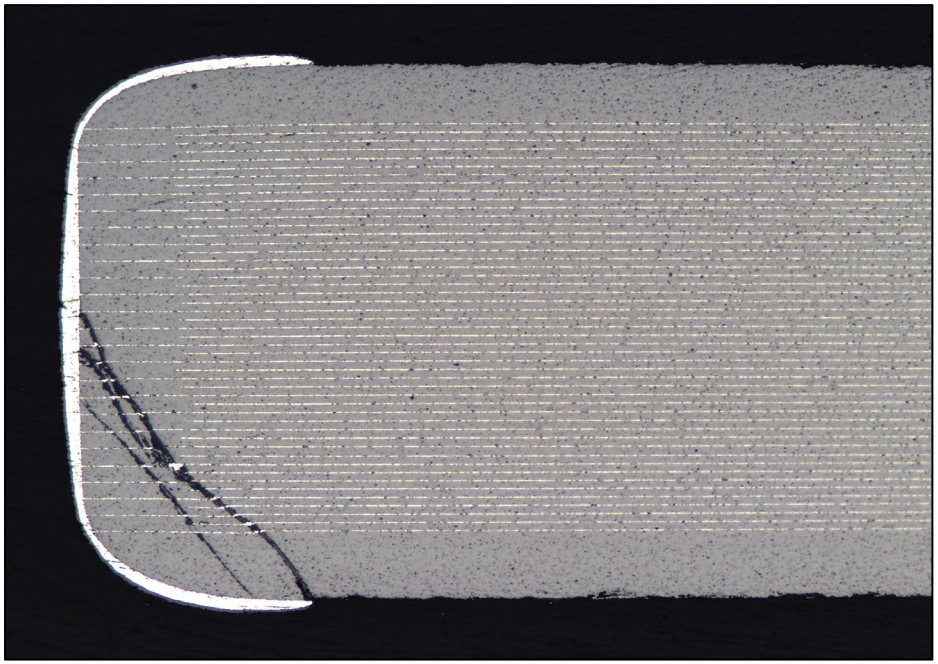
Metal-insulator-metal (MIM), left
Metal-insulator-semiconductor (MIS), right

Images from sciencedirect.com

Capacitors

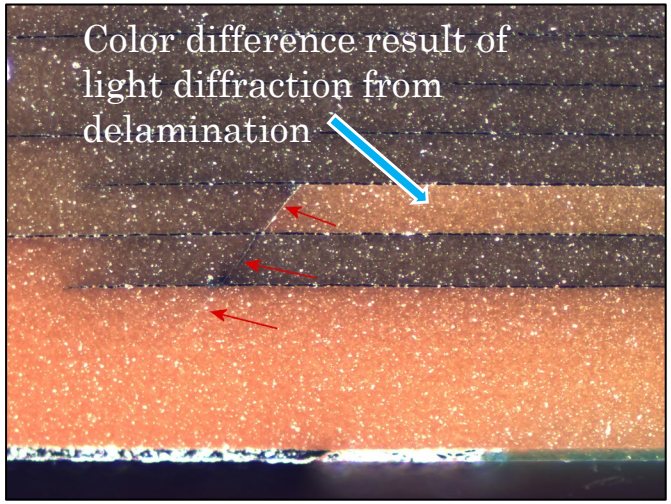
The electrical parameters most affected by failures are DC leakage current, ESR and capacitance. Care should be taken to test the capacitor at low voltage with sufficient current limiting to prevent exacerbation of the failure site.

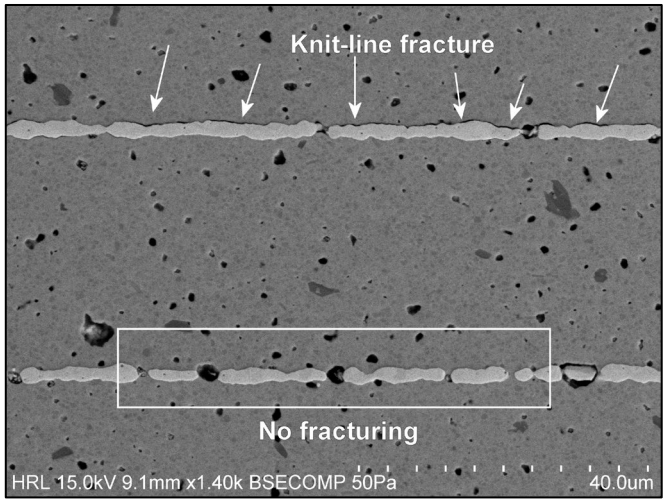
- Mechanical overstress
  - By far the most common failure mechanism for multi-layer ceramic capacitors.
  - Can begin as benign microfractures that propagate with time/temp/stresses, subsequently resulting in current leakage or short circuiting.
  - Flexure cracks have characteristic “45 degree” fracture spanning from the tip of the end metal towards the termination.



Capacitors

- Manufacturing defects
  - The most common defects include delamination, dielectric voiding, and knit line fractures.
  - Similar to mechanical overstress, capacitors affected by these defects can pass electrical testing and later fail in the field.
  - SAM analysis has high success in identifying these defects.



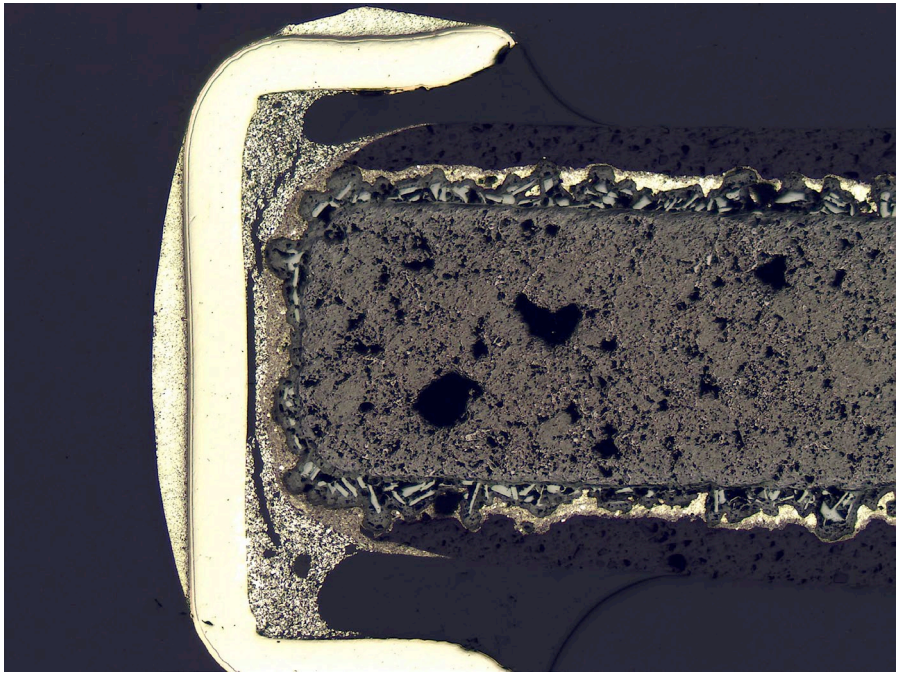


Capacitors

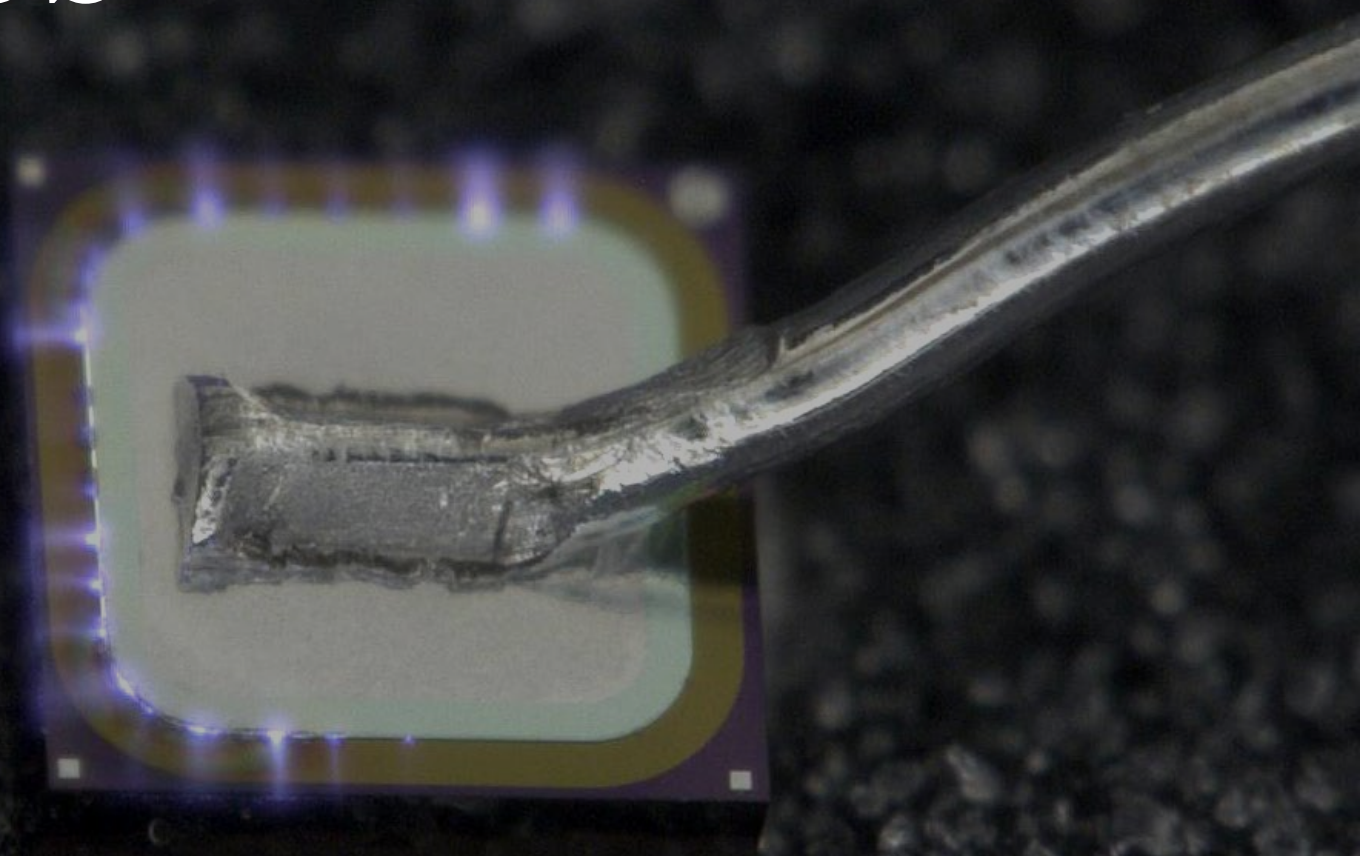
- EOS/Surge current and ESR considerations
  - Tantalum capacitors are commonly damaged by high in-rush current (i.e. surge current).
  - This type of failure can be due to equivalent series resistance (ESR) variations in tantalum capacitor banks.

Capacitors

- ESR failures
  - Typically, high ESR in tantalum capacitors is due to damage/defects in the cathode attach system.
  - Fracturing of the cathode silver epoxy is a common failure mechanism for ESR.



Diodes



Diodes can be damaged several ways. It's important to consider failure mode (open, short, degraded), temperature sensitivity and packaging when performing a failure analysis.

Diodes

Construction – Basic Diode

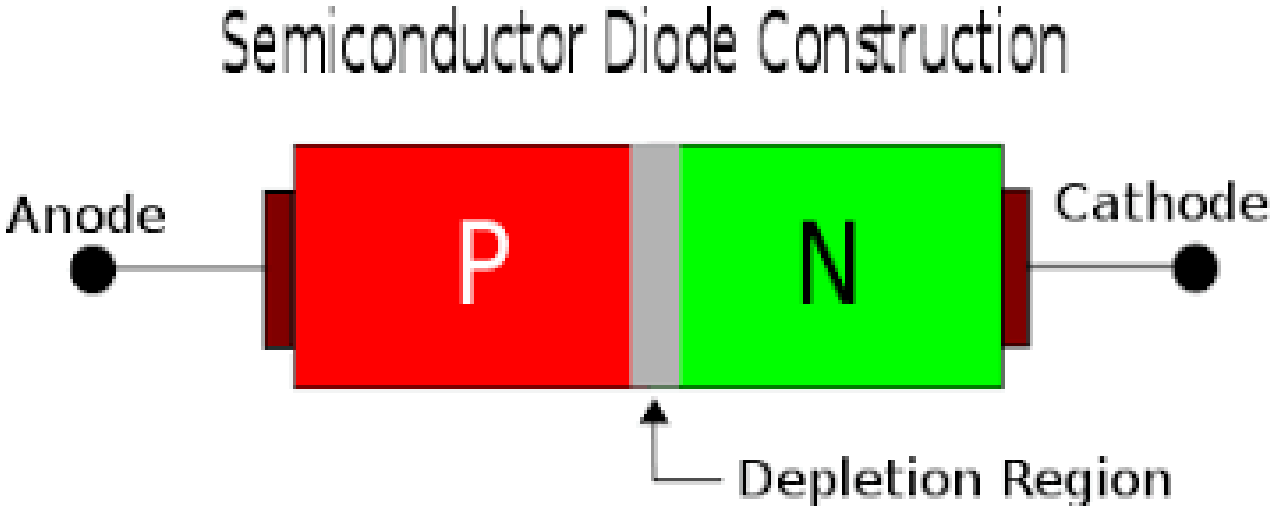
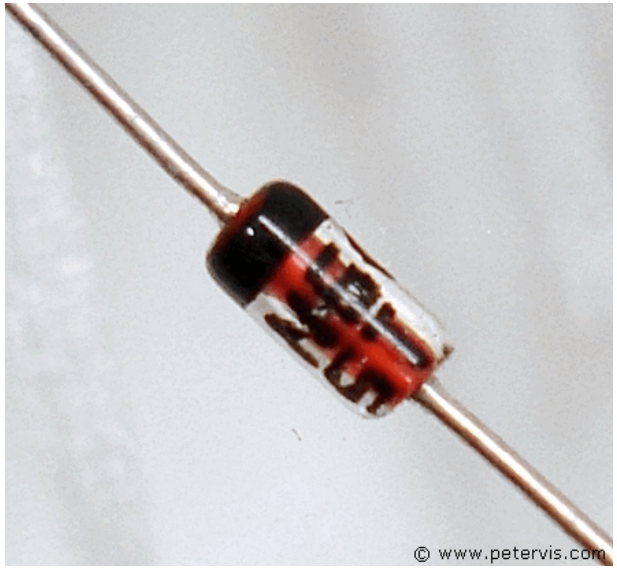


Image from seeedstudio.com

Diodes

Construction –Diodes



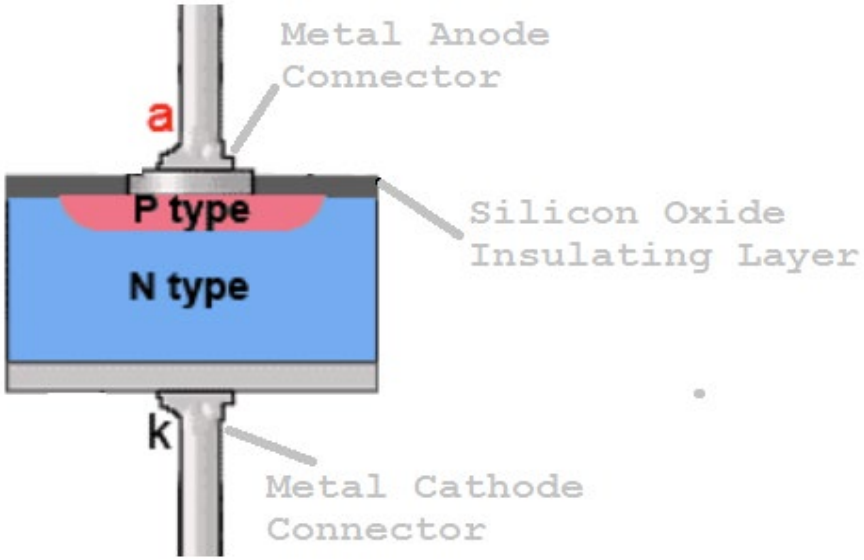


Image from engineersgarage.com

Diodes

Construction – Integrated Diode

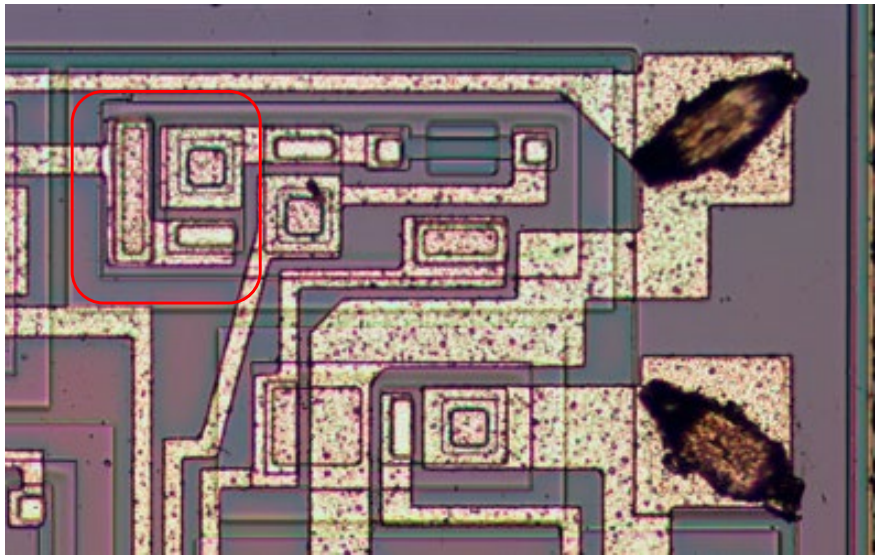
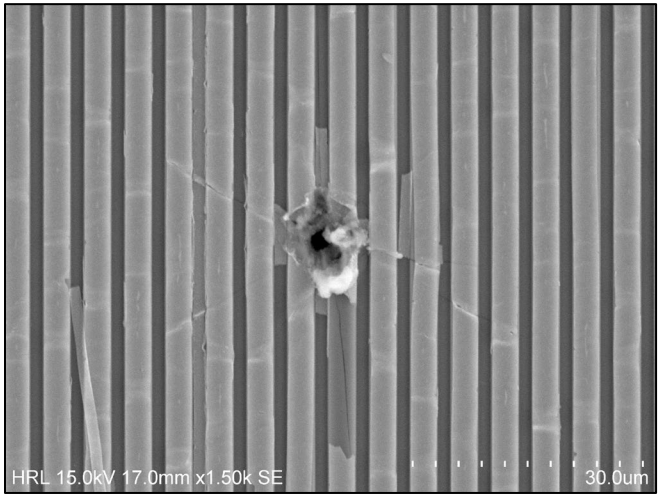


Image from righto.com

- Uses a BJT transistor structure, with the base-collector shorted as a diode.

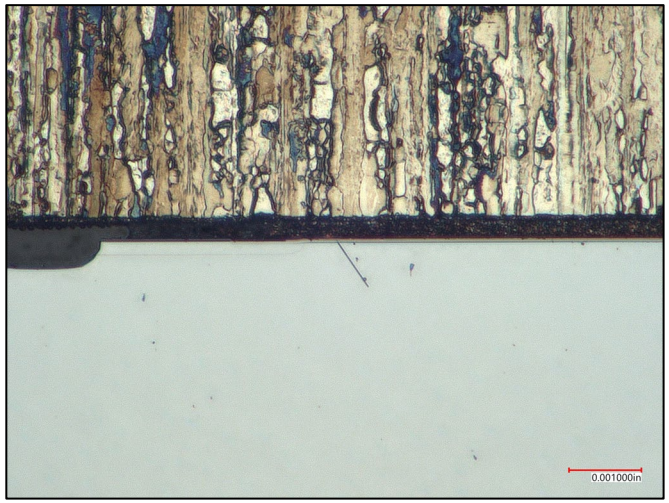
Diodes

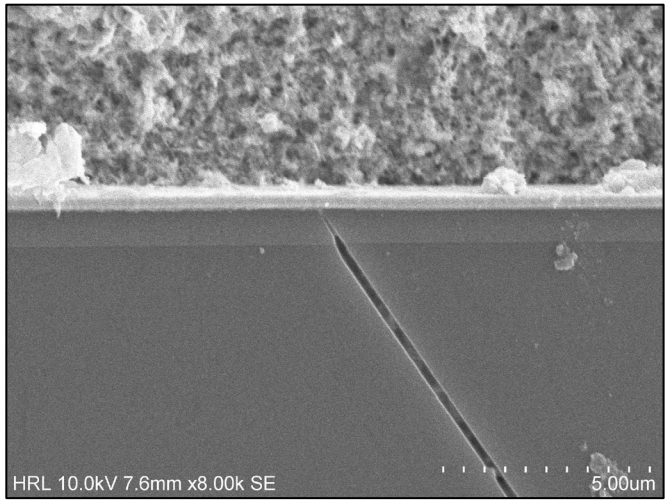
- Electrical overstress (EOS)
  - EOS is typically due to high reverse voltage, high forward current, or a high speed voltage transient.
  - Electrostatic discharge (ESD) damage is similar in appearance to reverse-biased high-speed voltage transients, and generally occur at the edge of the anode contact area (upper image), while forward biased current transients occur central to the die where current density is the highest (lower image).



Diodes

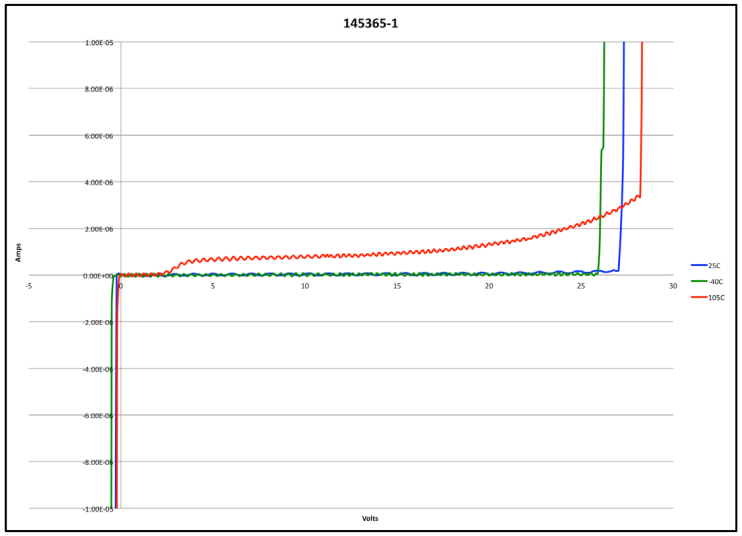
- Thermal/Mechanical overstress
  - Glass body diodes are susceptible to fracturing due to lead forming, handling, and thermal overstress induced during the soldering process.
  - These fractures can result in low level leakage, with the potential to worsen over time and temperature.

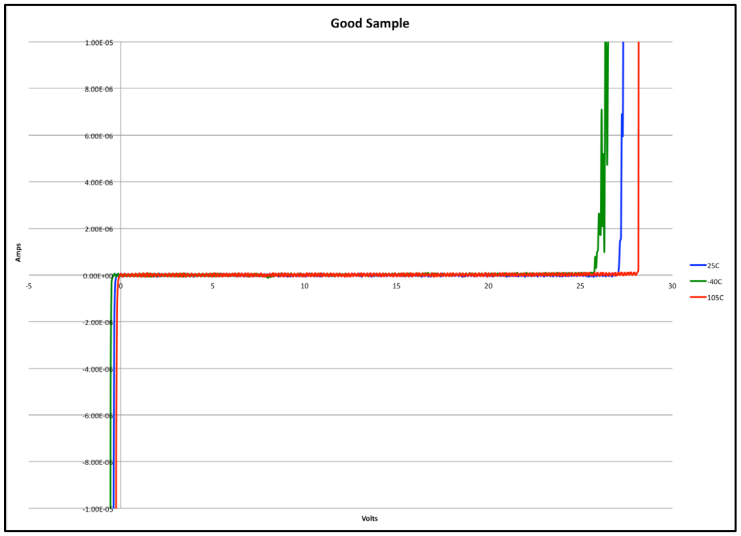




Diodes

- Ionic contamination
  - Can affect any PN junction and presents as temperature sensitive leakage current, commonly with “inversion” characteristics when plotting the I/V curve. Note red curve in below I/V plot showing leakage at +105C.
  - Often can recover with vacuum baking.
  - It is due to mobile ionic contamination on die surface or passivation layers.

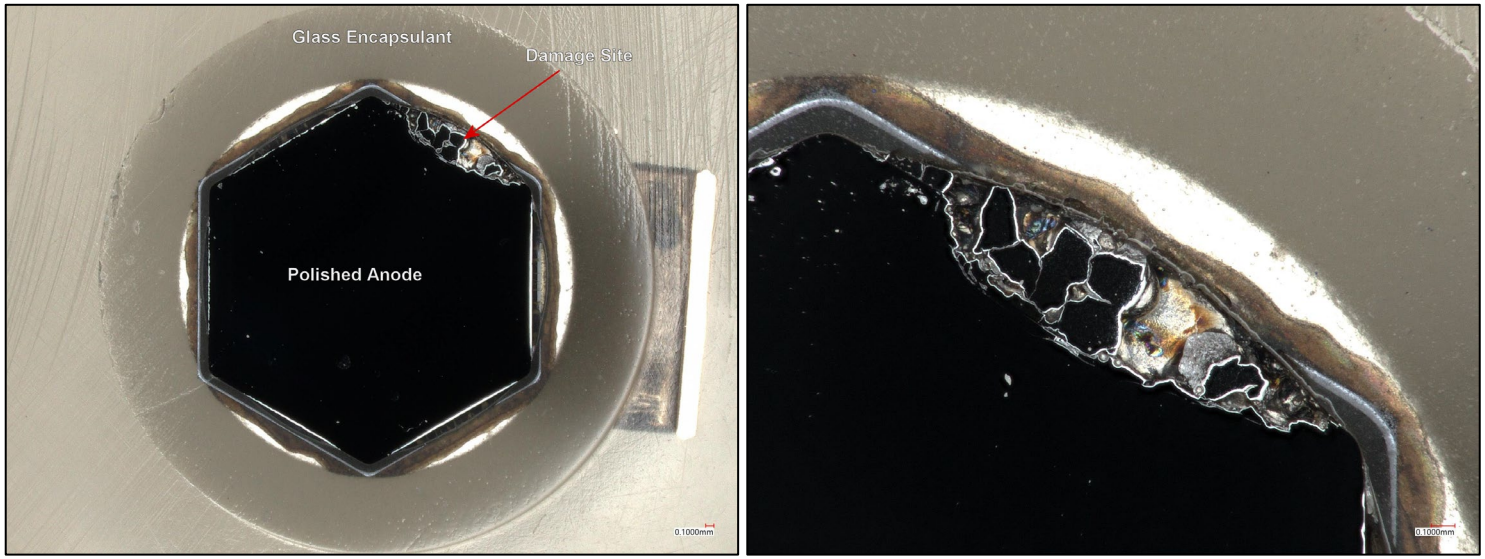




Diode Analysis - Example

A diode array failed after 13 years of service where the diode was under reverse bias.

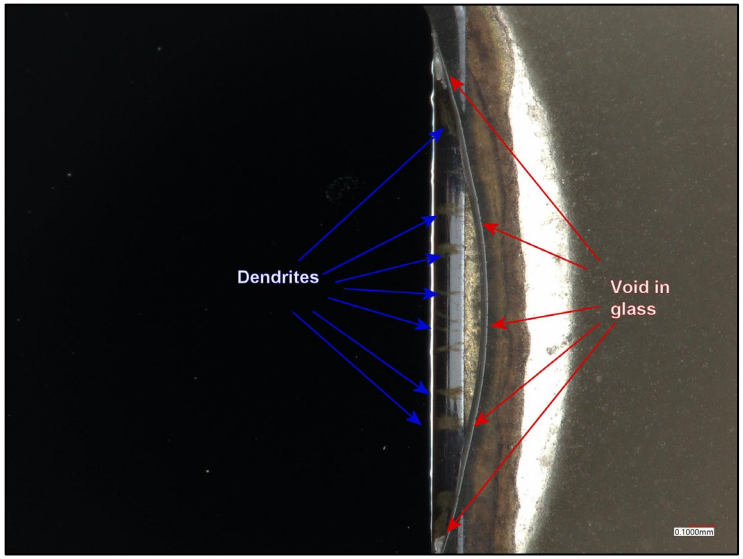
After scheduled maintenance, the diode failed catastrophically upon system startup.

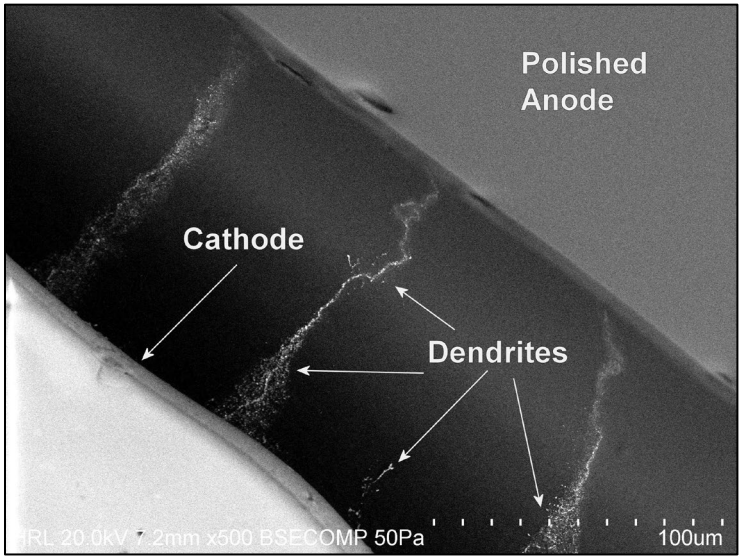


The location of this damage is consistent with failure due to a reverse biased over-voltage event, but the failure history is important in this case.

Diode Analysis - Example

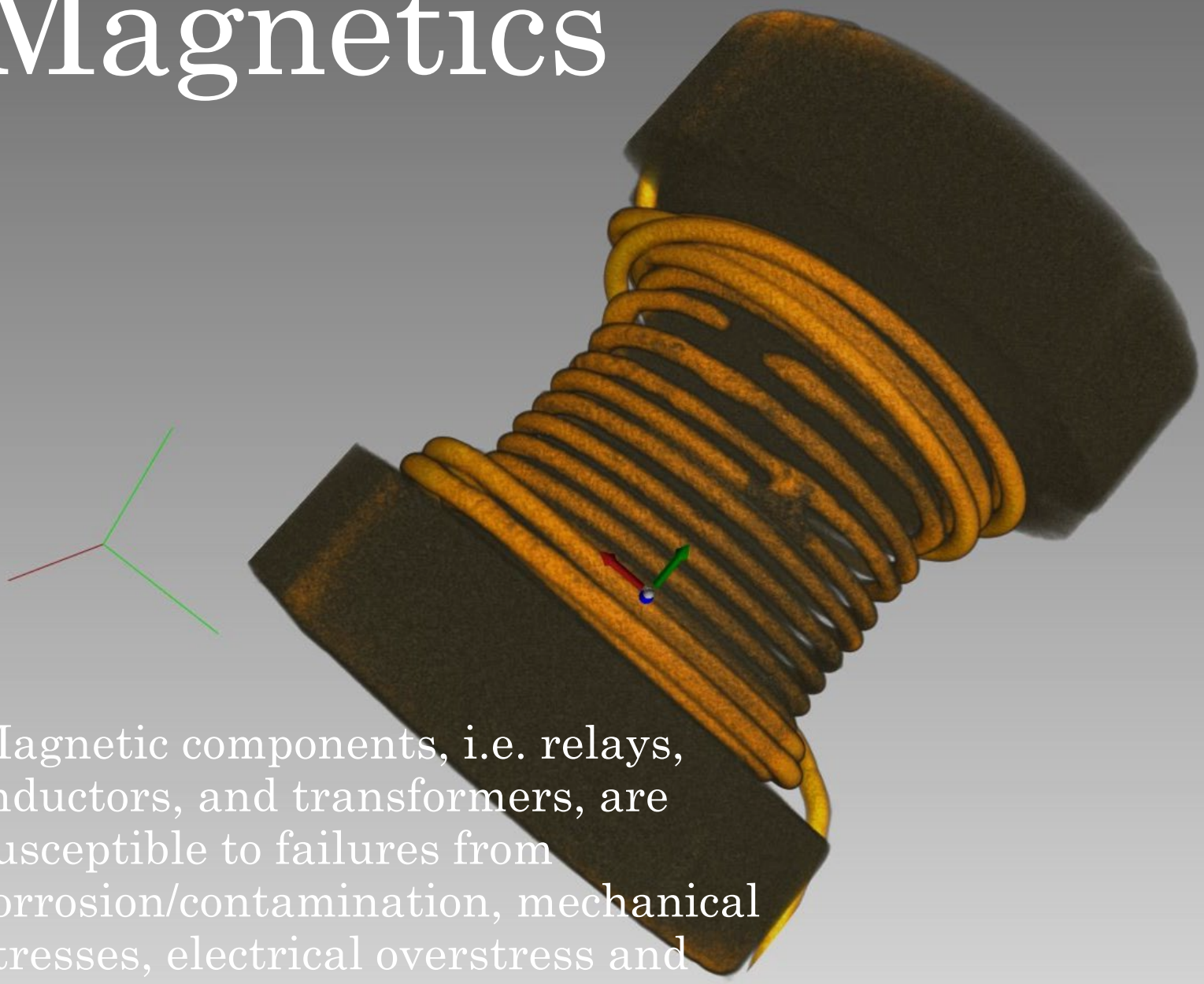
- This type of diode was built using silver die attach metallization, and silver is notorious for dendritic growth under the right circumstances, one of those being long-term voltage bias.





- In this instance, a combination of voiding in the glass envelope surrounding the die and the long-term voltage bias resulted in the formation of dendrites from the cathode of the diode towards the anode. The *normal,* short term, high-voltage turn-on transient was sufficient to arc from the anode to the dendrites, resulting in the catastrophic damage to the diode.

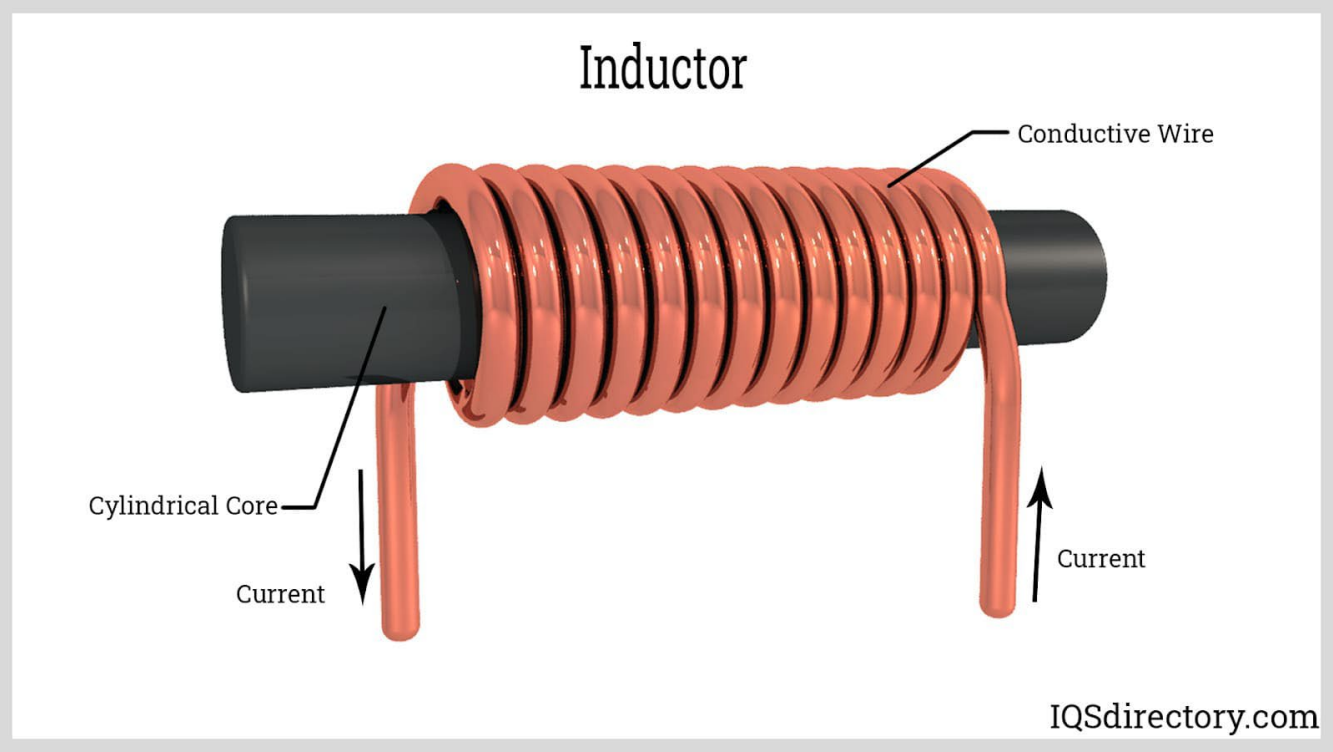
Magnetics



Magnetic components, i.e. relays, inductors, and transformers, are susceptible to failures from corrosion/contamination, mechanical stresses, electrical overstress and manufacturing defects.

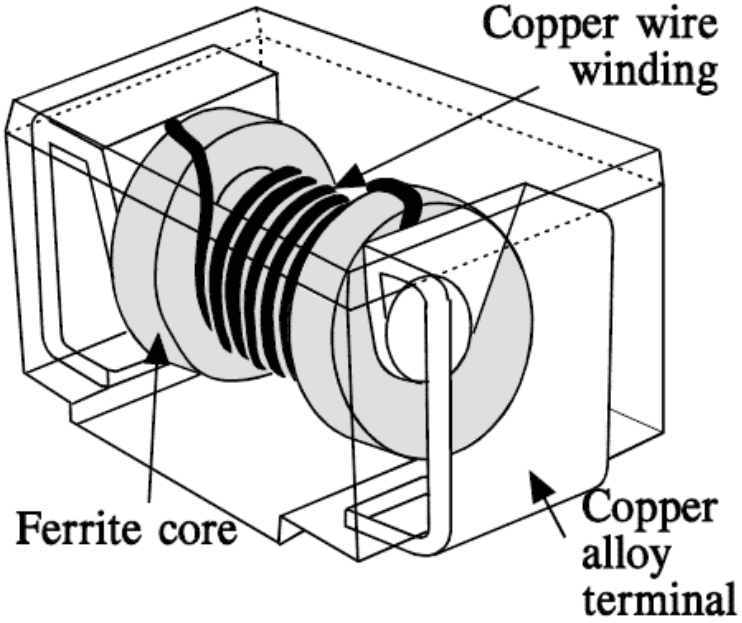
Magnetics

Construction – Inductor - Basic



Magnetics

Construction – Inductor - Typical



- Typical inductor designs, with exposed windings (left) and a potted SMT component (right).

Magnetics

Construction – Integrated Inductor

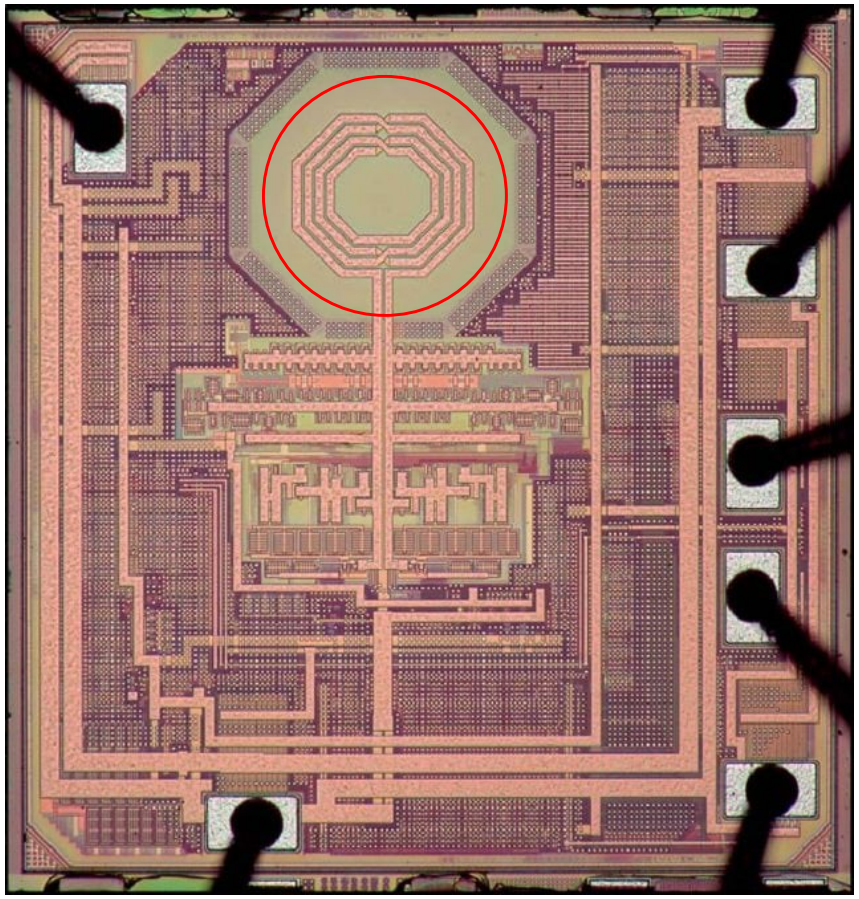


Image from miscircuitos.com

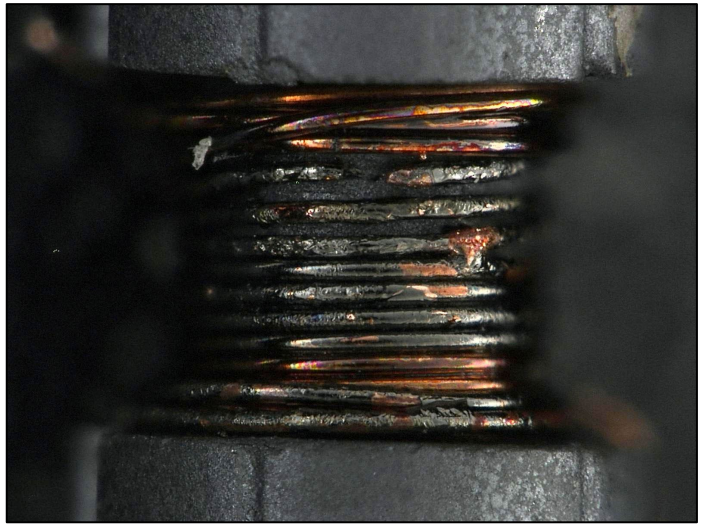
Magnetics

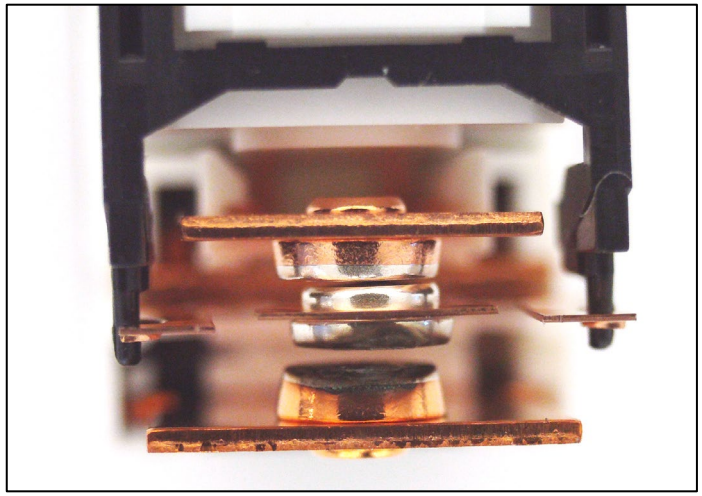
Construction – Transformer

Image from TDK.com

Magnetics

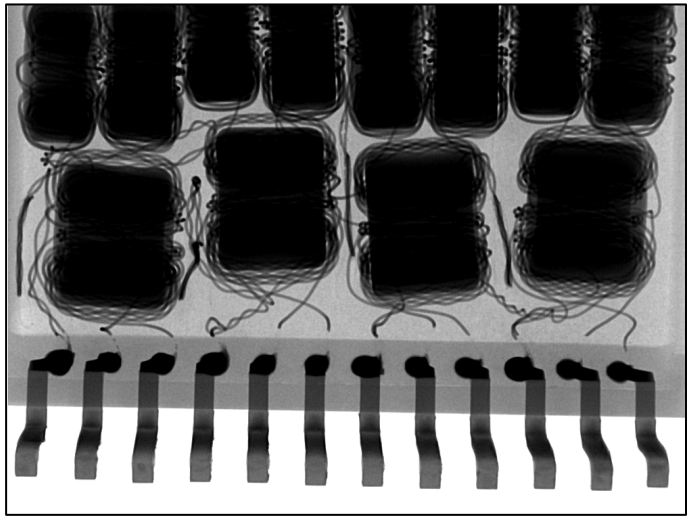
- Electrical overstress
  - Failure can result from excessive current, which will melt the entirety of the wire winding.
  - Electrical overstress can also be due to high voltage, sufficient to damage wire insulation or arc across relay contacts.

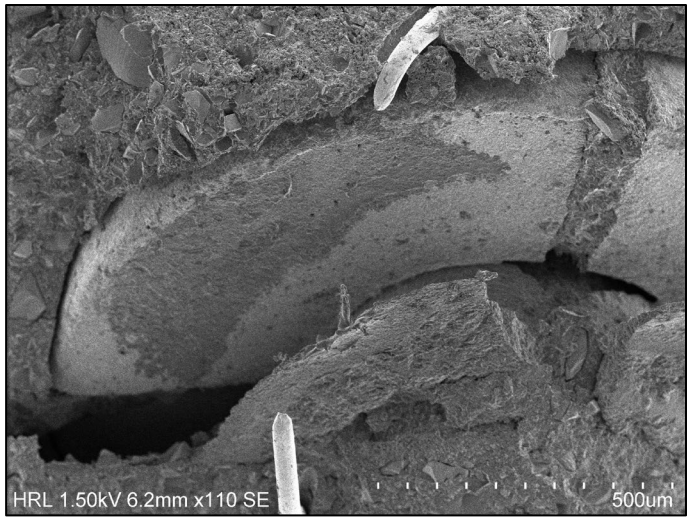




Magnetics

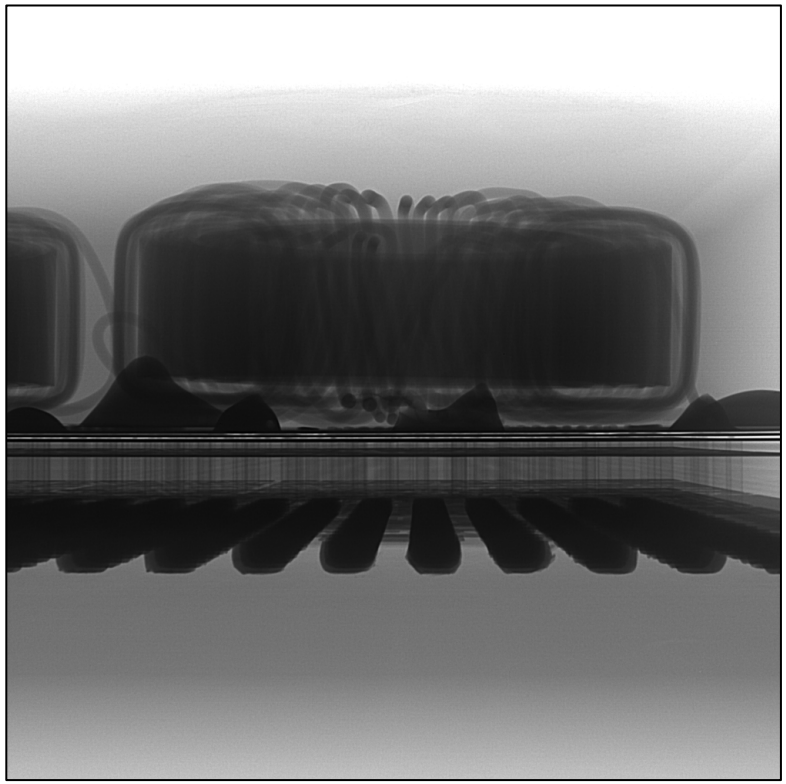
- Wire corrosion/fractures
  - As most magnetic components contain copper magnet wire, any uninsulated areas are prone to corrosion, especially where the wires are soldered to the leads.
  - Wire fractures due to tensile overload or fatigue are also common failure mechanisms, as is stress corrosion fracturing.





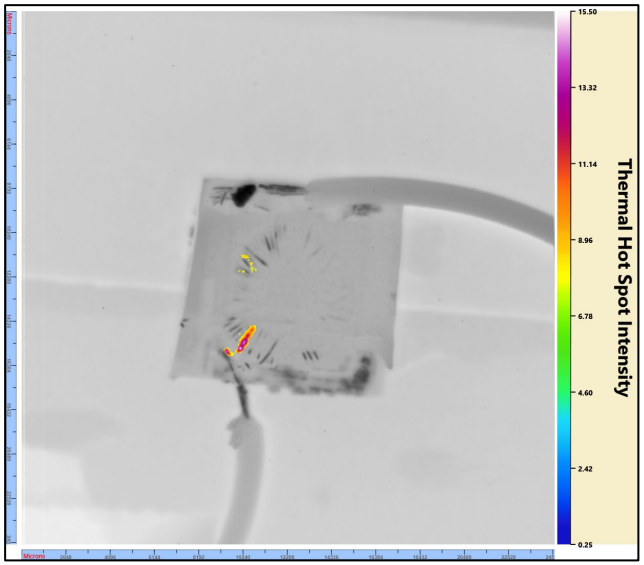
Transformer Failure Analysis - Example

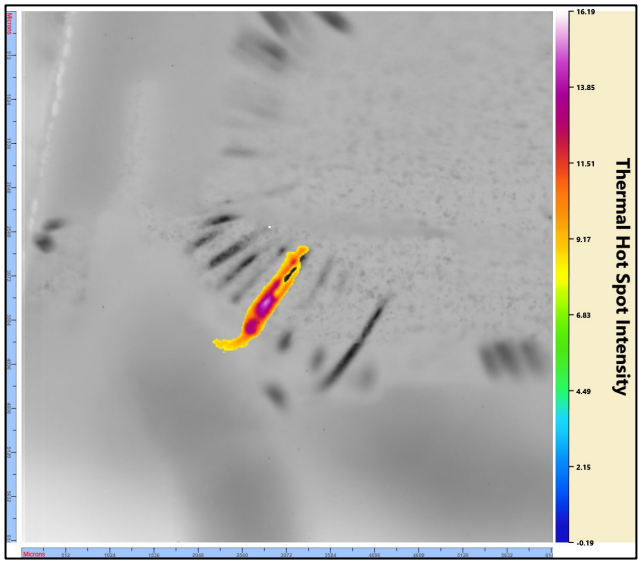
- A potted BGA module exhibited a <1Ω short circuit between two pads, and it was suspected that the failure was due to a short circuit in a transformer.
  - The challenge with short-circuited transformers is that the failure is due to an insulation breakdown, but most chemical depotting methods compromise the insulation.
- Non-destructive analysis included scanning acoustic microscopy, 2D real-time X-Ray and CT analysis, initially all inconclusive.



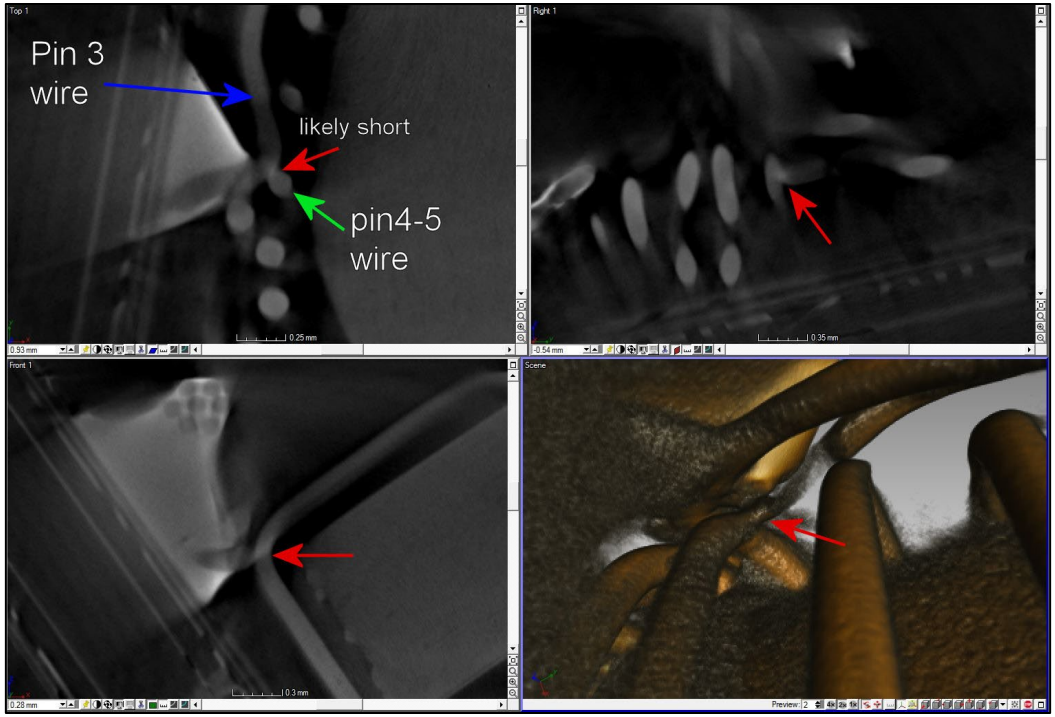
Transformer Failure Analysis - Example

- After additional testing and failure isolation, the transformer was removed from the module and partially depotted using laser ablation, allowing failure localization with IR hot spot detection.
- The short circuit was isolated to one winding, allowing more detailed inspection of that area via CT.





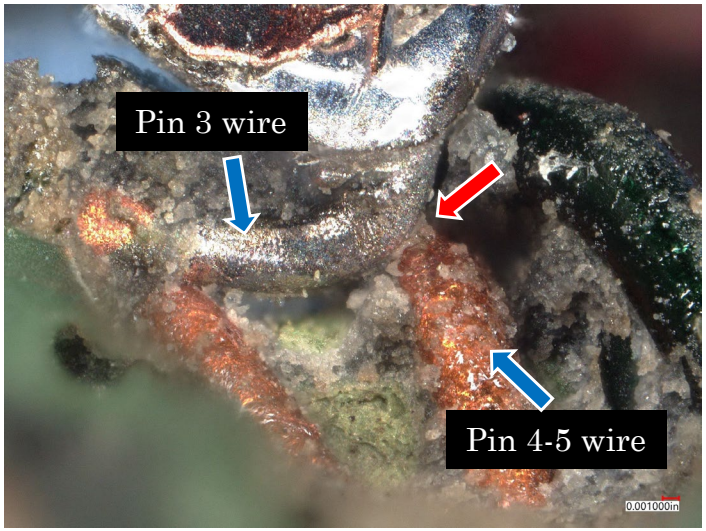
Transformer Failure Analysis - Example

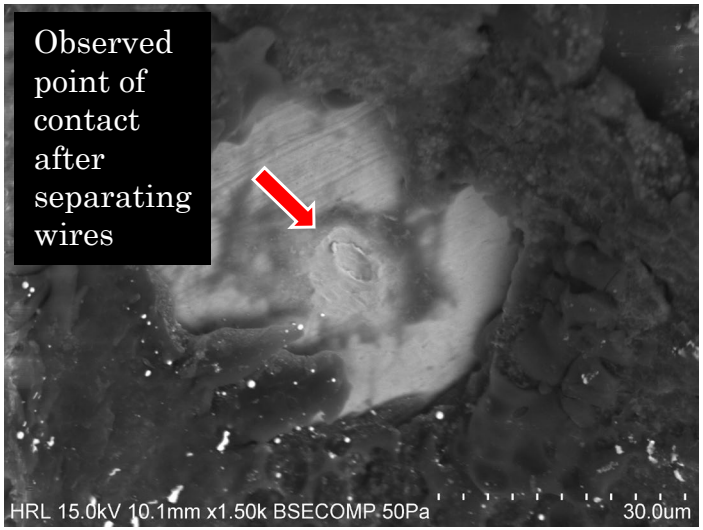


Detailed CT examination of the area indicated by IR hot spot detection revealed a single location where two wires from opposing windings made possible contact, tucked behind the solder joint on the substrate.

Now, instead of decapsulating the entire transformer we could target the area and uncover with laser ablation.

Transformer Failure Analysis - Example

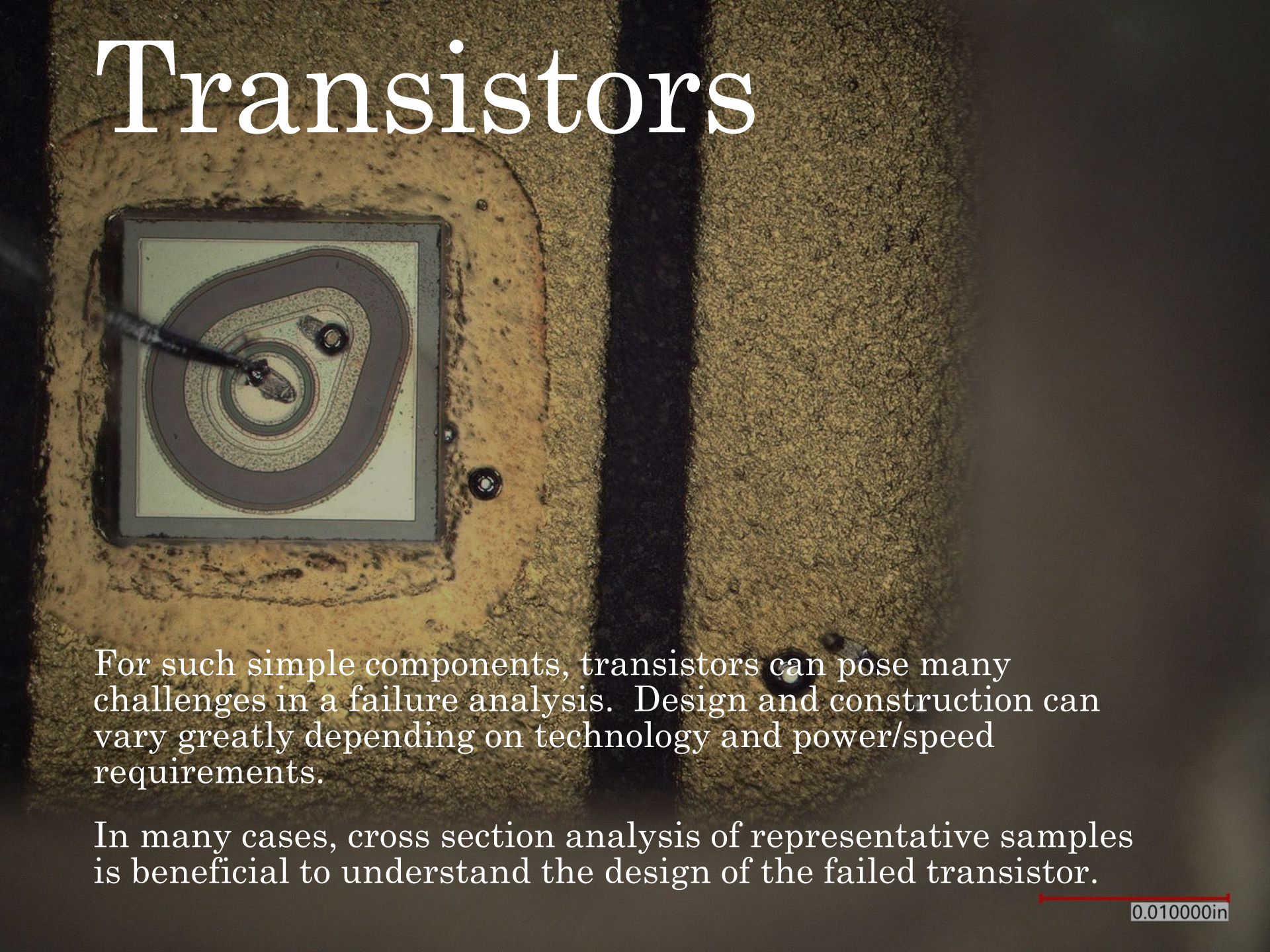




Laser ablation was successful in sufficiently uncovering the area of interest, revealing the failure site (upper left). The wires were separated, and subsequent inspection identified a breakdown of the wire insulation due to abrasion (upper right).

Note that the pin 3 wire is not insulated at that location due to the proximity of the solder pad.

Transistors



For such simple components, transistors can pose many challenges in a failure analysis. Design and construction can vary greatly depending on technology and power/speed requirements.

In many cases, cross section analysis of representative samples is beneficial to understand the design of the failed transistor.

Transistors

Construction – Basic BJT

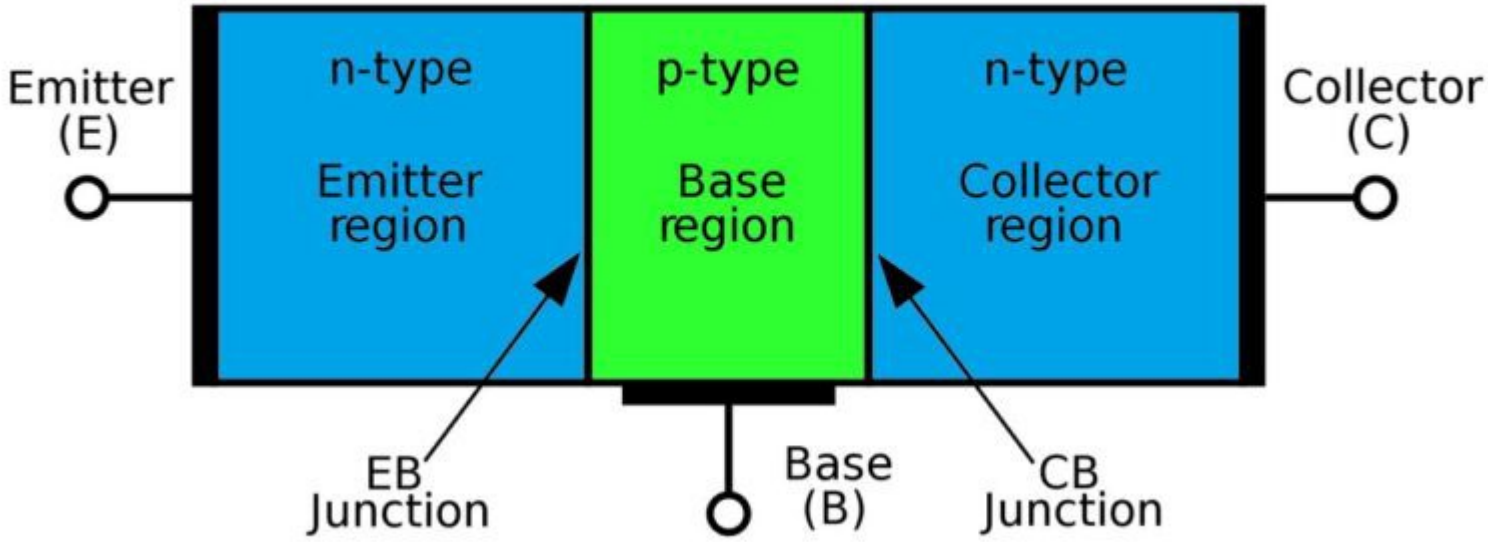
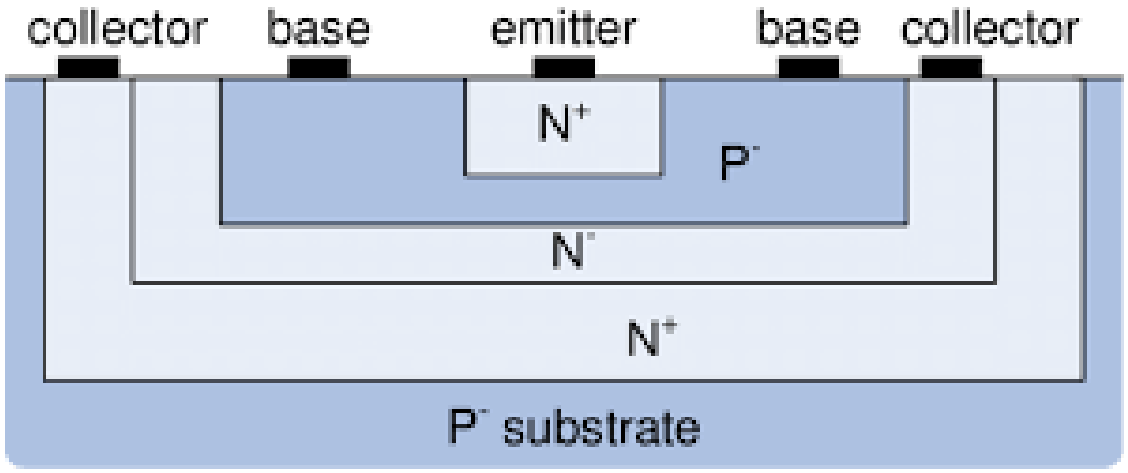


Image from hackatronic.com

Transistors

Construction – Basic BJT



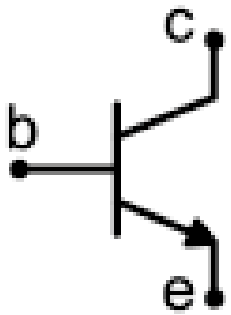


Image from researchgate.com

Transistors

Construction – Typical NPN BJT

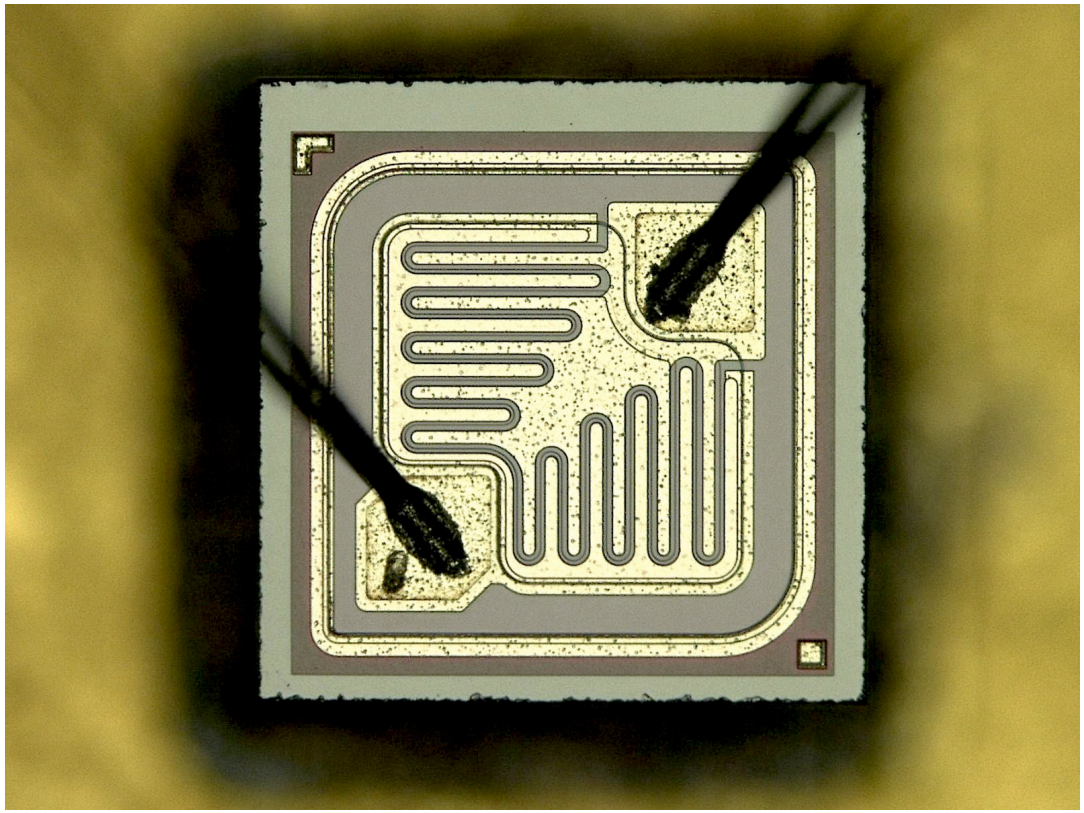


Image from hackatronic.com

Transistors

Construction – Integrated BJT

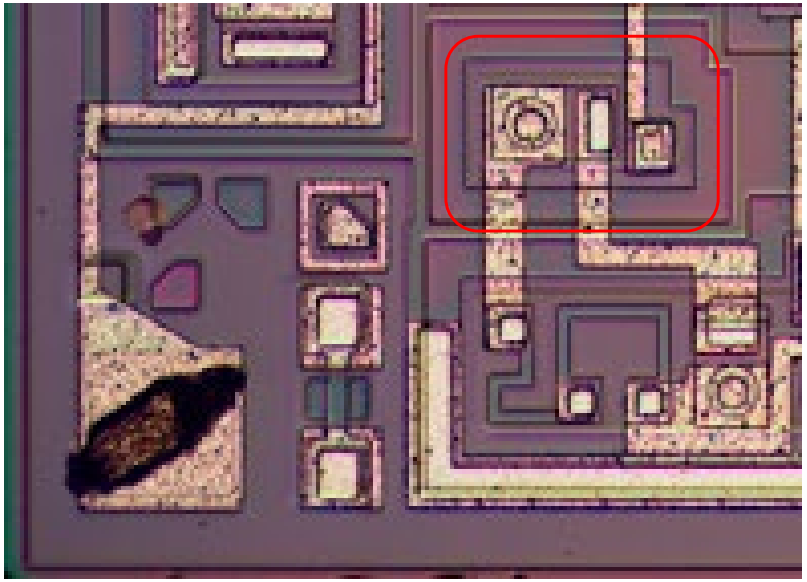


Image from righto.com

Transistors

Construction – Basic MOSFET

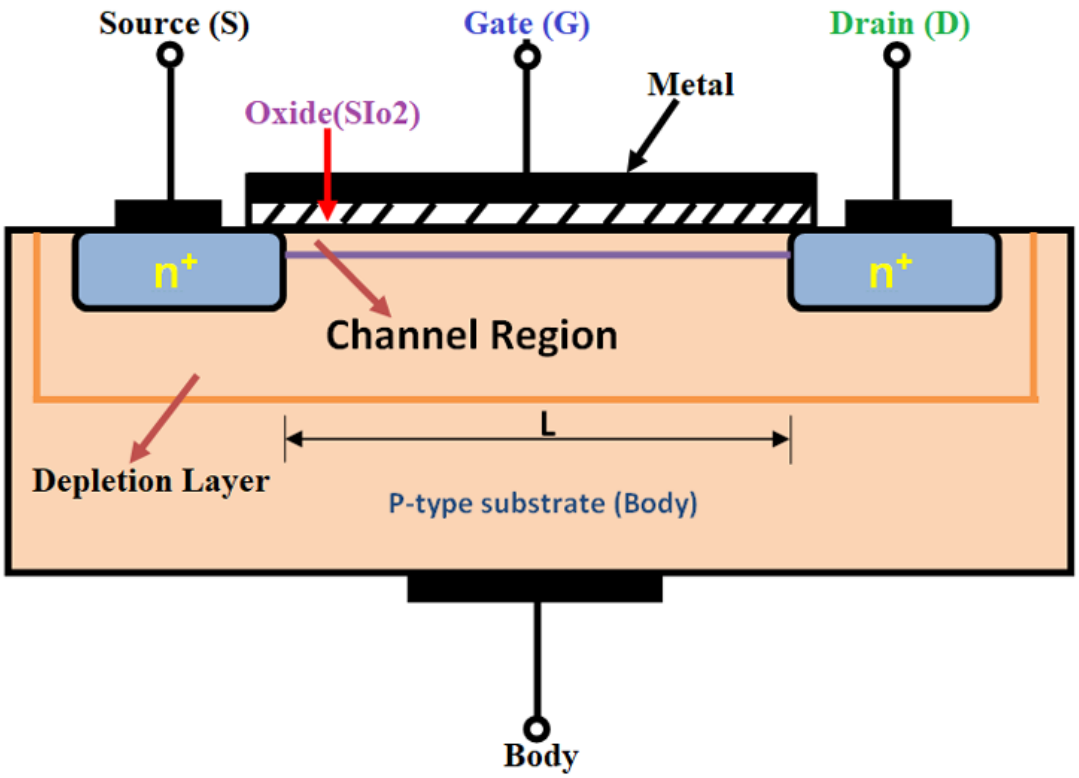


Image from zerotoasiccourse.com

Transistors

Construction – Basic MOSFET

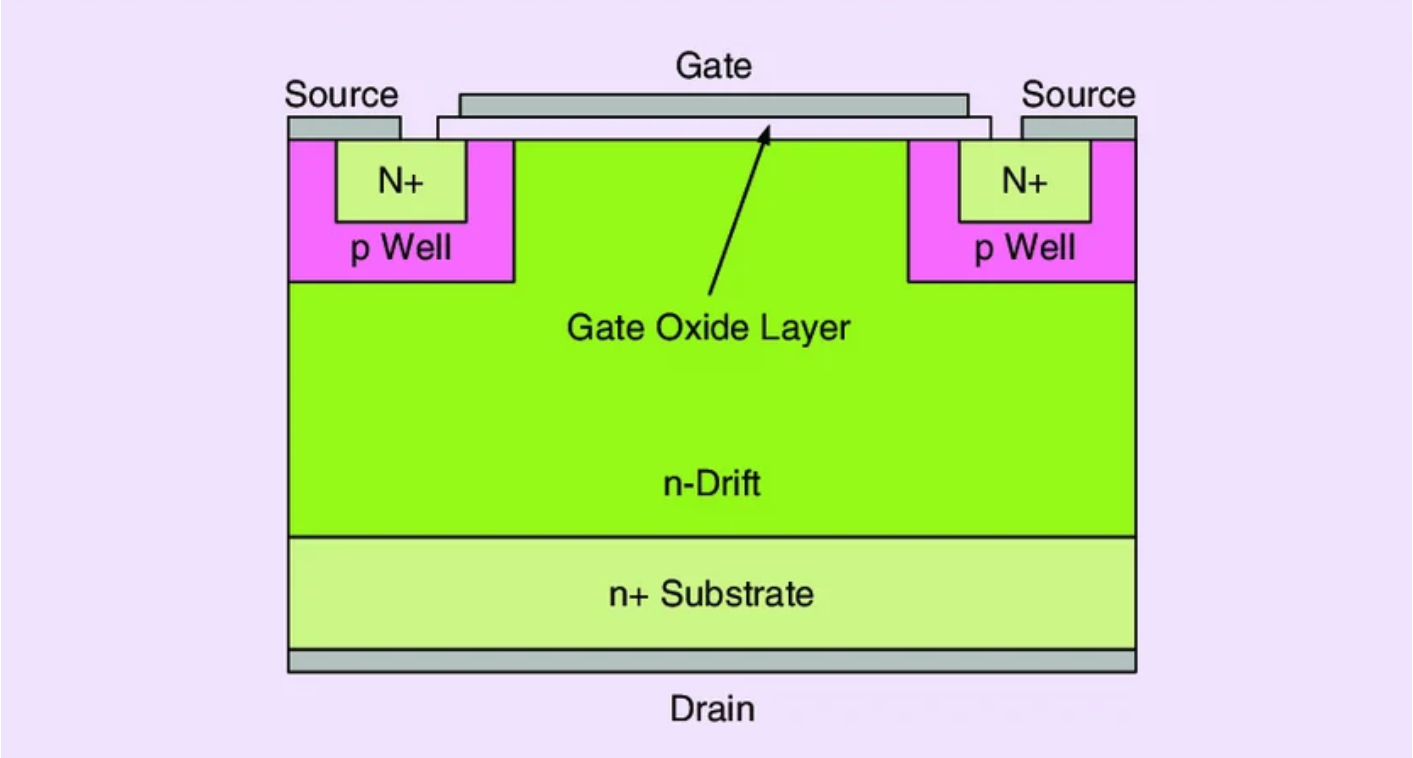


Image from researchgate.net

Transistors

Construction – Power MOSFET

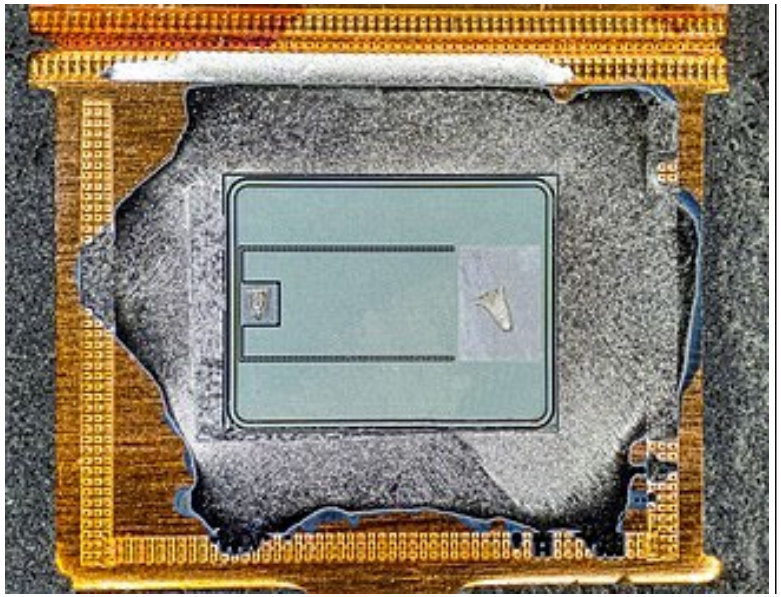


Image from wikipedia.org

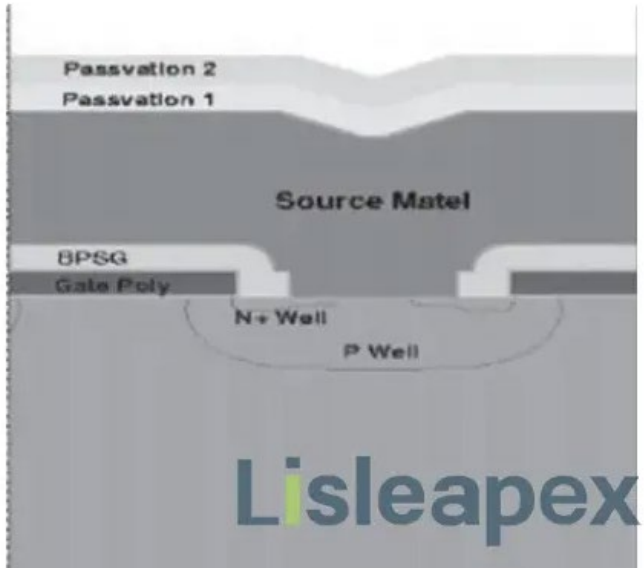
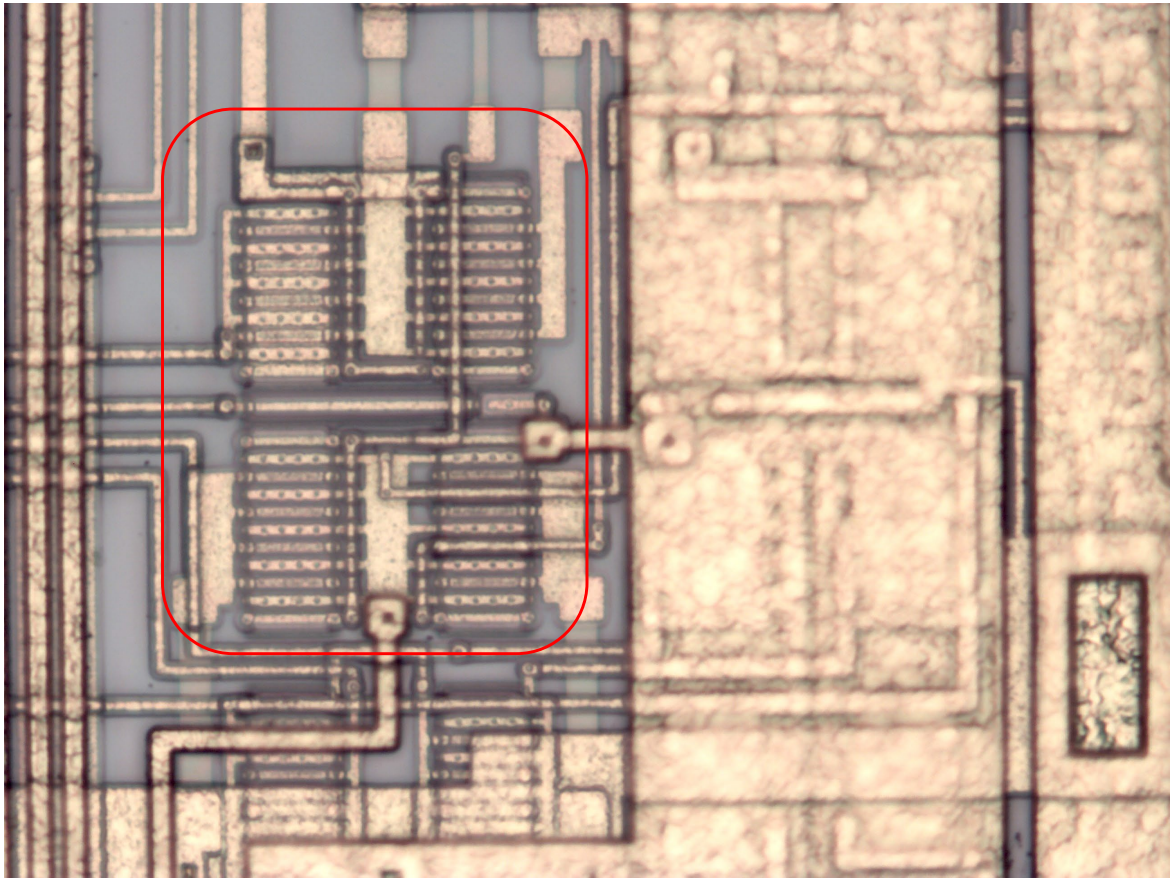


Image from lisleapex.com

Transistors

Construction – Integrated MOSFET

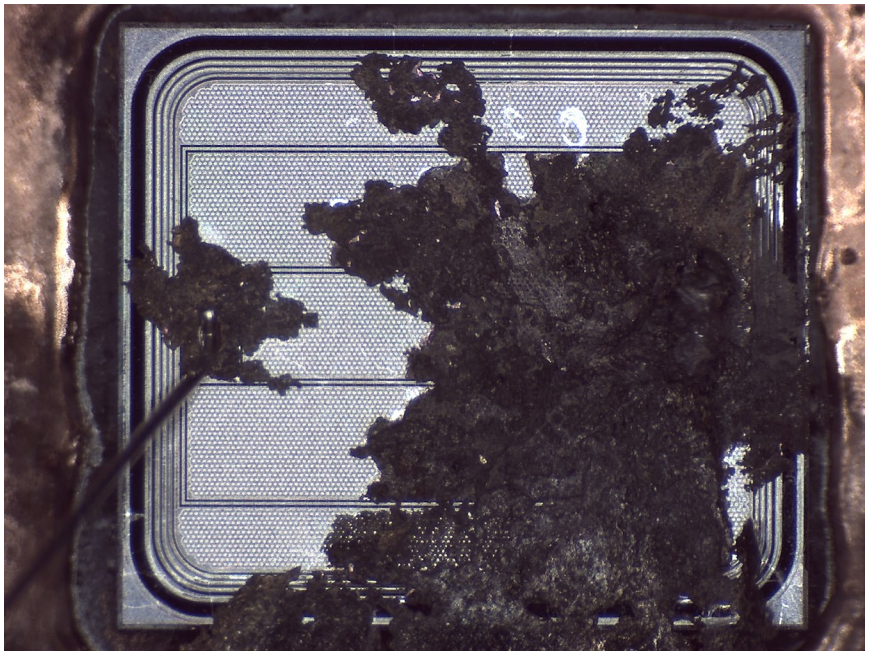


Transistors

- Transistor failure modes typically include:
  - Current leakage between terminals
  - Short circuited conditions
  - Open circuited terminals
  - Low-gain
- Each one of the above can be due to several mechanisms, but the electrical data can offer clues.
  - When current leakage is observed, testing over temperature (within the temperature limits of the DUT) is advisable.
    - 100uA or less current limiting is advisable during this testing.
    - Testing with an analog curve tracer such as a Tektronix 576 is also recommended to observe subtle fluctuations that may be missed with digital voltage sweeps. These fluctuations can be indicative of fracturing or dendritic growth.
  - Short circuits should have their resistances accurately measured as the resistance of a short correlates with the likely causes of damage.
  - Open circuits should be tested over temperature to test for any intermittent connections.
  - Care should be taken when measuring gain, as the gain parameter generally requires higher test currents and data can be destroyed.

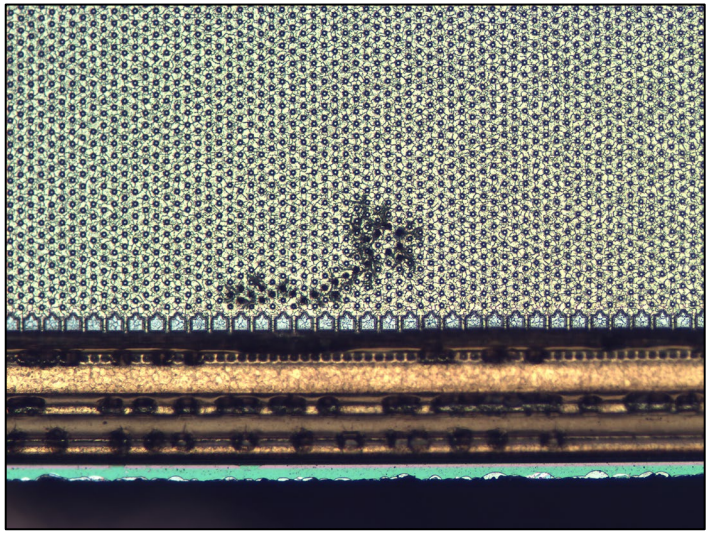
Transistors

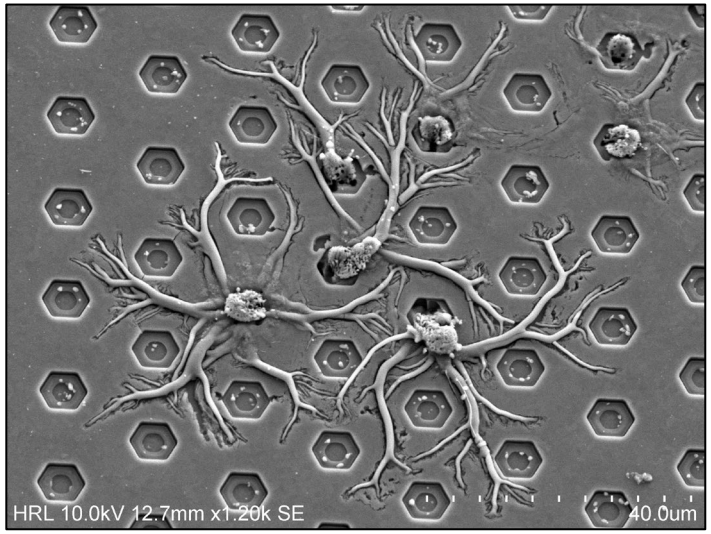
- Electrical overstress
  - Transistor failure analysis often results in EOS as the cause, or most probable cause of failure.
  - Sometimes interpreted as a “catch-all” conclusion, but there can be a lot of information depending on the characteristics of the observed damage.
  - Other times, as shown to the right, the damage is so severe that all evidence of the failure initiation has been destroyed.



Transistors

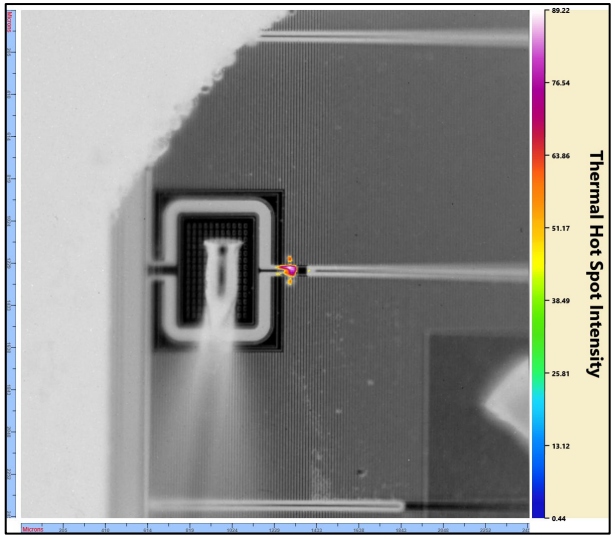
- Electrical overstress
  - High-speed voltage transients in switching circuits are expected and transient suppression is a standard part of circuit design.
  - In some instances, abnormal current draw on the circuit output can result in voltage transients in excess of what is expected, leading to the breakdown of the transistor junctions and short circuiting of the device.
  - The images below show examples of inductive “kickback” transients from a controlled experiment. Normally, these initiation sites become larger alloy sites when power continues to be applied after failure.

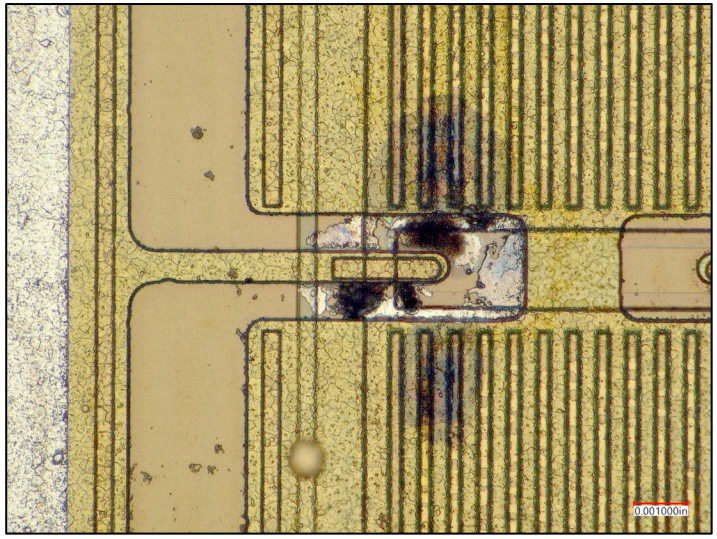




Transistors

- Electrical overstress
  - Gate damage is also a common result of electrical overstress. The gate structures in FETs are sensitive to over-voltage conditions, but are generally protected by a gate-driver microcircuit.
  - The failure mode is typically a resistive short circuit from the gate to source/drain, with a resistance lower than the source-drain (if the source-drain is involved).
  - Gross EOS of the gate, shown below, is usually obvious once the transistor die is exposed.
    - One of the key differentiators between EOS and ESD.



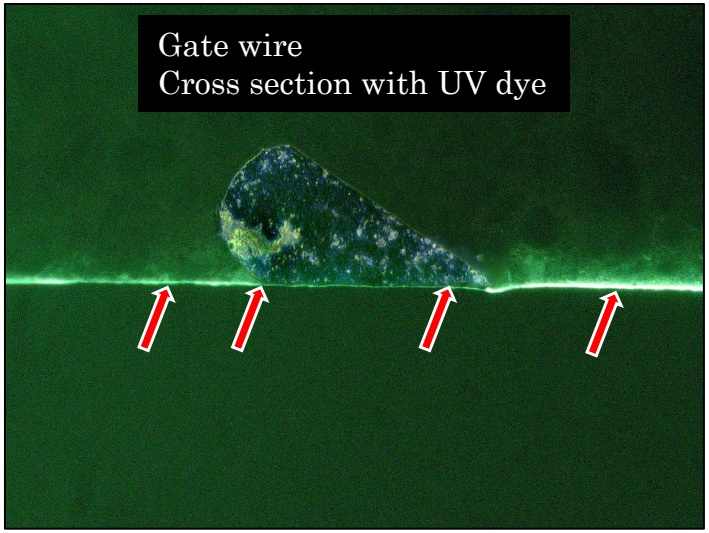


Transistors

- Electrical overstress
  - Failure due to excessive power dissipation can be the result of several initiators and can be difficult to determine the true cause. Common mechanisms can include:
    - High on-state current in excess of the specified rating
    - Inadequate heat sinking of power-devices
    - Linear-mode operation/operation outside of the specified SOA
      - Can be due to an open circuited gate or insufficient gate drive.
  - The damage is obvious and can sometimes be detected during radiographic inspection.
  - The resistance of the short circuit is often very low; <1Ω.

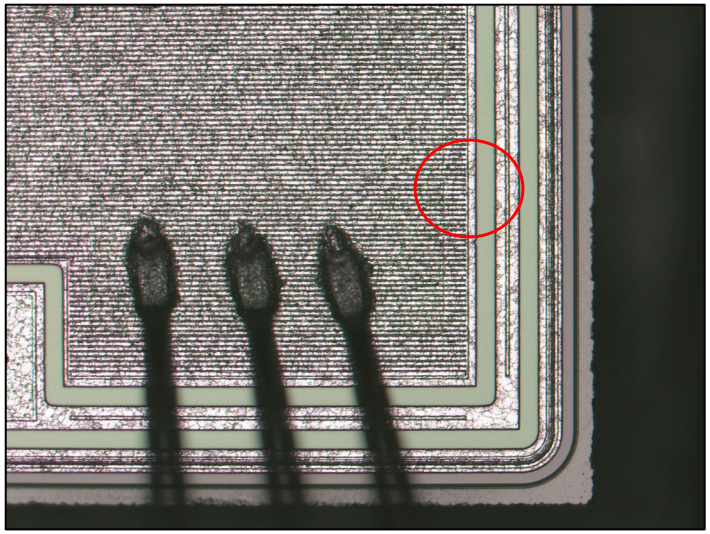
Transistors

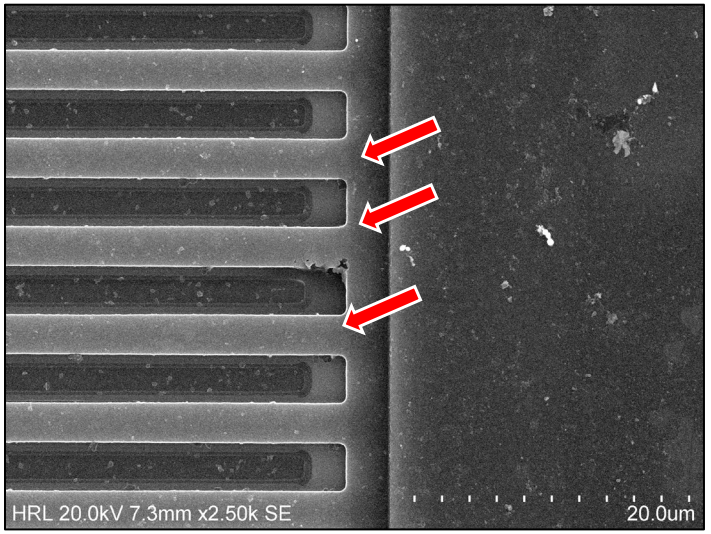
- Open gate – delaminations
  - In FETs, an open circuit at the gate results in a floating gate condition, which generally leads to the destruction of the transistor as it operates in the linear mode.
  - This can occur due to any failure in the gate drive circuit, but is also observed in the transistor itself when lead-frame delamination occurs, pulling the more fragile gate wire from the lead.
  - Scanning acoustic microscopy can identify lead-frame delamination, but beware of water ingress which can result in “false negatives”.



Transistors

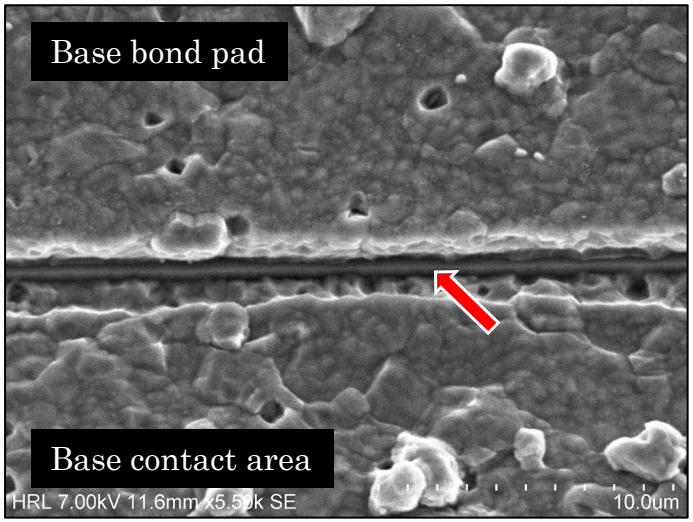
- ESD
  - The gates of FETs are very sensitive to ESD
  - Failures typically present as several 100Ω – kΩ resistive short circuits
  - Damage is often too small to see with optical microscopy, and is often beneath metal layers
  - Failure localization is almost always required, followed by deprocessing of the die layers and SEM inspection.
  - Below image on the left shows no apparent failure site, but ESD damage was discovered beneath the source metal at the edge of the gate fingers.

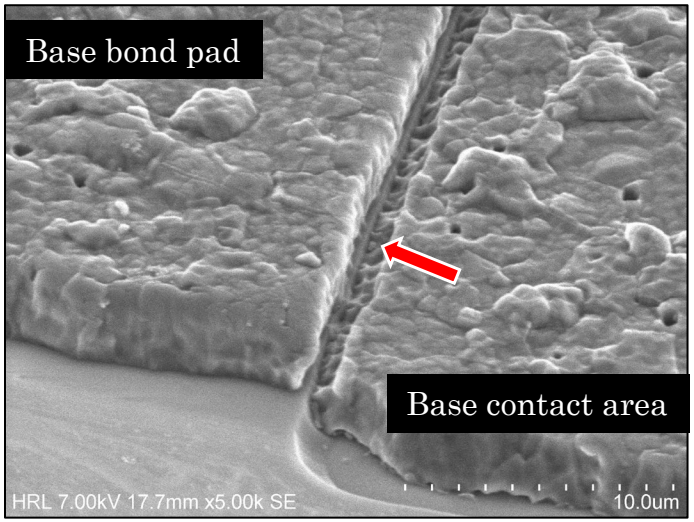




Transistor Failure Analysis - Example

- A transistor had reportedly failed with a temperature sensitive “open circuit”.
- Testing at Hi-Rel confirmed an intermittent open circuit on one of the base pins.
  - This data suggests an open circuit due to a failing bond or *possibly* corrosion of the die metallization, but we will keep an open mind.
  - Steps were taken to analyze these areas, but neither bond failure or corrosion was noted.

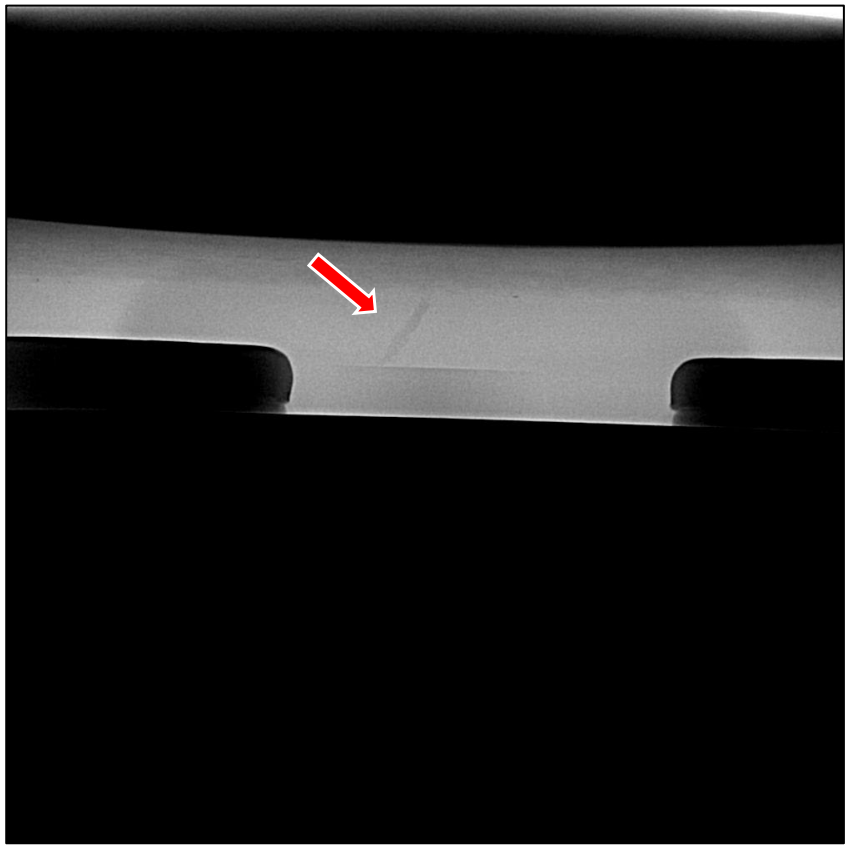




- Detailed SEM inspection revealed a step coverage defect creating an open circuit between the base bond pad and the base contact area.

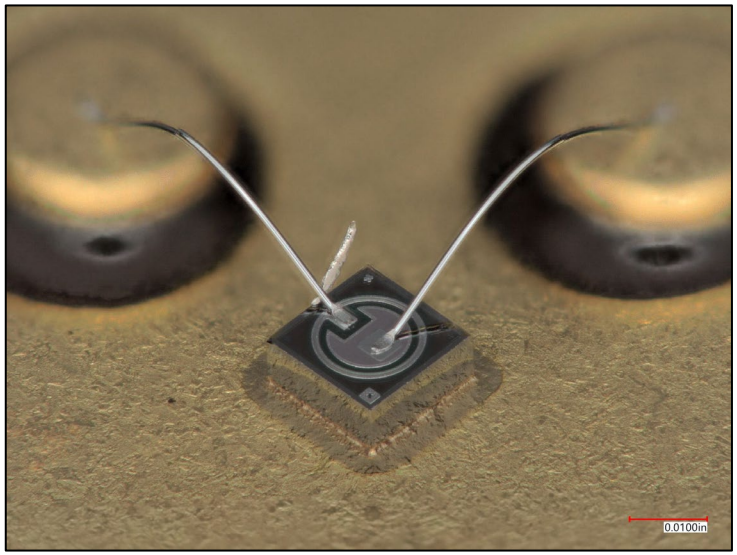
Transistor Failure Analysis - Example

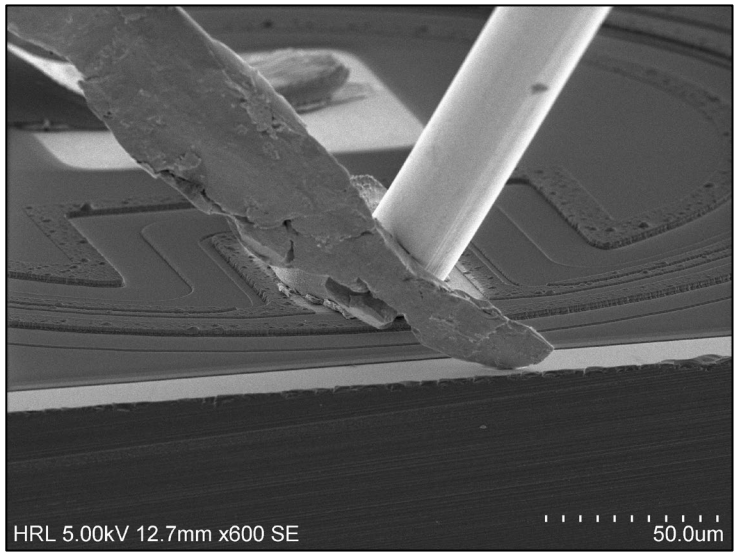
- A metal can “TO” style transistor failed with a short circuit between the base and collector.
  - A base-collector short circuit is a very common failure mode in transistors, but there are many different mechanisms that can cause the failure.
  - This failure resulted in a 14Ω short circuit, and initial radiographic inspection while the component was in-circuit revealed no anomalies.
  - Since metal can packages have a very long history (since the 60s) of potential nickel flakes, radiographic inspection was reperformed after removal of the component from the PCBA with low kV and high contrast.
    - A nickel flake was identified, bridging the base wire to the non-passivated die edge; the collector.



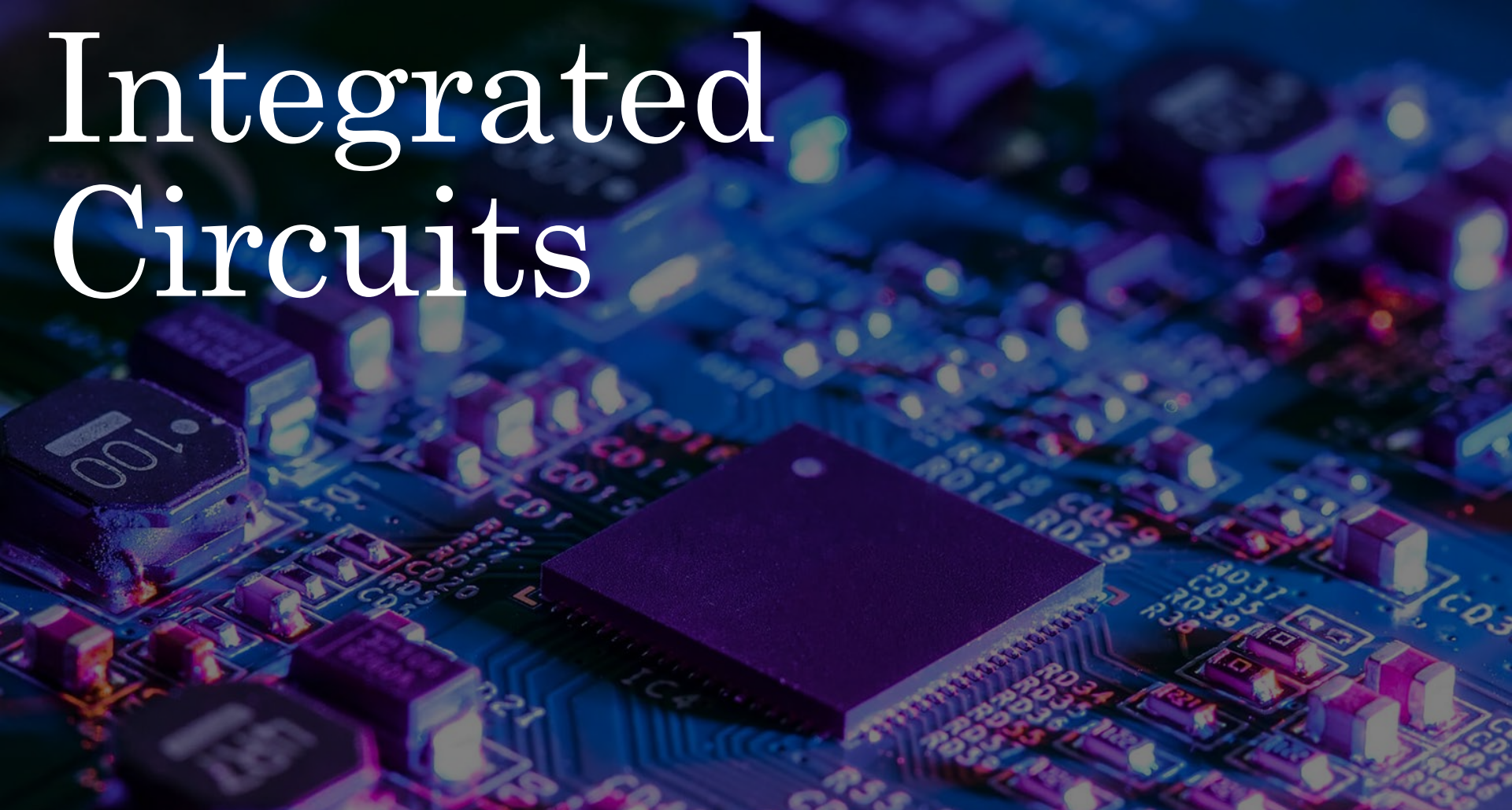
Transistor Failure Analysis - Example

- Nickel flakes have resulted in failures for decades
  - They can remain adhered to the internal surfaces of the packages, eventually dislodging.
  - Radiographic inspection and PIND are often not able to detect nickel flakes due to their low density.
- Hi-Rel continues to perform nickel flake inspections on metal lidded components to confirm that no process changes have occurred that may result in nickel flakes.





Integrated Circuits



Integrated circuits can fail due to nearly any of the previously discussed mechanisms. Because of this, failure history and supporting information is valuable for the analysis. Depending on your lab capabilities, testing and failure localization may be a challenge.

https://www.waferworld.com/post/what-are-the-components-of-an-integrated-circuit

Integrated Circuits

- Once board-level defects/damage are ruled out, the challenge with IC failure analysis is failure isolation/localization.
  - The failure analysis approach, *in most cases*, relies on isolating the failure to specific pin, or combination of pins.
  - If a component fails functional testing but exhibits no pin-pin degradation, the complexity of the analysis dramatically increases.
    - In some cases, failure analysis from the component manufacturer may be recommended as they have the capability to analyze devices during full functional testing.

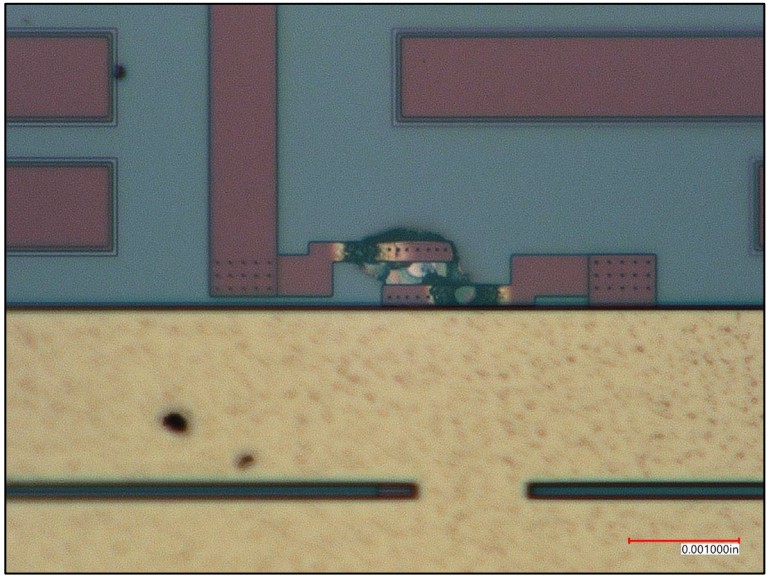
Integrated Circuits

- Comparison testing can be performed between a suspect sample and a known functional sample.
  - Automatic curve tracing is preferred, but not always possible due to package style or condition.
  - Manual curve tracer comparison can be performed
  - Ohmmeter testing can determine if short circuits or open circuits exist, but does not always revealed more subtle degradations.
    - I/V curve characteristics are significant clues in FA.
- After failure verification and isolation, the component can be analyzed in a manner similar to other part types, where all methods may be applicable.

Integrated Circuits

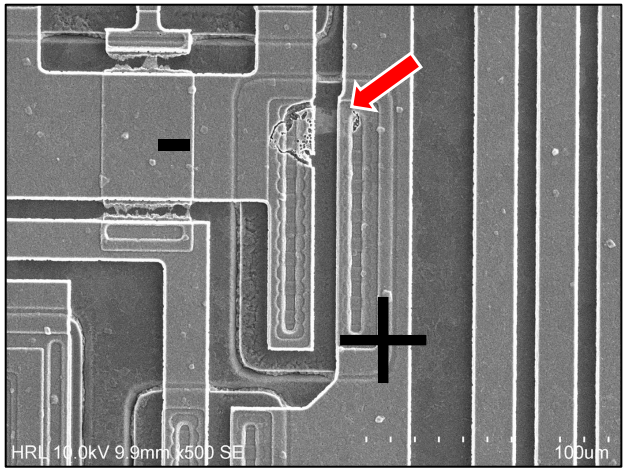
- Electrical overstress
  - Similar to the previous discussion of EOS in passive components, EOS can occur in integrated circuits and, depending on severity of the damage, can prevent a definitive determination of the original cause of failure.
    - The cause of less catastrophic EOS can be determined in most cases.
    - Voltage transients, high current conditions, polarity of failure condition can often be estimated/determined.

In the image to the right, EOS was identified as the cause of failure. The failure was the result of high current, less than the fusing current of the 1mil gold wire, ~1.5A. No evidence of arcing or breakdown was discovered, indicating the failure was strictly due to a high current condition.

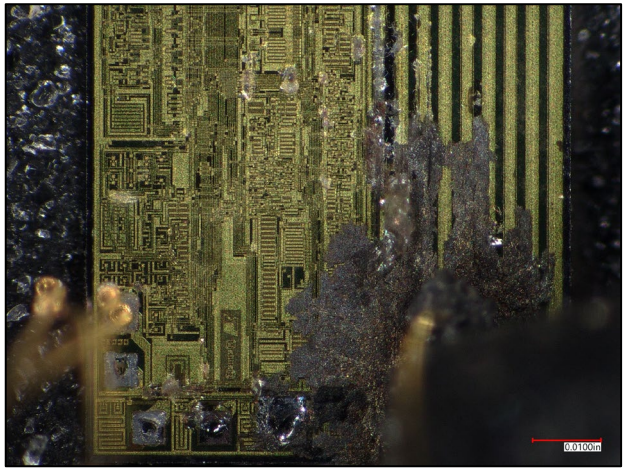


Integrated Circuits

In the image to the right, an overvoltage condition occurred resulting in the failure of the diode structure. The migration of the metal in this image follows the electron flow, so it could be determined that the area to the left was more negative.

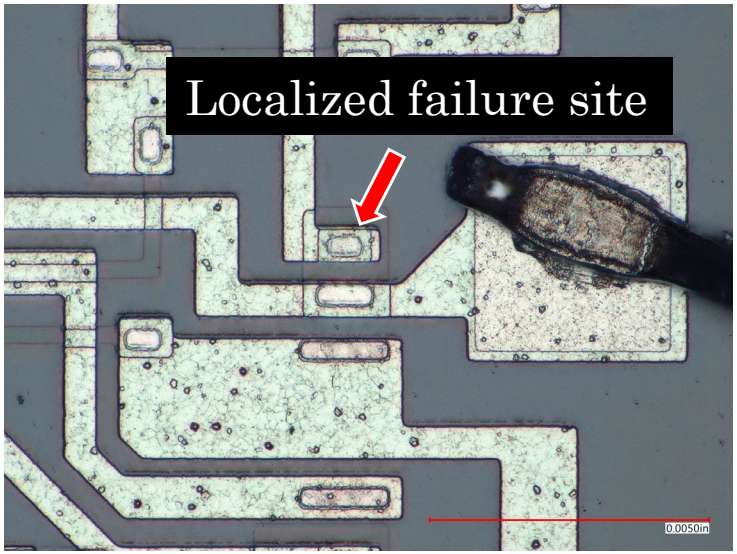


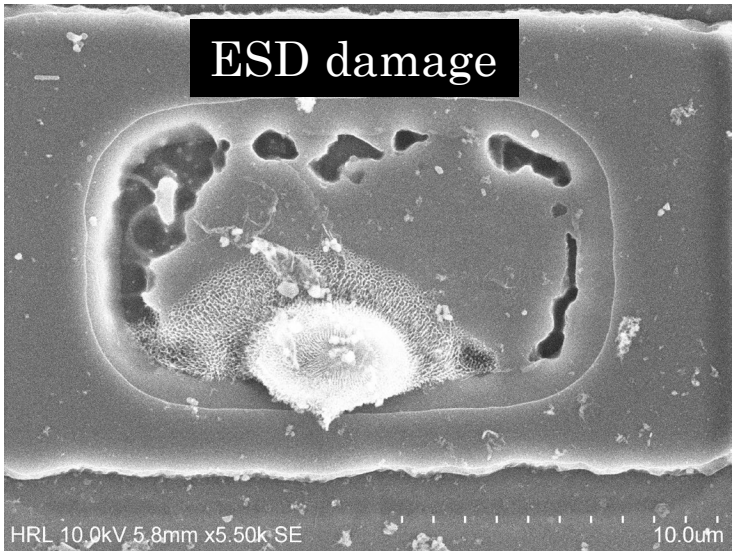
In the image to the right, the extent of damage was too severe to determine the true cause of failure. The root cause could only be speculated based on the severity of the damage in the output transistor.



Integrated Circuits

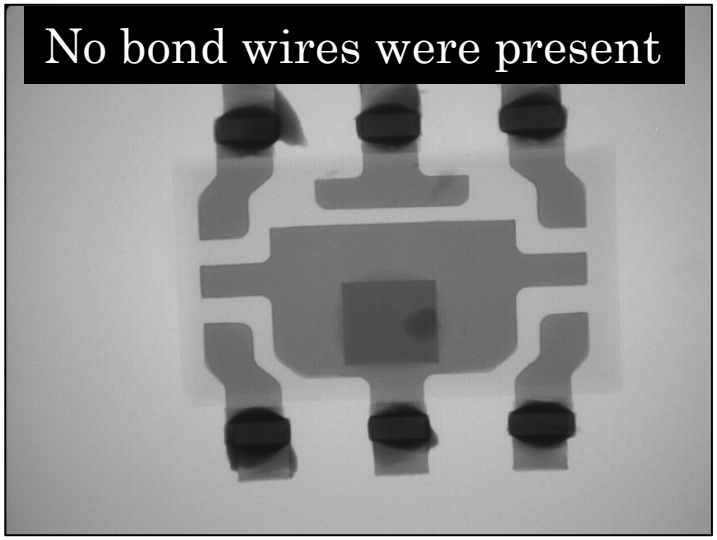
- Electrostatic Discharge
  - Integrated circuits can be very sensitive to damage from ESD.
  - ESD failures generally result in relatively high resistive short circuits or degraded PN junction in the sensitive I/O structures
  - Damage from ESD is typically not obvious during optical microscope inspection, requiring failure localization and delayering.





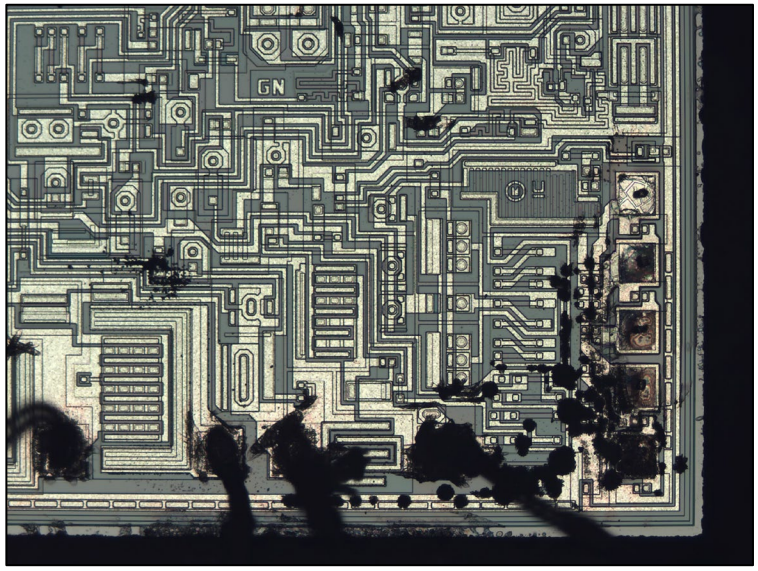
Integrated Circuits

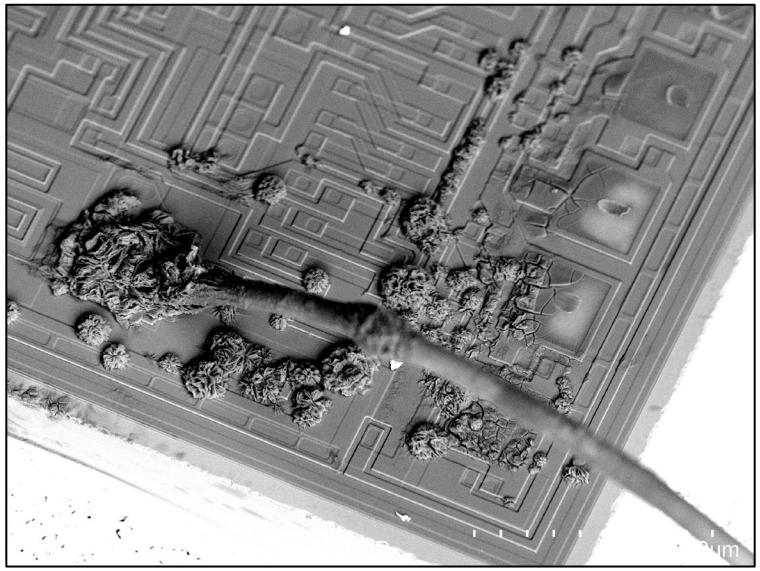
- Counterfeit components have been a problem in the electronics industry for many years. With recent supply chain shortages, some companies have been forced to procure components from less reliable sources.
- Counterfeit detection is performed by comparing the construction of each aspect of a device to a known good sample.
  - This includes part markings, dimensions, lead frame structure, test data, die layout and markings, etc.



Integrated Circuits

- Corrosion
  - Die metallization corrosion can occur when the hermeticity of the package is compromised.
    - In some rarer cases the corrosive material can be induced during manufacturing, prior to sealing the component.
  - The failure presents as open circuited metallization, which can appear as a complete open circuit or an abnormal I/V curve.



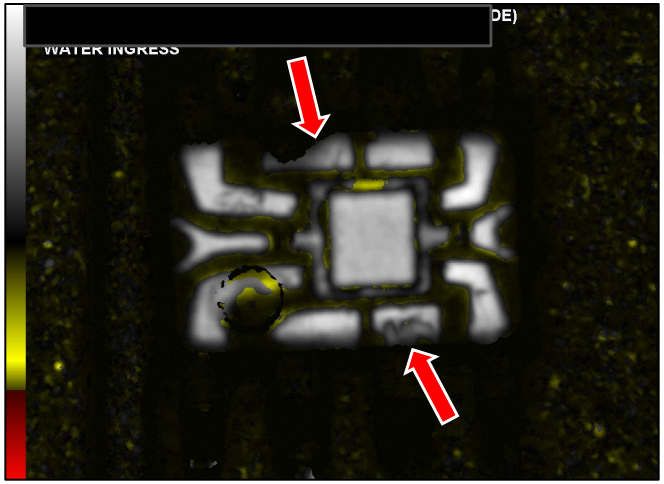


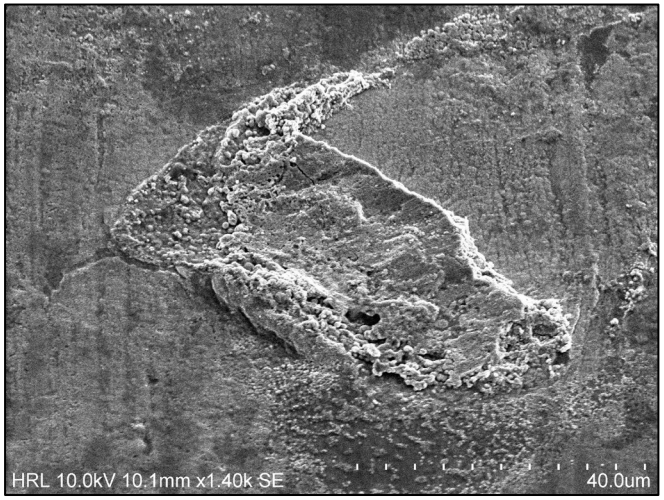
Integrated Circuits

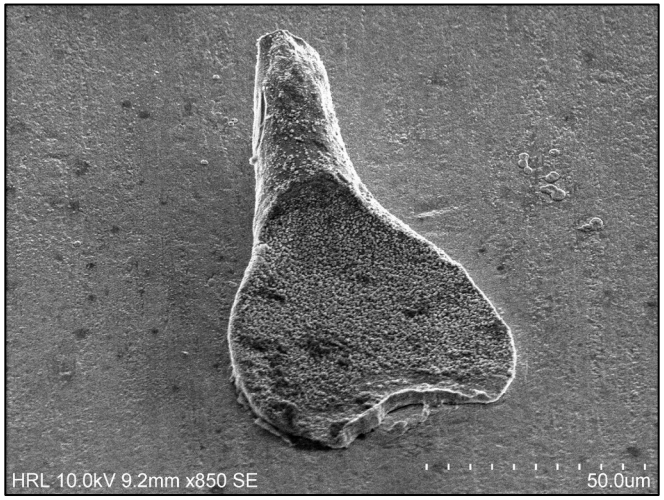
- Copper wire corrosion
  - As copper bond wires become more common than gold wires in plastic components, there are some drawbacks that need to be considered.
  - The most susceptible area of a copper wire in terms of corrosion is the lead-frame bond.
  - Hi-Rel has analyzed numerous plastic components that present an open circuit, sometimes intermittently.
  - Detailed radiographic inspection of the bonds can sometimes be inconclusive.
  - The failure is ultimately due to delamination of the potting material from the lead frame surface, and as such, scanning acoustic microscopy is recommended when copper wire corrosion is suspected.
    - As previously discussed, beware of water ingress masking delamination.
  - The wires corrode as a result of contamination becoming trapped in the delaminated interface.
    - Gold wires were not susceptible to corrosion even when delamination was present.
    - In some cases, a galvanic cell is formed from the dissimilar metals, accelerating the corrosion.

Integrated Circuits

These images show water ingress into the delaminated interface (upper right), a corroded copper stitch bond (lower left), and an intact bond showing the normal appearance (lower right).



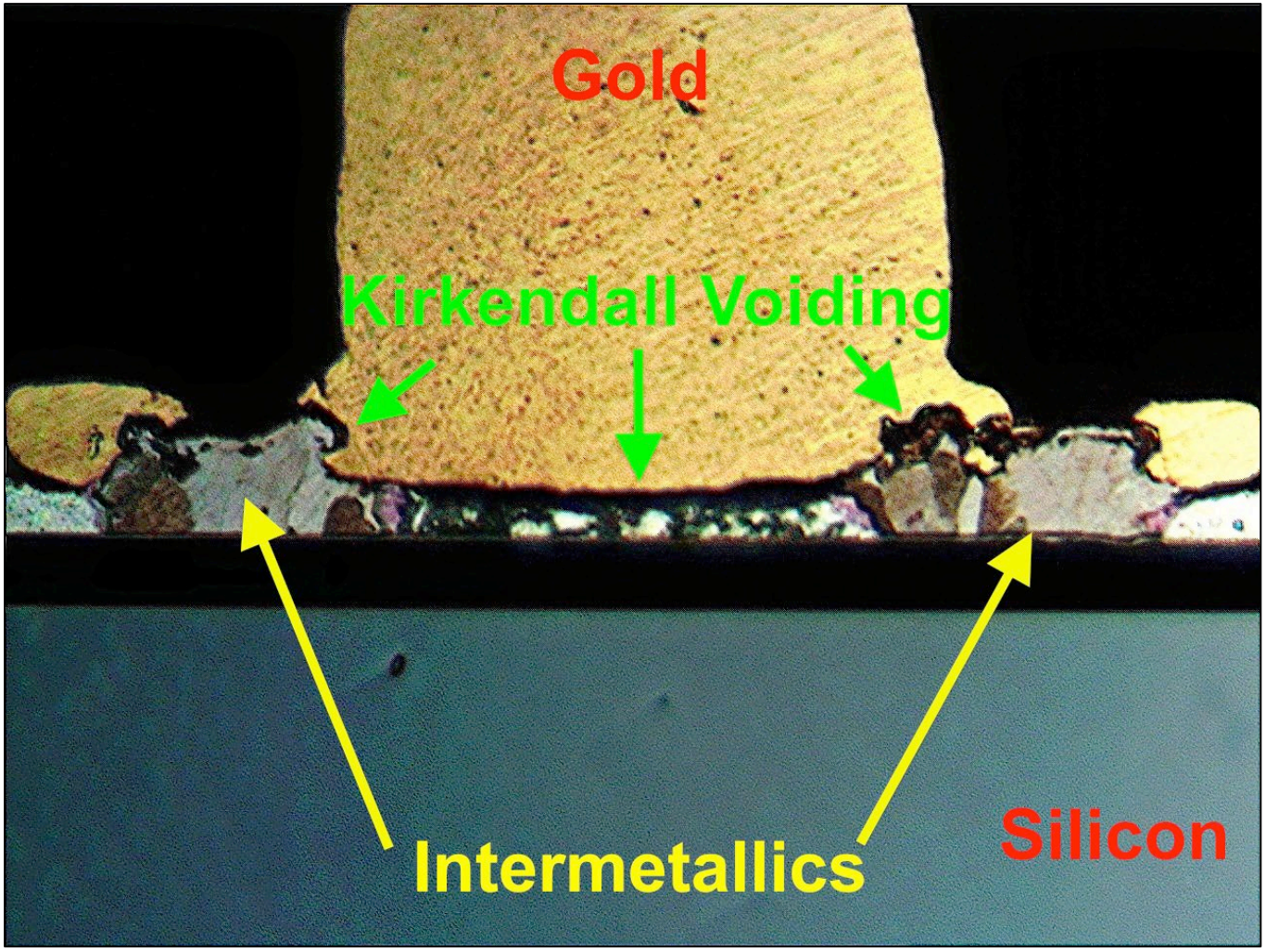




Integrated Circuits

- Kirkendall Voiding
  - When gold wires are bonded to an aluminum surface, or vice versa, a gold-aluminum intermetallic is created. The formation of this intermetallic region is normal, and indicative of a quality bond.
  - With time and temperature, the intermetallic region can grow due to the different growth rate of the various alloys in the bond.
  - Eventually voiding occurs at the interface between the AuAl intermetallics and the pure gold of the ball bond, leading to a bond failure.
    - Electrically, this can result in a resistive connection or an open circuit.
  - Bond pad contamination, typically oxidation, results in a lower reaction area during bonding and introduces impurities into the bond, which can become nucleation sites for voiding and accelerates the failure of the bond.
  - Identifying failures due to Kirkendall voiding can sometimes require testing over temperature to reveal the temperature sensitive bond lifts.

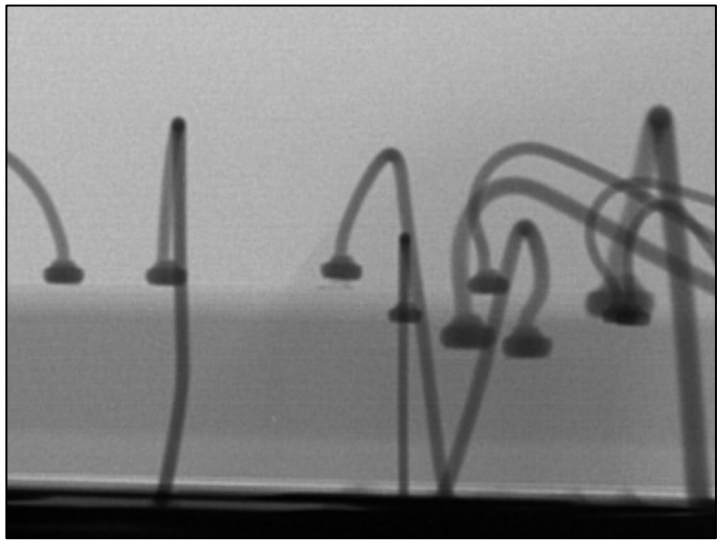
Integrated Circuits

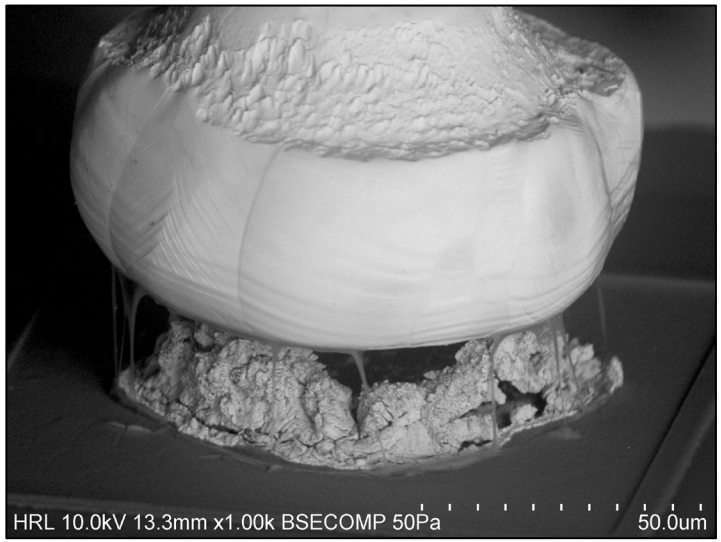


Integrated Circuits

The below images show a gold ball bond that failed due to Kirkendall voiding. The radiographic inspection (left) revealed a lifted ball bond with some gold remnants on the die surface, a classic indicator of this failure mechanism. The SEM image (right) revealed the lifted ball bond, resulting in the open circuit.

This component was in service for nearly 20 years.





Conclusion

- This presentation is intended as a brief overview of component failure analysis. Each component type can present its own unique challenges and there are always surprises.
- We at Hi-Rel love discussing failure analysis and are more than happy to help with any questions you or your team may have.