High-throughput Additive Manufacturing of Microelectronics including Passive and Active Components for 3D HI, Legacy Electronics and Advanced Packaging

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Abstract

We introduce a new high throughput and scalable technique to additively manufacture nano and microelectronics. The technique eliminates etching, vacuum deposition, and other chemically intensive processing by utilizing direct assembly of nanoscale particles or other nanomaterials at room temperature and atmospheric pressure onto an interposer, wafer, or board. The presented technology enables the printing of crystalline conductors and semiconductors. The technology enables the additive manufacturing of passive and active components including logic gates at the nano and microscale using a purely additive (directed assembly enabled) process utilizing inorganic semiconductors, metals, and dielectrics nanoparticles. The process demonstrates the manufacturing of transistors with an on/off ratio greater than 10^6. This new technology enables the fabrication of nanoelectronics and electronic components while reducing the cost by 10-100 times and can print 1000 faster and 1000 smaller (down to 25nm) structures than ink-jet-based printing. Results showing passive and active components will demonstrate high-throughput printing of interconnects and circuit components at a scale equal to or less than 2 microns. Fully additively manufactured capacitors printed on silicon and sapphire substrates will be presented. The results will show printed capacitors ranging in size from millimeters down to 20 x 20 μm with capacitance of femto Farad to nano Farads. The results will show additively printed logic gates such as NAND and MOSFET with high on/off ratios. This new Fab-in-a-Box platform is designed to print electronics and products with minimum features down to 300 nm for making custom legacy electronics as well as other advanced packaging applications.

Biography: Ahmed A. Busnaina, Ph.D., is the founding Director of the National Science Foundation's Nanoscale Science and Engineering Center for High-rate Nanomanufacturing since 2004 and the NSF Center for Microcontamination Control at Northeastern University, Boston, MA, since 2002. He is also the founder and CTO of Nano OPS, Inc. since 2017. Prior to joining Northeastern University, he was a professor and a director of the Particulate Control Lab at Clarkson University from 1984-2000. Dr. Busnaina is internationally recognized for his work on semiconductor fabrication with an emphasis on yield. He also developed nano and microscale additive manufacturing for making interconnects, passive and active electronic components, LEDs, and sensors. He authored more than 600 papers in journals, proceedings, and conferences. He also has 25 granted and more than 45 pending patents. He was awarded the 2020 American Society of Mechanical Engineers (ASME) William T. Ennor Manufacturing Technology Award and Medal. He is a fellow of the National Academy of Inventors, a fellow of the American Society of Mechanical Engineers, and a Fulbright Senior Scholar. He is an editor of the Journal of Microelectronic Engineering. He also serves on many advisory boards, including Samsung Electronics, the Journal of Electronic Materials Letters, the Journal of Nanomaterials, and the Journal of Nanomanufacturing.