Die Solutions for Space Constrained Hybrid Applications

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For the past 25 years, the trend has continued toward smaller size, lower voltage and lower power rails. However, we now see an ongoing trend toward higher voltage capability and ever-increasing levels of power density. When space constraints are of the highest concern, hybrid designs and the use of chip scale devices has become a required solution.

New techniques in the wafer fabrication of discrete bare die structures has enabled higher levels of power density while at the same time reducing footprint and profile. Increasingly, industrial and aerospace and defense segments are moving away from traditional packaged solutions and turning to bare die structures for high reliability applications.

Traditionally, bare die usage was reserved for the unique talents and capabilities of specialized low volume hybrid assembly houses. Newer capabilities for the provision of bare die are now, however, facilitating the high-volume usage of bare die components. Hence, the hard line between packaged surface mount components and bare die structures is vanishing quickly. Increasingly seen are mixed technology assemblies that provide the best of both worlds.