Understanding the Military Standards and Update on JEDEC and New Spec Initiatives

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Class time (16300-1900 hrs)

COURSE SUMMARY

The course will outline the basics of various military standards as it applies to EEE devices and what topics JEDEC JC-13, CE-12 and CE-11 are currently addressing. The course will also provide the current status of various standards on such items as PEMs, DPA, Derating, Advanced Technology, GaN and other initiatives.

1. Basics of MIL STDs and MIL PRFs foe Microcircuits, Hybrids and Semiconductor
2. Basics of MIL-STD-1580 - DPA
3. Workings of SAE CE-12/CE-11 and JEDEC JC13
4. What is the committee working on now from standards perspective
    a. PEMs
    b. Radiation
    c. GaN
    d. Advanced Technology Microcircuits
    e. COTs – Alternate grade
    f. Derating
    g. Long Term Storage
    h. IGA (Internal Gas Analysis)

INSTRUCTOR BIOS

Larry Harzstark has over 35 years of experience in parts and component management-related engineering areas. He has been involved in all aspects of component engineering from the design of custom radiation-hardened devices to meet strategic missile requirements, to failure analysis, parts selection, design reviews, supplier audits, technology reviews and parts control boards. Recently, Larry has been involved in aspects of Commercial Off the Shelf (COTS), as well as Plastic Encapsulated Microcircuits (PEMs) and their utilization in military systems. He developed the guidelines for use of PEMs in an Army missile system and in space applications. His extensive expertise and knowledge in the field of microelectronics has earned him a reputation as a problem solver. Larry currently is an Aerospace Fellow responsible for technical aspects of new technology insertion, PMP management, evaluations of alternative technologies and problem resolution for programs. He earned his BSEE from the Polytechnic Institute of Brooklyn in 1969, and his MSEE from Clarkson College of Technology in 1970.

Sultan Ali Lilani is Director of Technical Support at Integra Technologies. Sultan has in-depth knowledge of Reliability Engineering, Program Management, Testing and Qualification for Aerospace, Defense and Industrial applications for semiconductor products. Sultan serves in various industry committees including SAE as chair for PEM's sub-committee, co-chair for copper bond wire and is involved member of SAE's G19A Counterfeit Committee, DPA and various other committees.

Shri Agarwal currently works at the Jet Propulsion Laboratory and coordinates the NASA Electronic Parts Assurance Group (NEPAG). He has supported the NEPP/NEPAG Program as the Agency's point of contact for microcircuits and represents NASA on Defense Logistics Agency in the area of space microcircuits manufacturer audits, infusion of new technology into military standards, etc. Agarwal was instrumental in developing requirements for Class Y, a classification assigned to the advanced (system-on-a-chip complexity) ceramic-based non-hermetic microcircuits for space. He holds master's degrees from the University of Southern California, Los Angeles; the Indian Institute of Technology, New Delhi, India; and Agra University, Agra, India.