Heterogeneous Integration Packaging Reliability Challenges and Roadmap

Instructor: Richard Rao, Ph.D., Co-Chair IEEE HIR Reliability TWG, Marvell Technology, richrao2010@gmail.com

Class time (0900-1600 hrs)

COURSE SUMMARY

This tutorial examines the reliability implications of 'SysMoore', i.e. system-level heterogeneous integration (HI), that is being developed as a means to keep delivering the rate of performance increase, that we have come to expect because of Moore's Law. Increasing system complexity, functionality, diversity, and density, as a result of the twin drives for HI and on-chip advances, will pose new challenges for meeting and verifying customers' reliability targets. Multifunctional HI systems of the future are expected be complex multiscale and multiphysics systems. Heterogeneous integration requires a convergence between the semiconductor industry and the packaging industry, and a unified reliability approach across the entire product architecture hierarchy from device level to package, boards/ modules, and systems. The resulting complex chip-package-board interactions (CPBI) will pose new reliability challenges and will need to be addressed by an integrated reliability team across all these levels of device-to-system integration, to meet the customer's reliability targets. HI reliability engineers will also need to meet holistic constraints such as reducing the time required for new product introduction (NPI) and minimizing cost of ownership over the life-cycle of successive generations of products. Such an integrated approach towards reliability will require a rigorous, disciplined, and proactive fusion approach that strategically combines a bottom-up reliability physics approach with a top-down approach that leverages powerful artificial intelligence algorithms and the unprecedented levels of real-time field performance data, service condition data, product stress data and system/component reliability data that is becoming available via IoT infrastructure. This tutorial lays out the scope, challenges, disruptive opportunities, and potential approaches for achieving such an integrated reliability approach for HI technologies, that are likely to emerge over the next 0-5, 5-10 and 10-15 years.

This tutorial will focus on the following aspects of heterogenous integration reliability.

1. Introduction of heterogenous integration packages such as chiplet, 2.5D and 3D package integrations for electronics and Silicon Photonics packaging.

2. Reliability failure modes and degradation mechanisms for multi-level interconnects in the heterogenous integration system such as transistors, BEOL interconnects, TSV, uBumps, RDLs and hybrid bonding, etc.

3. Chip to package interaction reliability challenges for advanced Si nodes

4. Design for reliability

5. Qualification for reliability

Who Should Attend?

IC designers, quality, reliability and component engineers interested in learning about the reliability of heterogeneous integration (HI) including 2.5 and 3D packages. Undergraduate and graduate students with interests in reliability physics of advanced IC and Silicon Photonics packaging and advanced Si nodes. Technical managers responsible for developing next generation packaging technology and those interested in the future road map of microelectronic packaging.

INSTRUCTOR BIOS

Dr. Richard Rao is currently a Senior Principal Engineer at Marvell Technology and a Senior Member of IEEE. Prior to joining Marvell, he was a Fellow of Microsemi (Microchip) Corp and a consultant engineer at Ericson Inc. His responsibilities include the development of design for reliability flows for advanced circuits, packaging, and chip to package interaction. He was the chair of IEEE EPS (Electronics Packaging Society) Reliability Technical Committee and co-chairing the reliability roadmap for the IEEE Heterogenous Integration Roadmap. He is also the general chair and technical program chair for the IEEE REPP (Reliability of Electronics and Photonics Packaging) Symposium. He also serves as the technical committee chairs for the IEEE IRPS (International Reliability Physics Symposium). He has given many invited talks and keynote speeches to various international conferences. He has a Ph.D. degree in solid mechanics of materials from the University of Science and Technology of China and a post-doctor research fellow at Northwestern University studying the reliability failure mechanism of advanced integrated circuits. Prior to joining Marvell, Dr. Rao held senior technical positions in reliability physics and engineering for both academia and industries. He was an assistant/associate professor at University of Science and Technology of China and a research fellow for National Science and Technology Board of Singapore.