Microelectronic Component Engineering for the 2020s

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Note to attendee: Class includes coffee and pastries in the morning and a full sit-down lunch at noon.

Class time (0800-1600 hrs)

COURSE SUMMARY

This full-day seminar is focused on microelectronic components used in military, space, and other high reliability applications. Components include active integrated circuits (ICs) and monolithic microwave ICs (MMICs), ceramic and tantalum capacitors, thick/thin film resistors, various substrate materials, inductors, magnetics, filters, and other electronic components used and packaged as discrete devices or assembled in a hermetic or non-hermetic hybrid and multichip packages. The component engineer must understand the basic materials and processes used to build active and passive components and most importantly the reliability implications when choosing one part type or package configuration over others.

In addition to an understanding of the basic technology the component engineer must have a working knowledge of a myriad of specifications and issues needed to build or purchase quality components that work as advertised over the temperature range of interest (typically -55C to 125C) for the expected mission life of the system. In this overview seminar experienced experts in this field will review and explain in simple terms the following:

Component Engineering Functions (0800-930)

- Military and commercial part specifications and quality standards
- Parts Data Base & BoM management
- Component Reliability basic principles and metrics used
- Risk Analysis & obsolescence management and counterfeit mitigation
- Qualifying component suppliers for mil and space
- Source Controlled Drawings vs ‘standard’ components
- When might SCD be used vs standard components, what makes a good SCD
- Current export technology limitations & considerations ITAR
- Environmental legislation rules, trends and impacts upon design and sourcing

Materials and Processes for Passive Components (1000-1200)

Ceramic, Film, Stacked Modules and SuperCaps (Ron Demcko, AVX)

- Performance characteristics are discussed relative to time, temperature, voltage, and frequency. Distinctions are made between thin film capacitors and power film capacitors.
- Stacked capacitor modules - traditionally MLCC (multilayered ceramic capacitors)

- Super capacitor technology overview, super capacitor modules.
- A high-level selection guide and de-rating methods is given for all capacitors presented.

Tantalum & Electrolytic Capacitors (Jon Rhan, VISHAY)

- Capacitor construction and how performance characteristics are affected by time, temperature, voltage, and frequency.
- End applications are discussed along with reliability expectations, common failure modes and de-rating methods for increased lifetime performance.
- Processing guidelines and simulation models are presented.

Lunch (1200-1300)

Materials and Processes for Active Components (1300-1500)

Hybrids, RF MMIC Modules, Monolithic and discrete semiconductor devices

Manufacturing Assembly Process Overview
- Basic manufacturing process flows
- Clean room requirements and industry protocols

Wafer Fabrication Processes for ICs and MMICs

Substrate Technology
- Thin and thick film technology process fundamentals
- Laser trimming of resistors

Plating processes and industry specifications

Material and Process Fundamentals for Component Attach
- Epoxy attach of substrates and ICs
- Eutectic Soldering Processes

Packaging Design Considerations
- Thermal analysis, simulated stack up and junction temp calculations
- Coefficient of Thermal Expansion (CTE)

Wirebonding and Interconnect Process Overview
- Ultrasonic/thermosonic bonding ball/wedge/ribbon bonding

Hermetic Packaging Process Overview and test
- Seam sealing, laser welding aluminum alloys, solder sealing
  - Hermeticity Testing
- Nom-Hermetic Packaging Options and testing

DPA (destruct physical analysis) (1500-1600)

- Rationale and testing protocols
- Examples and what to learn from a DPA report
- FA (Failure Analysis) methods

Class Wrap up and Q&A (1600-1630)

INSTRUCTOR BIOS

Thomas J. Green has more than 40 years combined experience in industry/academia and the DoD. He earned a B.S from Lehigh University in Materials Engineering and an MEA from Univ of Utah. He is a recognized expert in materials and processes used to assemble hybrids, RF microwave modules/5G, Class III medical implants, optoelectronics, and other types of hermetic/non-hermetic packaged microcircuits and sensors. He has considerable expertise in hermetic testing methods per TM 1014 and moisture related failures in general. He is a consultant to companies developing next gen microelectroincs for military and space. Serving as a Research Scientist at the U.S. Air Force Rome Air Development Center, Tom worked as a reliability engineer analyzing component failures and in industry he was the process engineer at Lockheed Denver. He has invaluable experience in wirebond, die attach, hermetic sealing, FA and root cause identification, For the last 20 years, Tom's expertise has helped position TJ Green Associates, LLC as a recognized industry leader in teaching and consulting services for high-reliability military, space, and medical device applications. Tom is a Fellow of IMAPS (International Microelectronics and Packaging Society) and retired LtCol USAFR with 28 years of service.

Ron Demcko graduated in 1982 from the Clarkson College of Technology BSEE. He is currently an AVX Fellow and manages TSG team at AVX Headquarters in Fountain Inn SC. This role centers on projects ranging from simulation models for passive components to product support / new product identification & applied development. Prior to that, Ron was the EMC lab Manager AVX Raleigh N.C. This lab concentrated on sub assembly testing and passive component fixes for harsh electrical and environmental. Before the EMC lab work, he held an Application Engineering position at AVX Product work included integrated passive components, EMI filters and Transient voltage suppression devices. Before joining AVX he worked as a Product Engineer and later Product Engineering Manager at Corning Glass Works electronics division. In this role he supported production, sale and development of Pulse Resistant Capacitors, High Temperature Capacitors and radiation resistant capacitors. He developed high frequency test methods and co-developed high temperature test systems.

Trevor Devaney has been President of Hi-Rel Laboratories, Inc. for the last 21 years and has been involved in DPA Testing, Materials Analysis, and Failure Analysis of electronic components and for 41 years. He has a BSc. In Metallurgical Engineering from Cal Paly San Luis Obispo. He has been highly contributive to the development of Industry testing specifications such as Mil-Std-1580 Revisions A, B, and C respectively, as well as various Mil-Std-883 and 750 test methods over the last 30 years. Trevor is an ardent supporter of educating the newest generation of component engineers for the Space and Hi-rel industries. Trevor has been an annual presenter at SPWG for the last 21 years and routinely lectures on DPA findings and techniques on a regular basis.

Jon Rhan is a Senior Product Marketing Manager for Vishay Intertechnology in the Tantalum Capacitor Division. He is a Senior Member of the IEEE, a graduate of Penn State University in electrical engineering and MBA post graduate. A former analog power IC designer with Sprague, now Allegro Microsystems, Delco Electronics, now Delphi, Cherry Semiconductor and Analog Devices, Jon has been in the field for over 20 years in various application engineering roles. As product manager for Vishay, he is responsible for all wet tantalum offerings. He is based in New Hampshire and works out of the Bennington Tansitor site.