Overview of the Failure Analysis Process and Common Failure Mechanisms in Various Electronic Components

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Overview of the Failure Analysis Process

- Component history
  - In some industries component details are not available, but in others a comprehensive history can be obtained. Details such as test conditions, environment, and time to failure can strengthen a failure analysis.
- Inspect and document
  - It may seem inconsequential, but the condition of the component and electrical connection in-circuit can be related to the failure. It is good practice to inspect and document the suspected component(s) prior to rework or any destructive electrical testing, e.g. removal of the component from the circuit or aggressive probing of the solder joints.

Overview of the Failure Analysis Process

- Collect as much data non-destructively as possible
  - In failure analysis, the sample size is typically very small and because of this it is imperative to gather as much information as possible in a non-destructive manner. This includes thorough external examination, radiographic inspection, low-power electrical testing and failure characterization, and other techniques such as hermeticity testing and scanning acoustic microscopy when applicable.
- Keep an open mind
  - It is easy for biases to affect the failure analysis methodology. Things like the outcome of other analyses of similar components, or preconceptions based on data/history can result in an approach to the analysis that is focused on a set outcome. Many different mechanisms can result in the same type of electrical failure.

Failure Analysis Equipment

- Microscope cameras for documentation
- Real-time X-Ray for radiographic inspection/documentation
  - CT and laminography recommended
- Electrical test equipment to characterize failures with low power
  - Tektronix 576 curve tracer recommended, but due to age and availability, that may not be possible
  - Source/measuring units are very comparable and easy to use/implement with other benchtop equipment.
- Scanning acoustic microscopy is recommended for inspection of fractures and delaminations
- Decapsulation capabilities
  - Chemical decapsulation at minimum, with laser ablation and plasma etching recommended

Failure Analysis Equipment

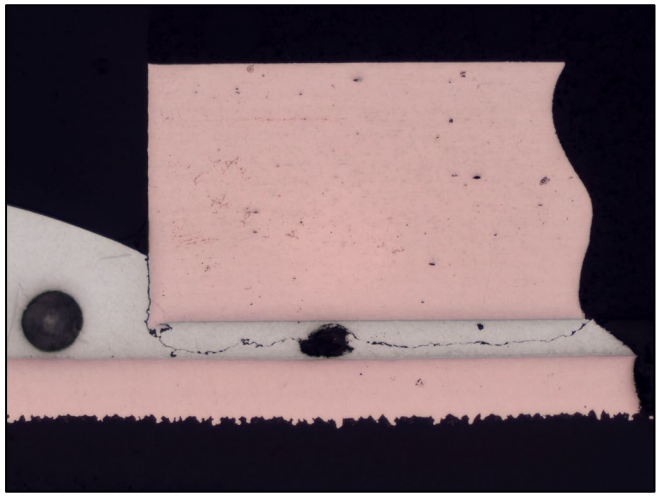
- Failure localization techniques
  - IR hot spot detection recommended
  - Liquid crystal hot-spot detection performs similarly, though less sensitive, and is very inexpensive and easy to set up.
- Micro-probe stations recommended for die level testing
- Deprocessing with wet-etch at minimum
  - Plasma etching recommended
- Cross section equipment
  - Manual cross sectioning
  - Focused Ion Beam
- Scanning electron microscopes for inspection of small defects and elemental analysis
- Fourier transform IR spectroscopy for analysis of organic materials

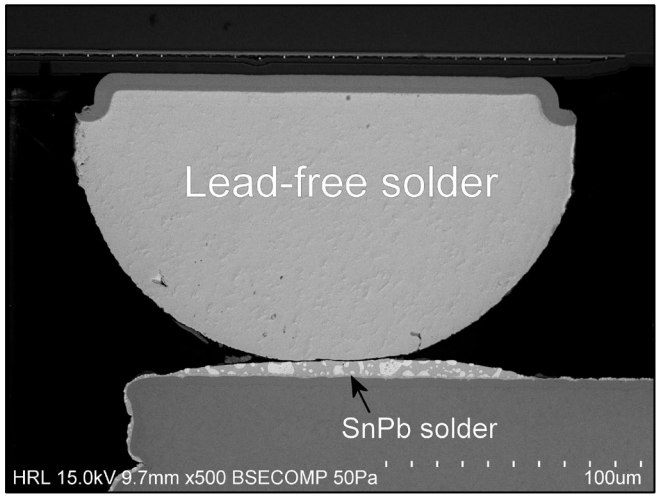
Board-Level Failures

Board-level failure mechanisms are a common cause of failure for every electrical component and must always be considered.

Board-Level Failures

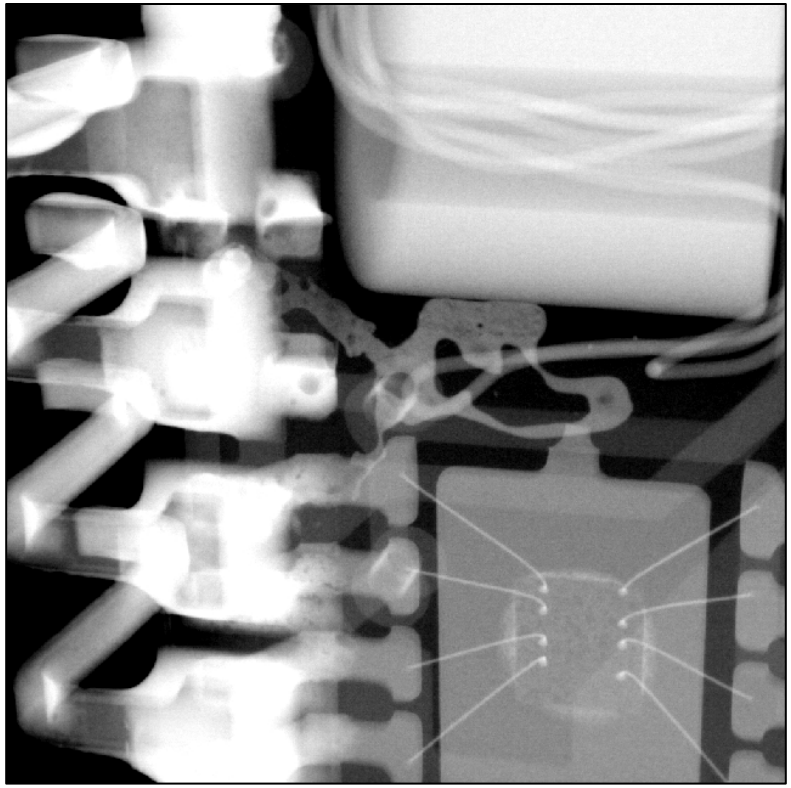
- Disconnected solder joints
  - Mechanical stresses
  - Non-wetting
  - Head-on-pillow
  - Each of these defects can be masked by solder reflow during component removal.





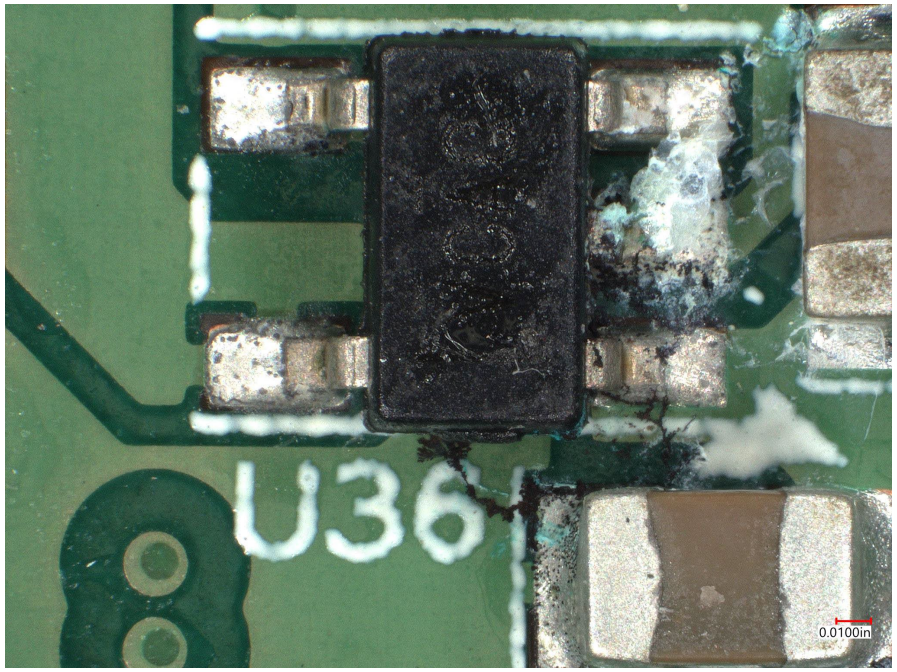
Board-Level Failures

- Reflowed solder
  - Incorrect solder compositions used
  - Incorrect solder reflow profiles
  - Hand soldering
  - Can be hidden beneath components
  - Can also be cleared with solder reflow during component removal



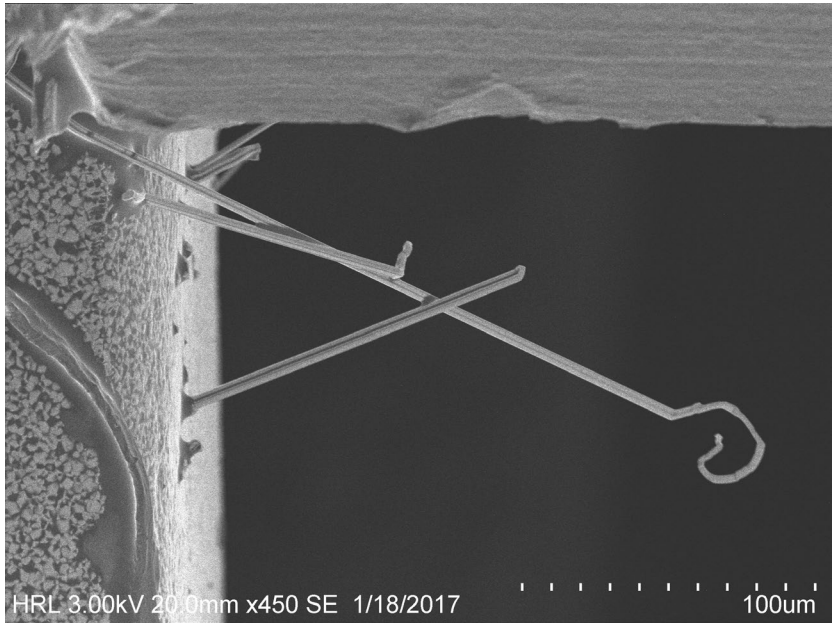
Board-Level Failures

- Dendrites/corrosion
  - Can occur in corrosive environments or due to improper board cleaning processes.
  - Typically results in resistive current leakage paths or open circuiting of metal traces
  - Can form beneath components



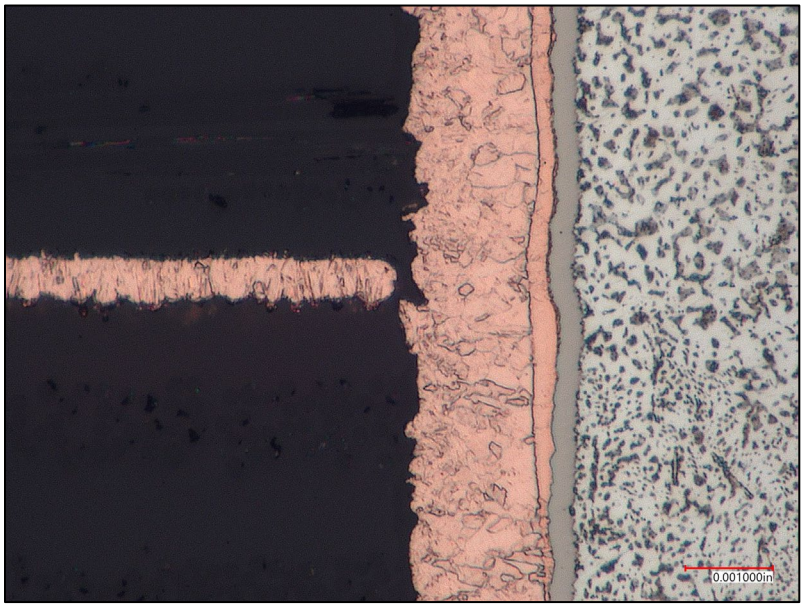
Board-Level Failures

- Tin Whiskers
  - Occur when pure tin plating is used, which is becoming increasingly more rare.
  - Can conduct high current for their size, but can also fuse open, resulting in a “self-heal”.
  - Can grow to surprising lengths.



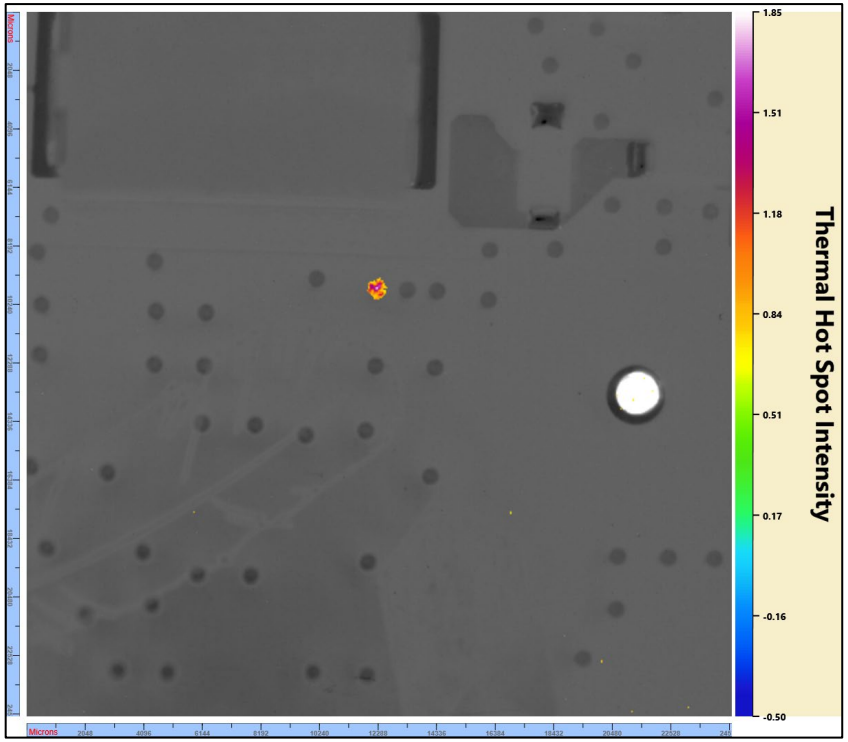
Board-Level Failures

- Internal PCBA failures
  - Board layer delamination
  - Over-etching of vias/through-holes
  - Conductive anodic filament (CAF)
  - Fracturing of board layers due to mechanical stresses
  - Masking/etching defects in metallization layers



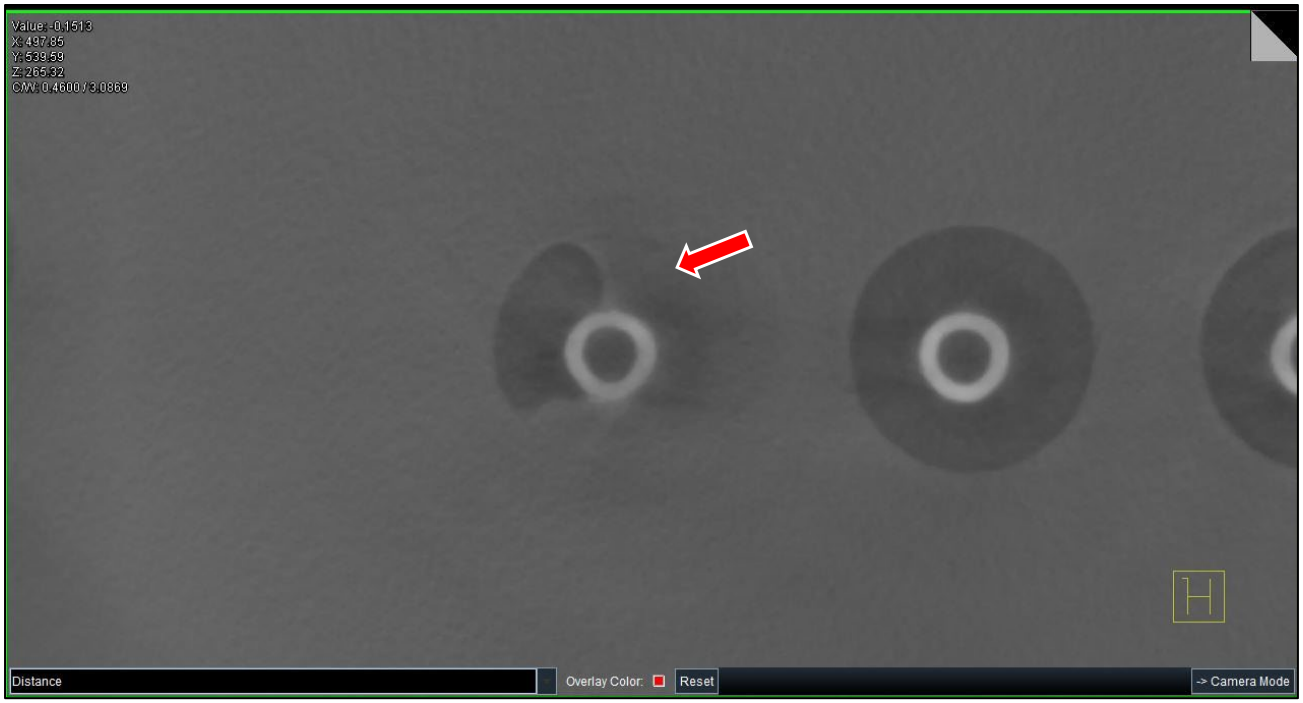
Board-Level Failure – Example

- A CCA exhibited a 4mΩ short circuit between two nodes.
- Customer-level testing isolated failure to two suspect planes.
- Infrared hot spot detection was performed and localized the failure to a single via, which was connected to the suspected planes.



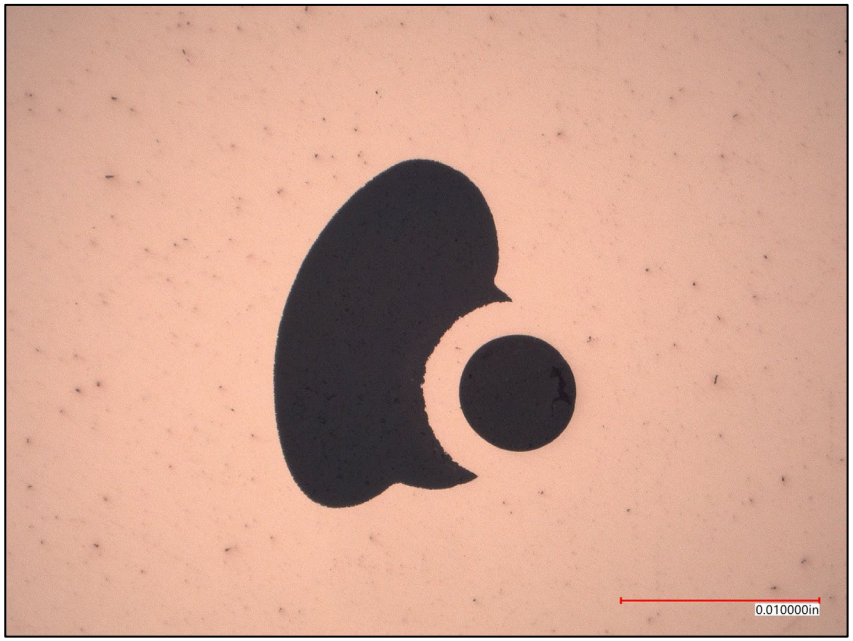
Board-Level Failure – Example

- 2D, real-time radiographic inspection was performed on the CCA in an attempt to identify any defects, but due to board density it was inconclusive.
- Laminography was then performed to “slice” through the layers of the board until the defect was identified.



Board-Level Failure – Example

- Metallurgical cross section was performed to verify and determine cause of failure; a copper metallization etching defect.

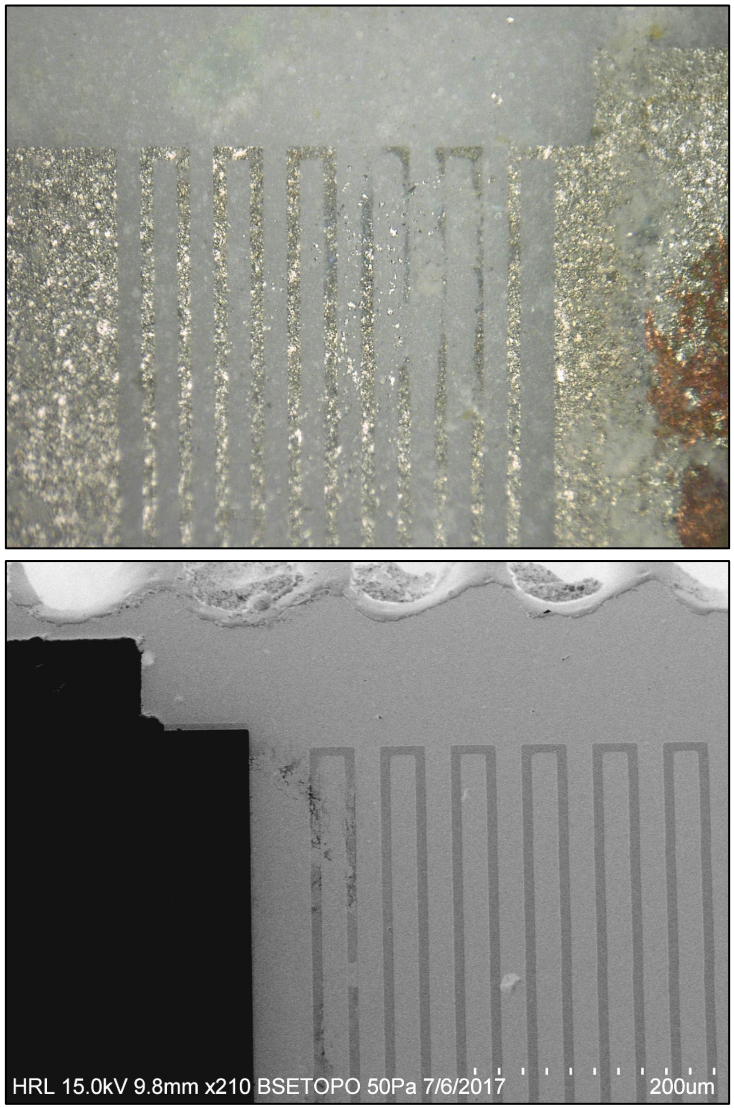


Resistors

Resistor failures are generally due to connection issues, electrical overstress or corrosion from their operating environment.

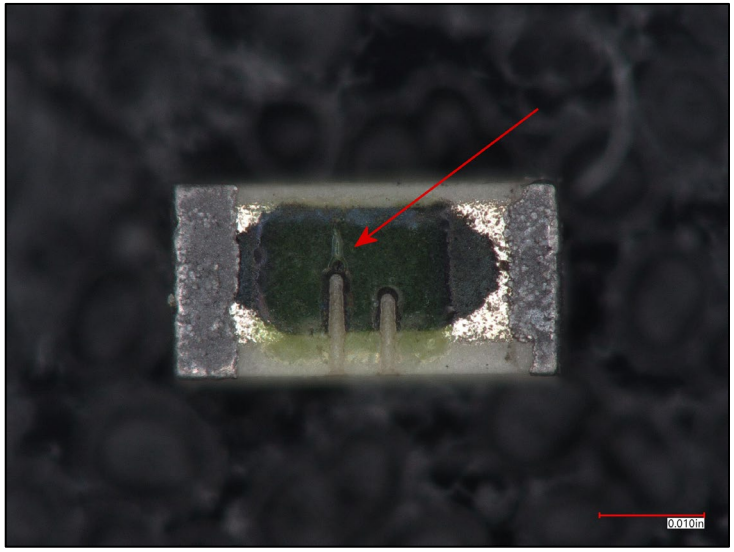
Resistors

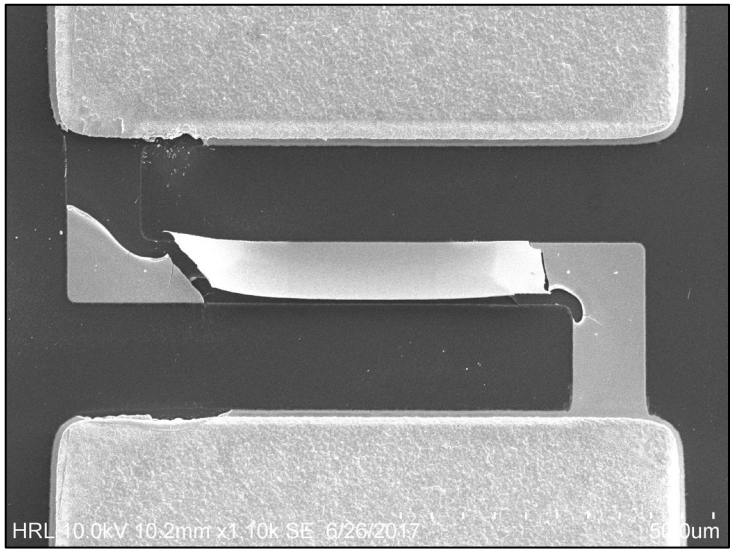
- Corrosion
  - Corrosion is a common failure mechanism for every style of resistor.
  - Can affect resistor element or interconnect metallization.
  - Generally attributed to packaging/seal issues.
  - Can be due to moisture or ionic contamination



Resistors

- Electrical Overstress
  - Electrical overstress is a broad term, but typically refers to failure due to excessive current or high voltage conditions.
  - The location of the failure within the device, the severity of the damage, and associated circuitry can determine more specific information related to the failure





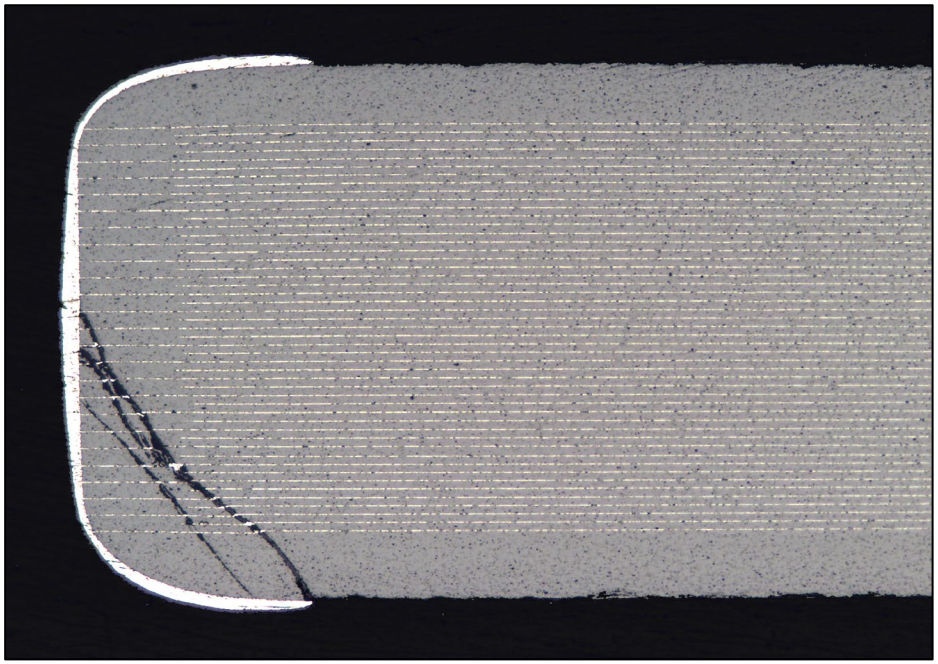
Capacitors

Multi-layer ceramic capacitors are often damaged by mechanical overstress, while tantalum capacitors are susceptible to damage from surge currents and moisture absorption.

Capacitors

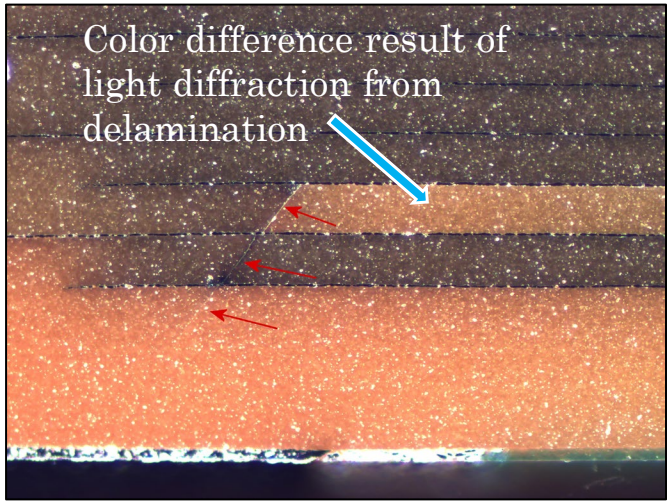
The electrical parameters most affected by failures are DC leakage current, ESR and capacitance. Care should be taken to test the capacitor at low voltage with sufficient current limiting to prevent exacerbation of the failure site.

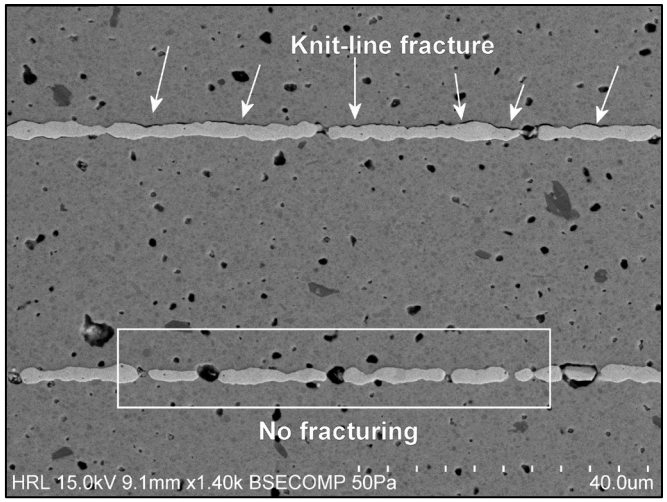
- Mechanical overstress
  - By far the most common failure mechanism for multi-layer ceramic capacitors.
  - Can begin as benign microfractures that propagate with time/temp/stresses, subsequently resulting in current leakage or short circuiting.
  - Flexure cracks have characteristic “45 degree” fracture spanning from the tip of the end metal towards the termination.



Capacitors

- Manufacturing defects
  - The most common defects include delamination, dielectric voiding, and knit line fractures.
  - Similar to mechanical overstress, capacitors affected by these defects can pass electrical testing and later fail in the field.
  - SAM analysis has high success in identifying these defects.



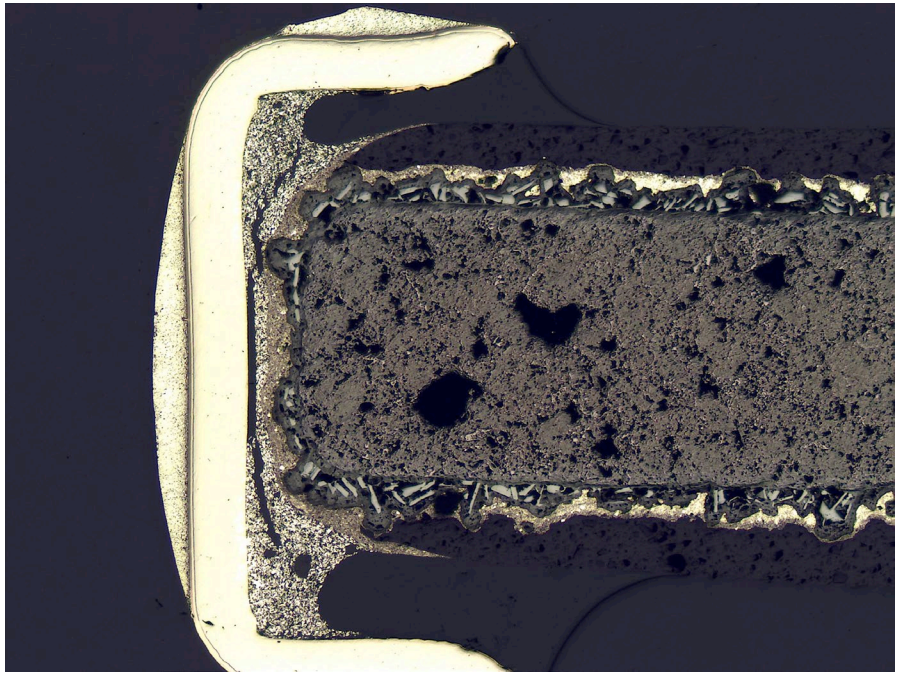


Capacitors

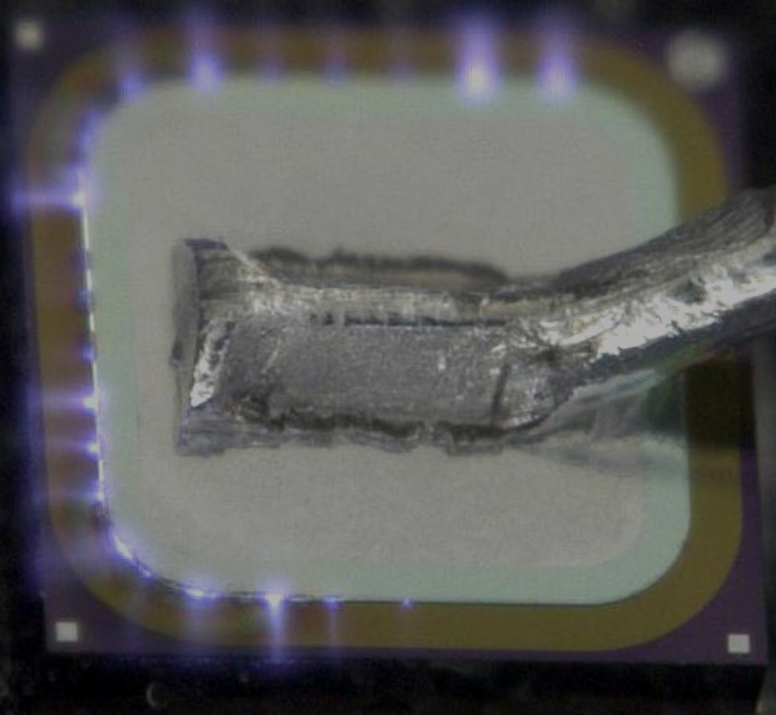
- EOS/Surge current and ESR considerations
  - Tantalum capacitors are commonly damaged by high in-rush current (i.e. surge current).
  - This type of failure can be due to equivalent series resistance (ESR) variations in tantalum capacitor banks.

Capacitors

- ESR failures
  - Typically, high ESR in tantalum capacitors is due to damage/defects in the cathode attach system.
  - Fracturing of the cathode silver epoxy is a common failure mechanism for ESR.



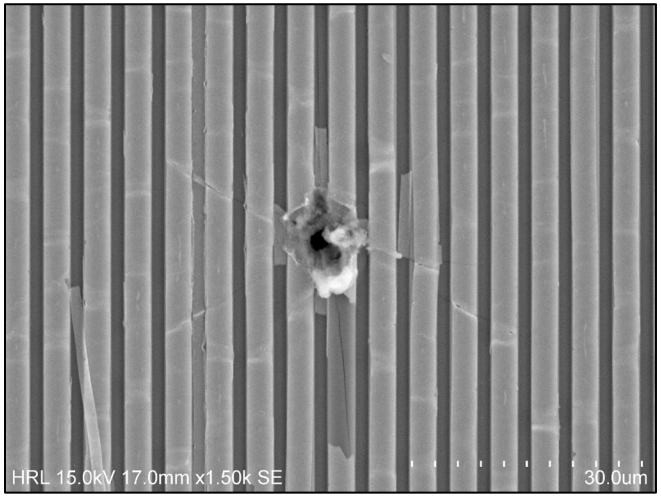
Diodes



Diodes can be damaged several ways. It's important to consider failure mode (open, short, degraded), temperature sensitivity and packaging when performing a failure analysis.

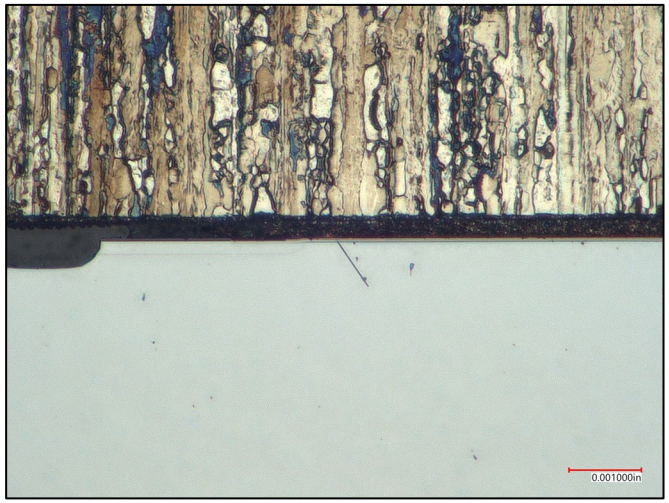
Diodes

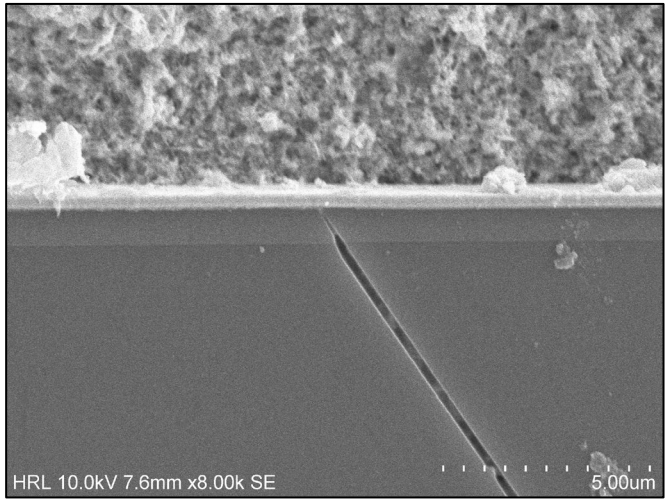
- Electrical overstress (EOS)
  - EOS is typically due to high reverse voltage, high forward current, or a high speed voltage transient.
  - Electrostatic discharge (ESD) damage is similar in appearance to reverse-biased high-speed voltage transients, and generally occur at the edge of the anode contact area (upper image), while forward biased current transients occur central to the die where current density is the highest (lower image).



Diodes

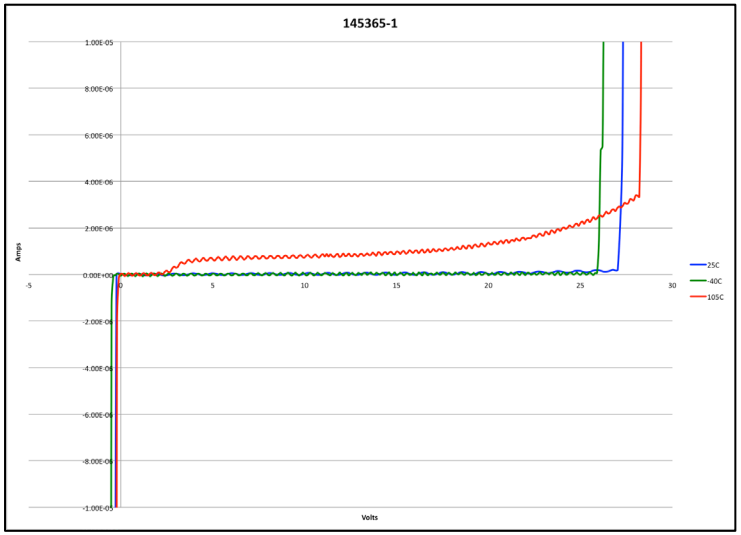
- Thermal/Mechanical overstress
  - Glass body diodes are susceptible to fracturing due to lead forming, handling, and thermal overstress induced during the soldering process.
  - These fractures can result in low level leakage, with the potential to worsen over time and temperature.

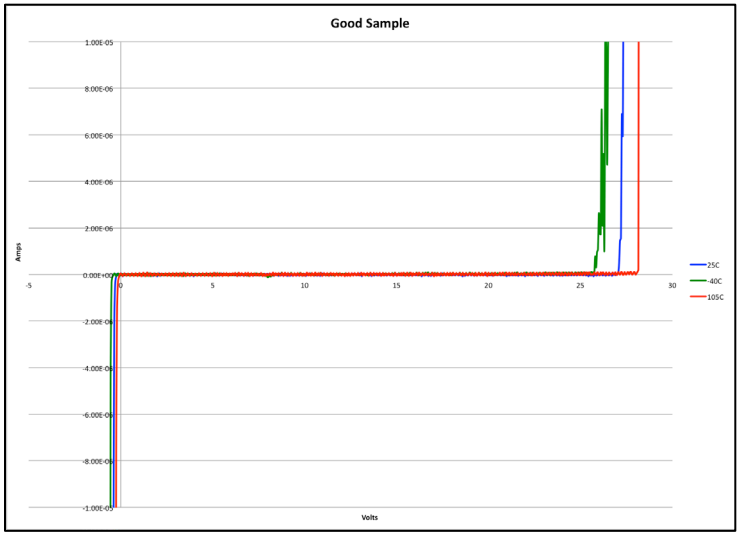




Diodes

- Ionic contamination
  - Can affect any PN junction and presents as temperature sensitive leakage current, commonly with “inversion” characteristics when plotting the I/V curve. Note red curve in below I/V plot showing leakage at +105C.
  - Often can recover with vacuum baking.
  - It is due to mobile ionic contamination on die surface or passivation layers.

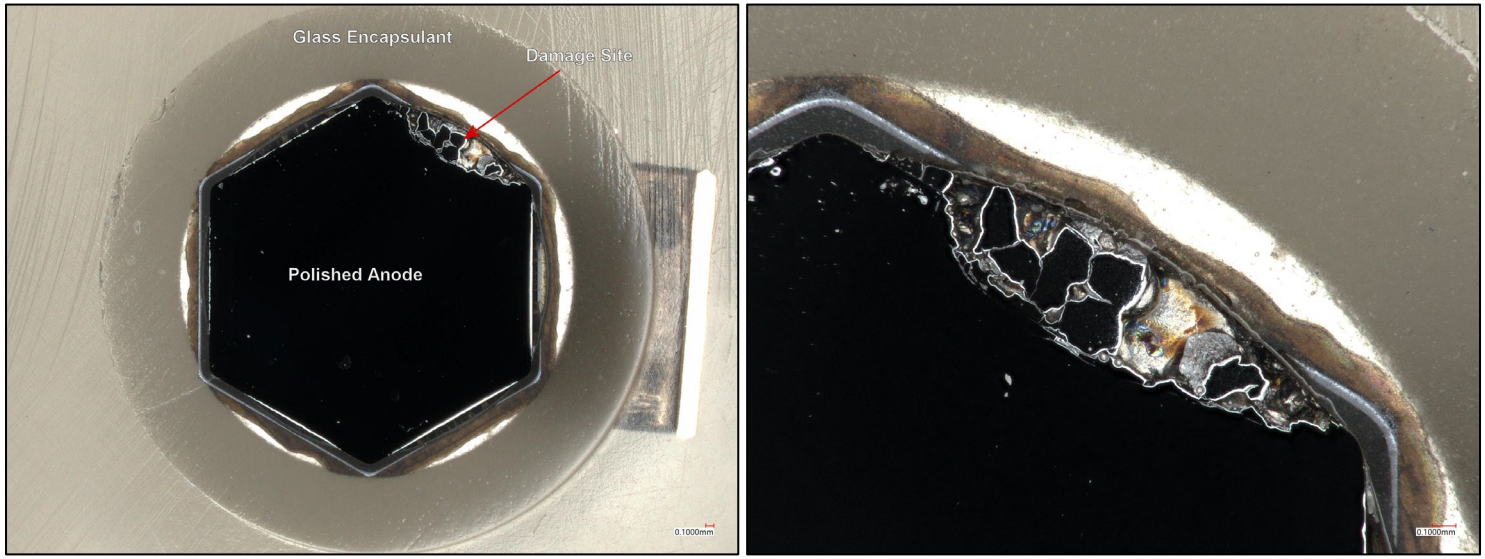




Diode Analysis - Example

A diode array failed after 13 years of service where the diode was under reverse bias.

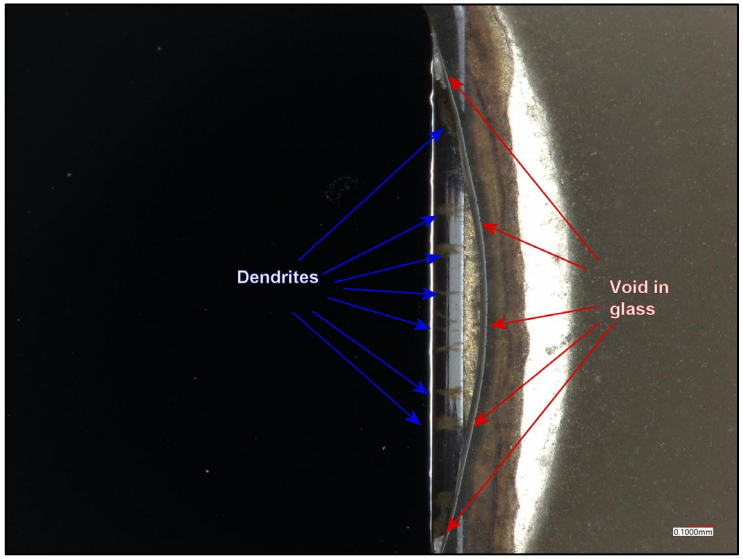
After scheduled maintenance, the diode failed catastrophically upon system startup.

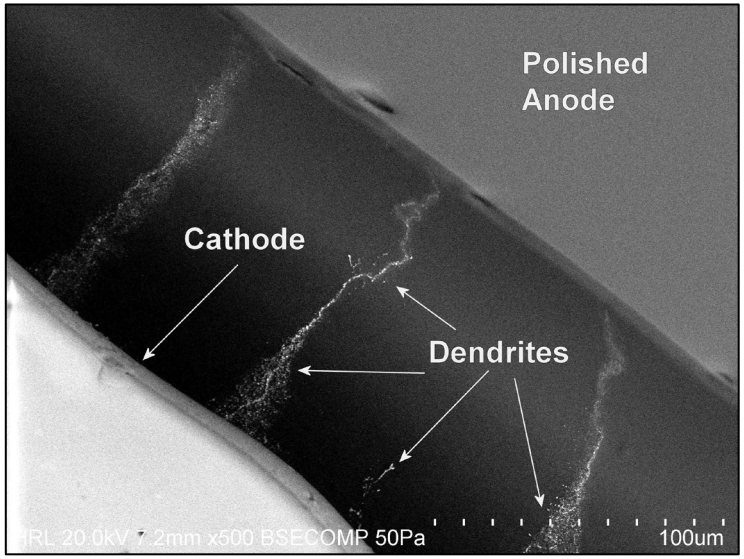


The location of this damage is consistent with failure due to a reverse biased over-voltage event, but the failure history is important in this case.

Diode Analysis - Example

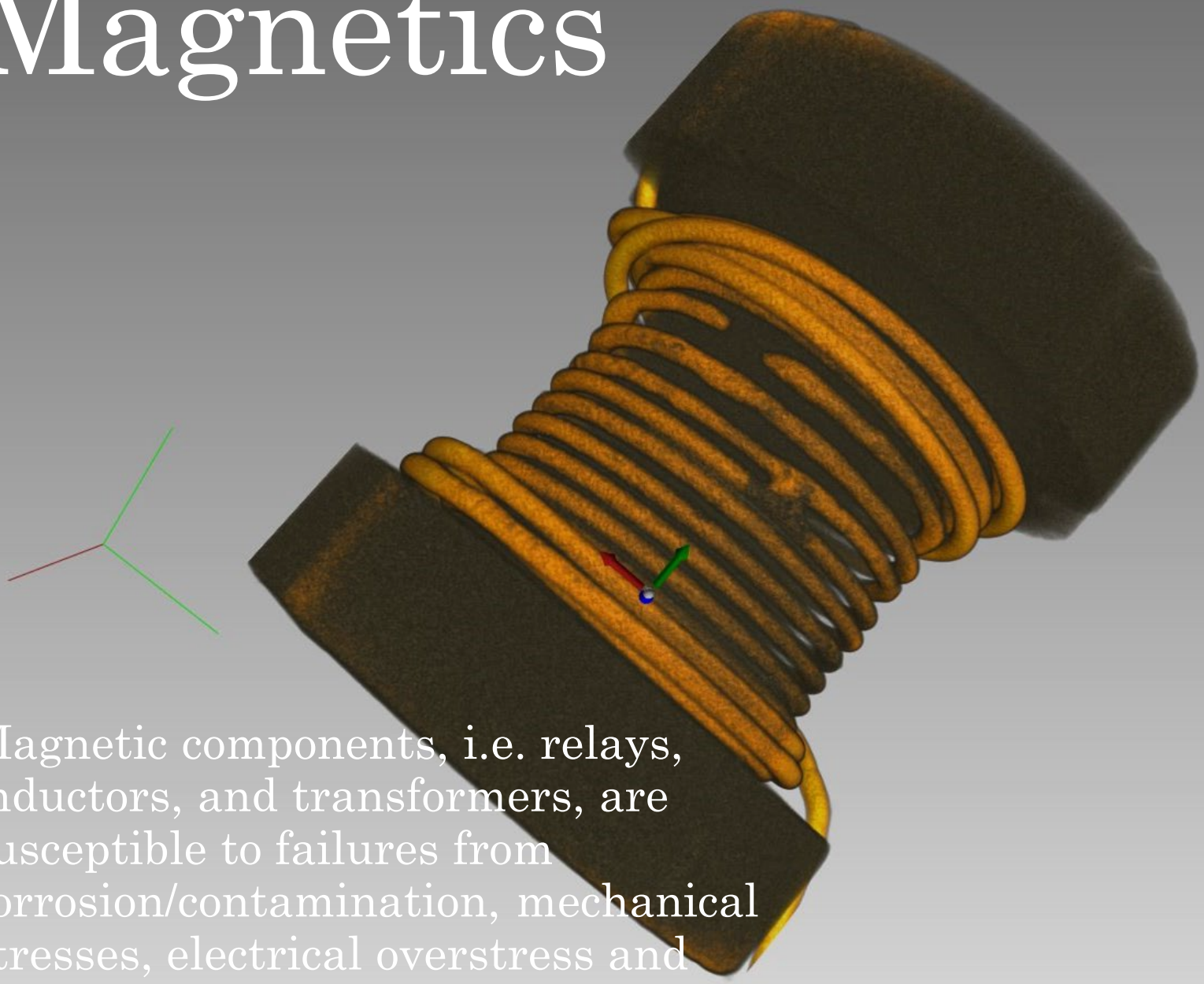
- This type of diode was built using silver die attach metallization, and silver is notorious for dendritic growth under the right circumstances, one of those being long-term voltage bias.





- In this instance, a combination of voiding in the glass envelope surrounding the die and the long-term voltage bias resulted in the formation of dendrites from the cathode of the diode towards the anode. The *normal,* short term, high-voltage turn-on transient was sufficient to arc from the anode to the dendrites, resulting in the catastrophic damage to the diode.

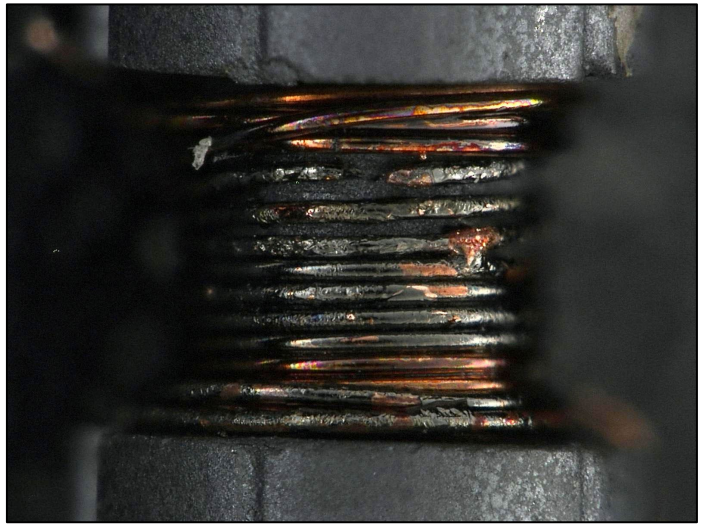
Magnetics

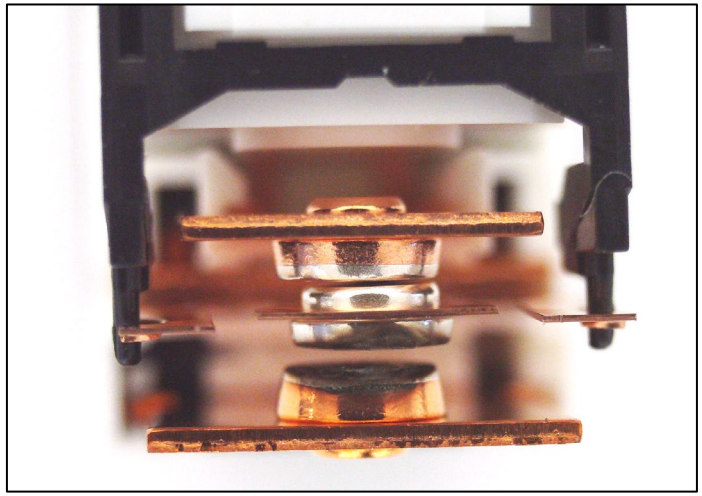


Magnetic components, i.e. relays, inductors, and transformers, are susceptible to failures from corrosion/contamination, mechanical stresses, electrical overstress and manufacturing defects.

Magnetics

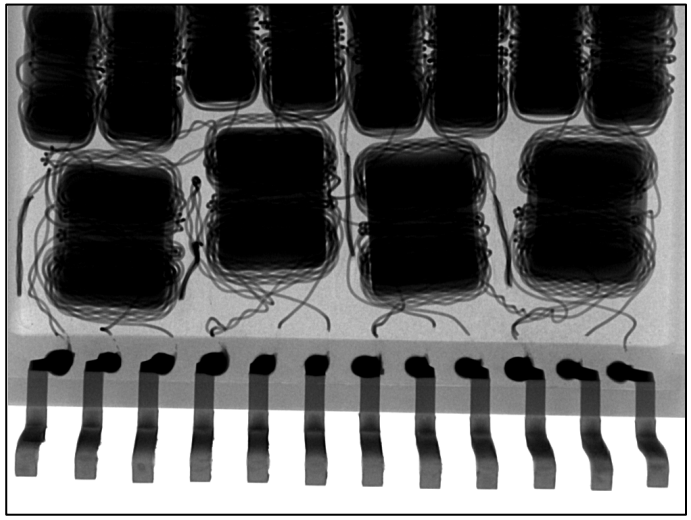
- Electrical overstress
  - Failure can result from excessive current, which will melt the entirety of the wire winding.
  - Electrical overstress can also be due to high voltage, sufficient to damage wire insulation or arc across relay contacts.

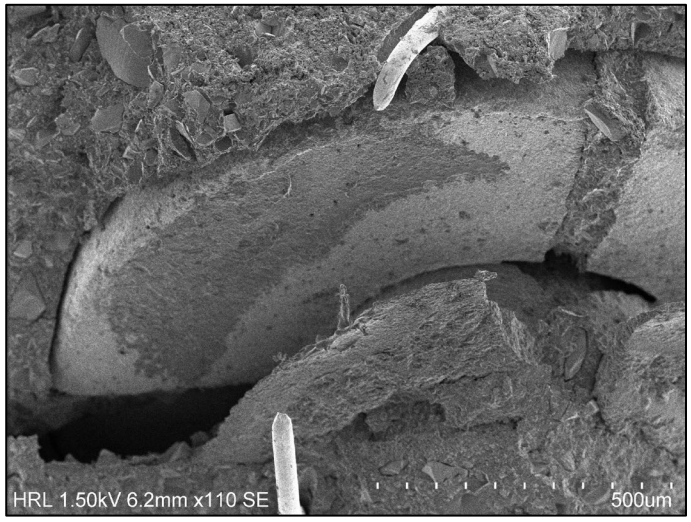




Magnetics

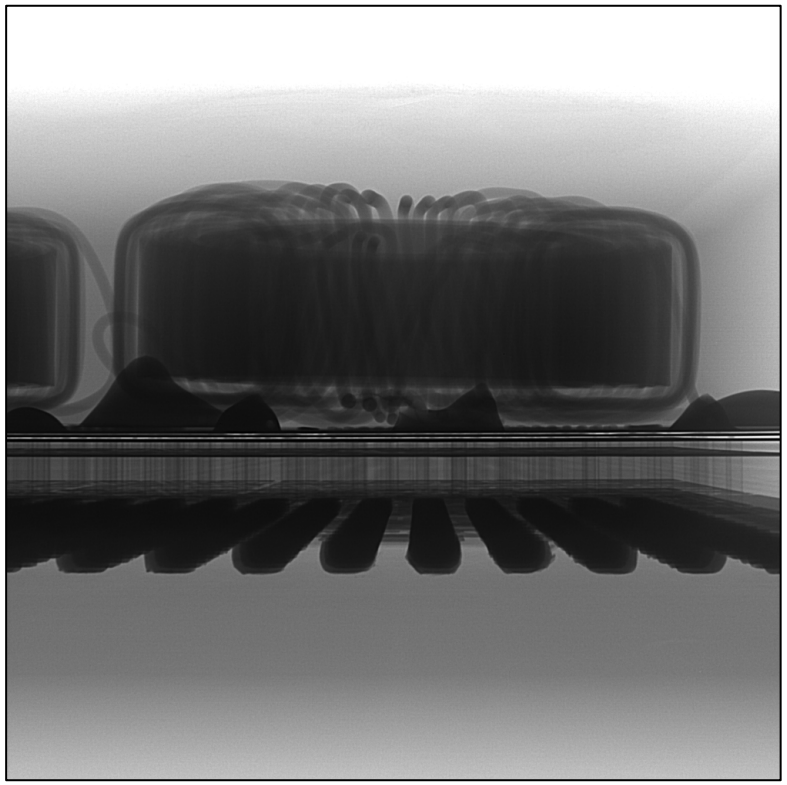
- Wire corrosion/fractures
  - As most magnetic components contain copper magnet wire, any uninsulated areas are prone to corrosion, especially where the wires are soldered to the leads.
  - Wire fractures due to tensile overload or fatigue are also common failure mechanisms, as is stress corrosion fracturing.





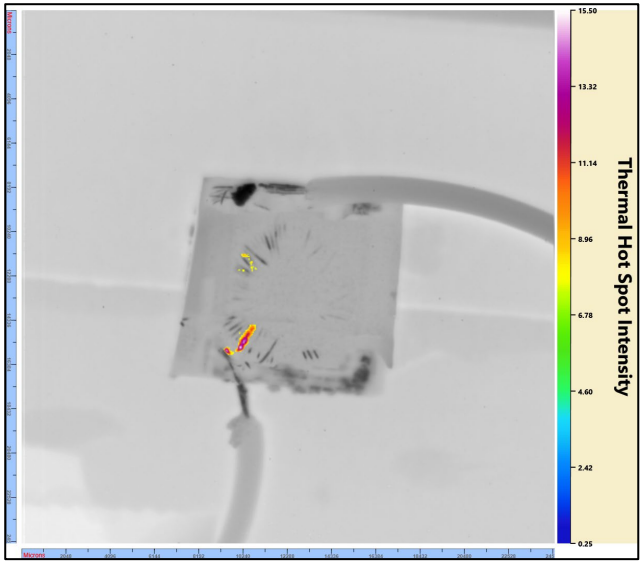
Transformer Failure Analysis - Example

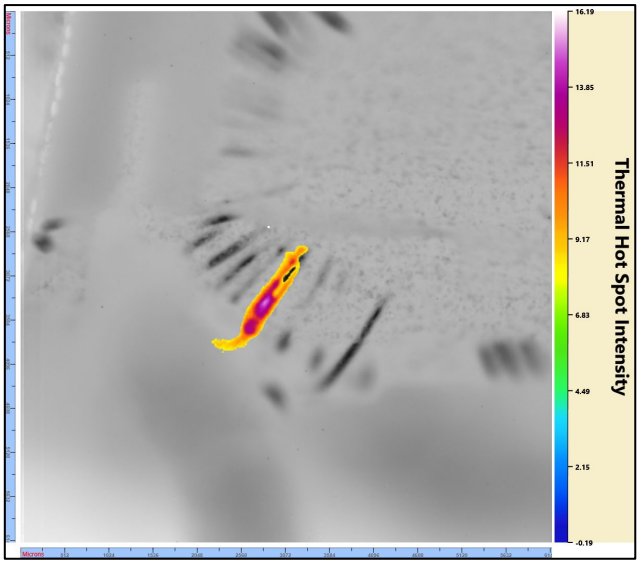
- A potted BGA module exhibited a <1Ω short circuit between two pads, and it was suspected that the failure was due to a short circuit in a transformer.
  - The challenge with short-circuited transformers is that the failure is due to an insulation breakdown, but most chemical depotting methods compromise the insulation.
- Non-destructive analysis included scanning acoustic microscopy, 2D real-time X-Ray and CT analysis, initially all inconclusive.



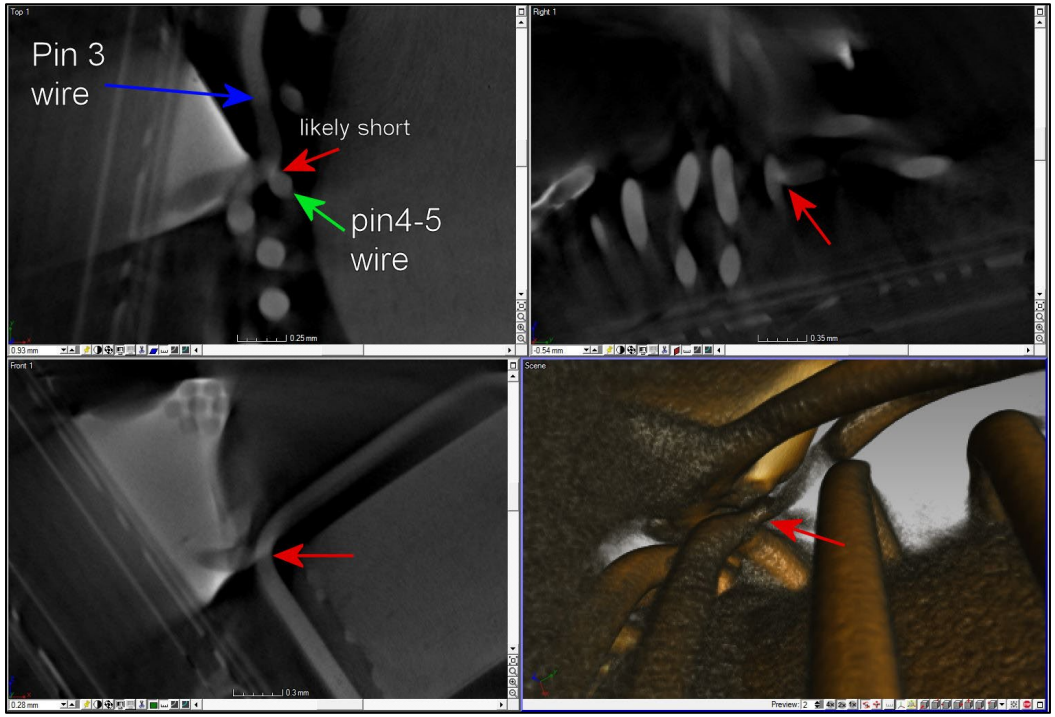
Transformer Failure Analysis - Example

- After additional testing and failure isolation, the transformer was removed from the module and partially depotted using laser ablation, allowing failure localization with IR hot spot detection.
- The short circuit was isolated to one winding, allowing more detailed inspection of that area via CT.





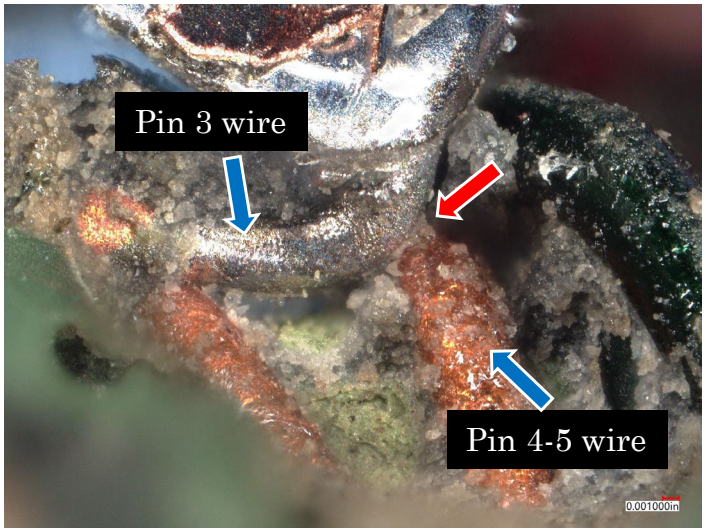
Transformer Failure Analysis - Example

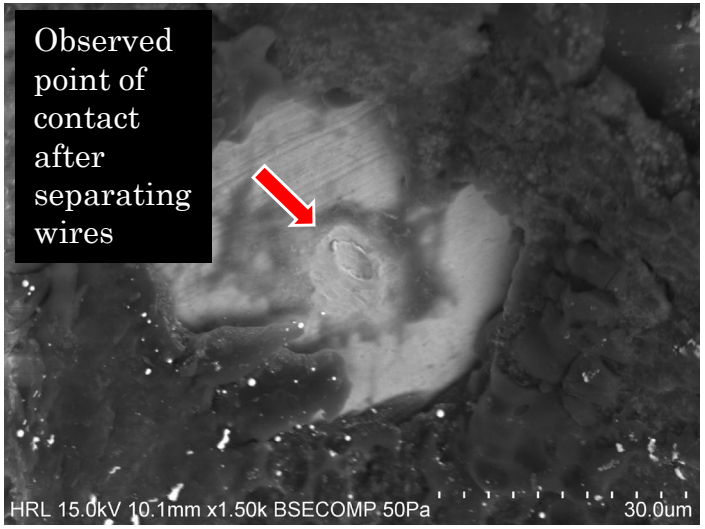


Detailed CT examination of the area indicated by IR hot spot detection revealed a single location where two wires from opposing windings made possible contact, tucked behind the solder joint on the substrate.

Now, instead of decapsulating the entire transformer we could target the area and uncover with laser ablation.

Transformer Failure Analysis - Example

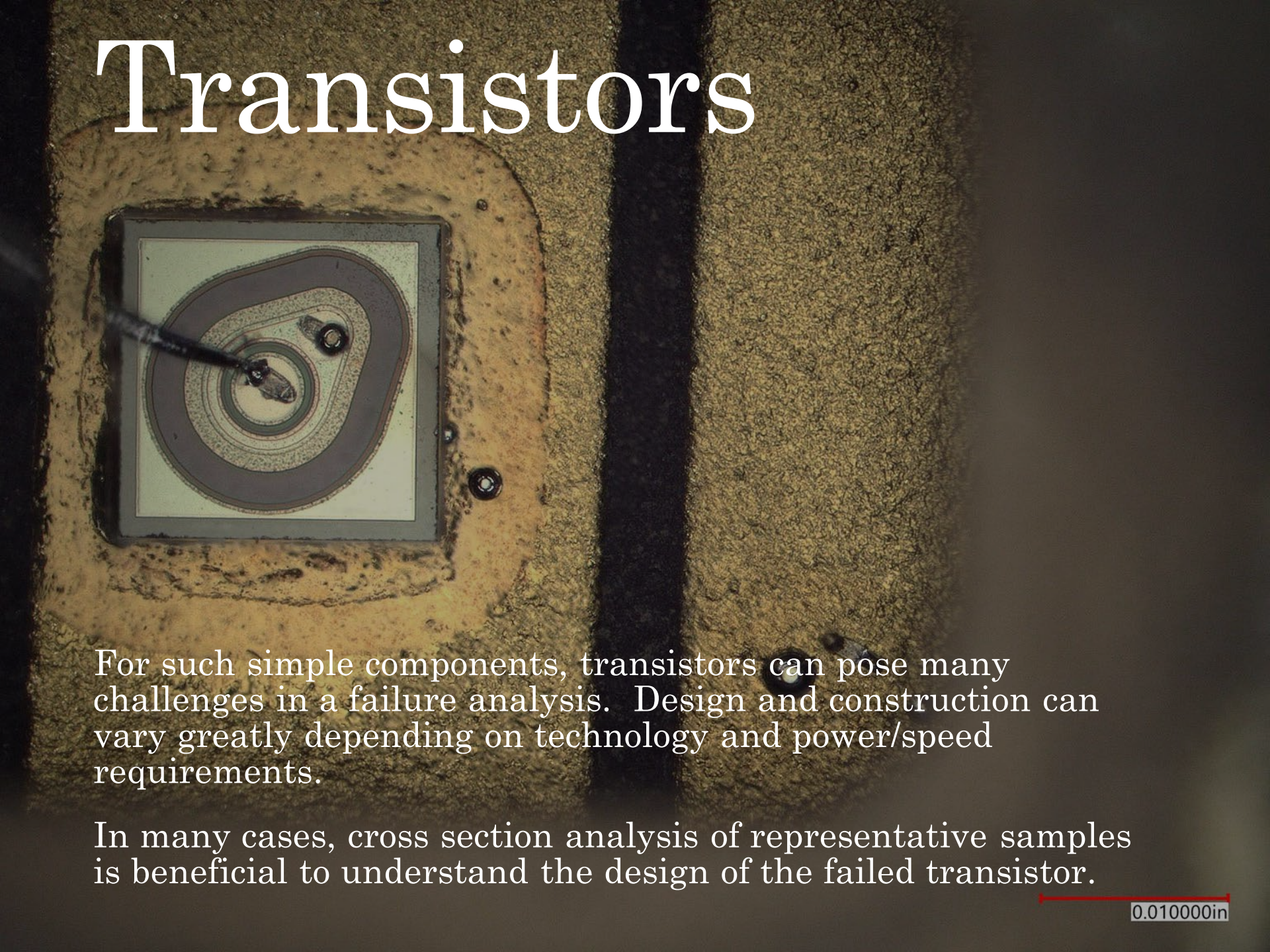




Laser ablation was successful in sufficiently uncovering the area of interest, revealing the failure site (upper left). The wires were separated, and subsequent inspection identified a breakdown of the wire insulation due to abrasion (upper right).

Note that the pin 3 wire is not insulated at that location due to the proximity of the solder pad.

Transistors



For such simple components, transistors can pose many challenges in a failure analysis. Design and construction can vary greatly depending on technology and power/speed requirements.

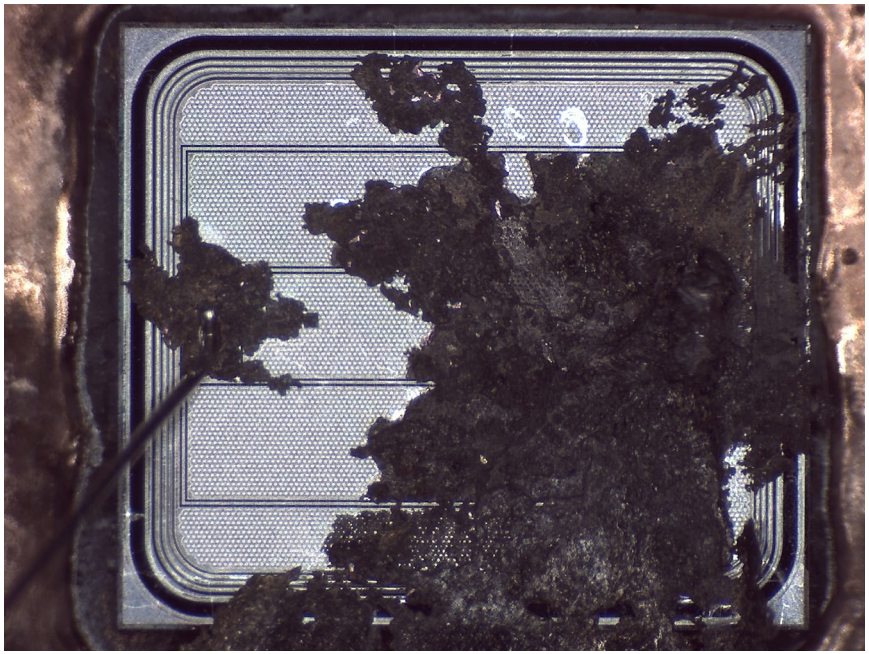
In many cases, cross section analysis of representative samples is beneficial to understand the design of the failed transistor.

Transistors

- Transistor failure modes typically include:
  - Current leakage between terminals
  - Short circuited conditions
  - Open circuited terminals
  - Low-gain
- Each one of the above can be due to several mechanisms, but the electrical data can offer clues.
  - When current leakage is observed, testing over temperature (within the temperature limits of the DUT) is advisable.
    - 100uA or less current limiting is advisable during this testing.
    - Testing with an analog curve tracer such as a Tektronix 576 is also recommended to observe subtle fluctuations that may be missed with digital voltage sweeps. These fluctuations can be indicative of fracturing or dendritic growth.
  - Short circuits should have their resistances accurately measured as the resistance of a short correlates with the likely causes of damage.
  - Open circuits should be tested over temperature to test for any intermittent connections.
  - Care should be taken when measuring gain, as the gain parameter generally requires higher test currents and data can be destroyed.

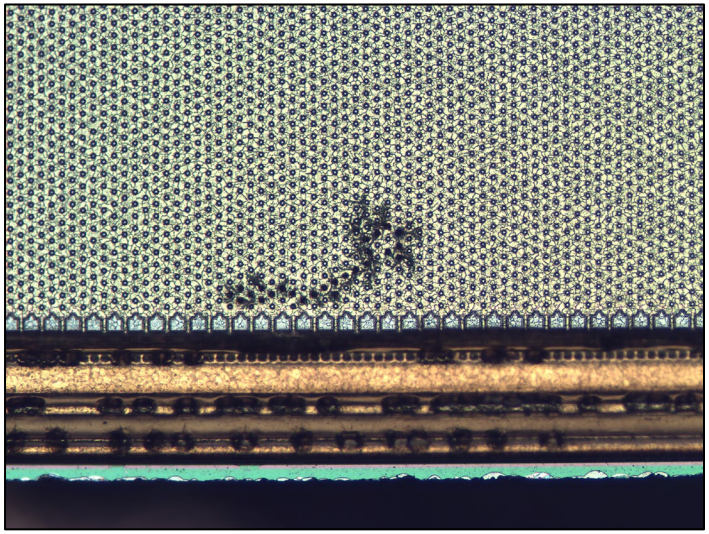
Transistors

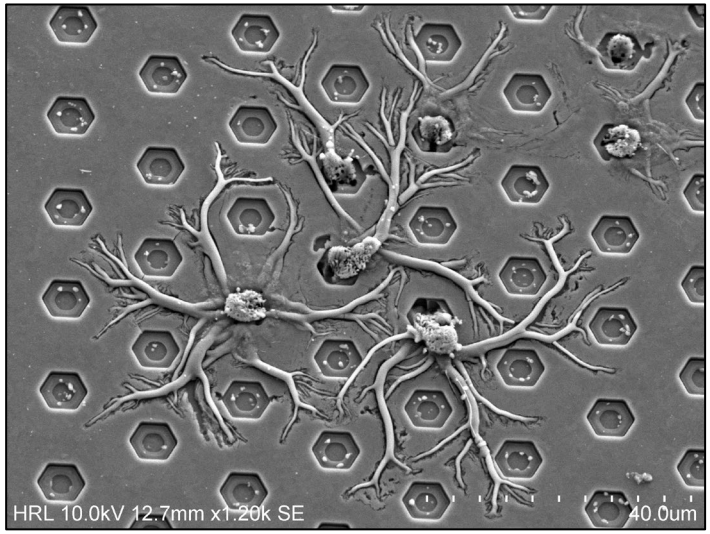
- Electrical overstress
  - Transistor failure analysis often results in EOS as the cause, or most probable cause of failure.
  - Sometimes interpreted as a “catch-all” conclusion, but there can be a lot of information depending on the characteristics of the observed damage.
  - Other times, as shown to the right, the damage is so severe that all evidence of the failure initiation has been destroyed.



Transistors

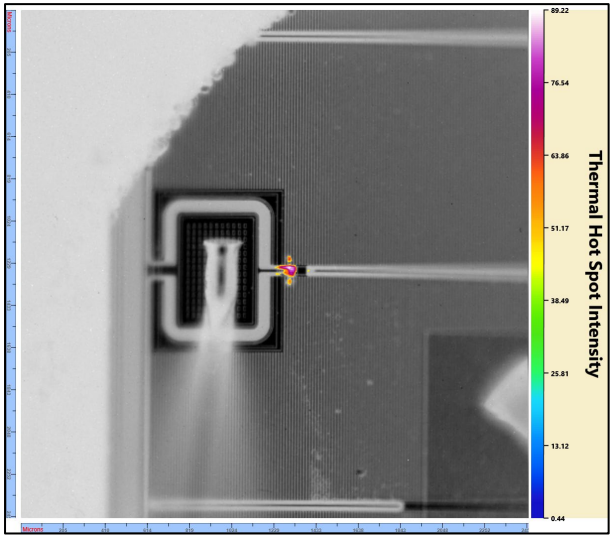
- Electrical overstress
  - High-speed voltage transients in switching circuits are expected and transient suppression is a standard part of circuit design.
  - In some instances, abnormal current draw on the circuit output can result in voltage transients in excess of what is expected, leading to the breakdown of the transistor junctions and short circuiting of the device.
  - The images below show examples of inductive “kickback” transients from a controlled experiment. Normally, these initiation sites become larger alloy sites when power continues to be applied after failure.

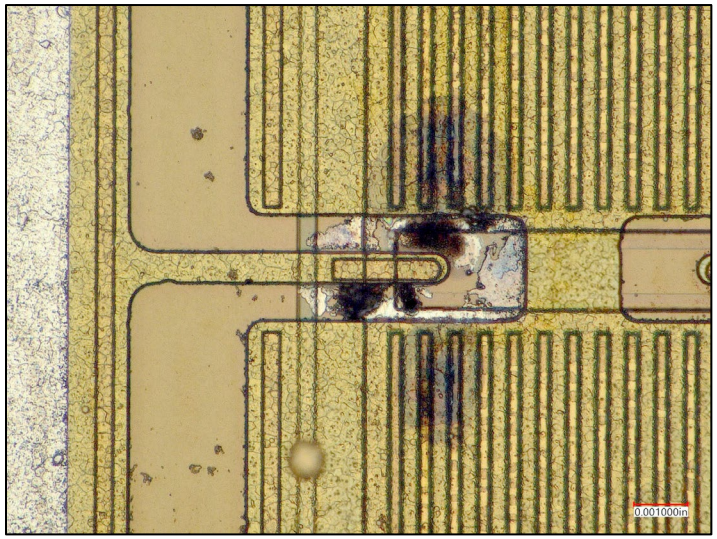




Transistors

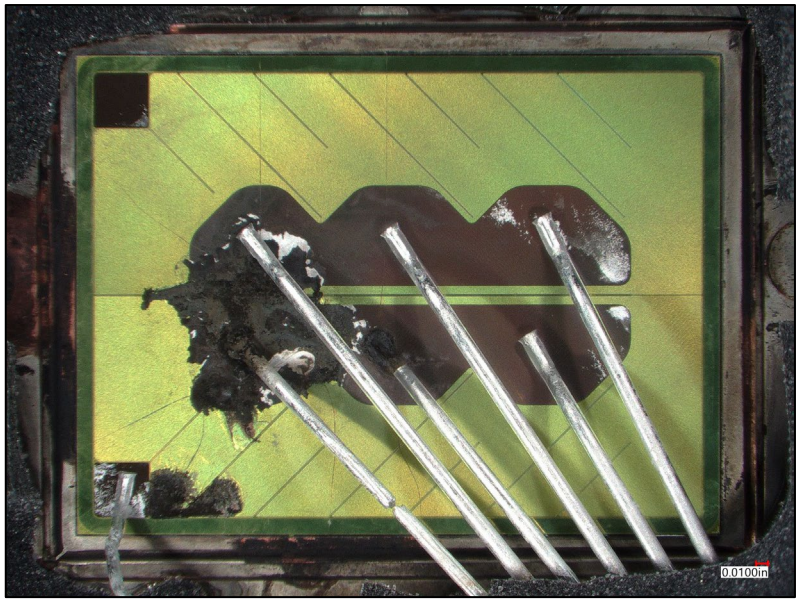
- Electrical overstress
  - Gate damage is also a common result of electrical overstress. The gate structures in FETs are sensitive to over-voltage conditions, but are generally protected by a gate-driver microcircuit.
  - The failure mode is typically a resistive short circuit from the gate to source/drain, with a resistance lower than the source-drain (if the source-drain is involved).
  - Gross EOS of the gate, shown below, is usually obvious once the transistor die is exposed.
    - One of the key differentiators between EOS and ESD.





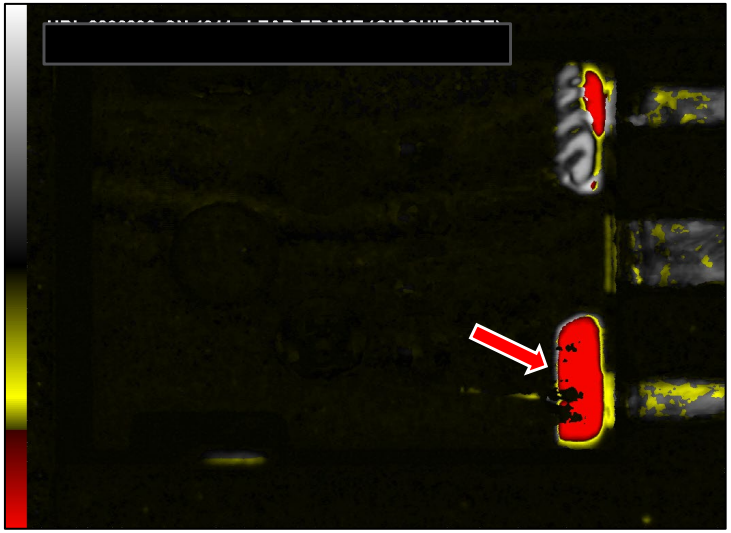
Transistors

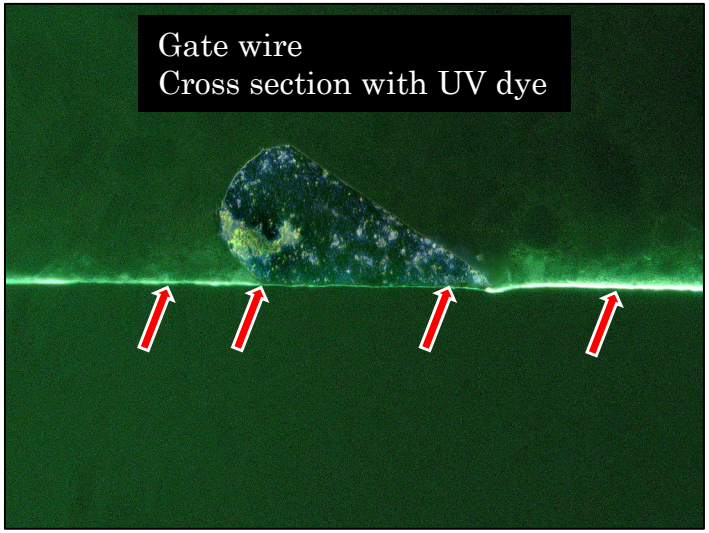
- Electrical overstress
  - Failure due to excessive power dissipation can be the result of several initiators and can be difficult to determine the true cause. Common mechanisms can include:
    - High on-state current in excess of the specified rating
    - Inadequate heat sinking of power-devices
    - Linear-mode operation/operation outside of the specified SOA
      - Can be due to an open circuited gate or insufficient gate drive.
  - The damage is obvious and can sometimes be detected during radiographic inspection.
  - The resistance of the short circuit is often very low; <1Ω.



Transistors

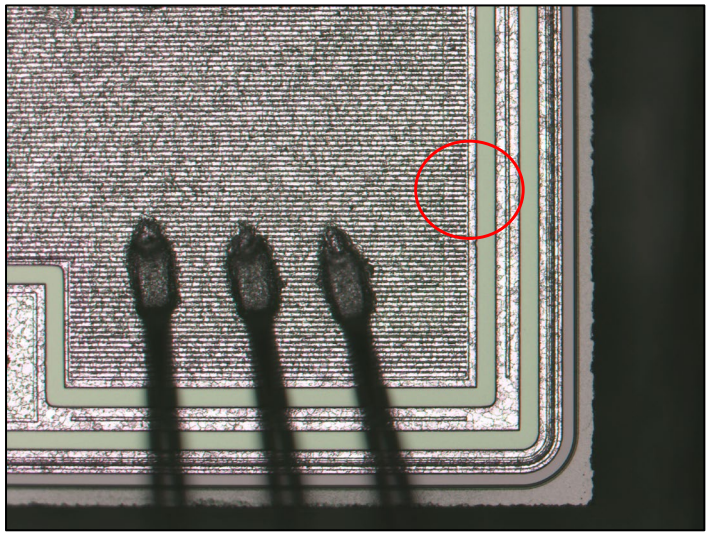
- Open gate – delaminations
  - In FETs, an open circuit at the gate results in a floating gate condition, which generally leads to the destruction of the transistor as it operates in the linear mode.
  - This can occur due to any failure in the gate drive circuit, but is also observed in the transistor itself when lead-frame delamination occurs, pulling the more fragile gate wire from the lead.
  - Scanning acoustic microscopy can identify lead-frame delamination, but beware of water ingress which can result in “false negatives”.

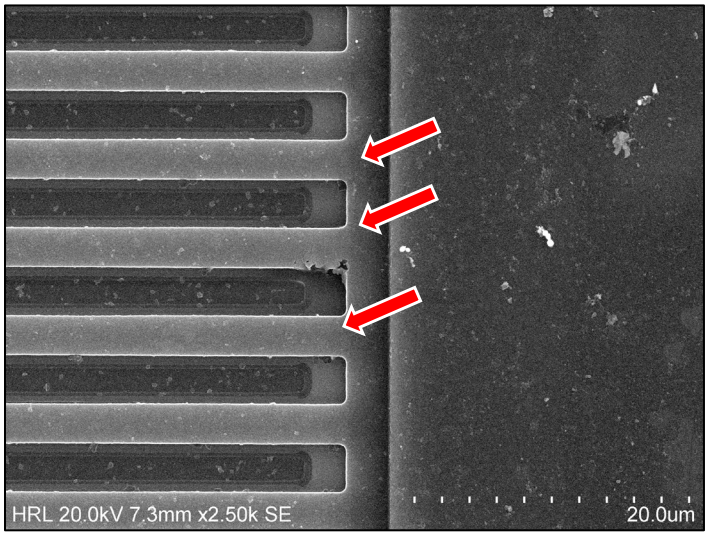




Transistors

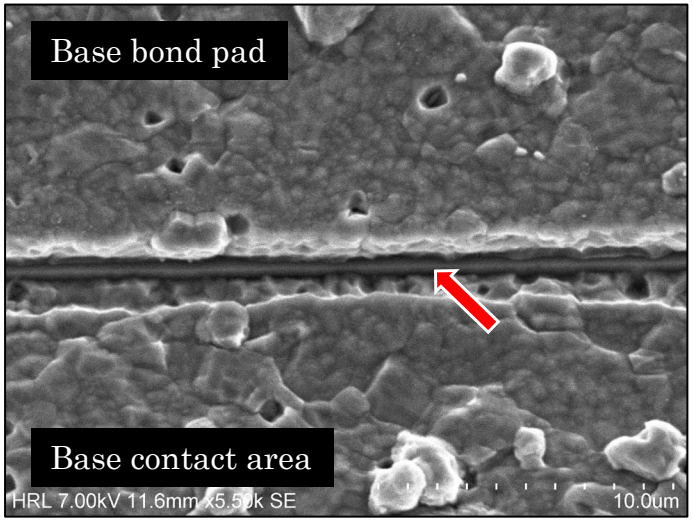
- ESD
  - The gates of FETs are very sensitive to ESD
  - Failures typically present as several 100Ω – kΩ resistive short circuits
  - Damage is often too small to see with optical microscopy, and is often beneath metal layers
  - Failure localization is almost always required, followed by deprocessing of the die layers and SEM inspection.
  - Below image on the left shows no apparent failure site, but ESD damage was discovered beneath the source metal at the edge of the gate fingers.

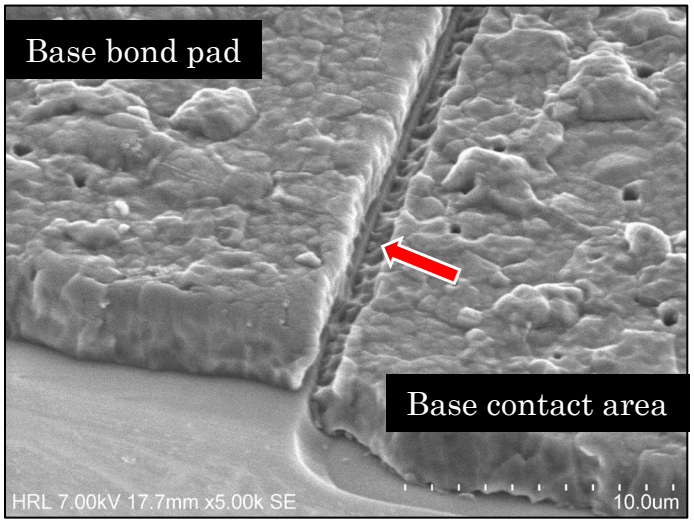




Transistor Failure Analysis - Example

- A transistor had reportedly failed with a temperature sensitive “open circuit”.
- Testing at Hi-Rel confirmed an intermittent open circuit on one of the base pins.
  - This data suggests an open circuit due to a failing bond or *possibly* corrosion of the die metallization, but we will keep an open mind.
  - Steps were taken to analyze these areas, but neither bond failure or corrosion was noted.

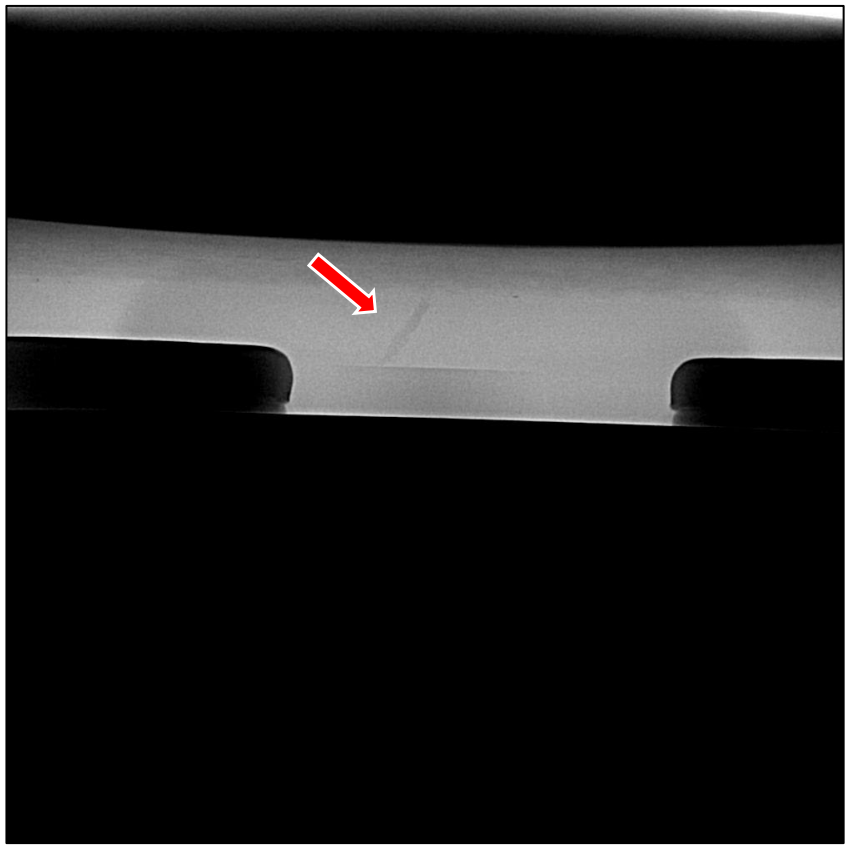




- Detailed SEM inspection revealed a step coverage defect creating an open circuit between the base bond pad and the base contact area.

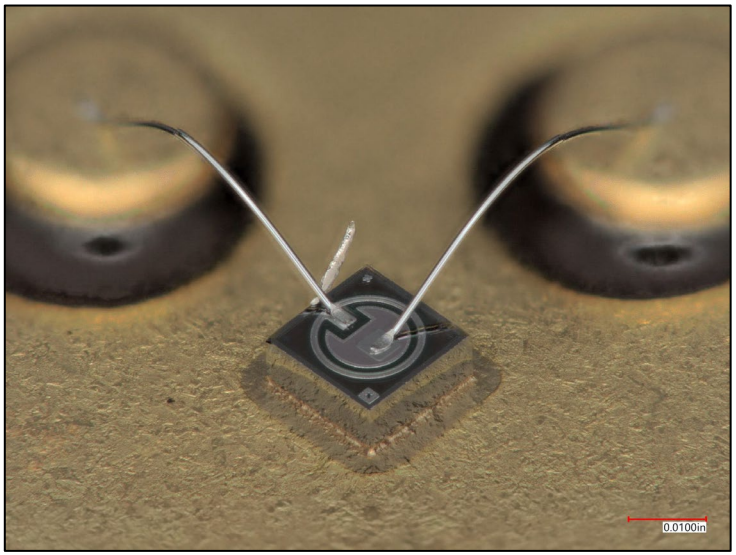
Transistor Failure Analysis - Example

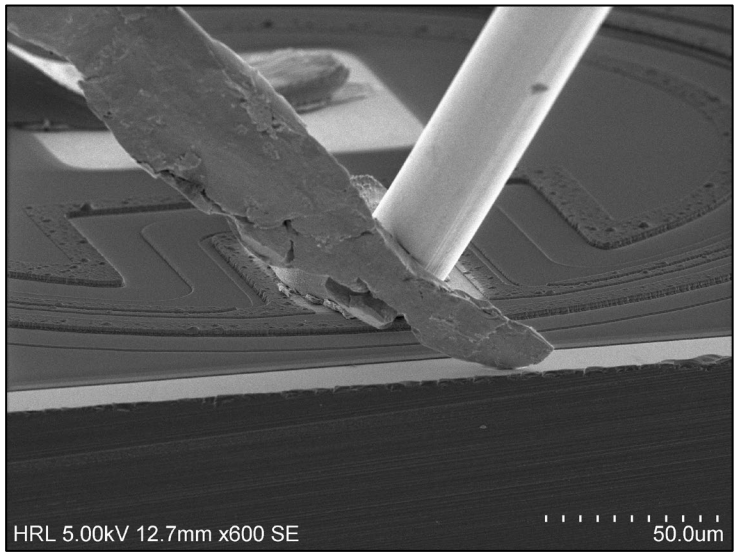
- A metal can “TO” style transistor failed with a short circuit between the base and collector.
  - A base-collector short circuit is a very common failure mode in transistors, but there are many different mechanisms that can cause the failure.
  - This failure resulted in a 14Ω short circuit, and initial radiographic inspection while the component was in-circuit revealed no anomalies.
  - Since metal can packages have a very long history (since the 60s) of potential nickel flakes, radiographic inspection was reperformed after removal of the component from the PCBA with low kV and high contrast.
    - A nickel flake was identified, bridging the base wire to the non-passivated die edge; the collector.



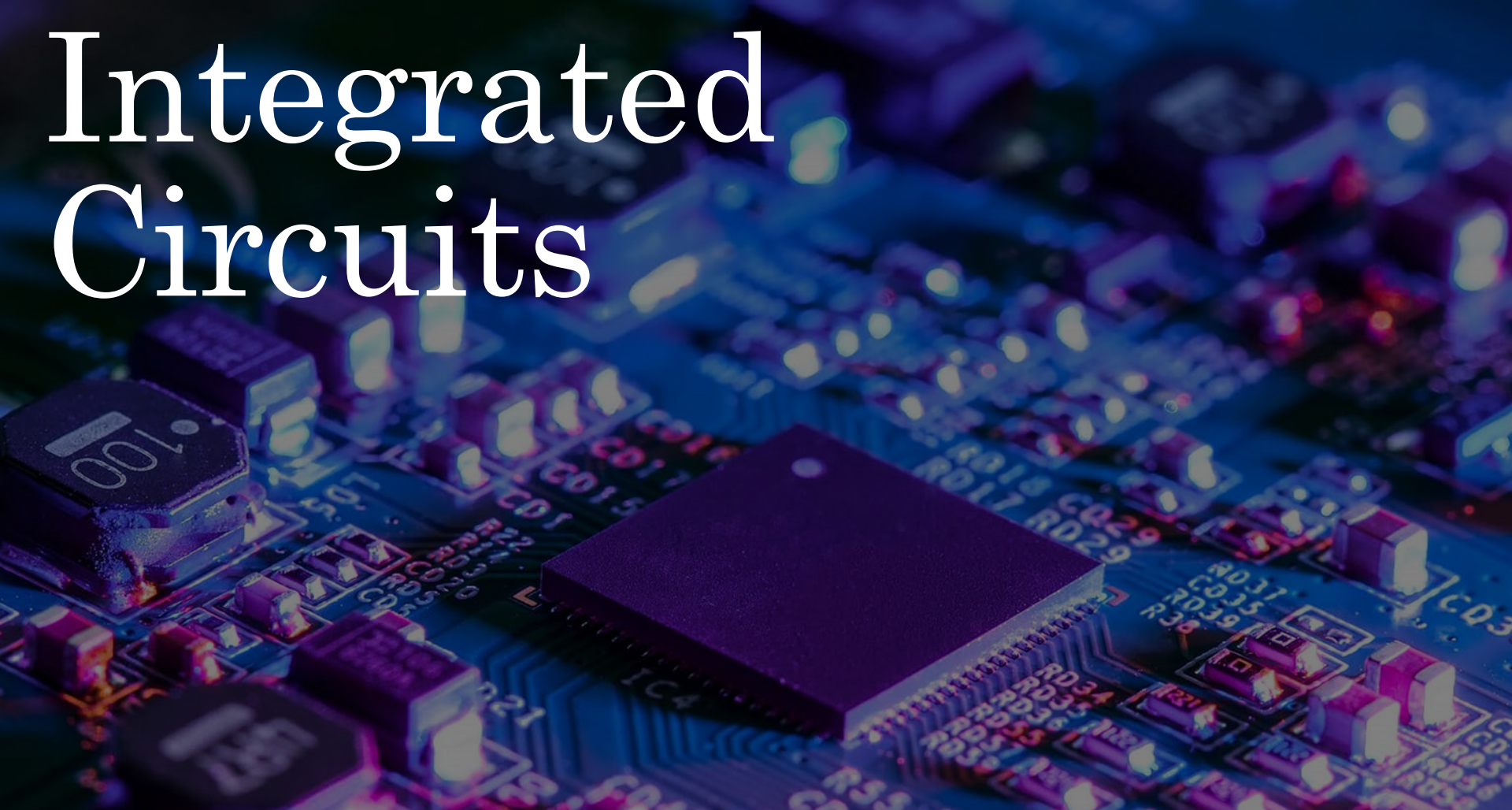
Transistor Failure Analysis - Example

- Nickel flakes have resulted in failures for decades
  - They can remain adhered to the internal surfaces of the packages, eventually dislodging.
  - Radiographic inspection and PIND are often not able to detect nickel flakes due to their low density.
- Hi-Rel continues to perform nickel flake inspections on metal lidded components to confirm that no process changes have occurred that may result in nickel flakes.





Integrated Circuits



Integrated circuits can fail due to nearly any of the previously discussed mechanisms. Because of this, failure history and supporting information is valuable for the analysis. Depending on your lab capabilities, testing and failure localization may be a challenge.

https://www.waferworld.com/post/what-are-the-components-of-an-integrated-circuit

Integrated Circuits

- Once board-level defects/damage are ruled out, the challenge with IC failure analysis is failure isolation/localization.
  - The failure analysis approach, *in most cases*, relies on isolating the failure to specific pin, or combination of pins.
  - If a component fails functional testing but exhibits no pin-pin degradation, the complexity of the analysis dramatically increases.
    - In some cases, failure analysis from the component manufacturer may be recommended as they have the capability to analyze devices during full functional testing.

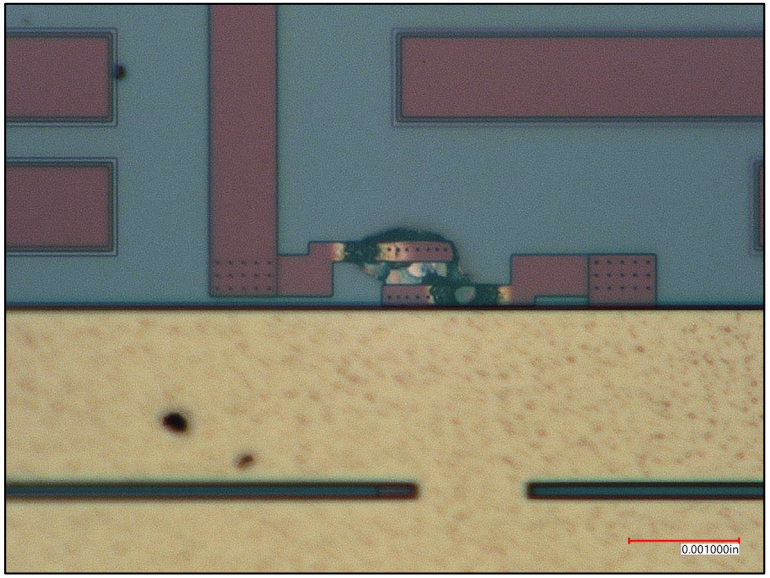
Integrated Circuits

- Comparison testing can be performed between a suspect sample and a known functional sample.
  - Automatic curve tracing is preferred, but not always possible due to package style or condition.
  - Manual curve tracer comparison can be performed
  - Ohmmeter testing can determine if short circuits or open circuits exist but does not always reveal more subtle degradations.
    - I/V curve characteristics are significant clues in FA.
- After failure verification and isolation, the component can be analyzed in a manner similar to other part types, where all methods may be applicable.

Integrated Circuits

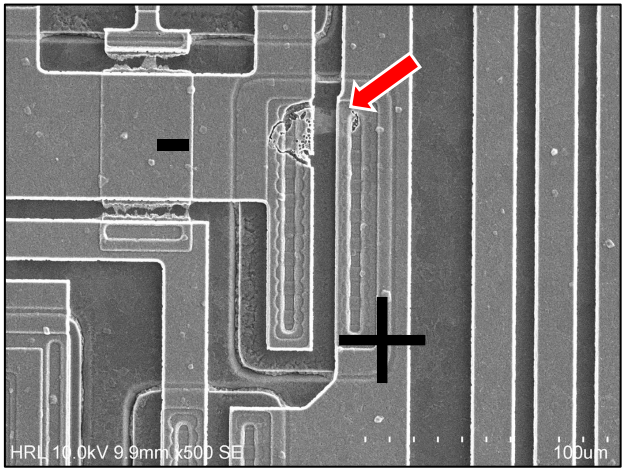
- Electrical overstress
  - Similar to the previous discussion of EOS in passive components, EOS can occur in integrated circuits and, depending on severity of the damage, can prevent a definitive determination of the original cause of failure.
    - The cause of less catastrophic EOS can be determined in most cases.
    - Voltage transients, high current conditions, polarity of failure condition can often be estimated/determined.

In the image to the right, EOS was identified as the cause of failure. The failure was the result of high current, less than the fusing current of the 1mil gold wire, ~1.5A. No evidence of arcing or breakdown was discovered, indicating the failure was strictly due to a high current condition.

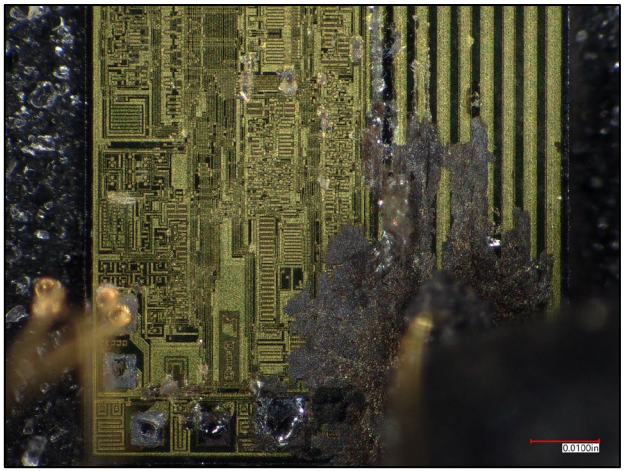


Integrated Circuits

In the image to the right, an overvoltage condition occurred resulting in the failure of the diode structure. The migration of the metal in this image follows the electron flow, so it could be determined that the area to the left was more negative.

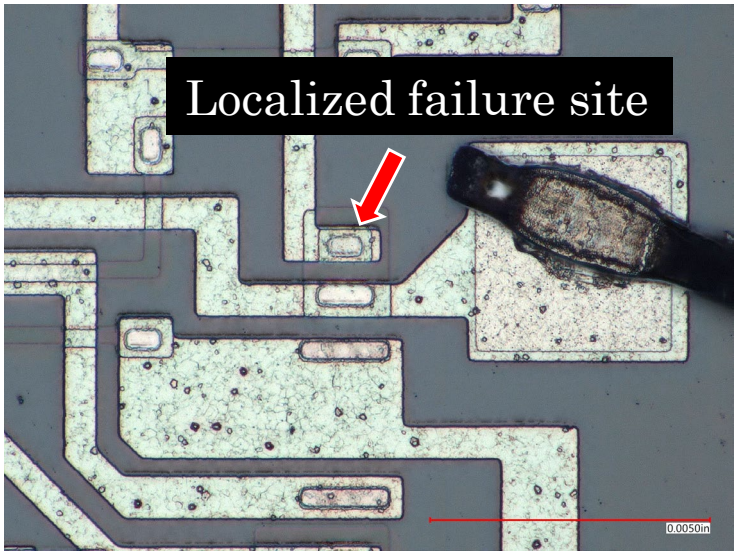


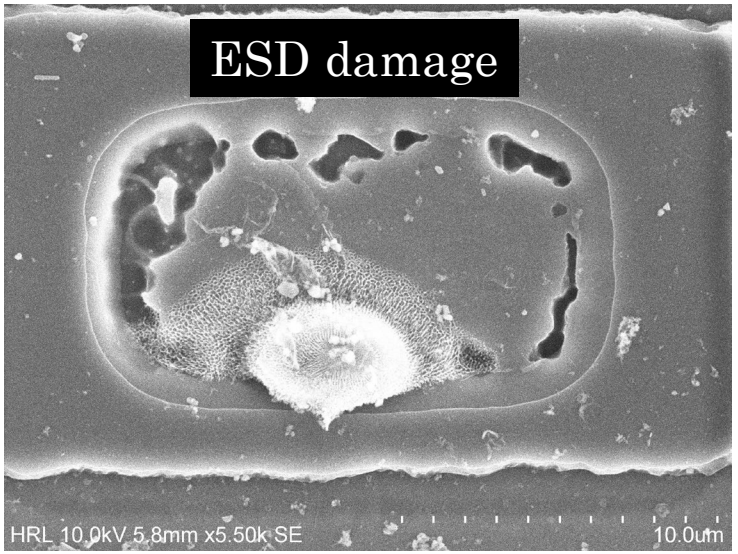
In the image to the right, the extent of damage was too severe to determine the true cause of failure. The root cause could only be speculated based on the severity of the damage in the output transistor.



Integrated Circuits

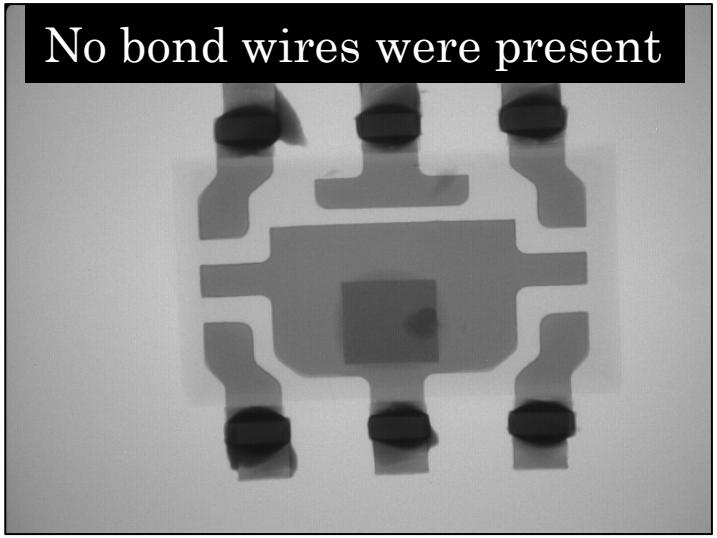
- Electrostatic Discharge
  - Integrated circuits can be very sensitive to damage from ESD.
  - ESD failures generally result in relatively high resistive short circuits or degraded PN junction in the sensitive I/O structures
  - Damage from ESD is typically not obvious during optical microscope inspection, requiring failure localization and delayering.





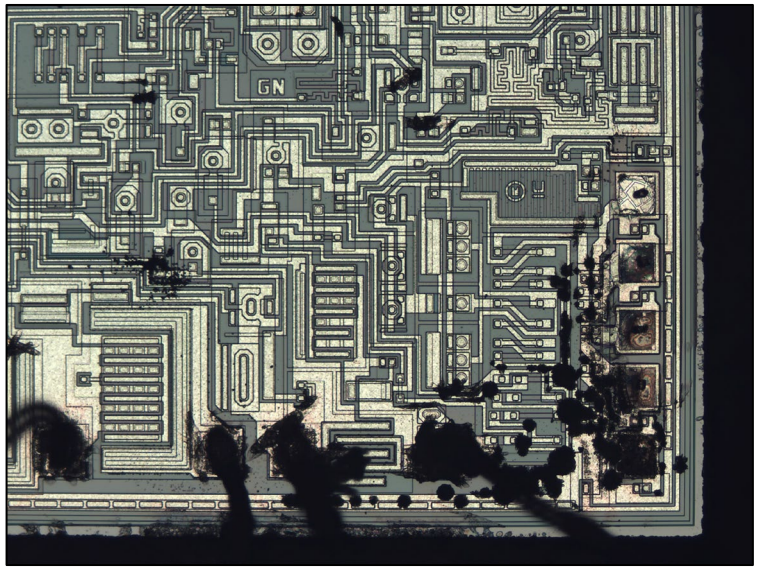
Integrated Circuits

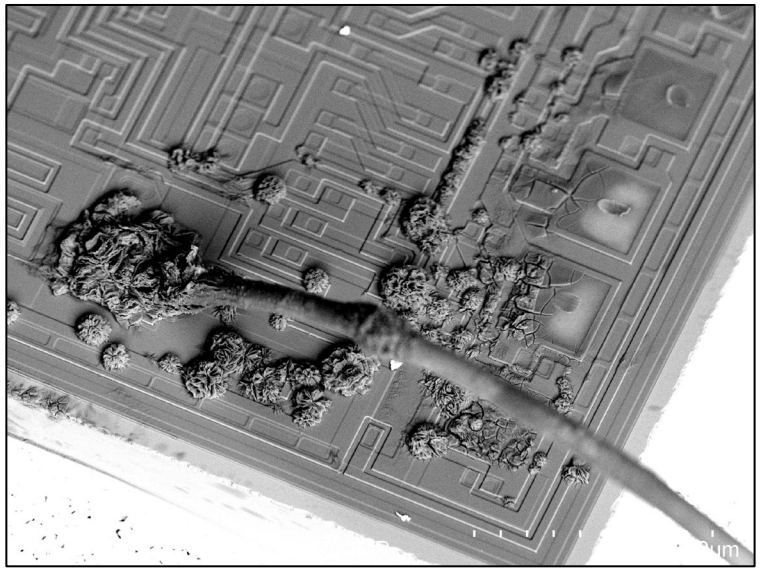
- Counterfeit components have been a problem in the electronics industry for many years. With recent supply chain shortages, some companies have been forced to procure components from less reliable sources.
- Counterfeit detection is performed by comparing the construction of each aspect of a device to a known good sample.
  - This includes part markings, dimensions, lead frame structure, test data, die layout and markings, etc.



Integrated Circuits

- Corrosion
  - Die metallization corrosion can occur when the hermeticity of the package is compromised.
    - In some rarer cases the corrosive material can be induced during manufacturing, prior to sealing the component.
  - The failure presents as open circuited metallization, which can appear as a complete open circuit or an abnormal I/V curve.



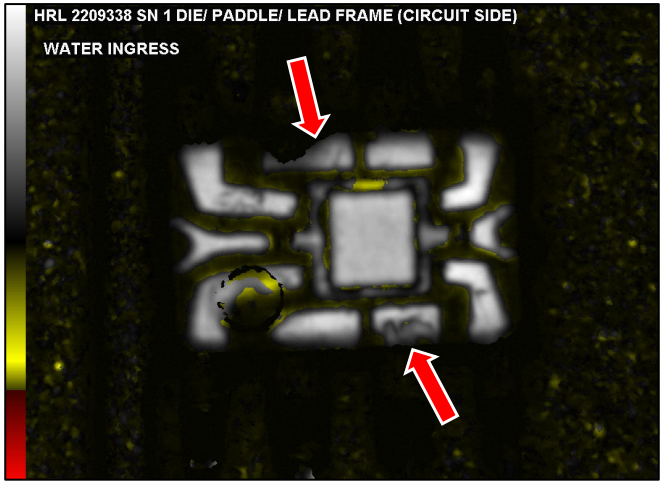


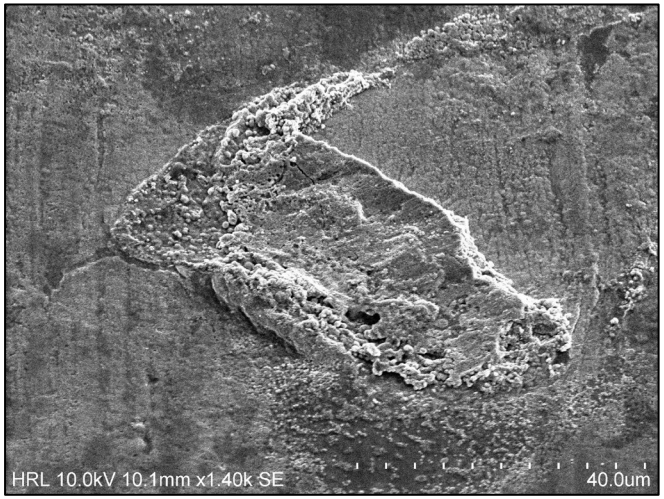
Integrated Circuits

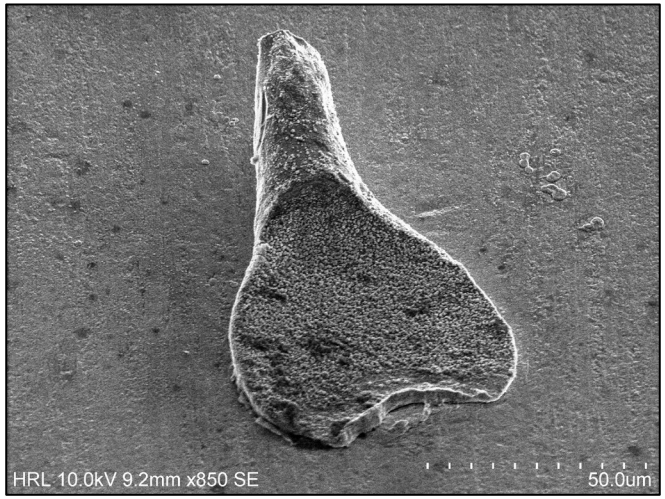
- Copper wire corrosion
  - As copper bond wires become more common than gold wires in plastic components, there are some drawbacks that need to be considered.
  - The most susceptible area of a copper wire in terms of corrosion is the lead-frame bond.
  - Hi-Rel has analyzed numerous plastic components that present an open circuit, sometimes intermittently.
  - Detailed radiographic inspection of the bonds can sometimes be inconclusive.
  - The failure is ultimately due to delamination of the potting material from the lead frame surface, and as such, scanning acoustic microscopy is recommended when copper wire corrosion is suspected.
    - As previously discussed, beware of water ingress masking delamination.
  - The wires corrode as a result of contamination becoming trapped in the delaminated interface.
    - Gold wires were not susceptible to corrosion even when delamination was present.
    - In some cases, a galvanic cell is formed from the dissimilar metals, accelerating the corrosion.

Integrated Circuits

These images show water ingress into the delaminated interface (upper right), a corroded copper stitch bond (lower left), and an intact bond showing the normal appearance (lower right).



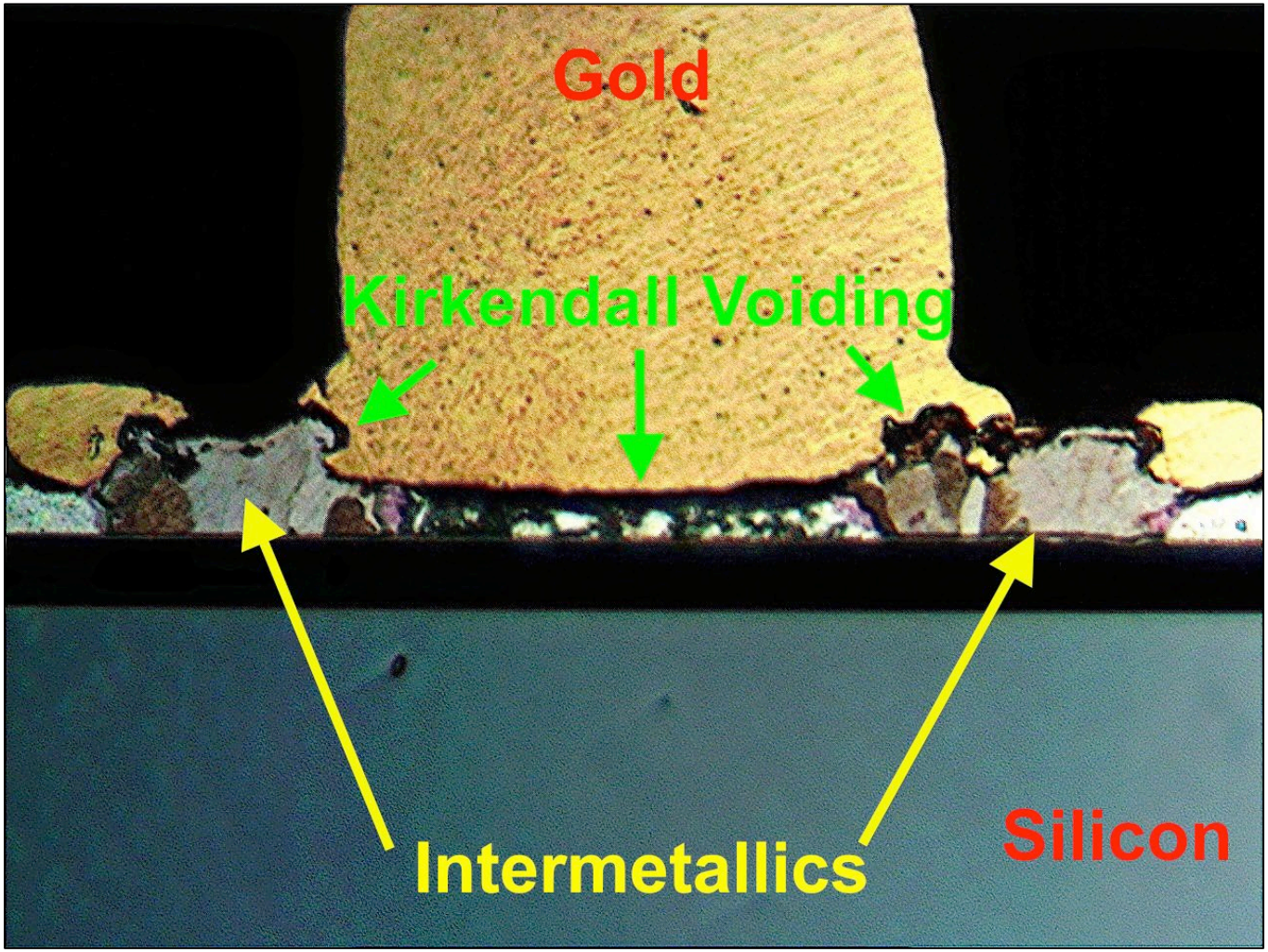




Integrated Circuits

- Kirkendall Voiding
  - When gold wires are bonded to an aluminum surface, or vice versa, a gold-aluminum intermetallic is created. The formation of this intermetallic region is normal, and indicative of a quality bond.
  - With time and temperature, the intermetallic region can grow due to the different growth rate of the various alloys in the bond.
  - Eventually voiding occurs at the interface between the AuAl intermetallics and the pure gold of the ball bond, leading to a bond failure.
    - Electrically, this can result in a resistive connection or an open circuit.
  - Bond pad contamination, typically oxidation, results in a lower reaction area during bonding and introduces impurities into the bond, which can become nucleation sites for voiding and accelerates the failure of the bond.
  - Identifying failures due to Kirkendall voiding can sometimes require testing over temperature to reveal the temperature sensitive bond lifts.

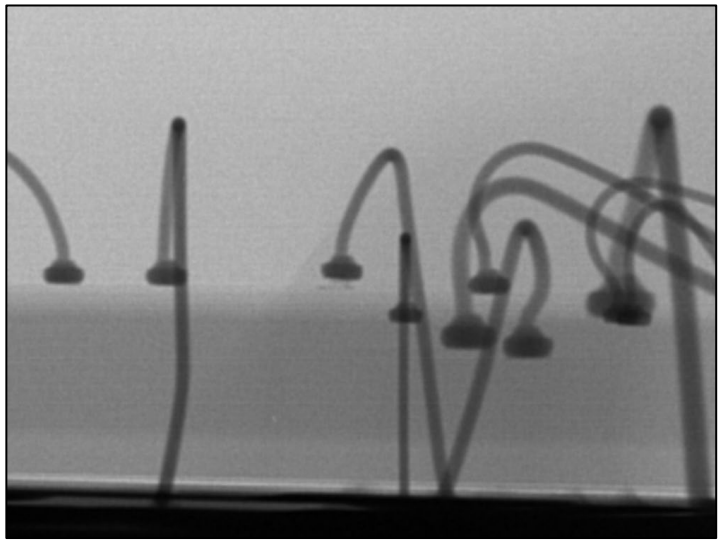
Integrated Circuits

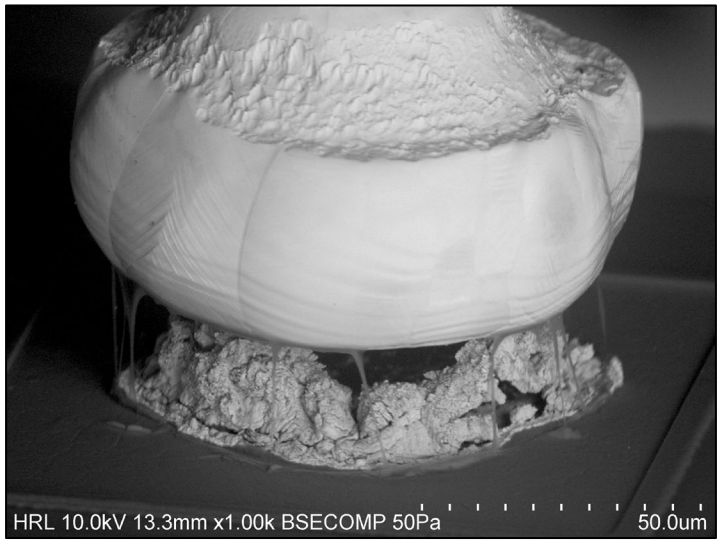


Integrated Circuits

The below images show a gold ball bond that failed due to Kirkendall voiding. The radiographic inspection (left) revealed a lifted ball bond with some gold remnants on the die surface, a classic indicator of this failure mechanism. The SEM image (right) revealed the lifted ball bond, resulting in the open circuit.

This component was in service for nearly 20 years.





Conclusion

- This presentation is intended as a brief overview of component failure analysis. Each component type can present its own unique challenges and there are always surprises.
- We at Hi-Rel love discussing failure analysis and are more than happy to help with any questions you or your team may have.