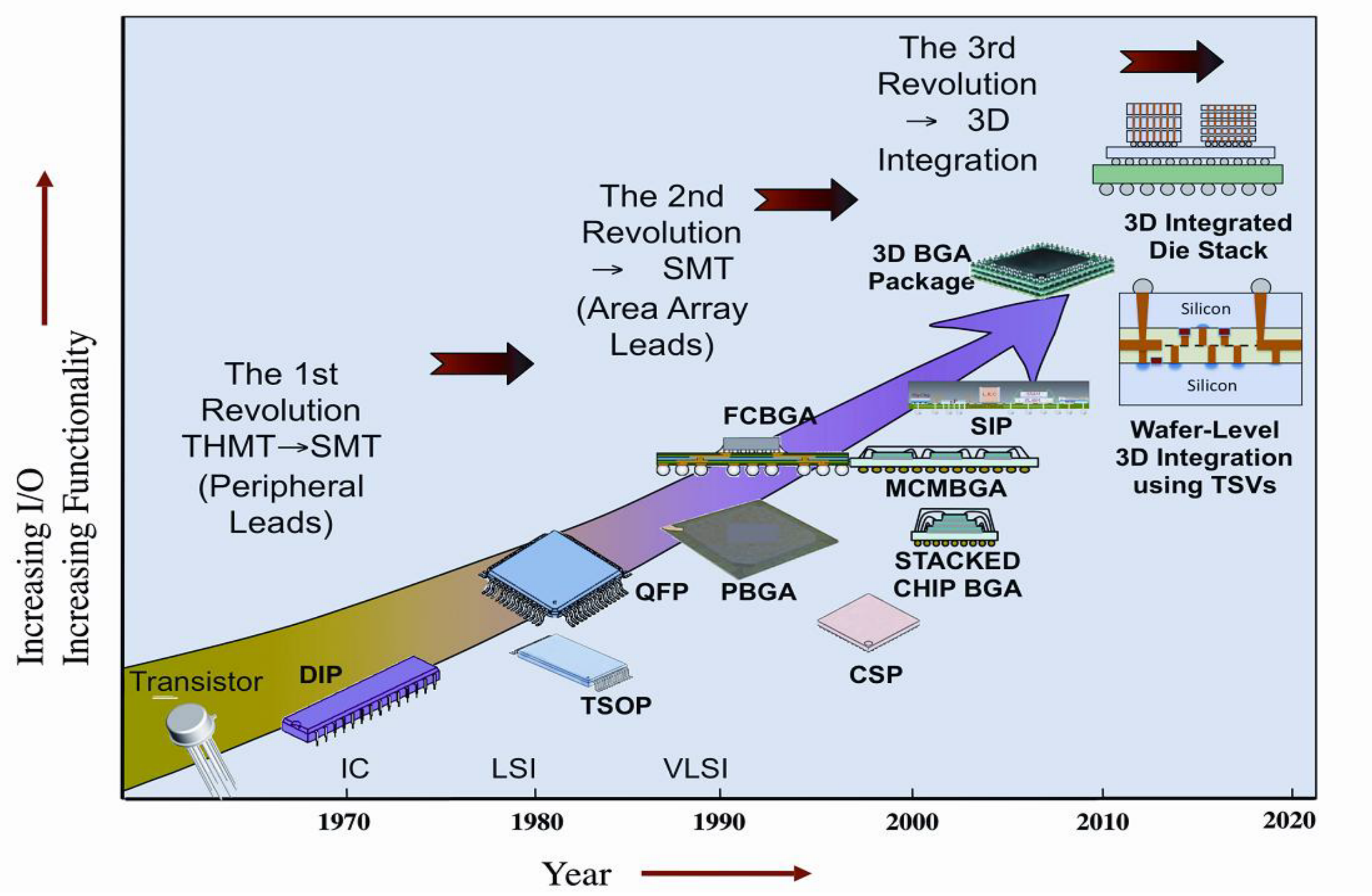
Materials and Processes for Non-Hermetic Packaging

Polymers in Semiconductor Packaging

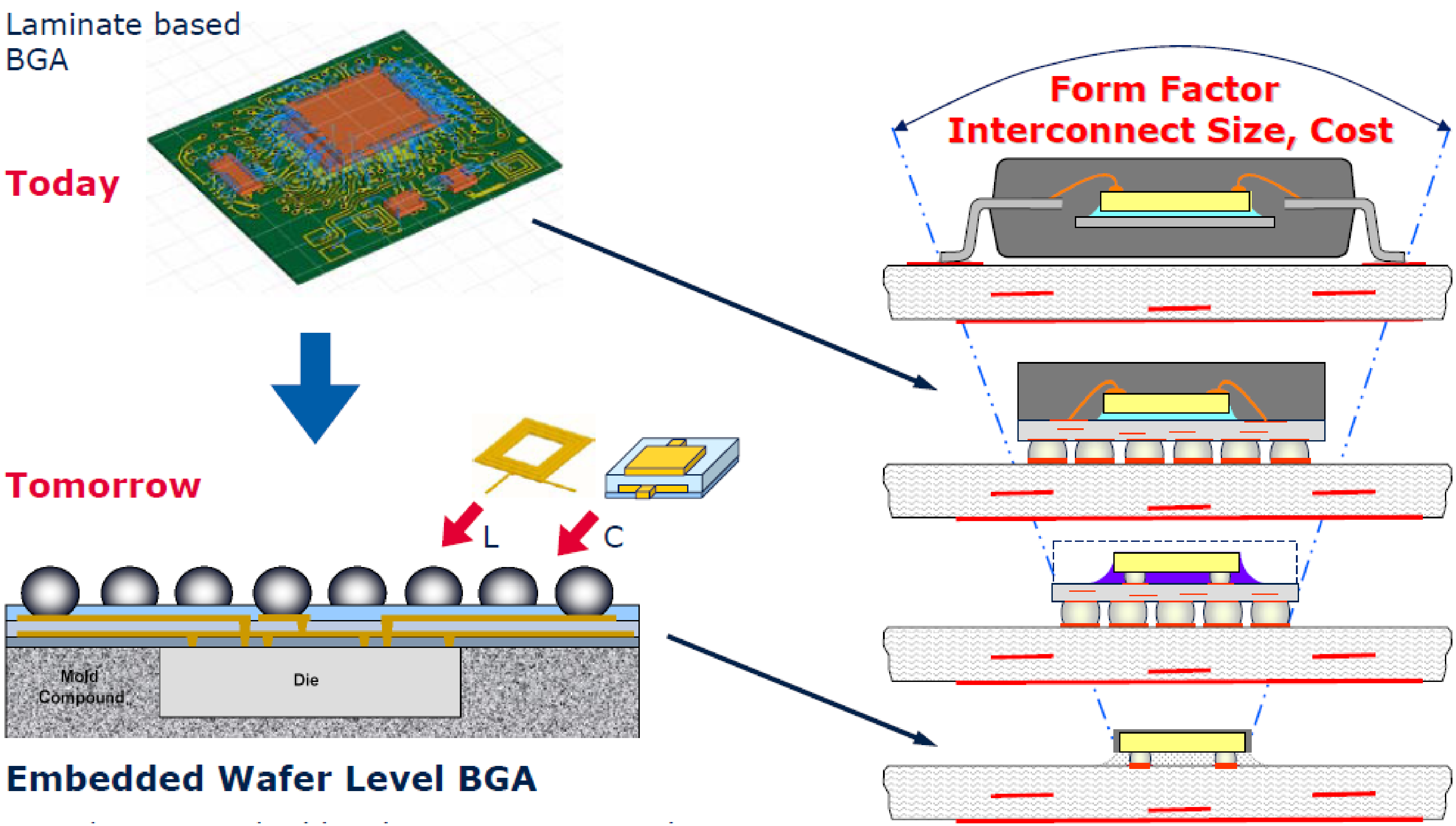
There are some tough material requirements

- Low viscosity to flow (die attach, mold compounds and underfills)
- Wide range of cure profiles
  - Thermal (oven, snap and spot cure) and UV cure
  - Partial cure (B-stage) for printable pastes and films
- Tailored modulus depending on the application
- Low coefficient of thermal expansion (requires fillers)
- High temperature stability for lead-free reflow profiles
- Low moisture absorption (JEDEC pre-con)

Non-Hermetic Packaging Evolution

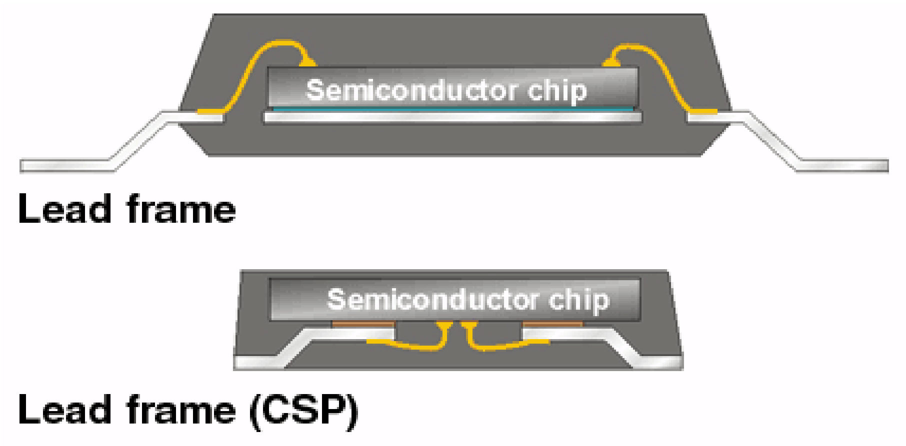


Non-Hermetic Package Evolution

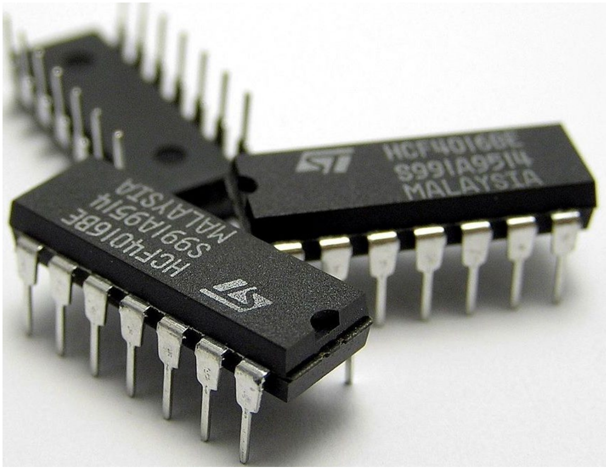


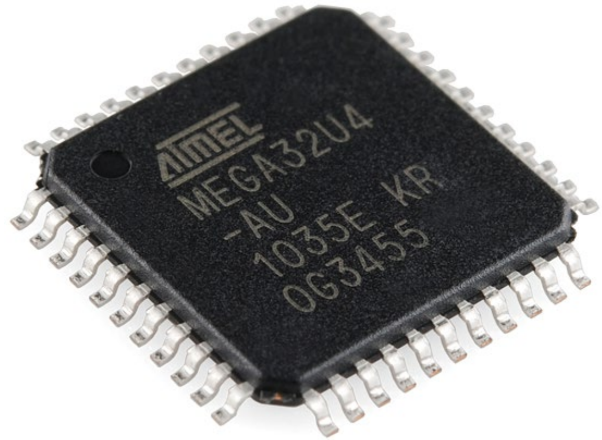
Source: Infineon

Leadframe Packages



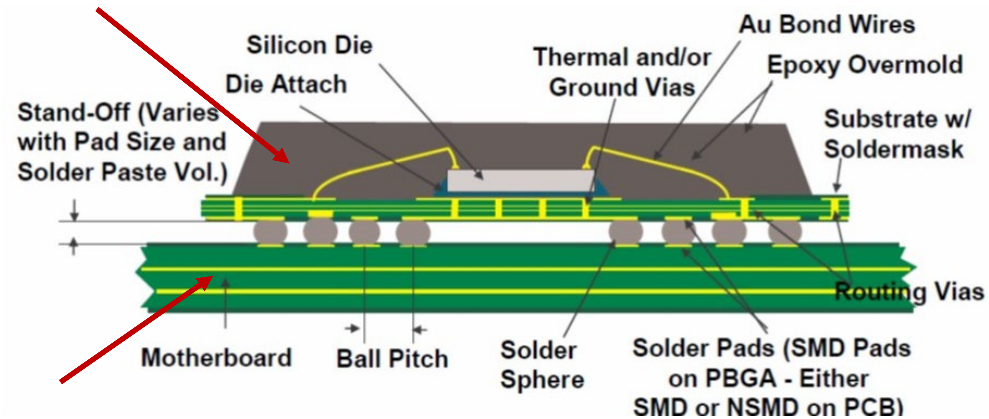
Materials:
Metal leadframe
Die attach adhesive (epoxy and maleimide/acrylate)
Epoxy mold compound
Gold or copper wire





Plastic Ball Grid Array (PBGA)

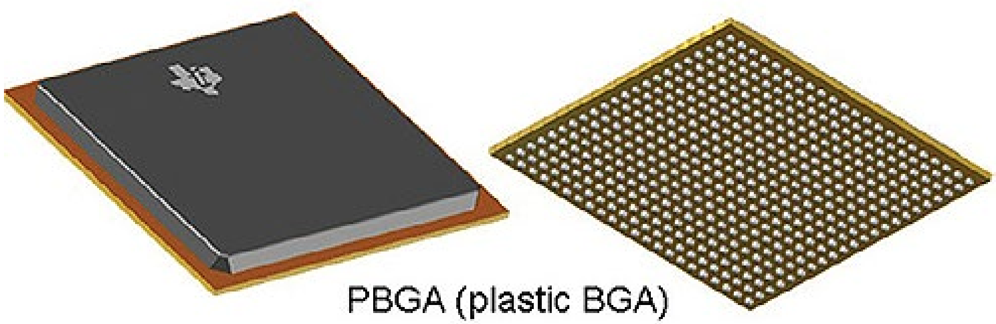
Packaging Level 1



Packaging Level 2

Materials:

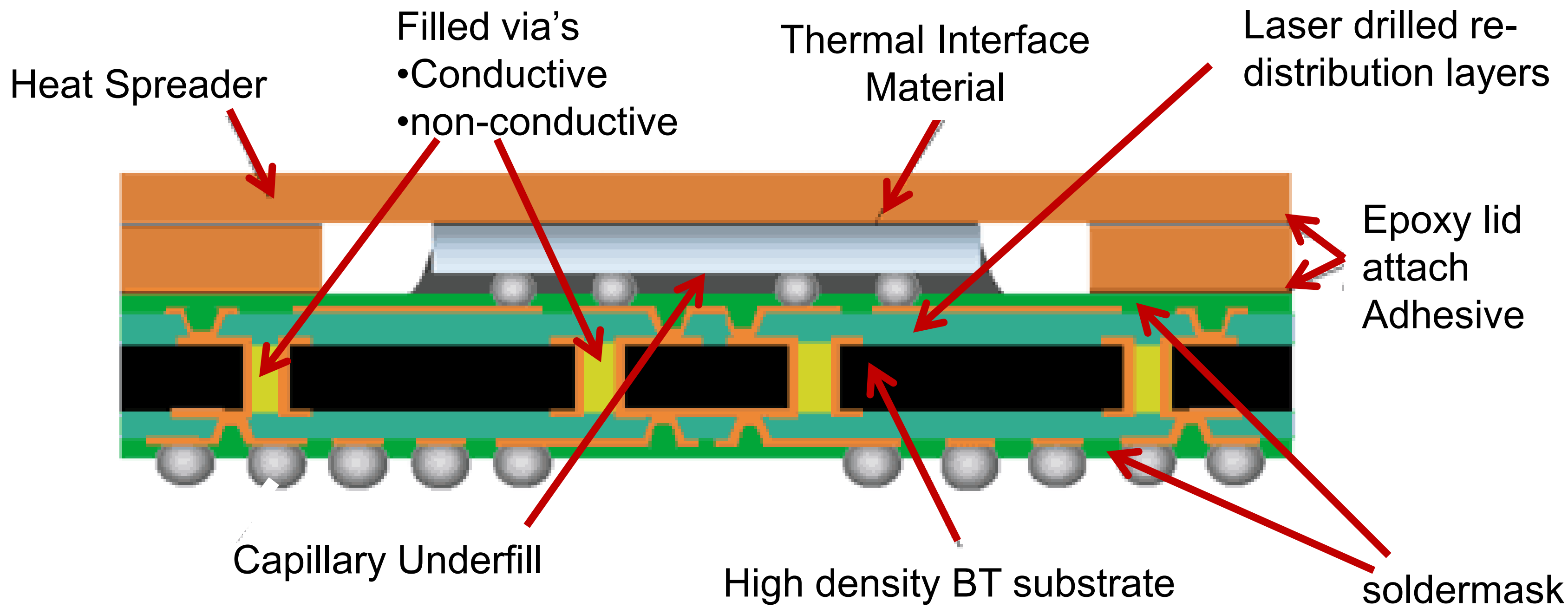
Bismaleimide triazine epoxy substrate
Die attach adhesive
Epoxy mold compound
Gold or copper wire bonded



Packaging Level 1 – semiconductor encapsulation including substrate

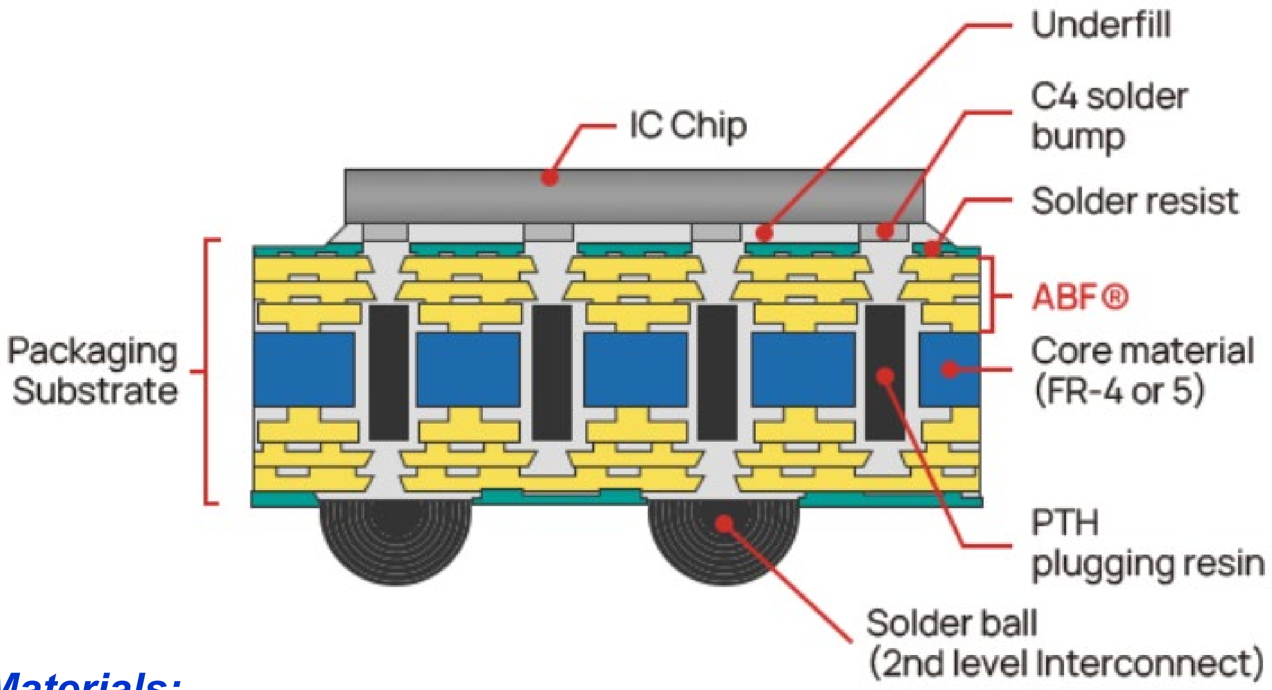
Packaging Level 2 – Printed Circuit Boards

Multiple Polymers Used



- Polymer film redistribution layers
- Bis-maleimide triazine epoxy (BT) laminate used in flip chip substrates
- Epoxy/acrylate soldermask
- Silicones/thermal greases in TIM materials
- Epoxy or cyanate ester/epoxy used in capillary underfills

Flip Chip BGA on HDI Substrate



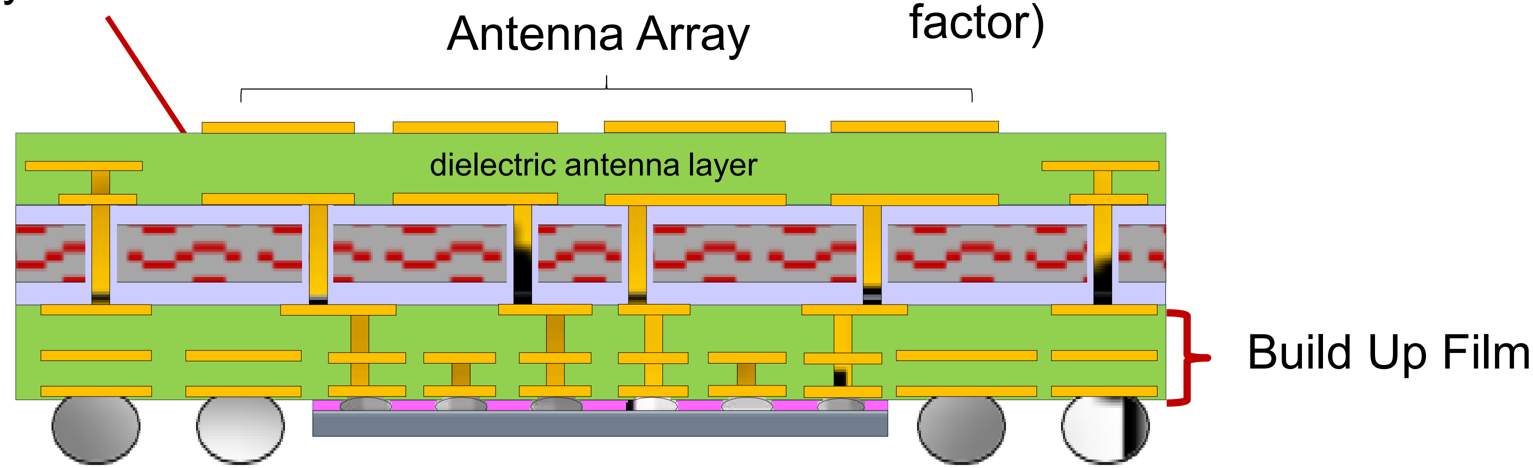
Materials:

Epoxy/glass fabric laminate (FR-4 or FR-5)
Epoxy Underfill
Epoxy mold compound
Epoxy or cyanate ester build-up film (ABF®)
Copper pillars or bumps

ASE Package with Integrated Antenna

D_f of dielectric antenna layer is driver

D_k – dielectric constant
D_f – dissipation factor (or loss factor)



Printed Circuit Board (PCB) process using advanced low D_k and D_f materials for antenna layer and build up films

Source: Advanced Semiconductor Engineering (ASE)

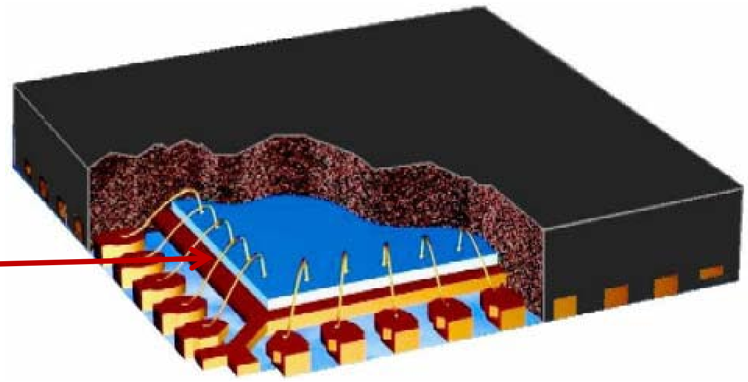
Overview of Polymers Used in Electronic Packaging

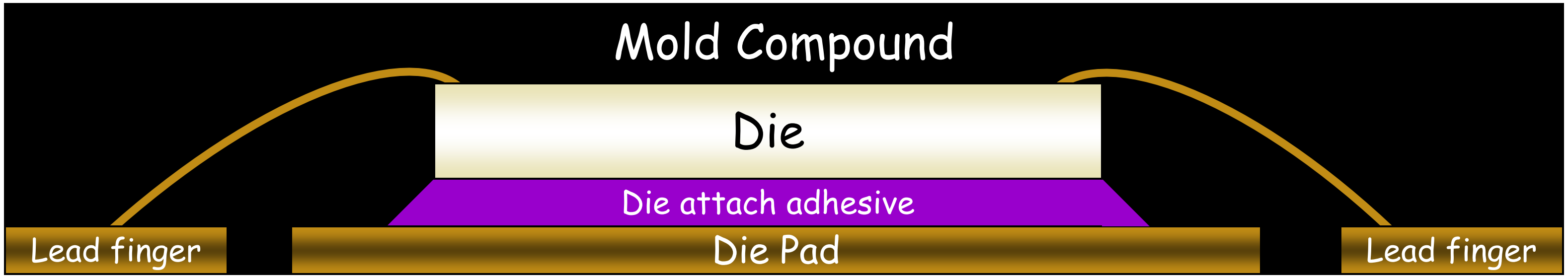
Uses of Polymers in Packaging

- Die attach adhesives
  - Conductive
  - Non-conductive
  - Dispensable paste and film formats
- Underfills
  - Capillary and wafer level (no-flow)
- Mold compounds
- Laminate substrates
  - Base laminate
  - RCC or film redistribution layers for laser via structures

Polymers in Leadframe Packages

Depending on the metal leadframe used, epoxy-based die attach or BMI/acrylate die attach adhesives are used



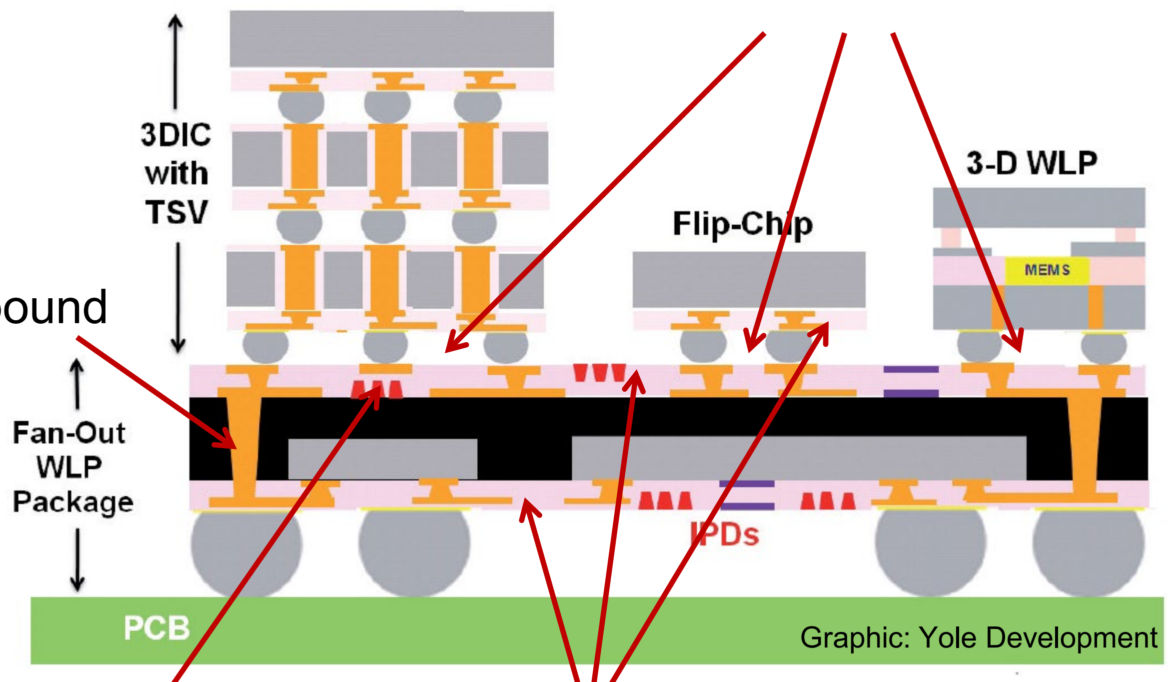


Mold compounds are typically epoxy-based

Polymers are Key Integration Enablers

Underfills

Thu-Via technology
- Laser friendly mold compound



Integrated passive devices

Redistribution layers

What is a Polymer?

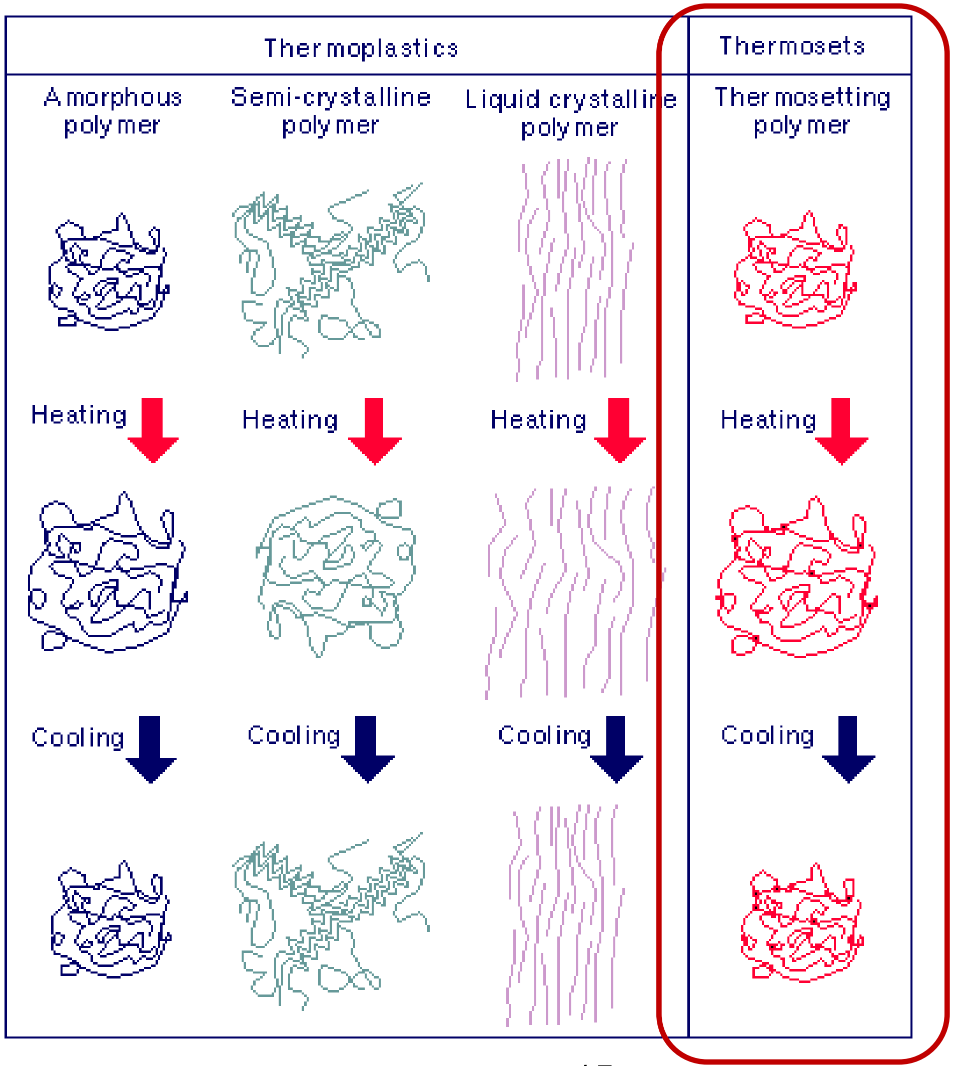
From the Greek word poly – meaning many and meros – meaning units

Merriam – Webster online dictionary;

"A chemical compound or mixture of compounds formed by polymerization and consisting essentially of repeating structural units."

As we will see, polymers gain their unique and useful properties by being long molecules with specific chemical repeat units.

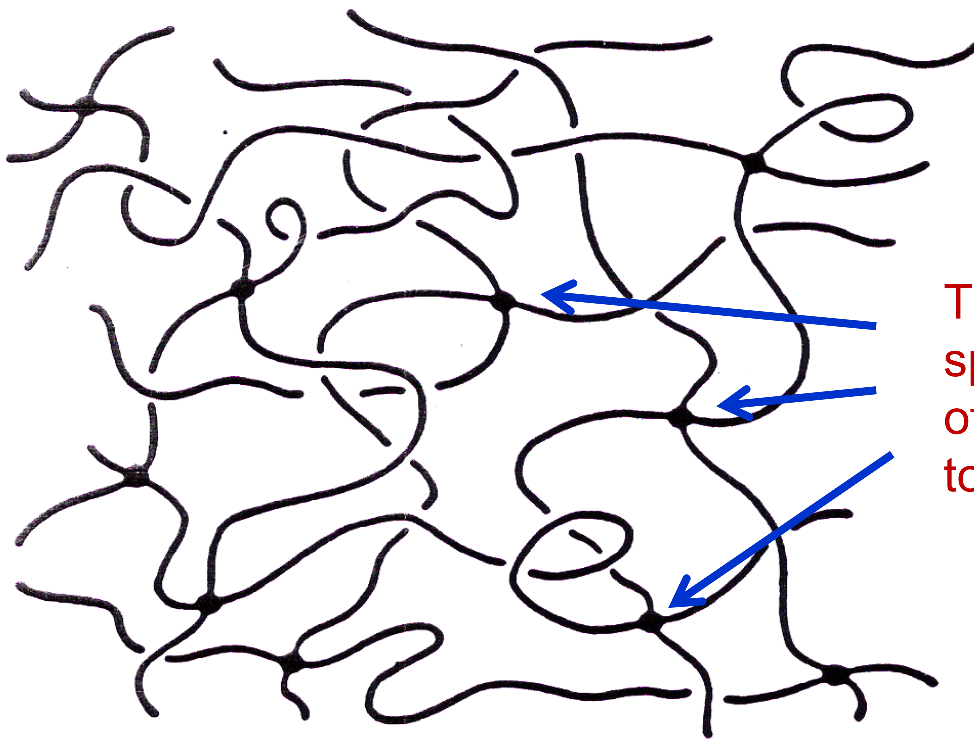
Thermoplastics vs. Thermosets



Thermosets expand on heating, but no phase change occurs

Polymers Can Have Different Morphologies

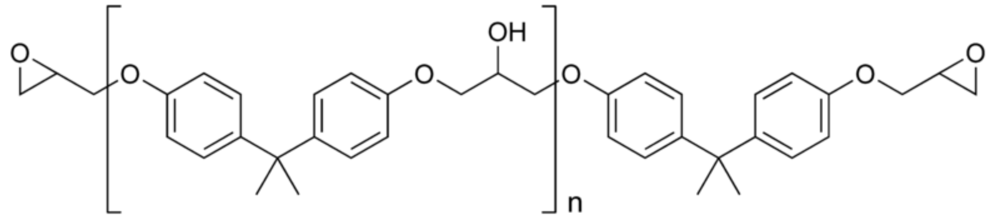
Thermoset crosslinked polymers



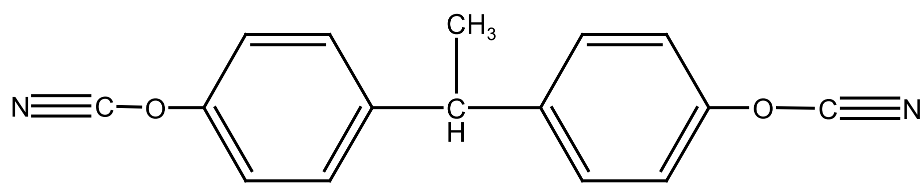
Think of the bowl full of spaghetti, but now some of the chains are tied together (crosslinks)

Thermoset Polymers

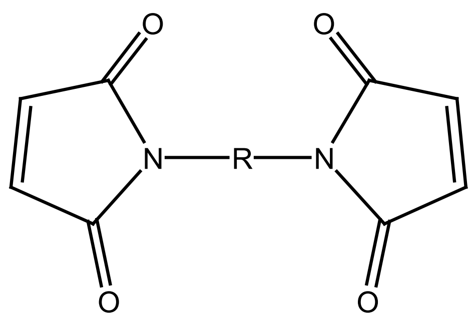
Epoxy



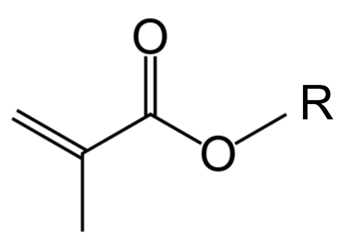
Cyanate Ester



Bismaleimide

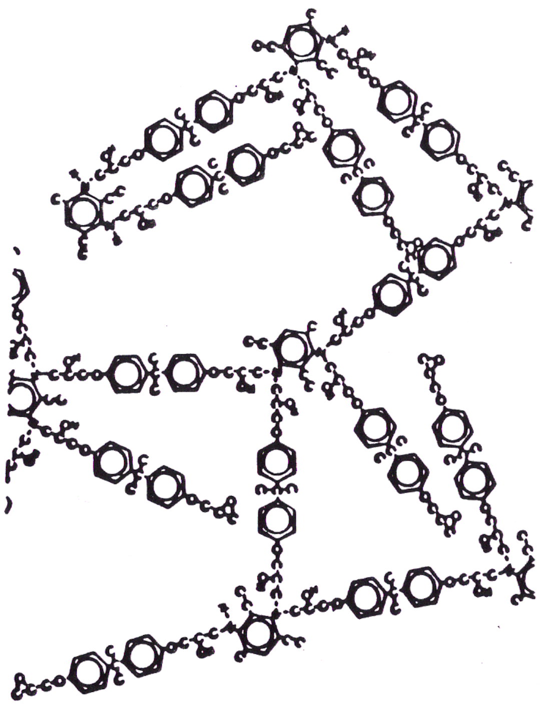


Acrylate

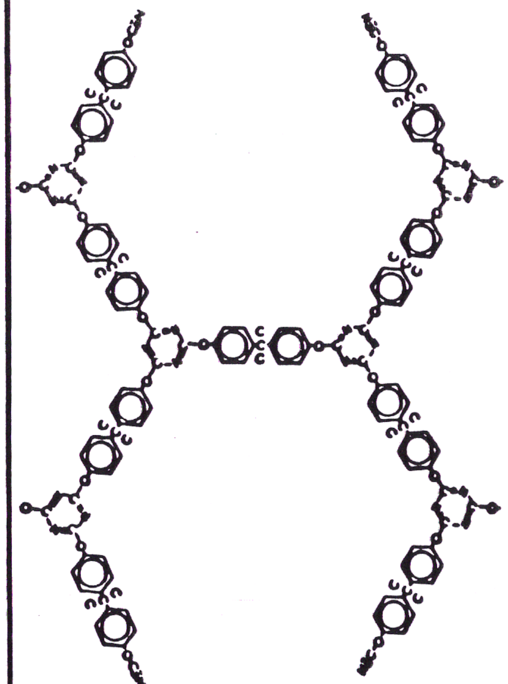


Examples of Different Network Structures

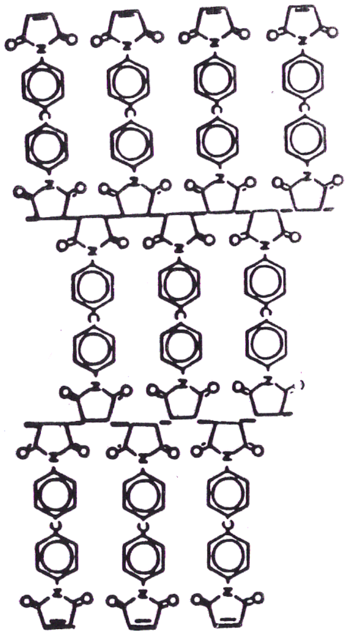
Epoxy



Cyanate Ester

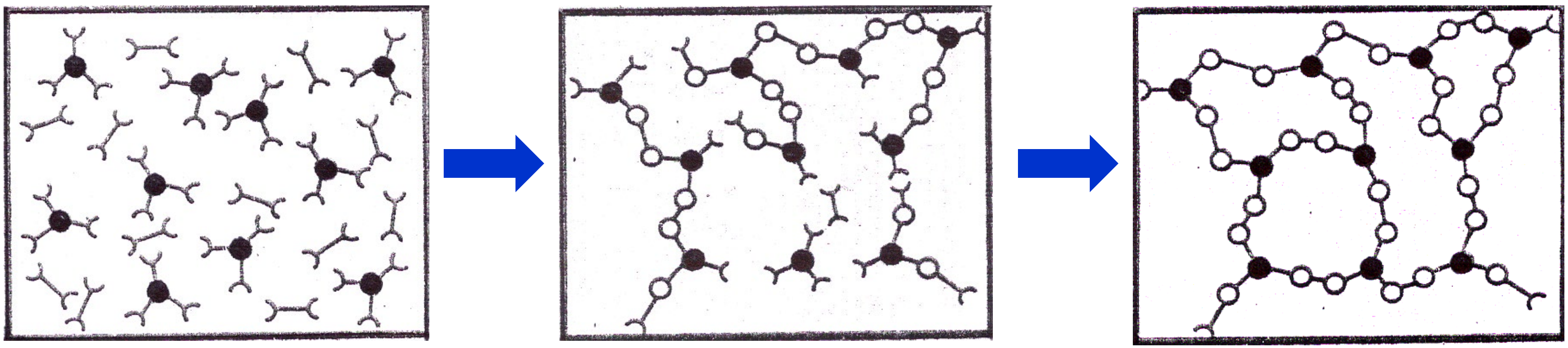


Bis-maleimide



Morphology has an impact on moisture absorption

Thermosets Offer Wide Processing Range



Monomers/Oligomers
- Low viscosity
- Good flow/dispensing
- Use various monomers to tailor properties
- Reactive diluents to control viscosity

Partially cured
- B-staged
- Film-like properties
- Can still flow with additional heat

Fully Cured Network
- No flow
- Tailored Tg depending on chemistry
- High temp stability
- Controlled CTE

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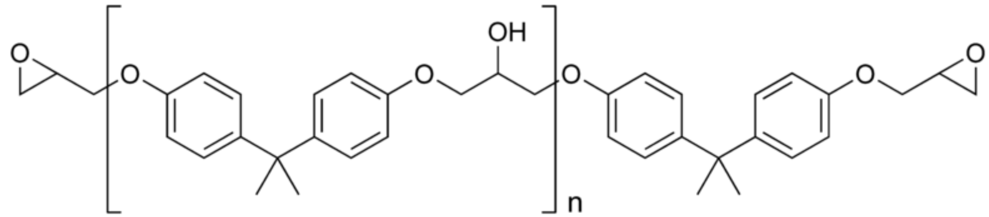
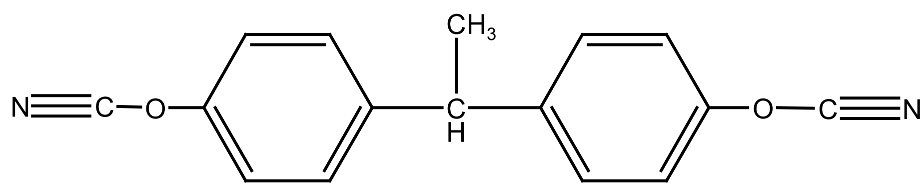
Thermoset Polymers

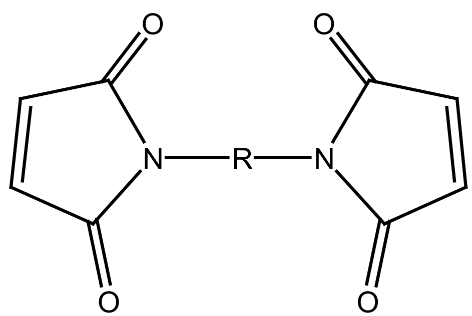
Epoxy



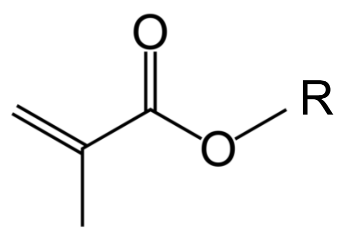
Cyanate Ester



Bismaleimide

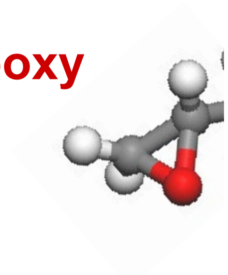


Acrylate



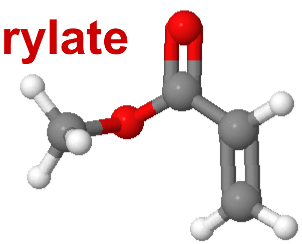
Common Reactive Chemistries

Epoxy



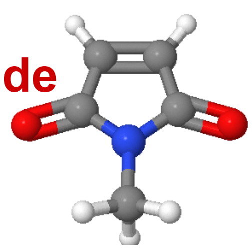
Established Technology: not best for very fast curing systems. Chemistry limitations for new increased temperatures demanded by lead free systems.

Acrylate



Competitive technology: fast cure but sensitive to air. Bleed, odour and shelf-life issues.
Wide range of commercially available materials.

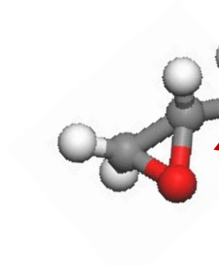
Maleimide



Excellent potential: fast cure, high extent of reaction and low sensitivity to air. Most commonly used in die attach and in BT epoxy laminates for package substrates.
Current range of formulation materials limited.

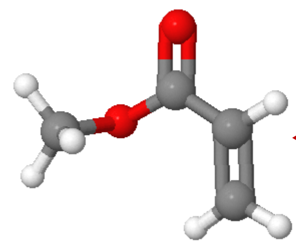
Common Reactive Chemistries

- Epoxies, liquid epoxies



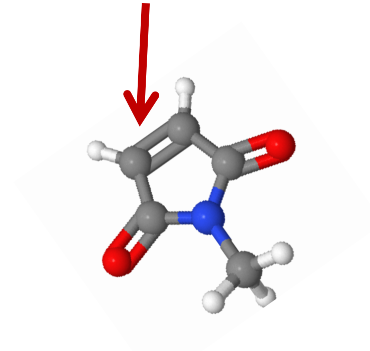
Epoxy ring opening

- Acrylate monomers, oligomers

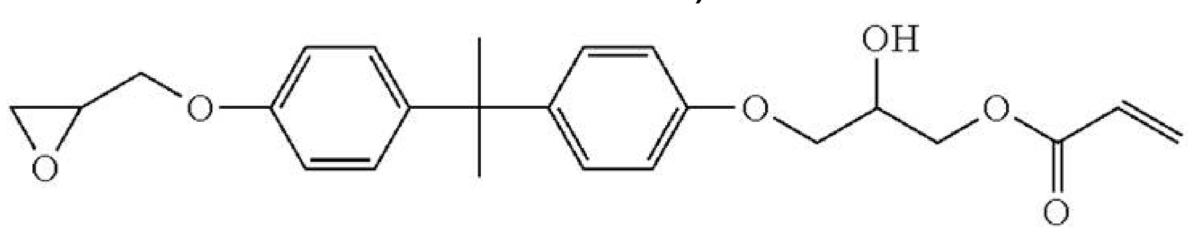


Polymerize across the double bond

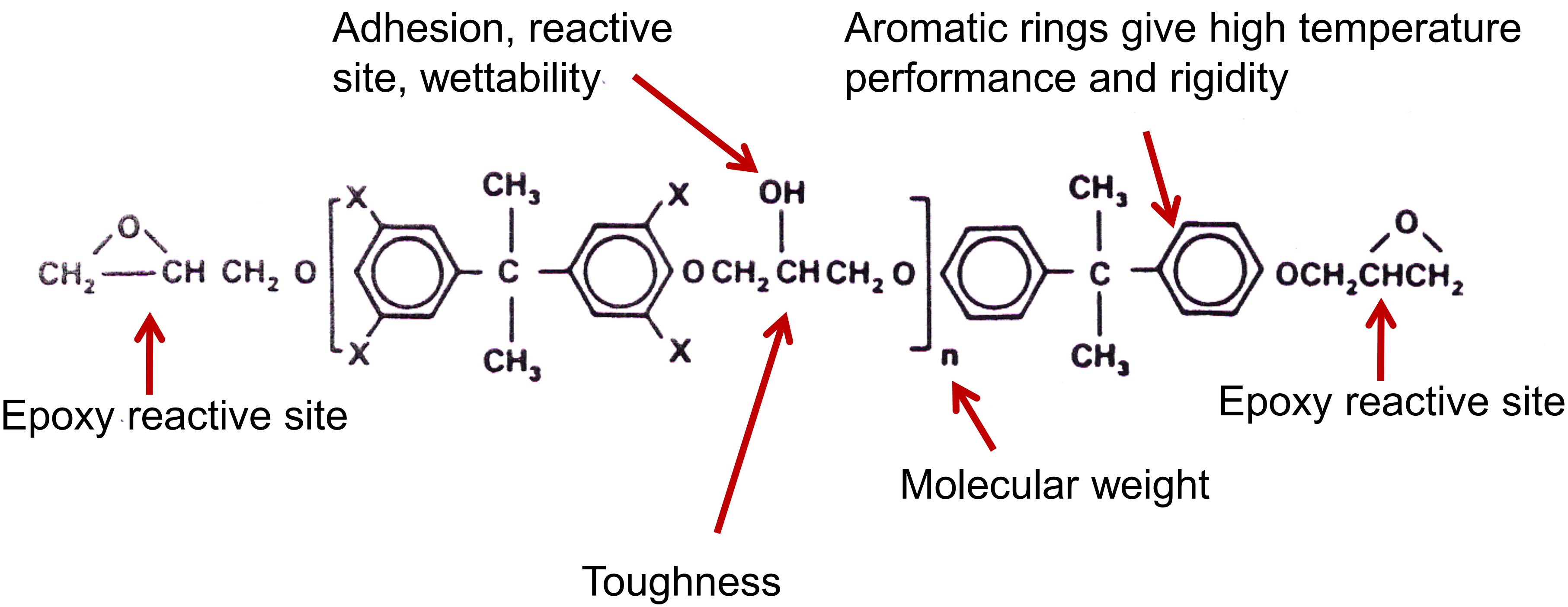
- Reactive diluents
  - Acrylates and methacrylates



- Bismaleimides (aliphatic, low viscosity)
- Hybrid resins
  - Dual functionality (i.e. epoxy on one end and acrylate or bismaleimide on the other end)



Epoxy is Most Common Thermoset



Bisphenol A epoxy; X=H, for tetrabromobisphenol A; X- Br

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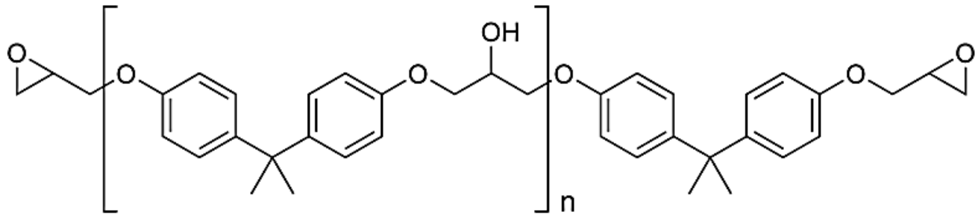
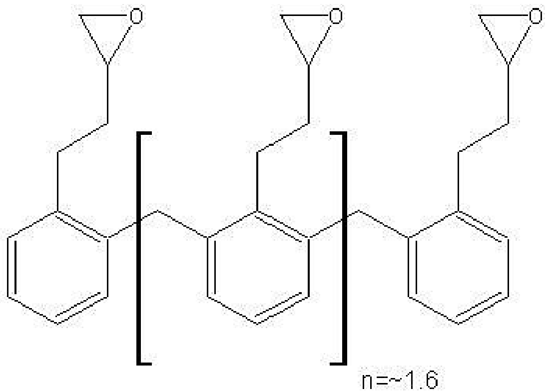
Types of Epoxies

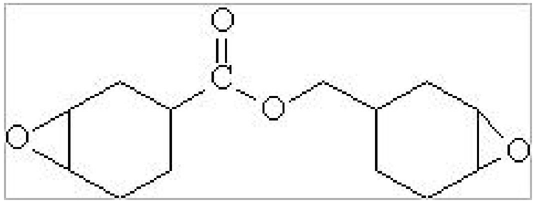
Bis Phenol Epoxy



Epoxy novolac



Cycloaliphatic epoxy



Polymers Used in Electronic Packaging

Advantages

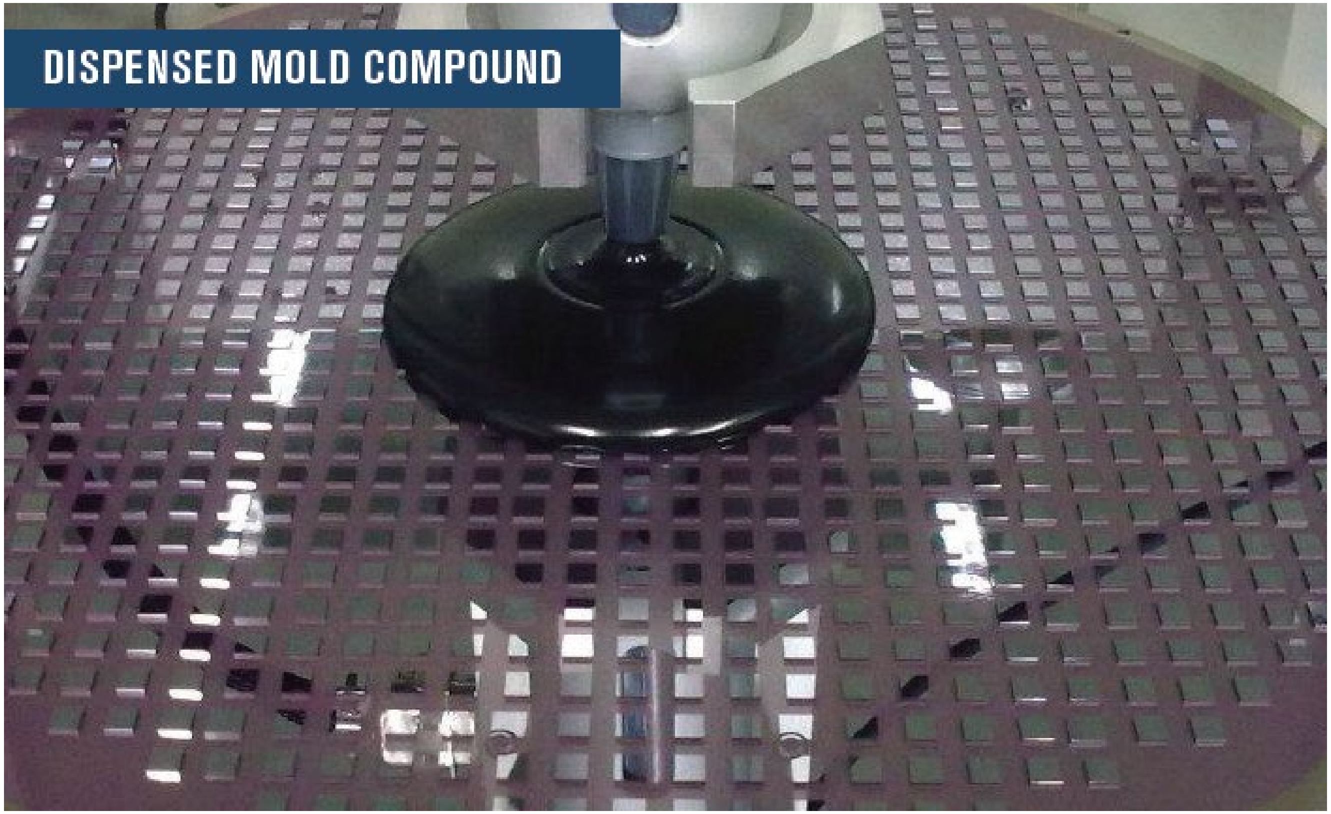
- Extensive chemistry toolbox available
- Tailorable to meet required material properties
  - Glass transition temperature, CTE, modulus
- Process window from liquids (i.e., adhesives, coatings, mold compounds, underfills, etc.) to fully cured solids
- Stable on heating at solder reflow temperatures
- Good chemical resistance

Disadvantages

- Non-hermetic (absorbs moisture)
- Residual stresses lead to warpage (lower assembly yields)
- Potential for material incompatibility (i.e. polymer-metal adhesion)

Epoxy Mold Compounds

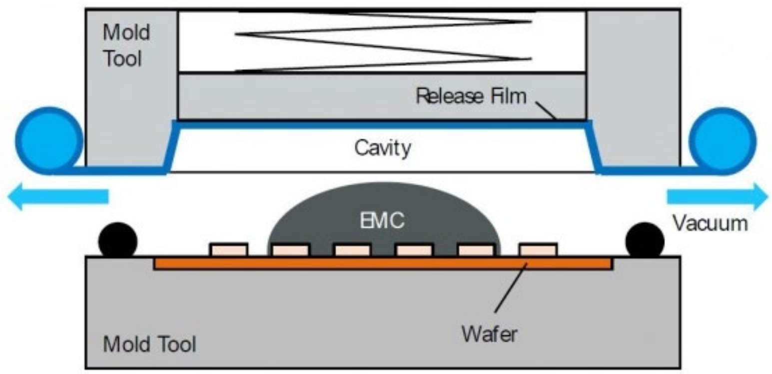
Liquid Mold Compound on Reconstituted Wafer

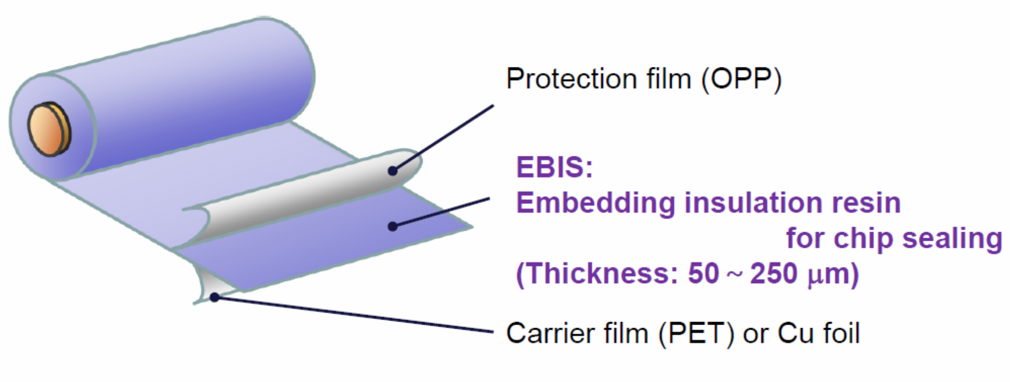


Source: Nanium

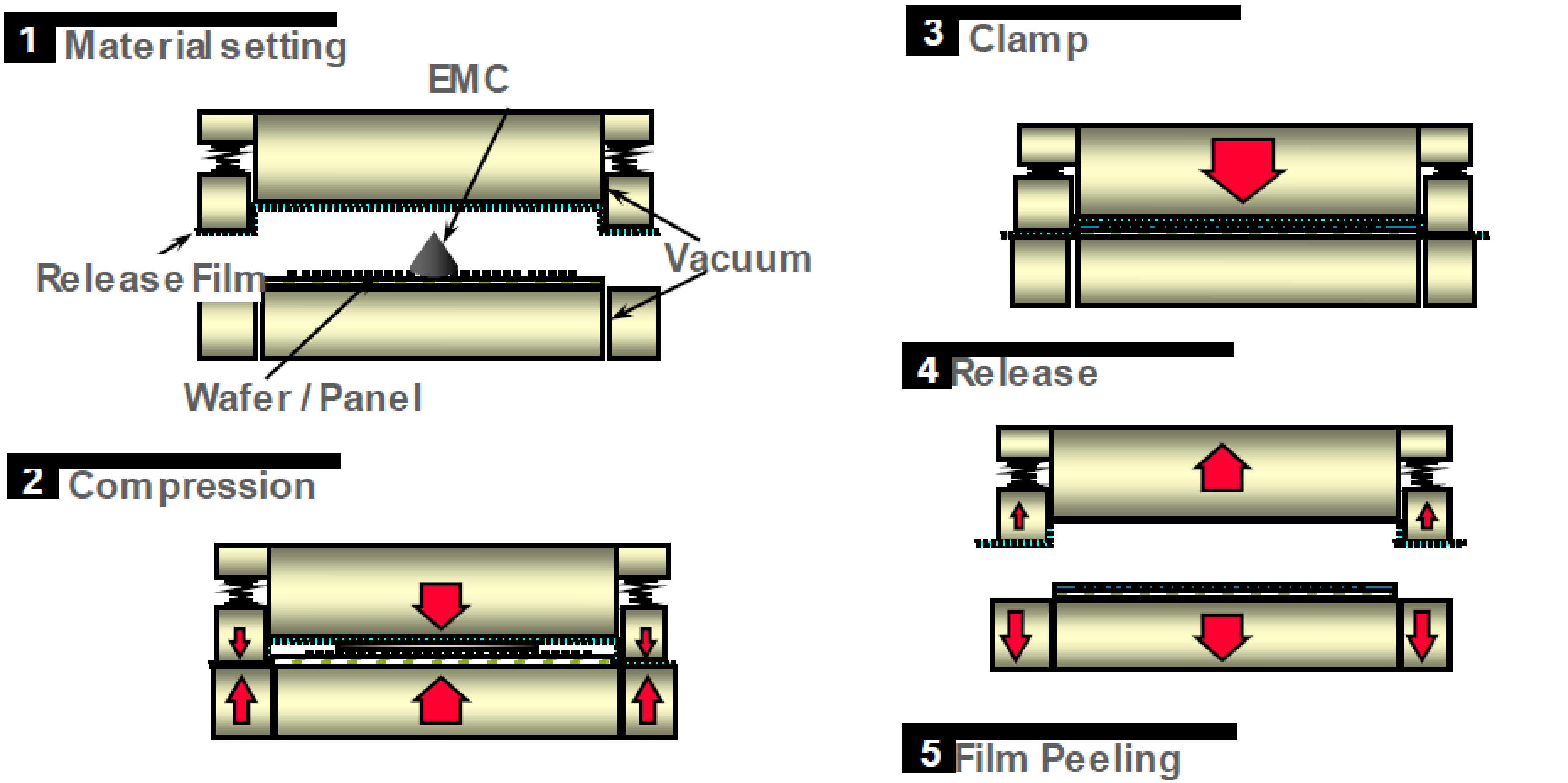
Mold Compounds for FOWLP

- Solid EMC
  - Hitachi
  - Sumitomo
- Liquid EMC
  - Nagase
  - Panasonic
- Film Type (Embedding Insulation Sheet (EBIS) – Hitachi Chemical



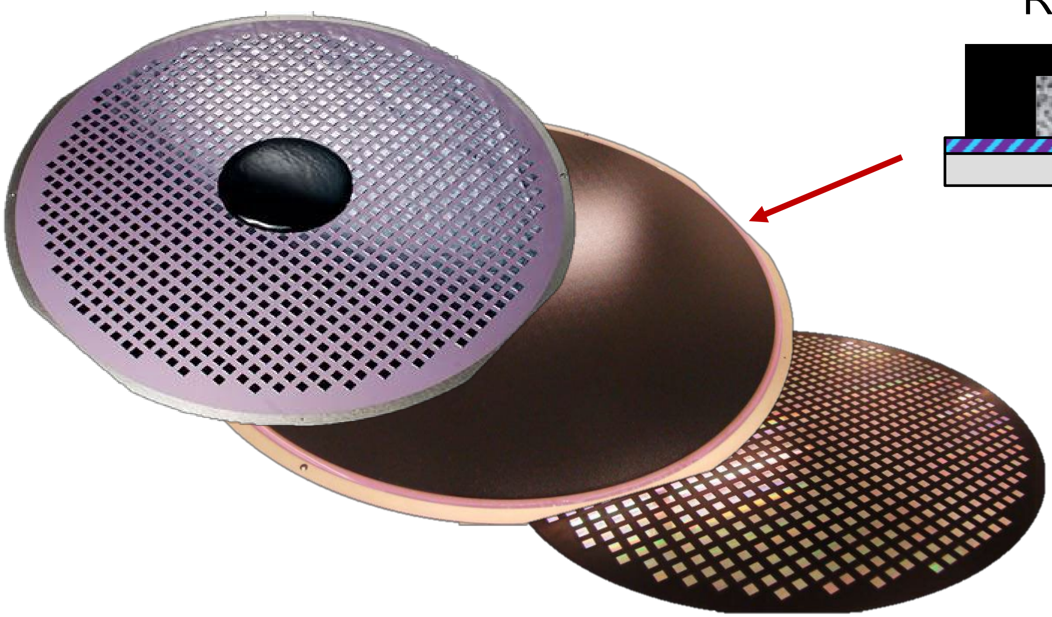


EMC Compression Molding Process

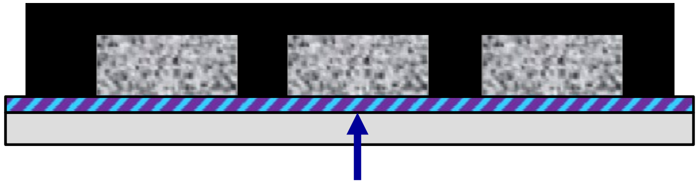


Reconstituted Wafer Example

Chips mounted on temporary adhesive layer with liquid EMC



Reconstituted wafer on carrier



Temporary adhesive layer

Source: Nanium

Reconstituted wafer after carrier release

Mold Compound Technology

- Epoxy cresol nolovak mold compounds (EMC)
  - Phenol novolak cured
  - Ease of processing, flow, molding
  - Good adhesion, small shrinkage
  - Chemical and moisture resistance
- Biphenyl mold compounds
  - Low viscosity for wire sweep control
  - High filler loading
  - Lower moisture absorption
- Multifunctional mold compounds
  - Mixture of biphenyl and multifunctional resins
  - High Tg
  - High filler content (rounded fused silica)

Typical Mold Compound Formulation*

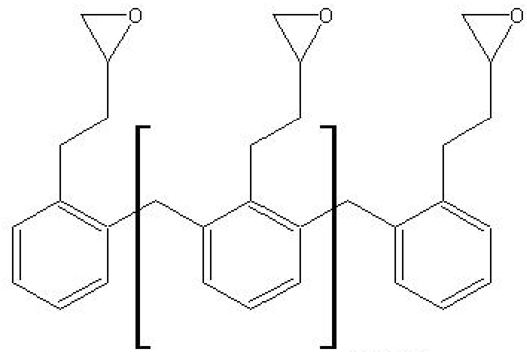
Component	Chemistry	Amount
Epoxy Resin	Epoxy Cresol Novolak	5-15%
Curing Agent	Phenolic Novolak	5%
Accelerator	Imidazoles	
Fillers	Silica filler	65-75%
Flame retardant	Brominated epoxy**	5%
Adhesion promoters	Epoxy silanes	
Parting agents	Synthetic waxes	
Proprietary additives	Flexibilizers (stress control)	
Pigments	Carbon blacks	

* Reference: S. Komori and Y Sakamoto, Materials for Advanced Packaging, Chapter 10, D. Lu and CP Wong, Editors, Springer, 2009

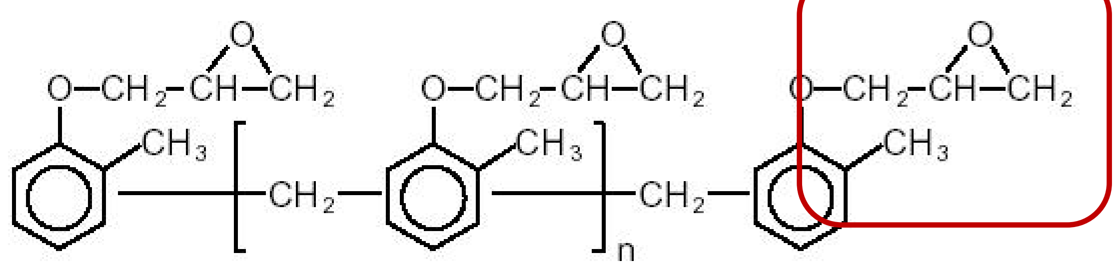
** The use of halogens is being eliminated in next generation “green” mold compounds

Chemistry of Epoxy Mold Compounds

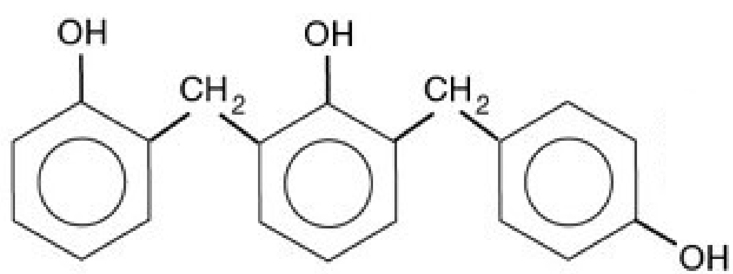
Epoxy novolak



Epoxy cresol novolak

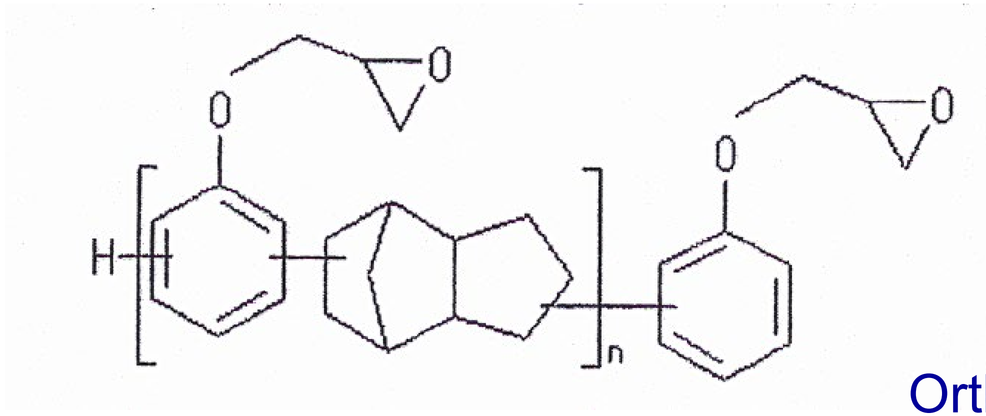


Phenolic novolak
(curing agent)

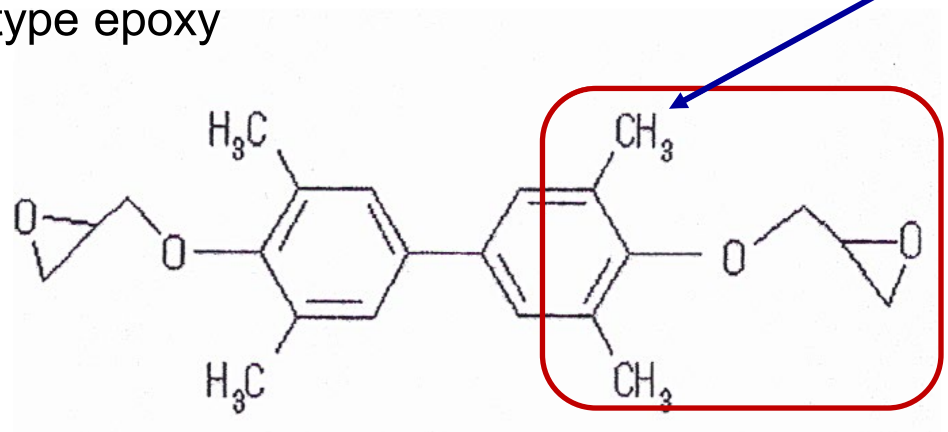


Mold Compound Chemistry

Dicyclopentadiene type novolak epoxy



Biphenyl type epoxy



Ortho methyl groups ($-CH_3$)

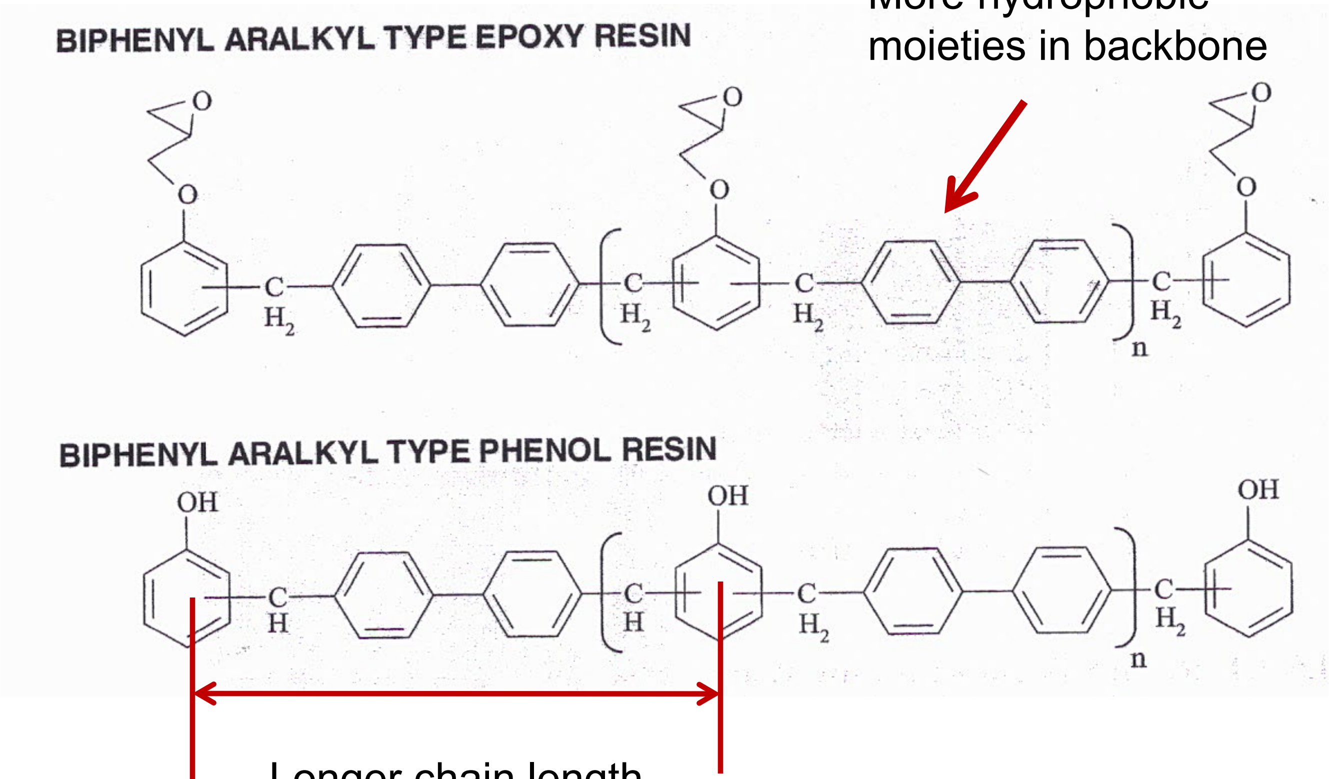
Steric hindrance around epoxy linkage lowers moisture absorption

Next Generation EMC

- Add Multi Aromatic Resin (MARs) into the base epoxy cresol novolak/phenol novolak
- Lower the high temperature elastic modulus by decreasing the crosslink density
  - Longer polymer chains between crosslinks
- Lower moisture absorption
  - Addition of hydrophobic aromatic rings

Next Generation EMC*

More hydrophobic moieties in backbone

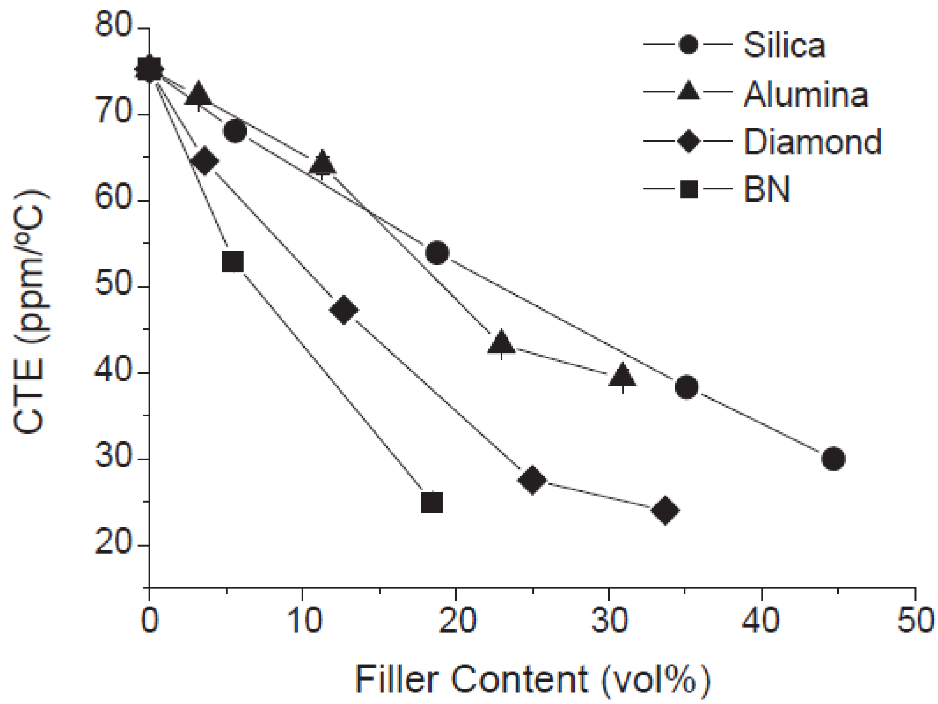


Longer chain length between crosslink points

* Reference: S. Komori and Y Sakamoto, Materials for Advanced Packaging, Chapter 10, D. Lu and CP Wong, Editors, Springer, 2009

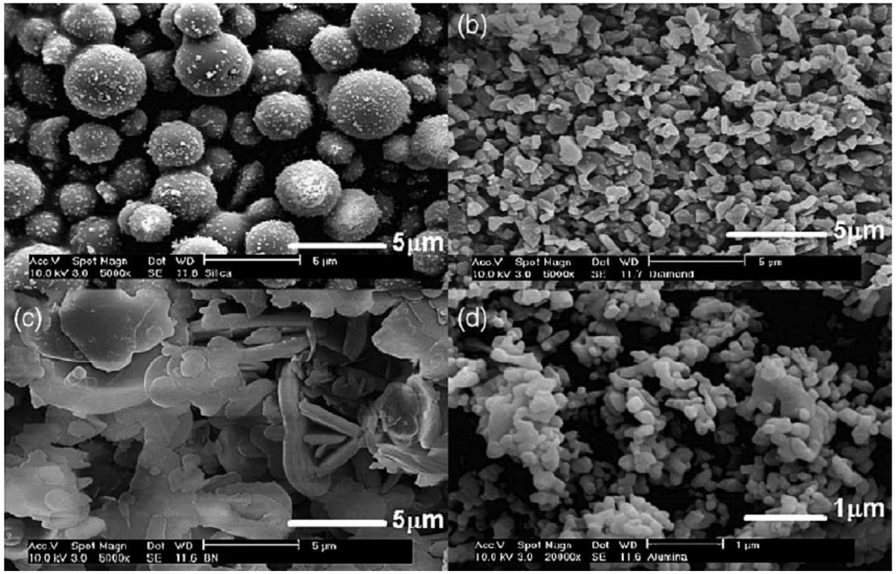
Fillers Play a Key Role in Lowering CTE

Coefficient of Thermal Expansion



Silica

Diamond

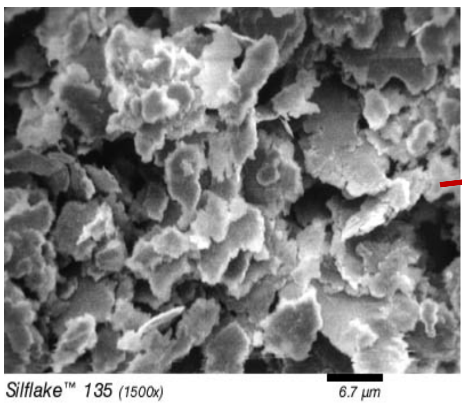


Boron nitride (BN)

Alumina

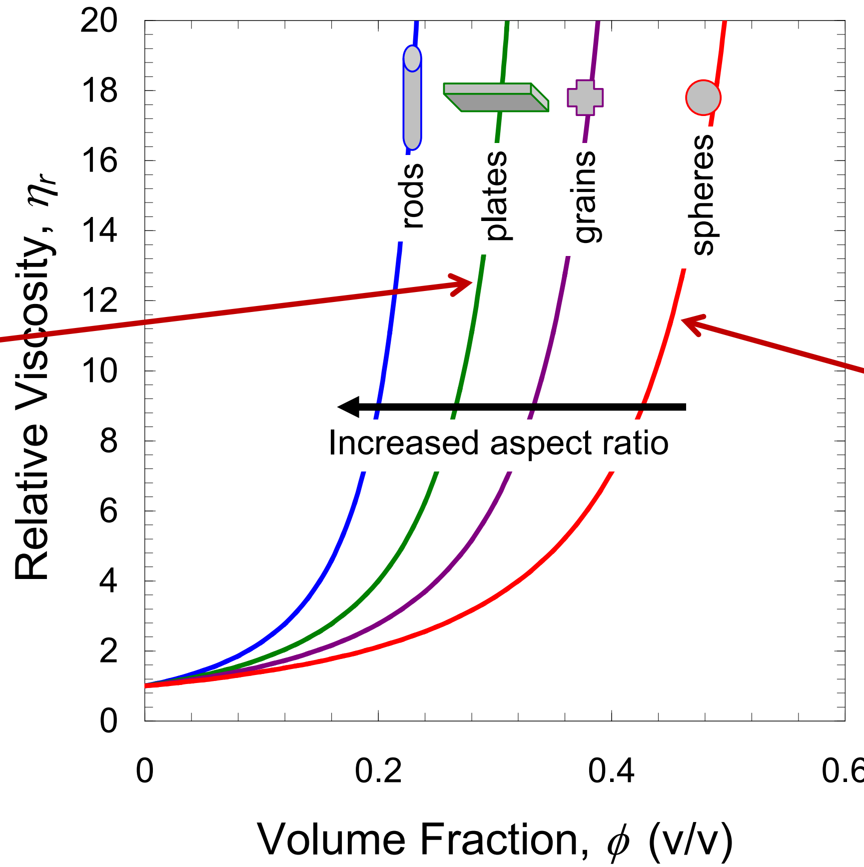
Source: W. Sun Lee, J. Yu, Diamond & Related Materials, vol. 14, p.1647-1653 (2005)

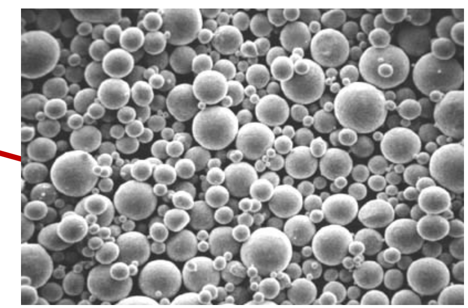
Aspect Ratio Impacts Viscosity



Silver flakes for die attach adhesives

Source: Technic

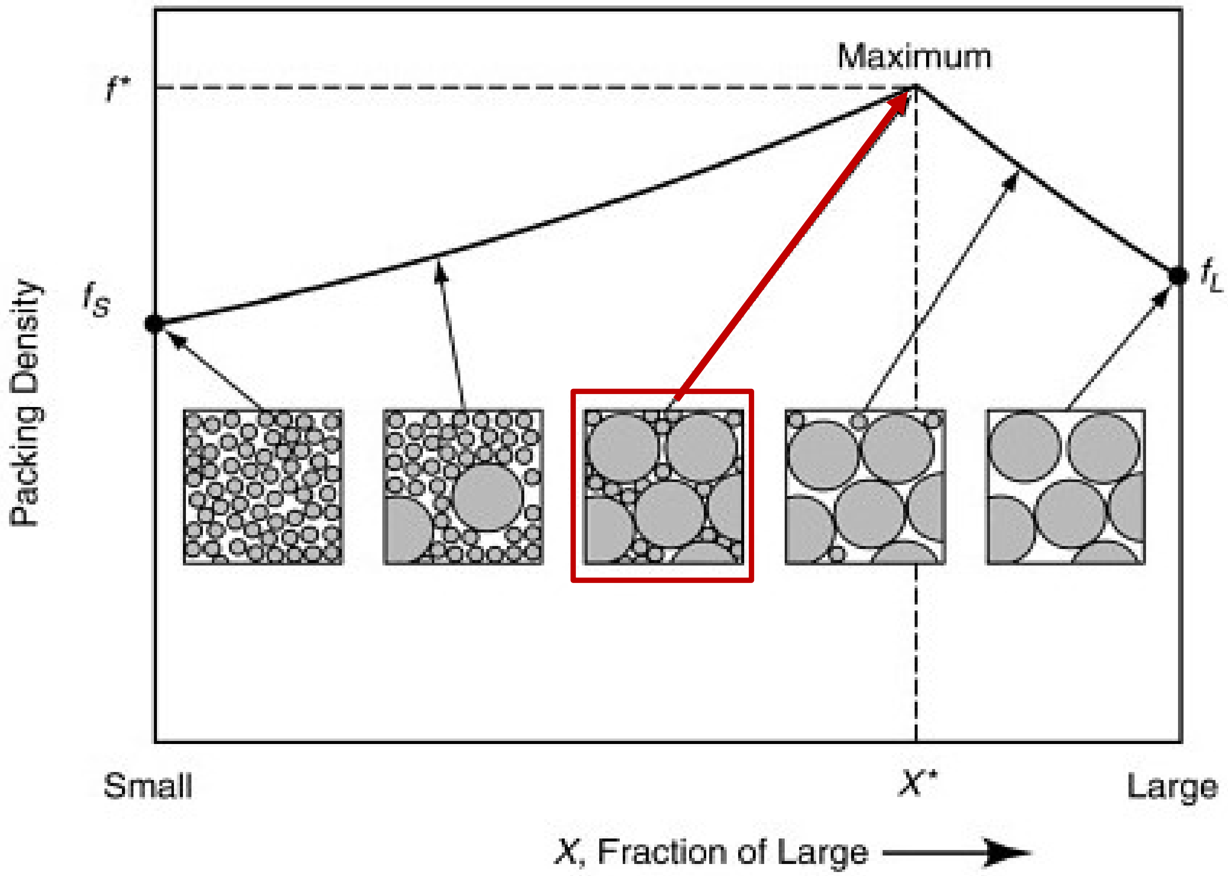


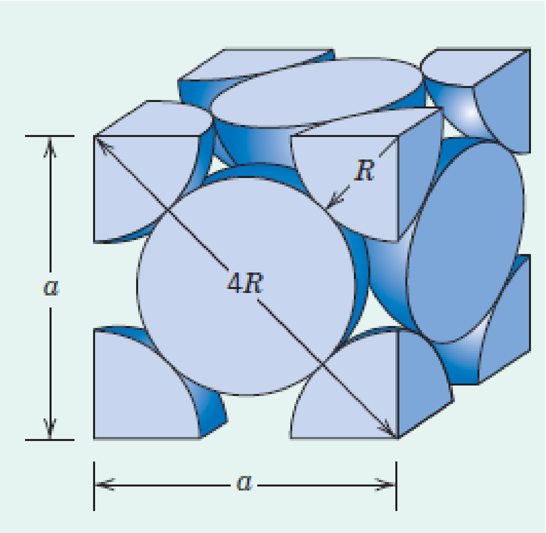


Silica spheres for underfills

Source: Sumitomo

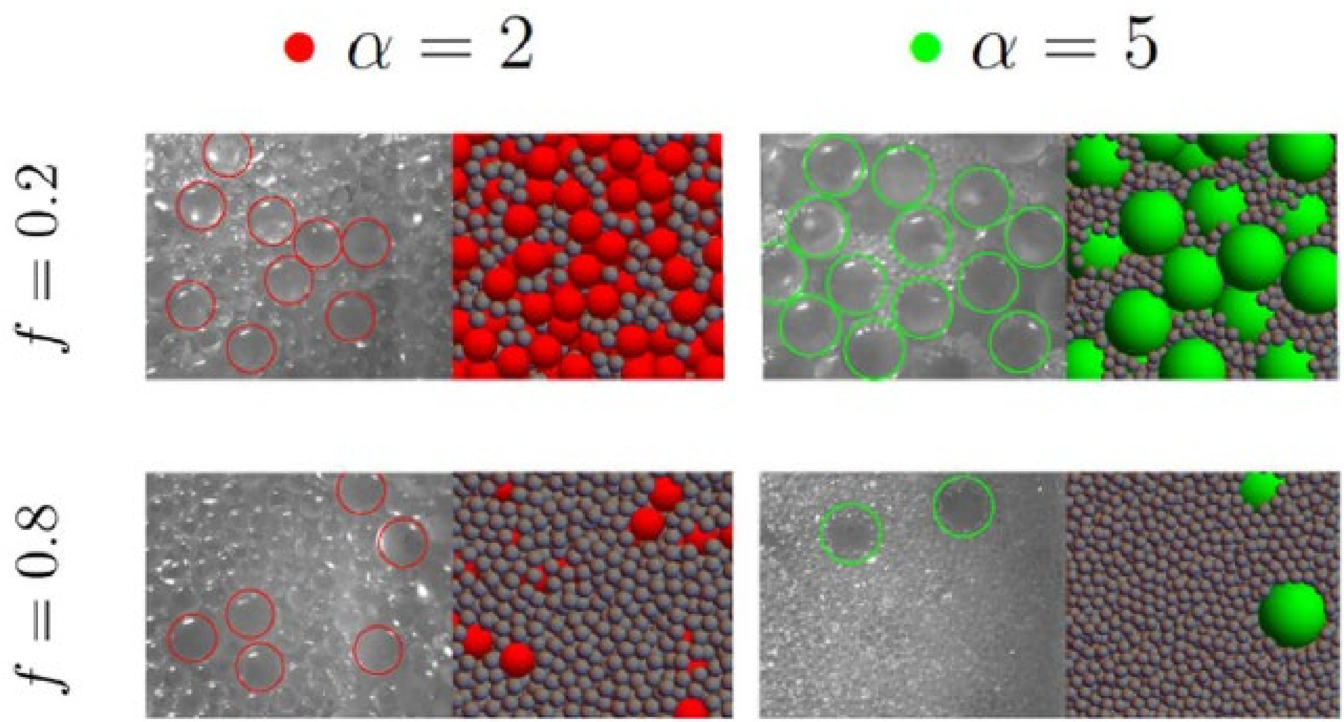
Filler Packing for a Bimodal PSD





The packing density for face centered cubic geometry is 74%

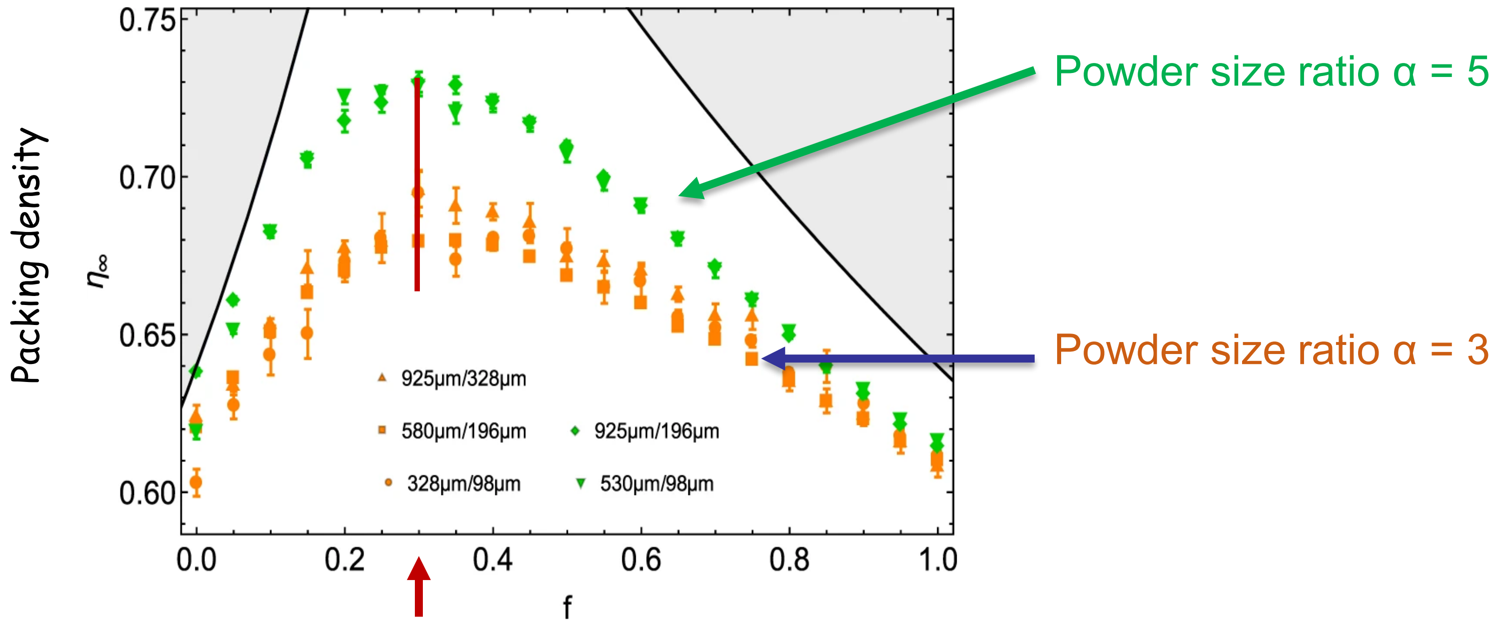
Particle Size Ratio



$$\alpha = \frac{d_L}{d_S} = \frac{diameter\ large}{diameter\ small}$$

Pillitteri, S., Lumay, G., Opsomer, E. *et al.* From jamming to fast compaction dynamics in granular binary mixtures. *Sci Rep* **9,** 7281 (2019). https://doi.org/10.1038/s41598-019-43519-6

Filler Packing for a Bimodal PSD



- Maximum packing density when the volume fraction (f) of the smaller particles is ~ 0.3, when using ideal mono-size powders
- Effect is more pronounced when increasing the size ratio *α*

Pillitteri, S., Lumay, G., Opsomer, E. *et al.* From jamming to fast compaction dynamics in granular binary mixtures. *Sci Rep* **9,** 7281 (2019). https://doi.org/10.1038/s41598-019-43519-6

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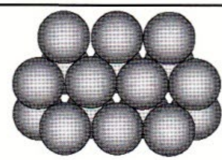
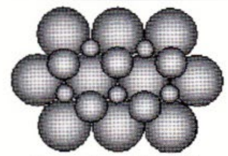
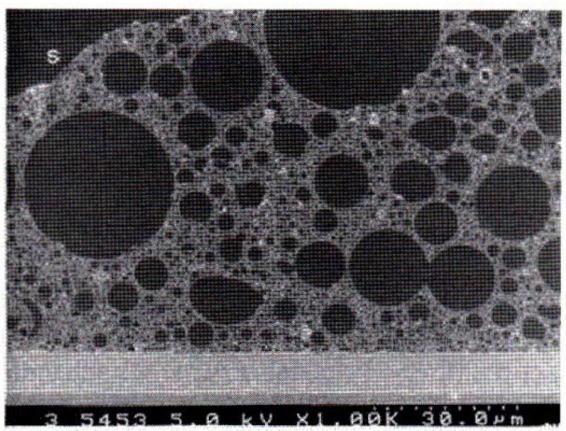
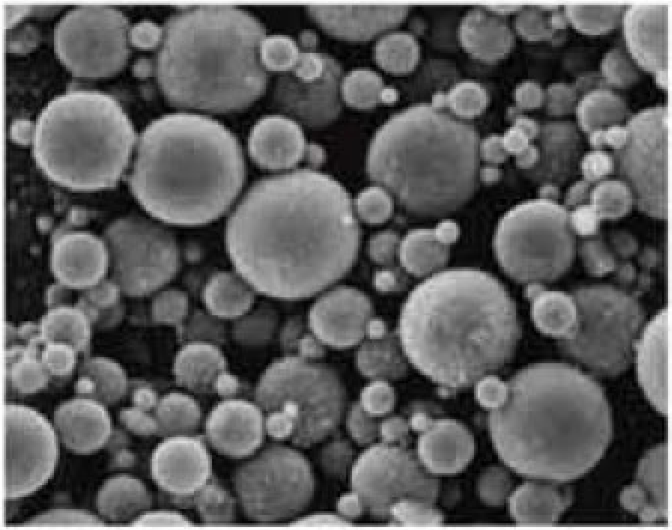
Epoxy Mold Compound Filler Loading

Diameter of the filler	Filler Content	
R 0.414R 0.225R	100% 0 0	91.5% 6.5% 1.85%
Schematic illustration of filler packing	 Porosity: 29.5%	 Porosity: 19.0%

(a)





Source: Sumitomo

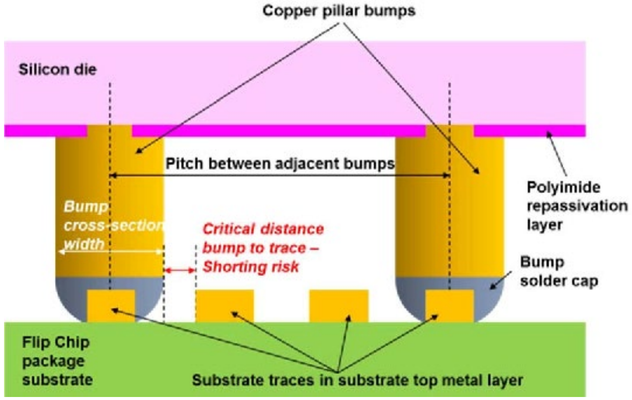
Use "generational" packing to increase the packing density

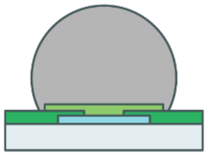
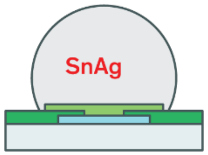
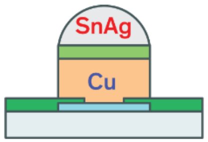
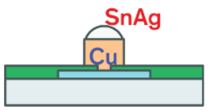
Advanced Underfills

Challenges with Capillary Underfill

Flow issues with capillary underfills

- Cu pillar pitch is going to < 35 µ
- Pillar diameter is moving < 30 µ



	SnPb C4 Bump	Pb-Free C4 Bump	Cu Pillar + Pb-free Cap	Cu µ-Pillar + Pb-free Cap
Structure				
Diameter	75 – 200 µm	75 – 150 µm	50 – 100 µm	10 – 30 µm

Old Technology → Current Technology → Next-Generation Technology

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Underfill Material Drivers

- Optimize for stress control (warpage)
  - Tailor the Tg and modulus
- High modulus (around 10 GPa)
- Mid-range Tg (around 90°C)
- Low CTE (target < 25 ppm/°C)
- Low cure temperature (stress control)
- Low cure shrinkage (stress control)
- Tailored rheology depending on application
  - Flow speed
  - Good wetting to chip & substrate
  - Good adhesion to chip & substrate

Capillary Underfill Formulation Challenge

- Needs to flow under die using capillary force
  - Requires low yield point (or no yield point)
- Required to have low CTE for stress management
  - Achieve low CTE with high filler loading
  - High filler loadings increase the yield point, viscosity, and potentially develop thixotropy
- Ideal capillary underfill has very low yield point and exhibits Newtonian viscosity after dispense
  - Silica has small filler-filler interaction parameter
  - Surface treatment can reduce particle agglomeration
  - Low viscosity monomers/diluents used in resin component

Capillary Underfill Flow Considerations

Hele-Shaw model for underfilling time:

$$t_f = \frac{3\eta L^2}{\sigma h(cos\theta)}$$

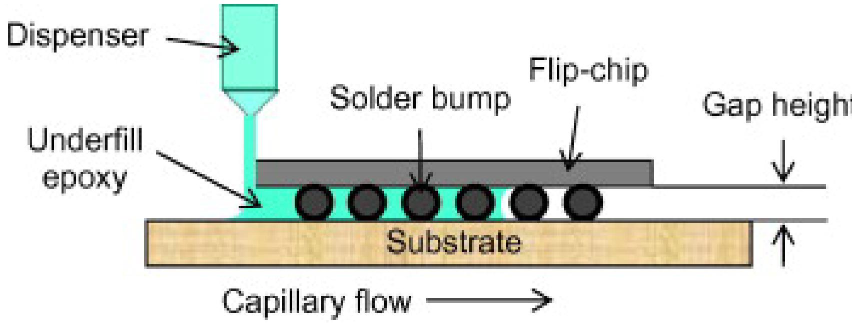
L= chip length

θ = contact angle

h= gap height

η = viscosity

σ = surface tension



From this relationship we can see that filling time decreases when:

- L and η *decrease*
- h and σ *increase*

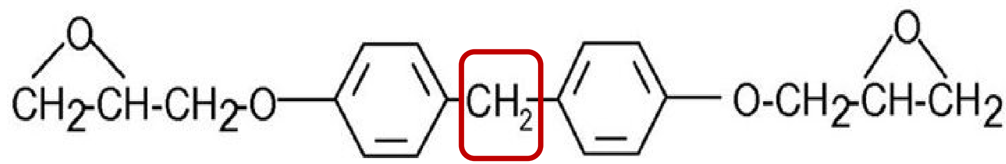
Capillary Underfill Flow Considerations

- The packing trend is to smaller gap height (lower h) with tighter bump pitch
- Low CTE requirements (i.e., addition of fillers) impacts flow
- Design challenges:
  - Reduce viscosity (use temperature and molecular design)
    - Fillers play a key role in viscosity
  - Increase surface tension (better wetting leading to faster flow)
  - As die size increases, keep h as large as possible

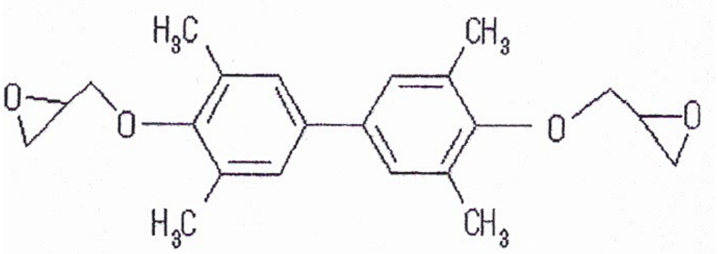
Capillary Underfill Formulations

Resins and hardeners

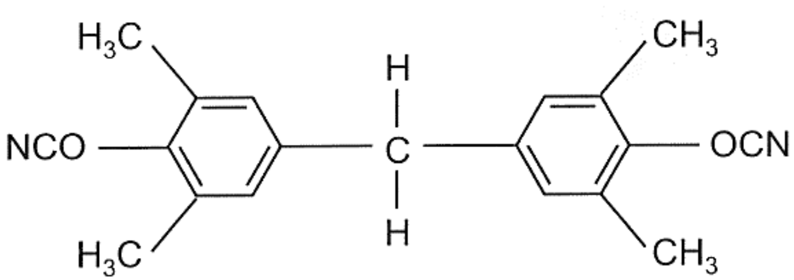
- Liquid Bis F epoxy – amine
- Liquid Bis F epoxy – anhydride



- Biphenyl epoxy



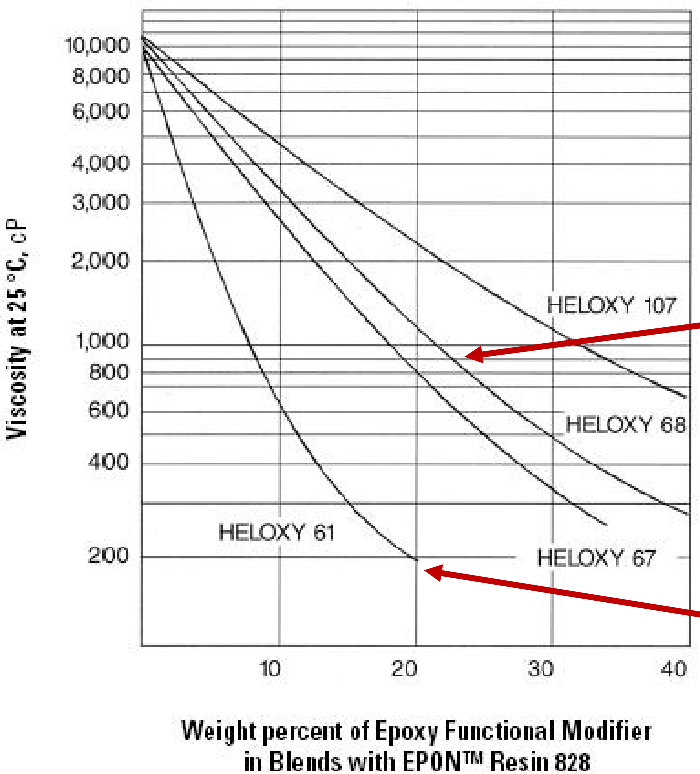
- Liquid cyanate ester – metal coordination catalyst

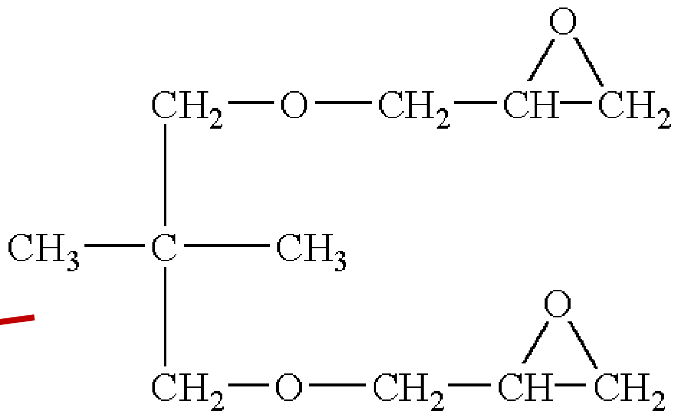


Formulation Components

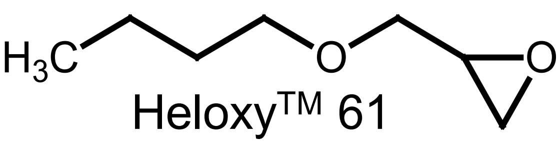
- Latent Hardeners (flow first then cure)
  - Anhydrides (generate fluxing in-situ)
  - Liquid primary aromatic amines (DETDA)
  - Hindered primary aliphatic amines (isophorone diamine, IPDA)
- Catalysts
- Fluxing agents
  - Carboxylic acids, sulfonic acids, hydroxyl containing agents
- Reactive diluents
- Adhesion promoters such as silanes
- Surface energy modifiers
- Flow modifiers, defoaming agents, tougheners

Reactive Diluents Play Dual Role





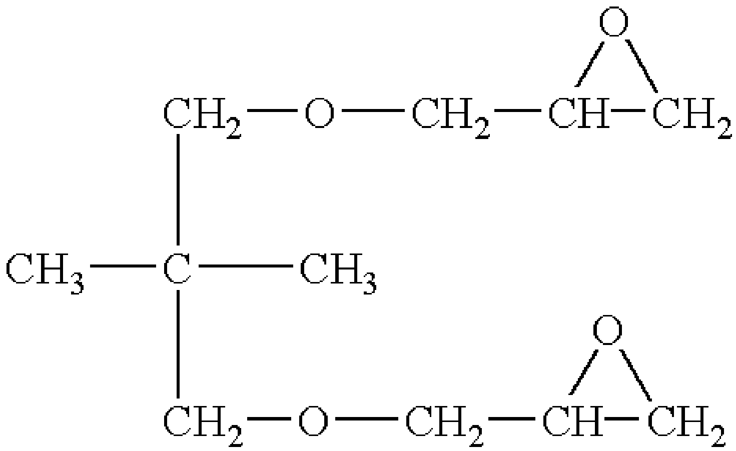
Heloxy™ 68



Heloxy™ 61

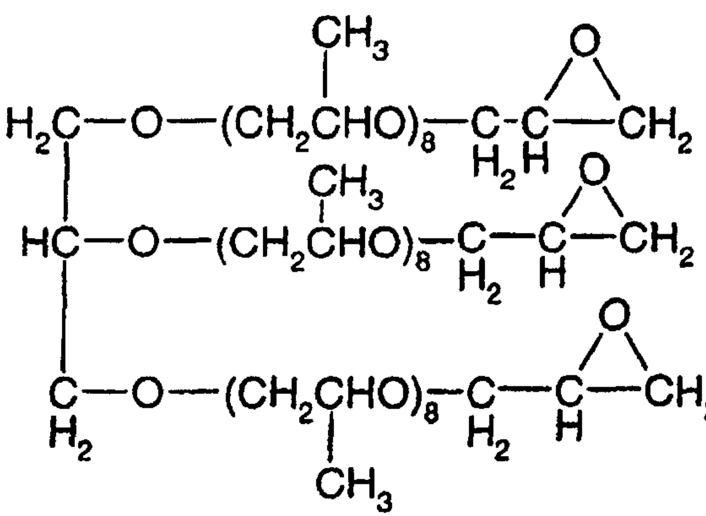
Control the viscosity before curing

Multifunctional Reactive Diluents



- Heloxy 68 is one of the most common reactive diluents for epoxies
- Small, di-functional molecule that retains properties well

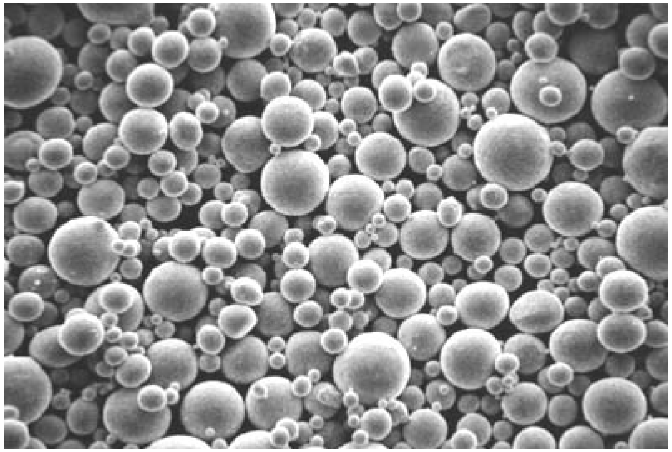
- Heloxy 505 is a large tri-functional reactive diluent
- Excellent for increasing toughness and impact resistance



Fillers

- Non-conductive, electrically insulating
  - Fused silica is widely used; high purity, chemical resistance and low coefficient of thermal expansion (CTE)
  - Spherical fused silica is the most common filler
  - Used in high filler loadings (> 65 wt%)

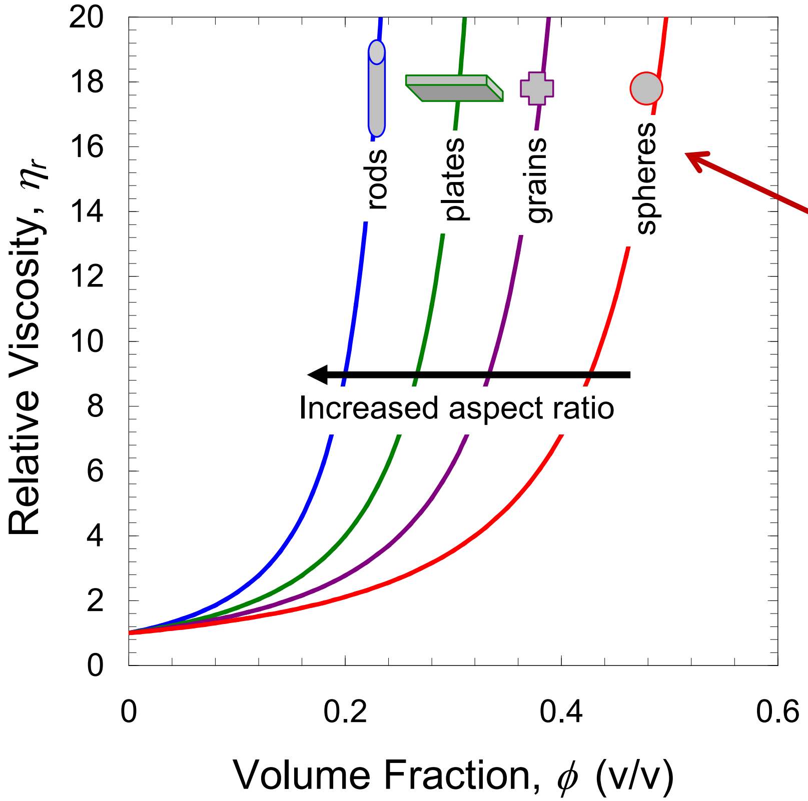
- Surface treatment is key
  - Lower viscosity
  - More Newtonian flow behavior
  - High filler loadings

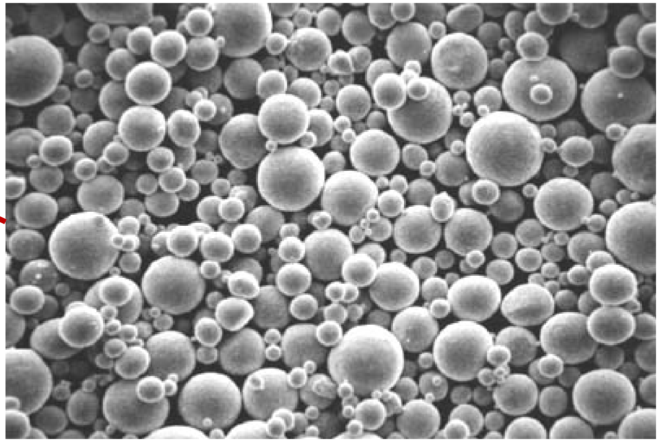


Source: Sumitomo

Filler Loading Controls Viscosity

Uncured model epoxy formulation with various filler aspect ratios

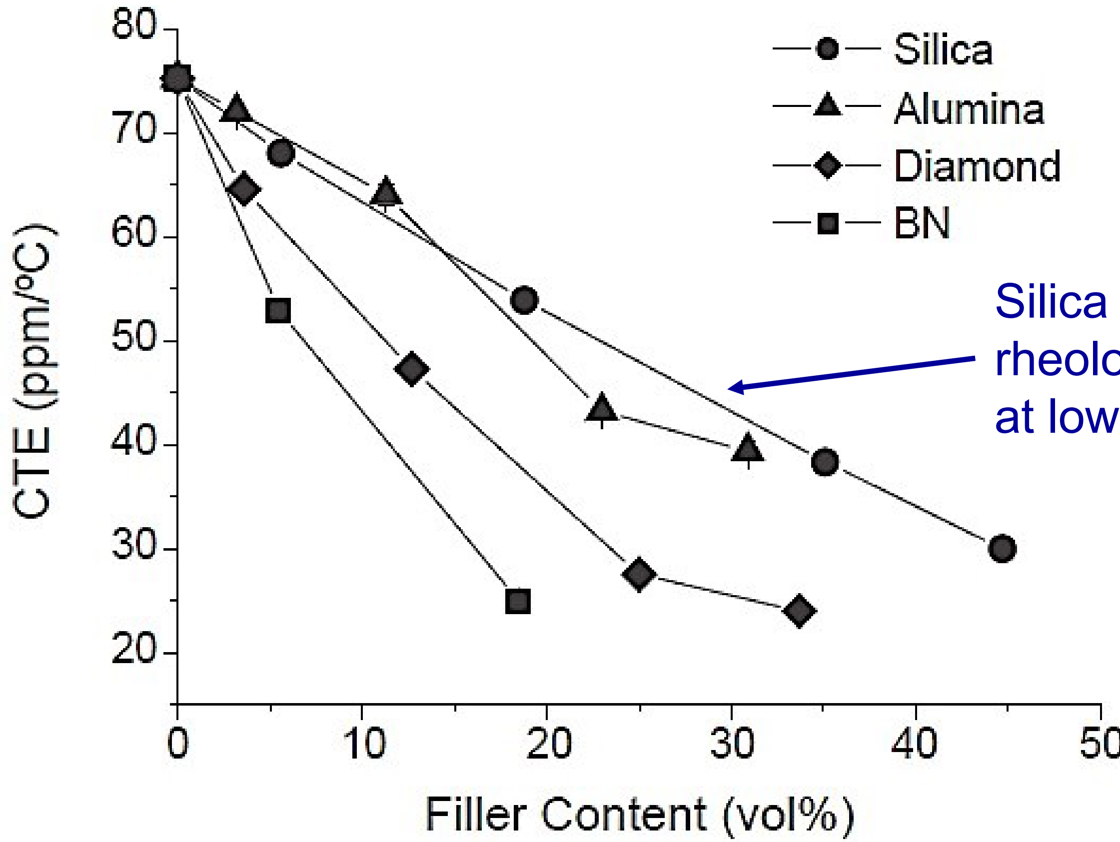




Silica powder

Source: Sumitomo

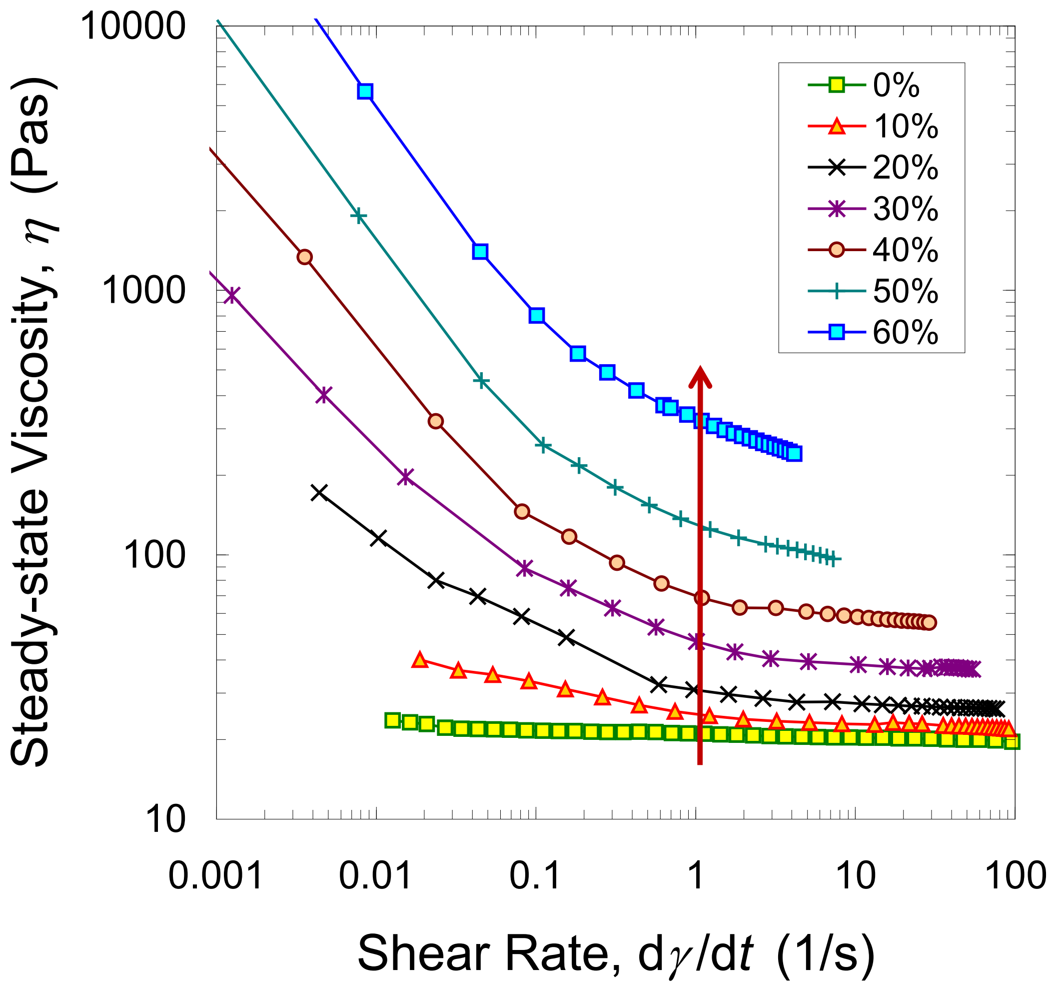
CTE as a Function of Volume Percent



Silica good for rheology least effective at lowering CTE

W. Sun Lee, J. Yu, Diamond & Related Materials, vol. 14, p.1647-1653 (2005)

Silica Filler Loading Impacts Flow

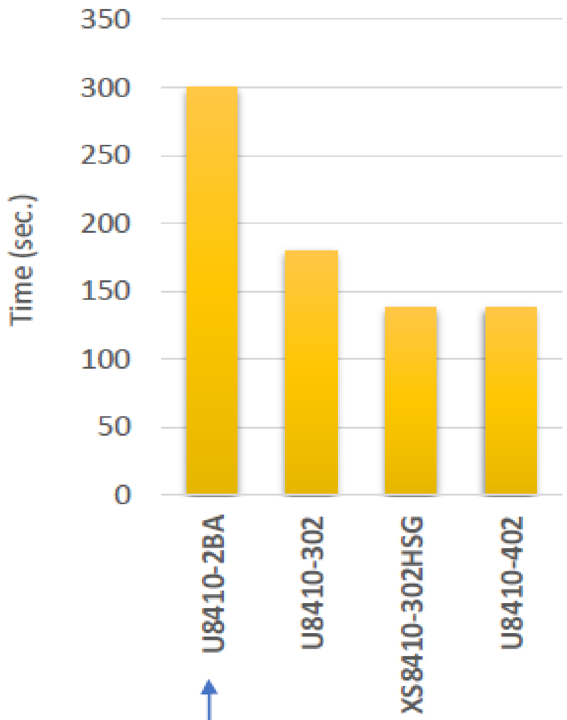


Viscosity increases dramatically with filler loading

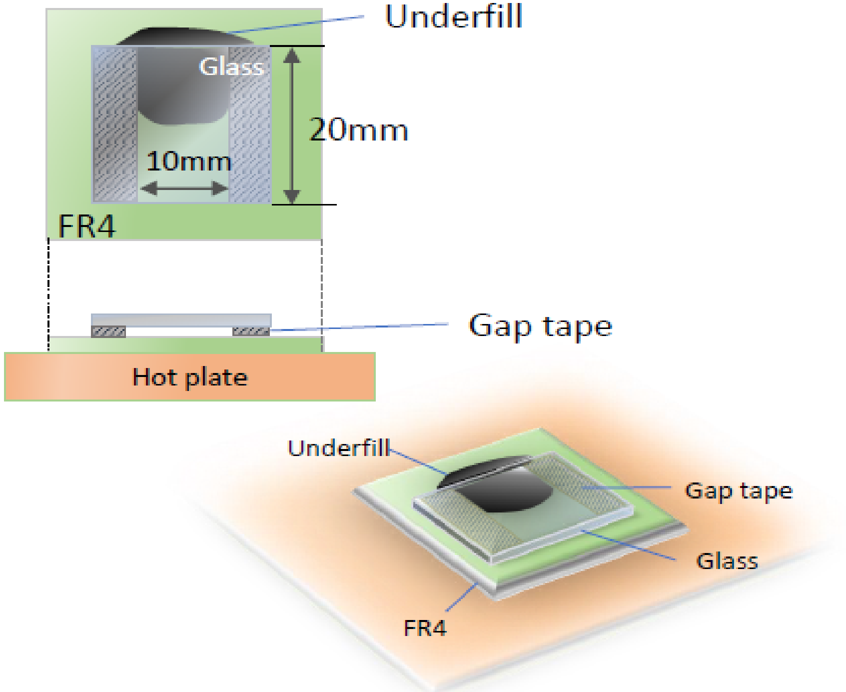
Measuring Underfill Flow Time

Flowability

Dispensing temperature: 110C
Flow gap: 50um



Test specimen



Due to formulation, lower stress materials exhibits slower flow.

Source: Namics

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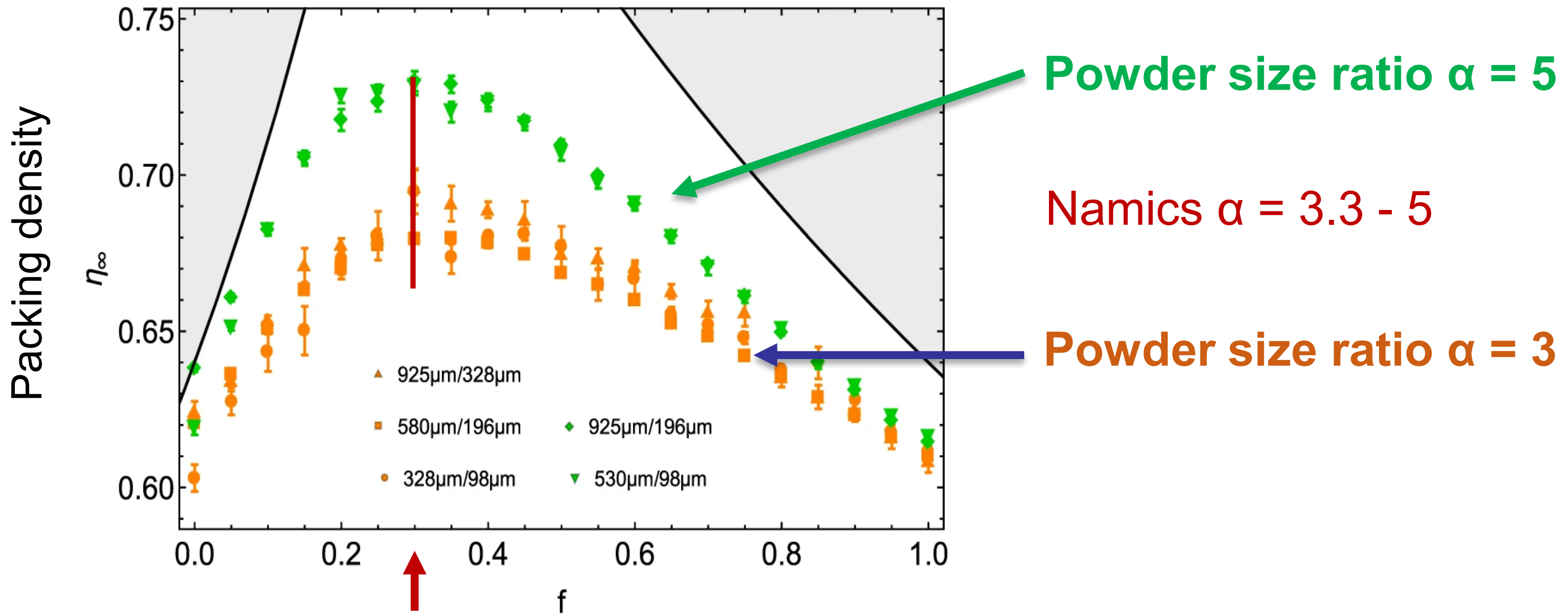
Filler Packing for a Bimodal PSD



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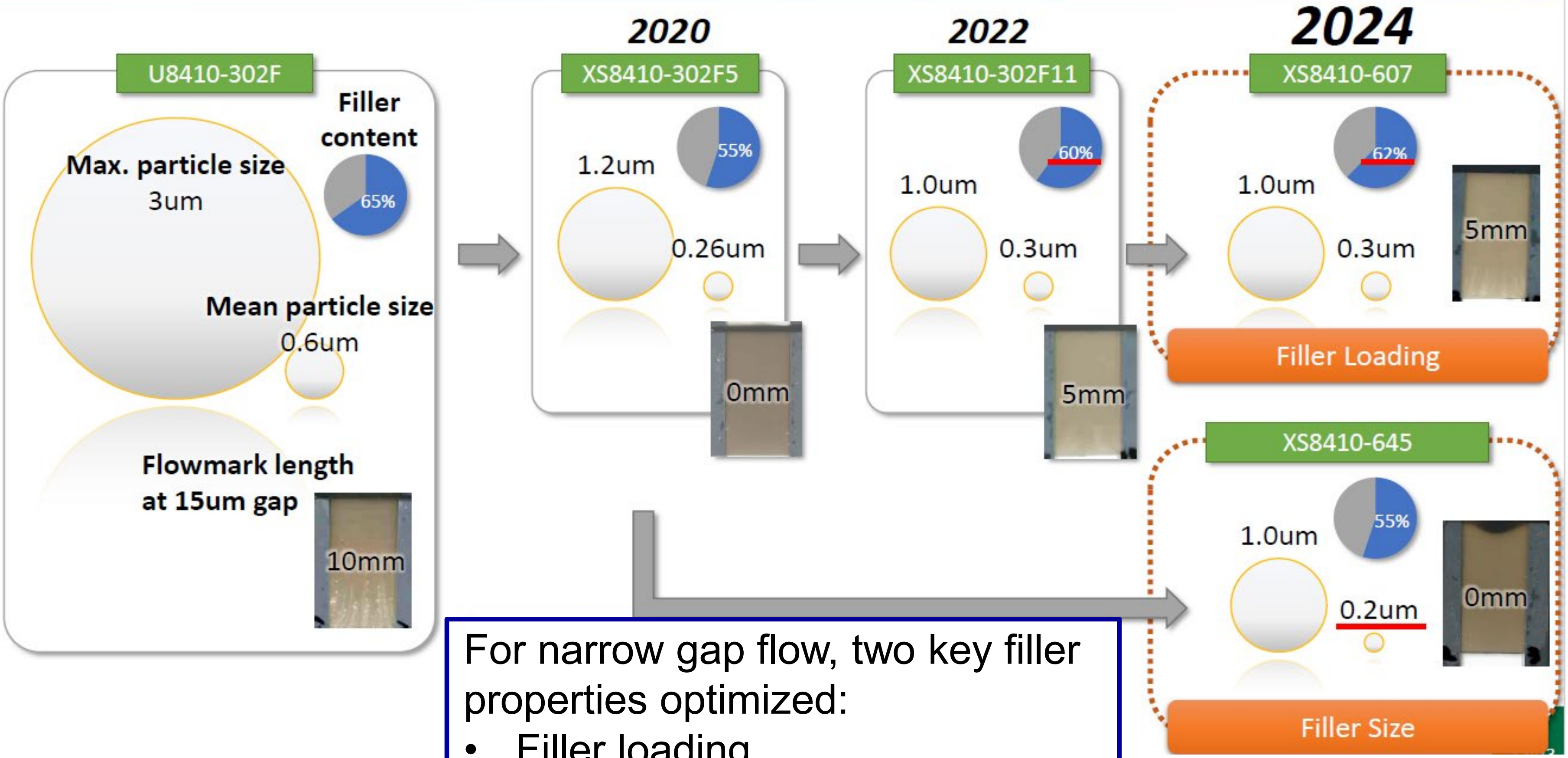
Narrow Gap Underfills

Powder size ratio α = 3.3



For narrow gap flow, two key filler properties optimized:

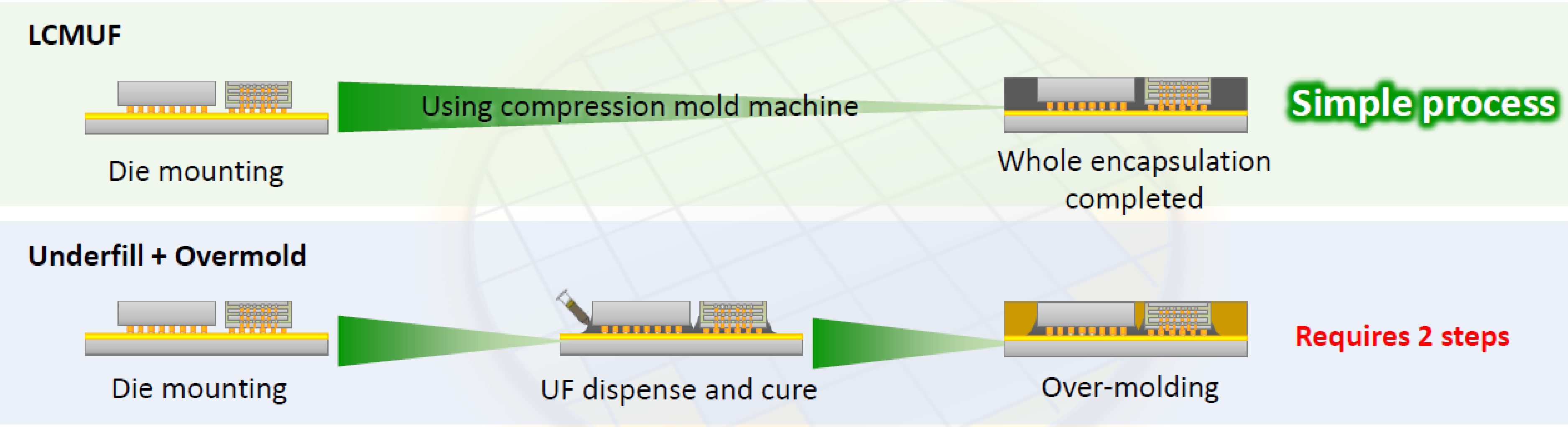
- Filler loading
- Filler size ratio (α)

Powder size ratio α = 5

Source: Namics

Namics Molded Underfill

New technology: LCMUF *Liquid Compression Mold Under Fill*



Eliminate process step and utilize compression molding equipment (used for fanout processes)

Source: Namics

Namics Molded Underfill

Fine filler type

Item		Unit	XLM8901-53A	XLM8901-185
Filler	Content	wt%	84	77
	Mean size	um	1.7	0.3
	Top cut size		5	1
Viscosity	25C, 10rpm	Pa.s	220	130
Tg	DMA	C	154	129
CTE	< Tg	ppm/C	13	23
	> Tg		31	43
Storage modulus	< Tg	GPa	14.0	11.0
	> Tg		2.0	2.0

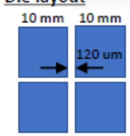
Test wafer information

(Mold thickness: 450 um, Die: w/)

: Si die w/ bump

Die w/ bump
- Die size: 10 mm x 10 mm
- Die thickness: 300 umt
- Bump material: Cu pillar 12 umt + SnAg 8 umt
- Pitch: 40 um
- Bump layout: Area array
- Passivation: SiN
- (Die w/o bump is attached by cured resin on wafer.)

Die layout

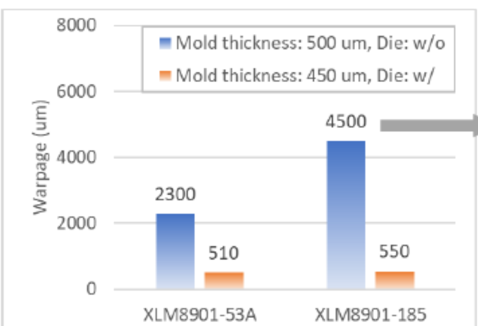


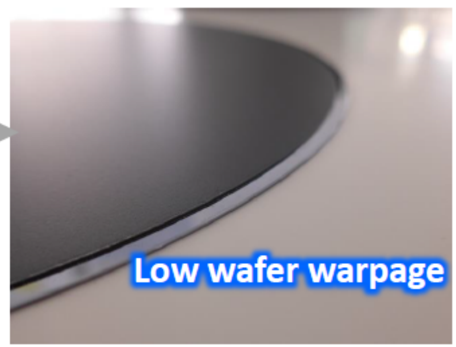
Wafer
- Wafer size: 12 inch
- Wafer thickness: 775 um
- Pad material: Cu 3 umt
- Passivation: SiN

Test conditions

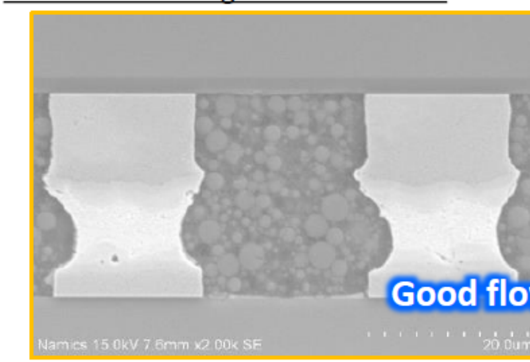
- Equipment: CPM1080 made by TOWA
- Compression force: 37 ton
- Molding temperature: 120 C
- Molding time: 600 sec
- PMC condition: 150 C / 1 h

Warpage data





Cross section image at center of die

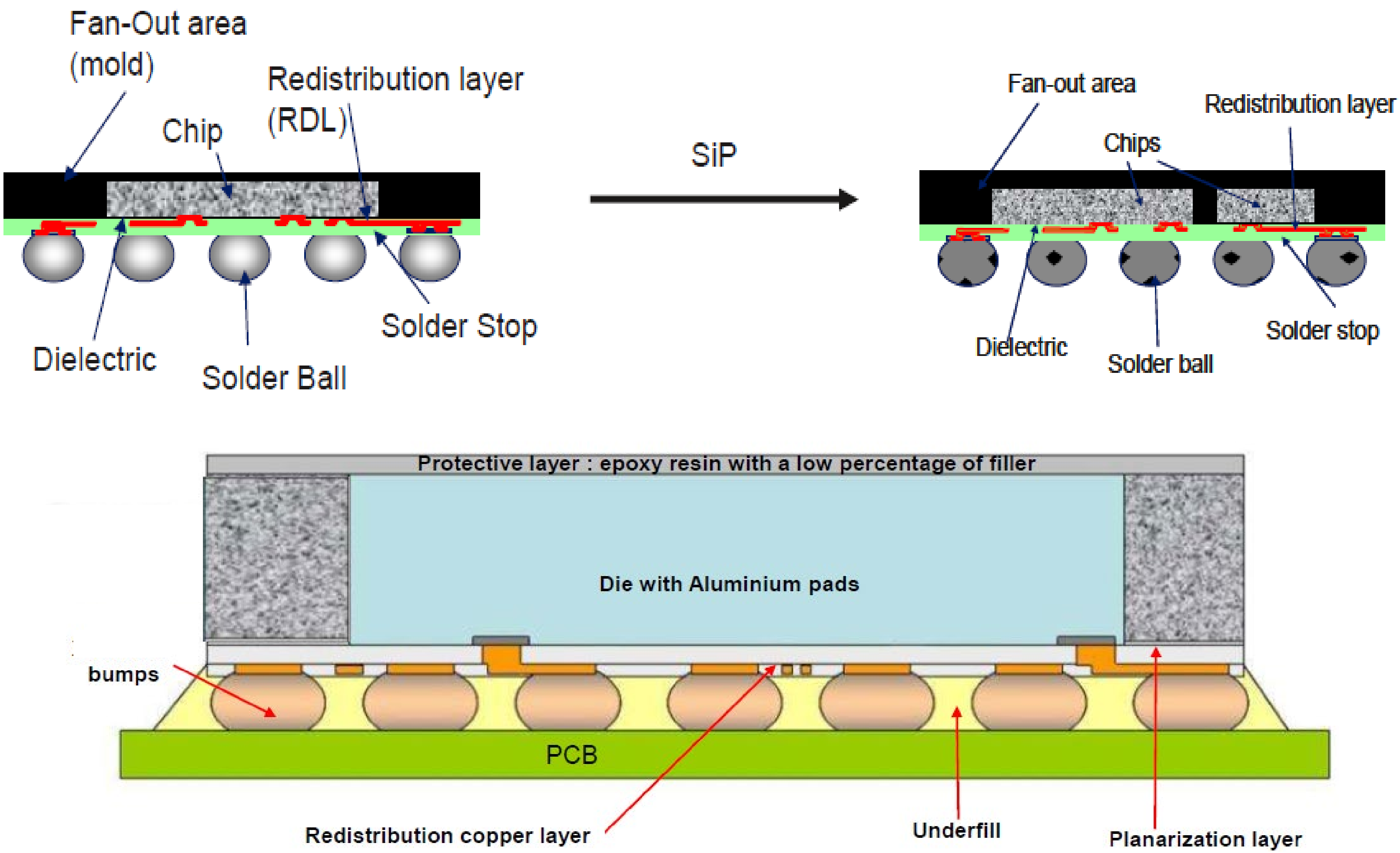


Source: Namics

Recent Advances in Advanced Packaging

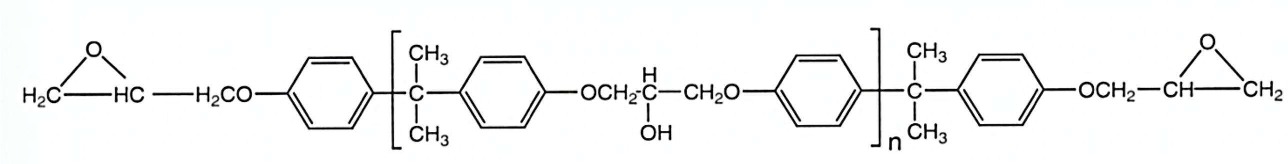
- Fan Out Wafer Level Packages (FOWLP)
- Fan out Panel Level Packages (FOPLP)
- Antenna in Package for 5G
- Ultra low loss substrates

Embedded Wafer Level Packaging (eWLP)

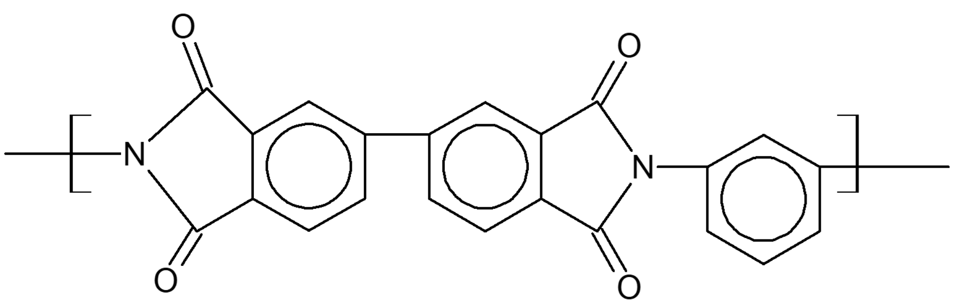


Source: Infineon eWPL fanout package

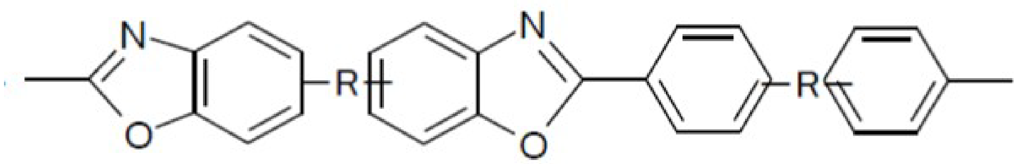
Polymers Used In Wafer Level Packaging



Epoxy

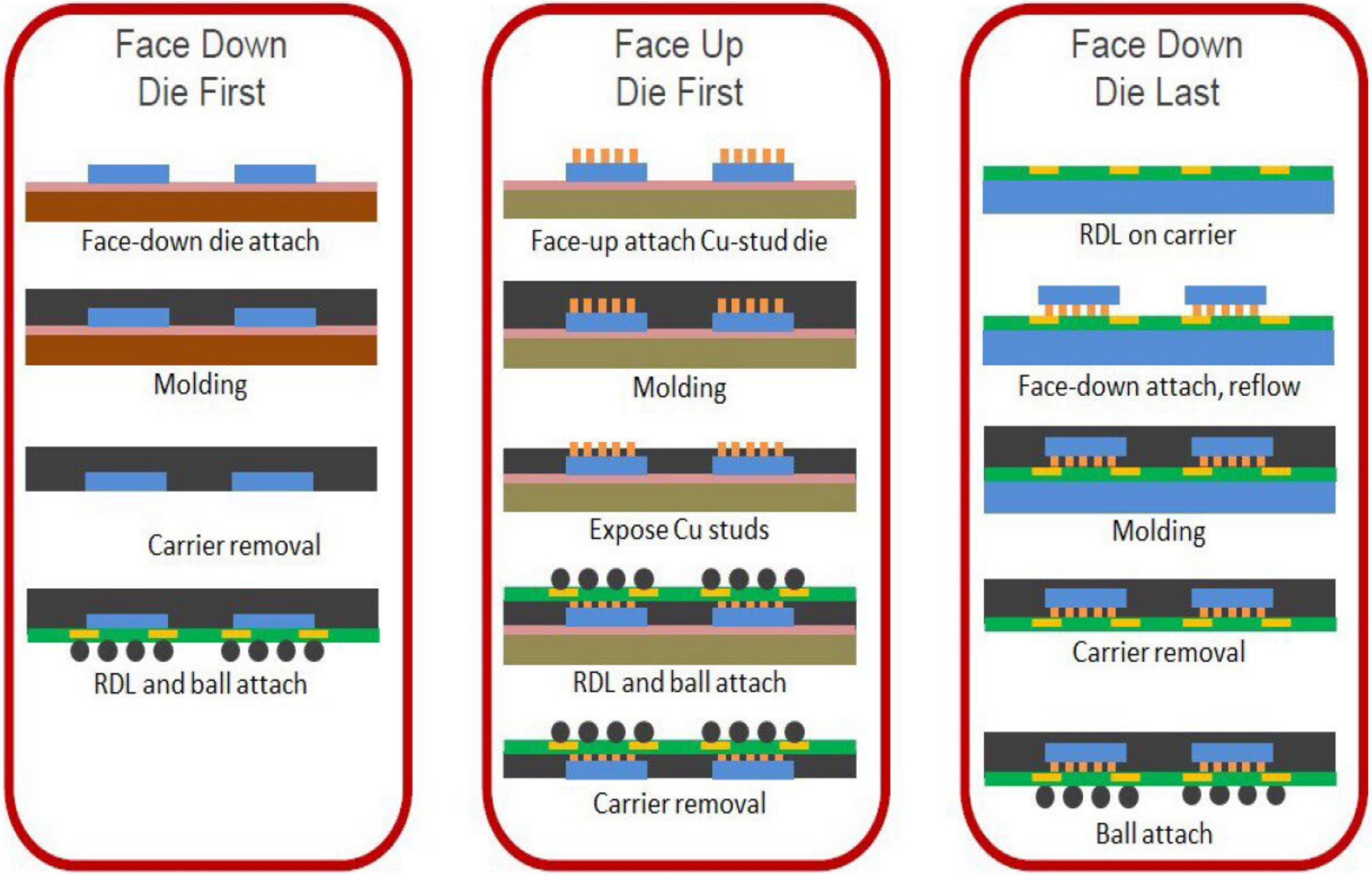


Polyimide (or photosensitive (PSPI))



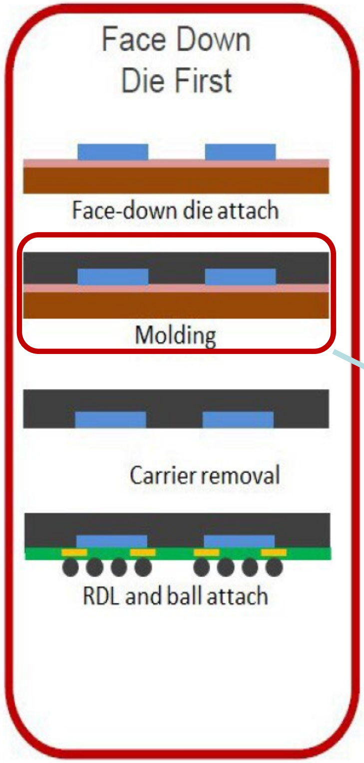
Polybenzoxazole (PBO))

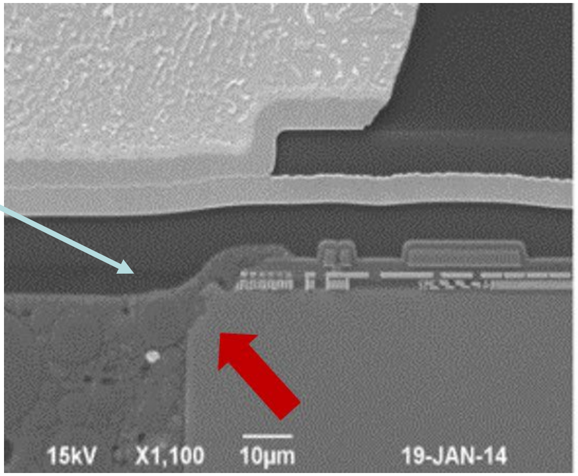
Fan-Out Wafer Level Process Flows

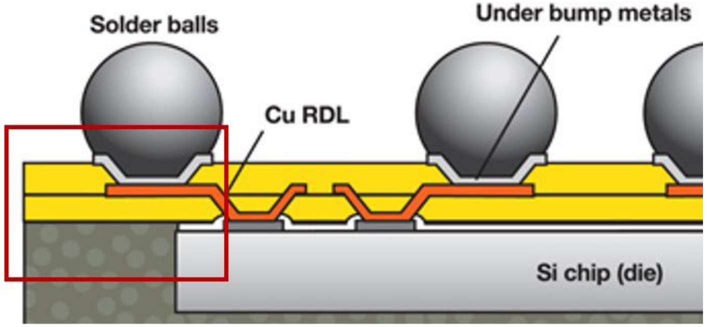


Source: SPIL

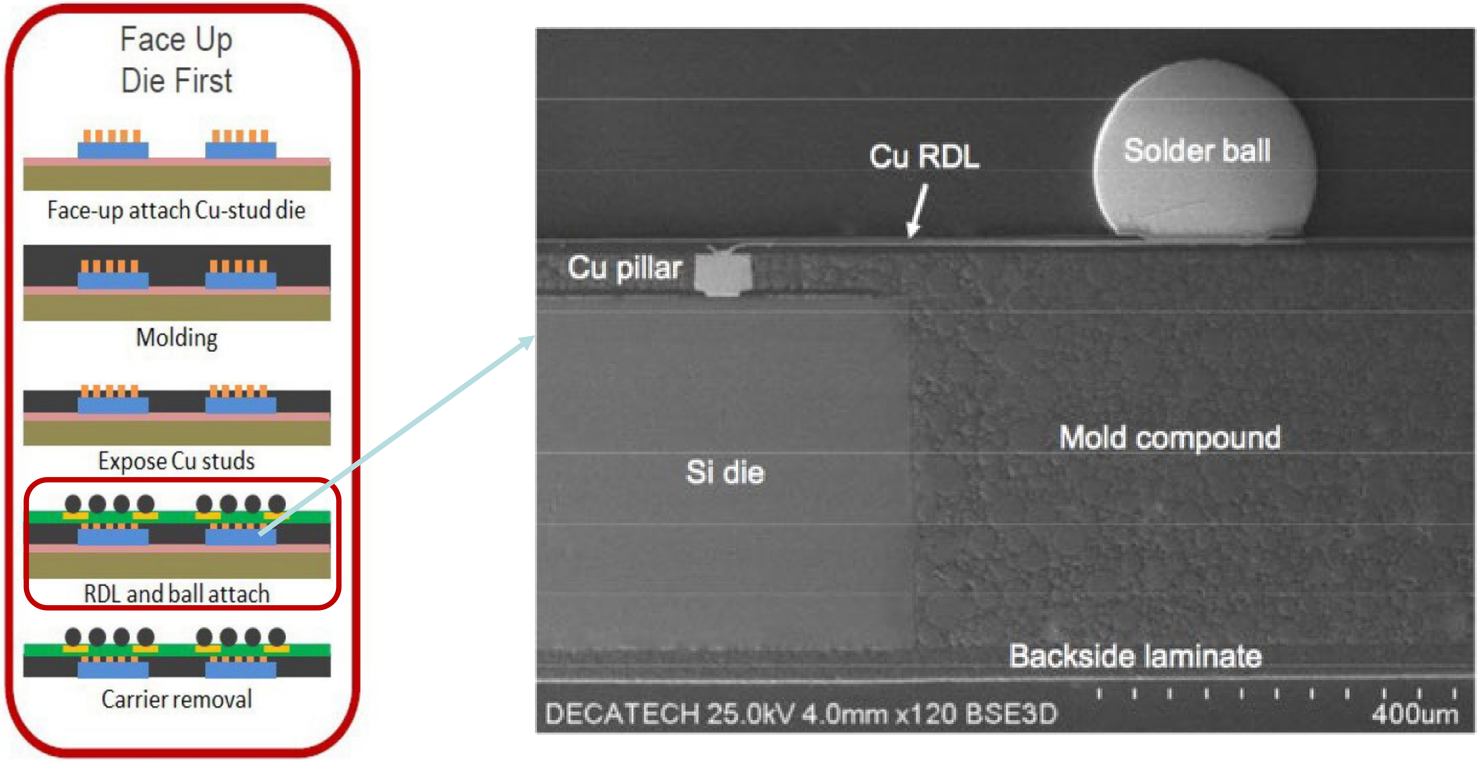
Chip First Planarity Issue





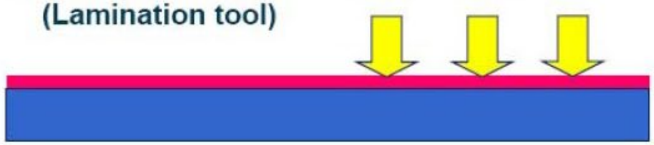


DECA Chip First Face Up

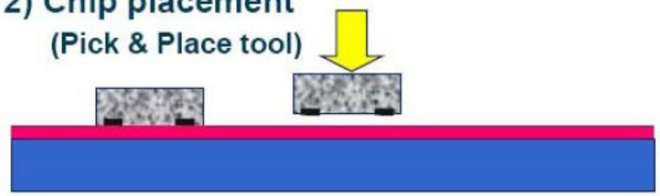


Reconstituted Wafer Process

1) Lamination of Foil onto Carrier
(Lamination tool)



2) Chip placement
(Pick & Place tool)



3) Compression Molding
(Mold Press)

4) Delamination of carrier and foil
(Delamination Tool)

Ready for standard WLB thin-film processing

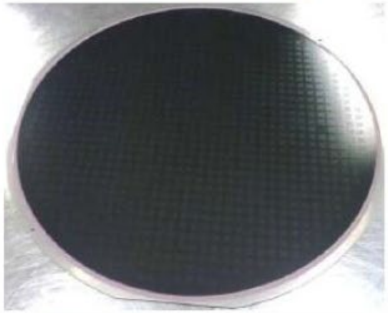
: Metal Carrier
: Adhesive Foil
: Chip with Pads
: Mold Compound

Carrier (Metal Plate)

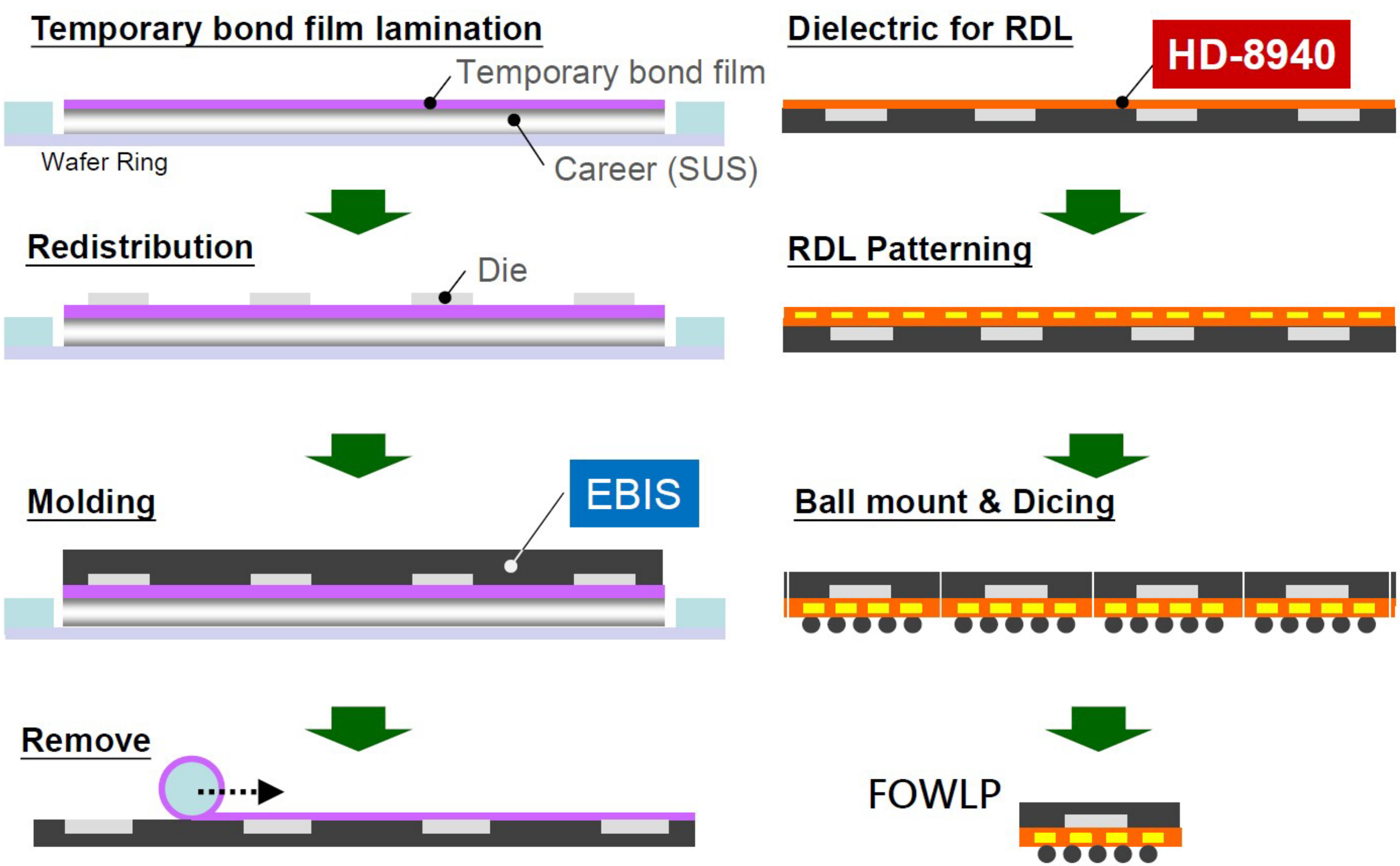
Carrier with Foil and Chips

Molding with
Liquid Moldcompound

Reconstituted
Wafer after Molding



Fan Out Wafer Level Package Process

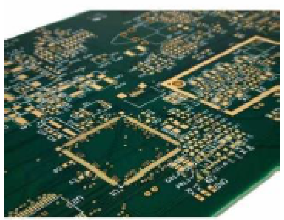


Antenna Integration for 5G mmWave

Current solution for 4G and upcoming 5G sub 6GHz

From SMT

Antenna integrated on Board (**AoB**)

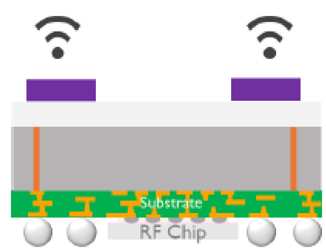


Signal loss
Antenna tuning issues
Transceivers far from antenna elements

Solution for 5G mmWave

to SiP

Antenna integrated in Package (**AiP**)

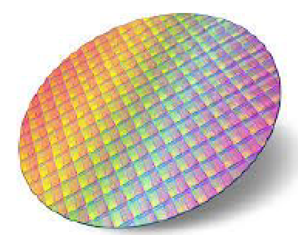


Best solution for 5G mmWave

Future solution for >=6G ??

to SoC ??

Antenna integrated on chip in BEOL (**AoC**)



Lossy
Manufacturing issues

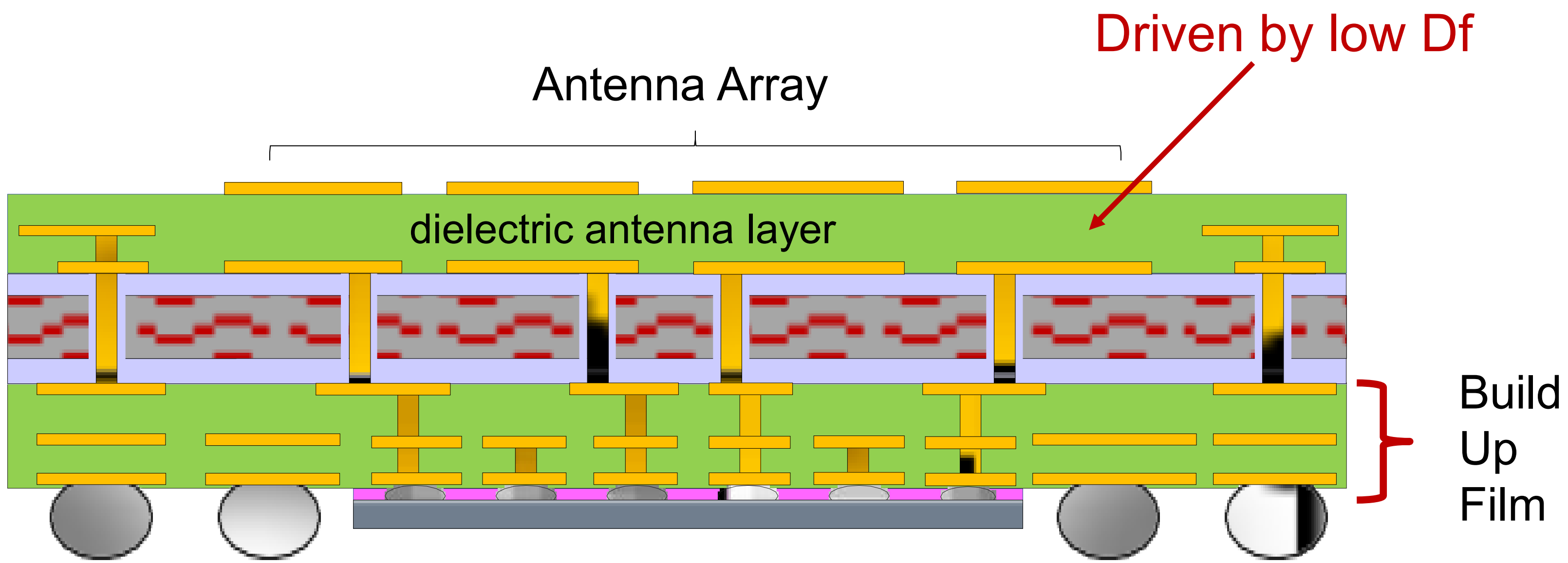
Source: Yole Developpement

Material Drivers for AiP

- Very low Df – primary driver
  - Needs to be < 0.002
- Low Dk – secondary
- Film format – drop-in PCB-like process
  - Lamination capable, i.e. flowable film during lamination
- Laser ablation capable
  - Form via’s
  - CO_2, excimer and Nd:YAG
  - Via walls capable to accept semi-additive plating

ASE Package with Integrated Antenna

Antenna is a key area for packaging innovation



Printed Circuit Board (PCB) process using advanced low Dk and Df materials for antenna layer and build up films

Antenna Gain

$$G(\vartheta,\varphi) = D(\vartheta,\varphi) * e_{diel.} * e_{cond.} * e_{mat.}$$

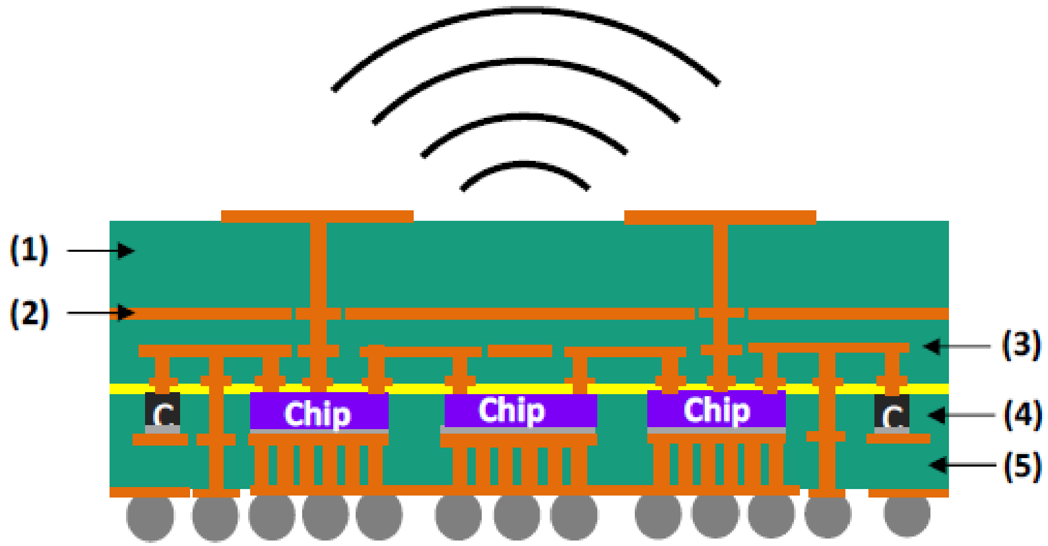


Figure 1: Example of a stack-up of the novel AiP platform for 5G mmWave. (1) antenna layer; (2) shielding layer; (3) re-distristribution/rougting layer; (4) component layer; (5) temperature control layer.

Courtesy Dr. Ivan Ndip, Fraunhofer IZM

Antenna Gain

$$G(\vartheta,\varphi) = D(\vartheta,\varphi) * e_{diel.} * e_{cond.} * e_{mat.}$$

Directivity

$$D \propto \frac{1}{\sqrt{\varepsilon r}}$$

Lower ε_r to increase gain

Dielectric Efficiency

Lower Df increases dielectric efficiency

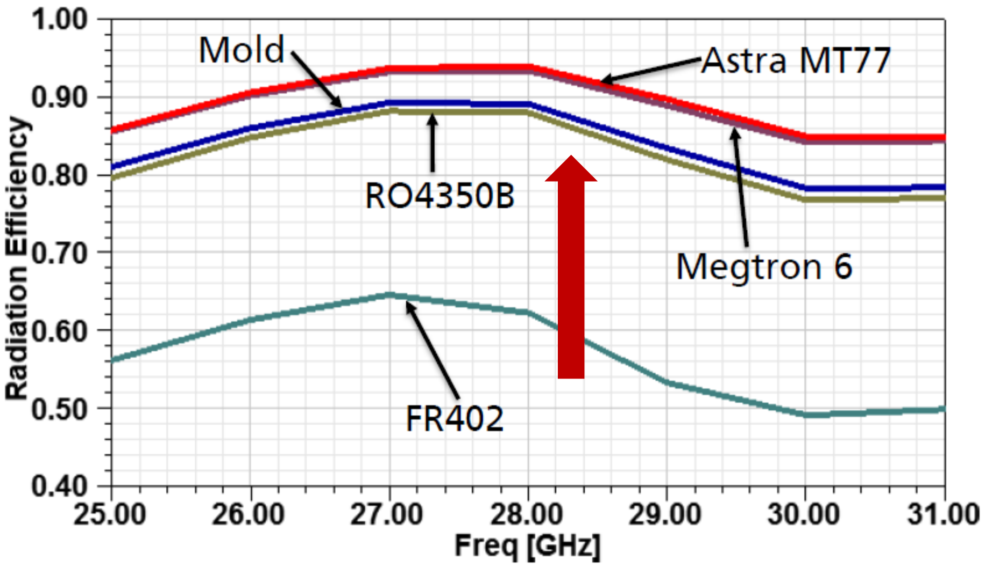
Conductor efficiency and impedance matching

Lower both the Dk and the Df to increase antenna gain

Courtesy Dr. Ivan Ndip, Fraunhofer IZM

Antenna Radiation Efficiency

Higher is better



	DK	DF
RO4350B	3.66	0.004
Astra MT77	3	0.0017
Megtron 6	3.35	0.002
Mold	3.65	0.0035
FR402	4.3	0.015

Radiation efficiency tracks with dielectric loss factor

Courtesy Dr. Ivan Ndip, Fraunhofer IZM

Transmission Loss

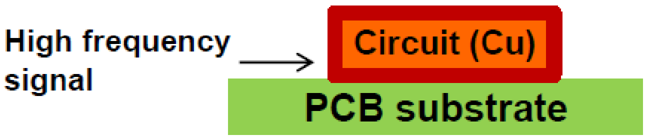
Conductor Loss + Dielectric Loss = Transmission Loss

$$\propto \sqrt{F} \times \mathrm{R}$$

$$\propto 27.3\ \frac{F}{C}\sqrt{Dk}\ \mathrm{Df}$$

F=frequency
C = speed of light
Dk = dielectric constant
Df = dissipation factor
R = conductor resistance

Transmission Loss



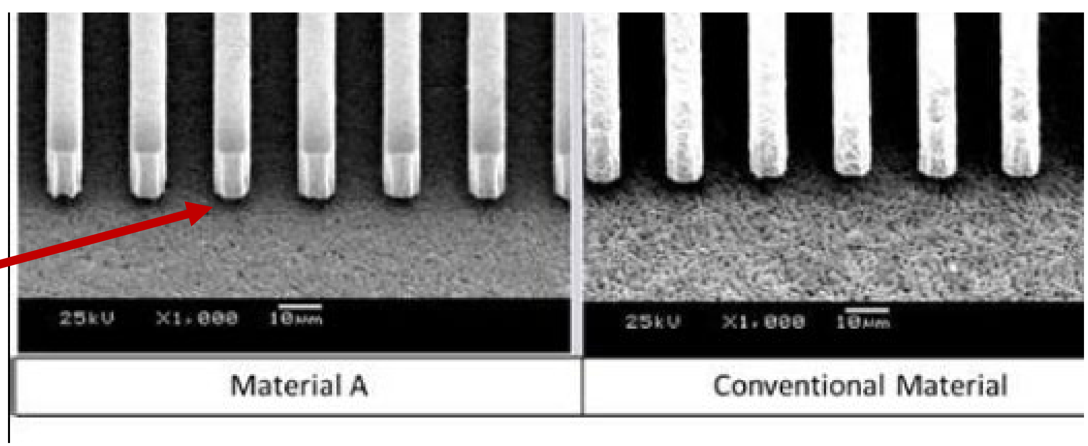
Roughened surface
Low transmission because of high resistance at the interface of Cu and resin

Smooth surface
High transmission because of low resistance at the interface.

To reduce the transmission loss…

- *Low dielectric loss tangent (Df)*
- *Low dielectric constant (Dk)*
- *Low smooth surface at the interface between resin and conduct layer*
- *Good adhesion strength with smooth surface*
- *Thinner layer*

Adhesion of smooth copper to laminate is critical



Ideal 5G Dielectric

Ideal Dielectric

Optimized Material Properties

- Lower Dk/Df
- Moisture absorption
- Thermal stability
- Adhesion to thin copper
- Mechanical properties (modulus, CTE, Tg)

Process Compatibility

- Lamination, rheology profile
- Laser drillable
- Compatible with lithography process
- Compatible with plating solutions
- Low warpage during process

Need both for a successful new product

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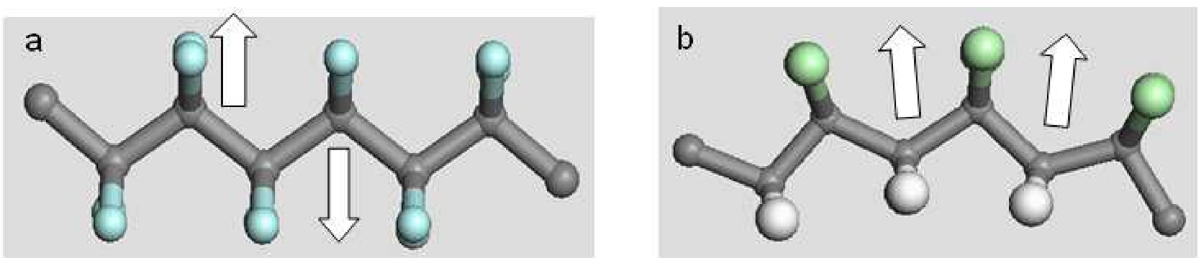
Design of Low Dk/Df Dielectric

There are two strategies:

1. Decrease dipole strength
   - Use materials with low polarizability
   - Symmetric orientation of dipole moments

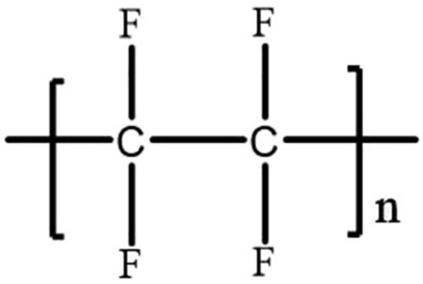


2. Decrease the number of dipoles
   - Lower the density of a material by increasing free volume
   - Introducing porosity (thermally volatile second phase)

Design Strategies

Use the following design approaches to reduce Df:

- Minimize presence of polar groups (dipoles) such as hydroxyl (-OH), carboxyl (-COOH), amide (-CONH-)
  - Also, will increase moisture absorption which increases Dk
- Add fluorine (-F), methylene (-CH2-), and alicyclic groups such as cyclohexyl
- Helical chain structure
  - Symmetric dipole moments

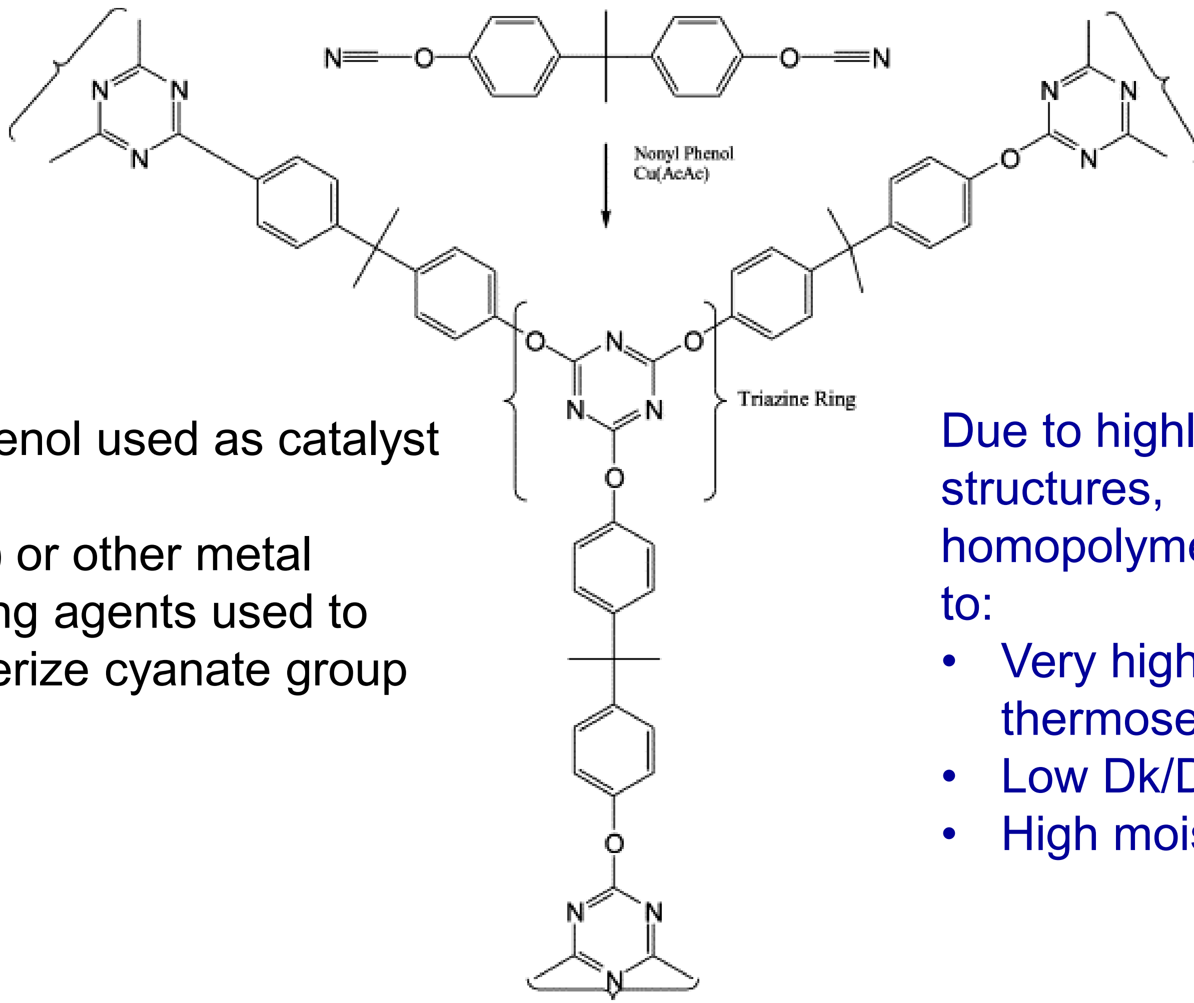


- Introduce fluorine, phenyl, naphthyl

Specialty Thermoset Low Dk/Df Materials

- PTFE: Rogers 3003 (ceramic filled PTFE)
- Nelco N4000 series (i.e. N4350-13RF, Df=0.0065)
  - Modified epoxy
- Modified epoxies
  - Isola GETEK® and Panasonic Megtron®; modified epoxies with functionalized polyphenylene oxide (PPO to lower Df)
- Cyanate ester epoxy blends
  - Nelco N8000 series (low polarity)
- Cyanate esters (Df = 0.008)
  - Low polarity due to cyclotrimerization mechanism

Cyanate Ester Chemistry



Nonyl Phenol used as catalyst

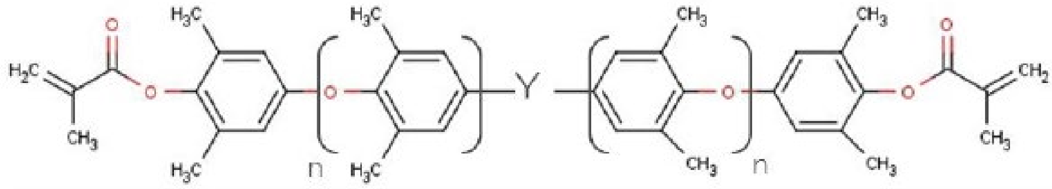
Cu(AcAc) or other metal complexing agents used to cyclotrimerize cyanate group

Due to highly aromatic ring structures, homopolymerization leads to:

- Very high Tg, but brittle thermoset
- Low Dk/Df
- High moisture absorption

AGC Low Df Laminates and Prepregs

- AGC (formerly Asahi Glass Co. in Japan) See: https://www.agc-multimaterial.com
- PTFE systems
  - PTFE glass (ex. TLY-5A, lightweight woven fiberglass)
  - PTFE ceramic (ex, NF-30, ceramic-filled composite)
- Meteorwave® PPE/Modified Epoxy
  - Poly(phenylene ether) (PPE) modified epoxy
  - Meteorwave® 8000 Ultra low loss PPE (Df = 0.0016 @ 10 GHz)
    - Spread weave fiberglass, amorphous silica filler (7-15%)



Recent Isola Low Df Offerings

Astra® MT77 (target mm wave frequencies and beyond)

- Very low loss laminate and prepreg
- Dk = 3.00 / Df = 0.0017
- Tg = 200°C

Tachyon® 100G

- Ultra low loss laminate and prepreg
- Dk = 3.02, Df = 0.0021
- Tg = 200°C

TerraGreen®

- Halogen free, very low loss laminate and prepreg
- Dk = 3.44 / Df = 0.0039
- Tg = 200°C

Dk/Df of Glass Reinforcements

Reinforcement impact, i.e., predominantly glass cloth

Reinforcement	D_k@ 1 MHz	D_k@ 1 GHz	D_f@ 1 MHz	D_f@ 1 GHz
E-Glass	6.6	6.1	0.0020	0.0035
NE-Glass	4.4	4.1	0.0006	0.0018
S-Glass	5.3	5.2	0.0020	0.0068
D-Glass	3.8	4.0	0.0010	0.0026

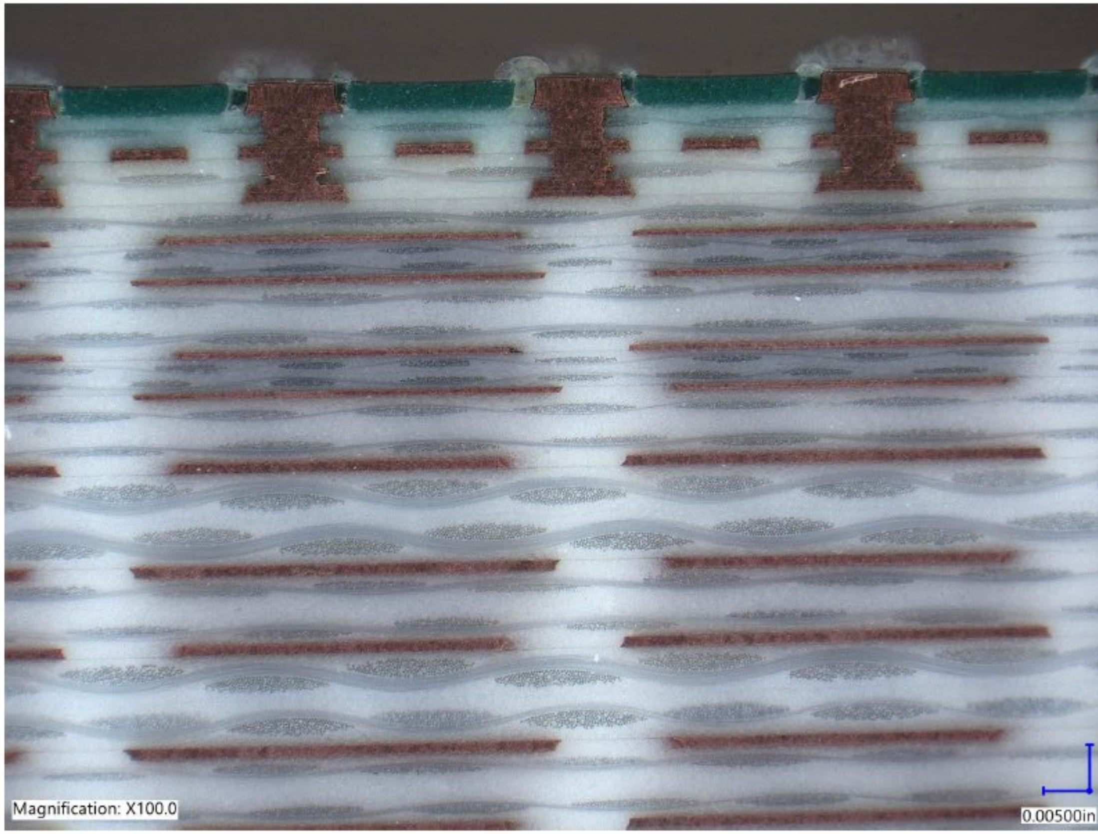
Glass has low Df

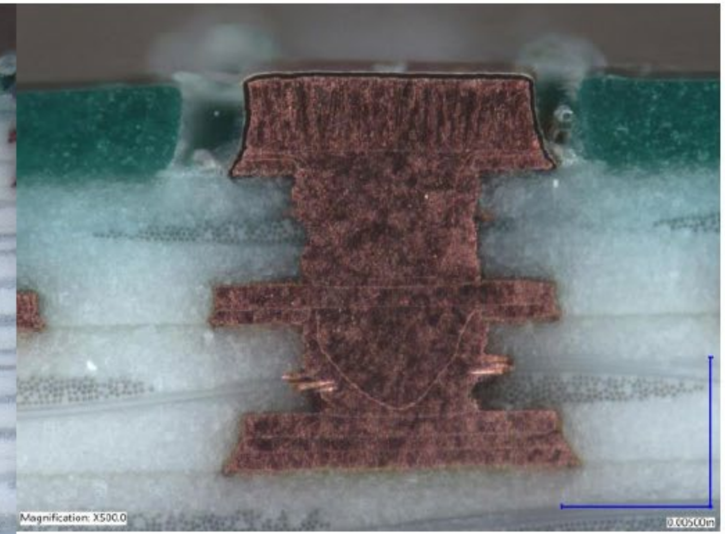
AGC Glass Laminates

	BCDR		
Extremely low loss laminate with NE glass	Freq. / GHz	Dk	Df
	14	3.07	0.0011
	28	3.07	0.0013
	40	3.07	0.0015
Extremely low loss laminate with NER glass	Freq. / GHz	Dk	Df
	14	3.05	0.0009
	28	3.05	0.0011
	40	3.05	0.0012
Extremely low loss laminate with L2 glass	Freq. / GHz	Dk	Df
	14	3.01	0.0009
	28	3.01	0.0011
	40	3.01	0.0012

Source: AGC presentation at IMAPS 2023

AGC Laser Processability





Source: AGC presentation at IMAPS 2023

Multiple woven glass fabrics used, typically spread fiberglass

Properties of AGC ELL Halogen Free (HF)

Property	Item	Typical value	Unit
Thermal	Tg	190	°C
	CTE, Z-axis	42	ppm/°C
	Z-axis Expansion	2.4	%
	Td (5%)	410	°C
	T300	120+	min
Electrical	Dk	3.4	
	Df	**0.0013**	
Physical	Peel Strength	3.5	lbs/in
	Flexural Strength	290	MPa
	Flame Resistance	V-0	

Source: AGC presentation at IMAPS 2023

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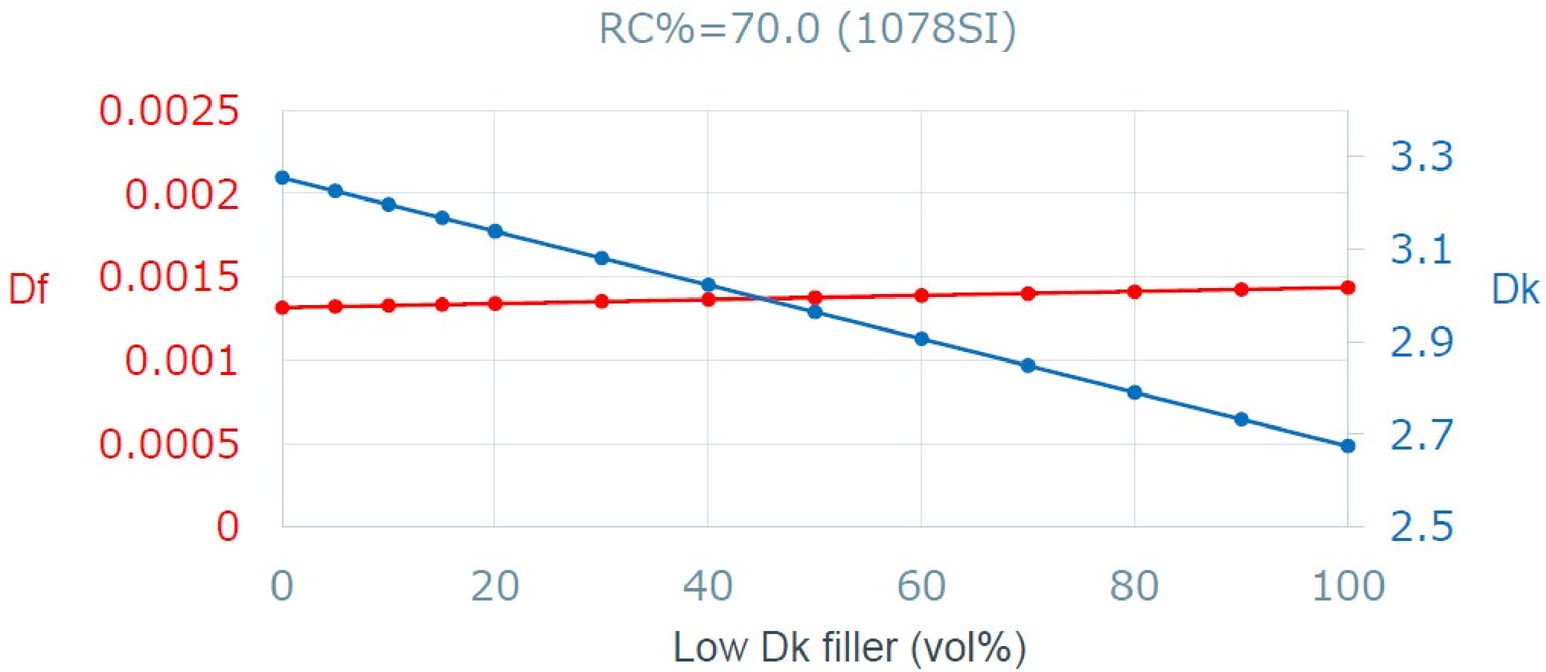
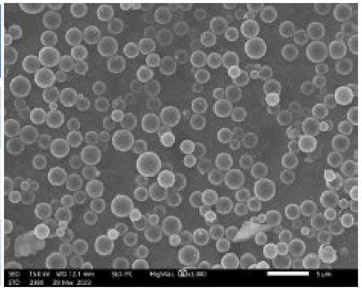
AGC Next Generation for Chip Packaging



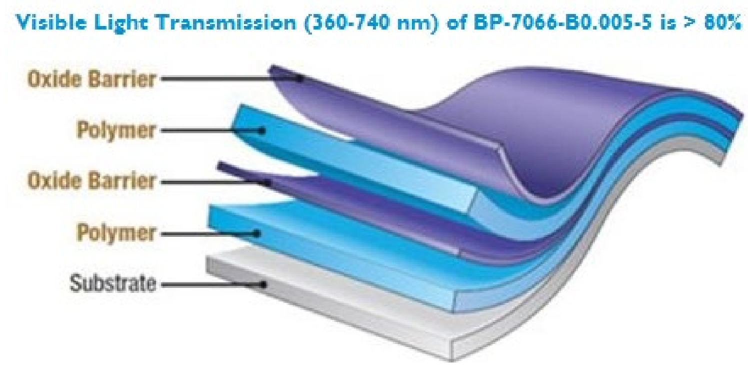
	Solid Silica	Low Dk filler
Dk	4.0	1.5
Df	0.001	0.001
D_{50} (µm)	2-5	2-3



Source: AGC presentation at IMAPS 2023

Non-Hermetic Coatings

- Material Properties:
  - low stress coatings that resists mobile ion permeation and moisture ingress are desirable
  - Resistance to degradation of the interfacial adhesive strength and delamination
- Types of Coatings:
  - Silicone elastomers
  - High purity epoxies
  - Room temp vulcanized (RTV) silicones
  - Fluorinated silicones and acrylics
  - Parylenes with bi-layer and tri-layer designs



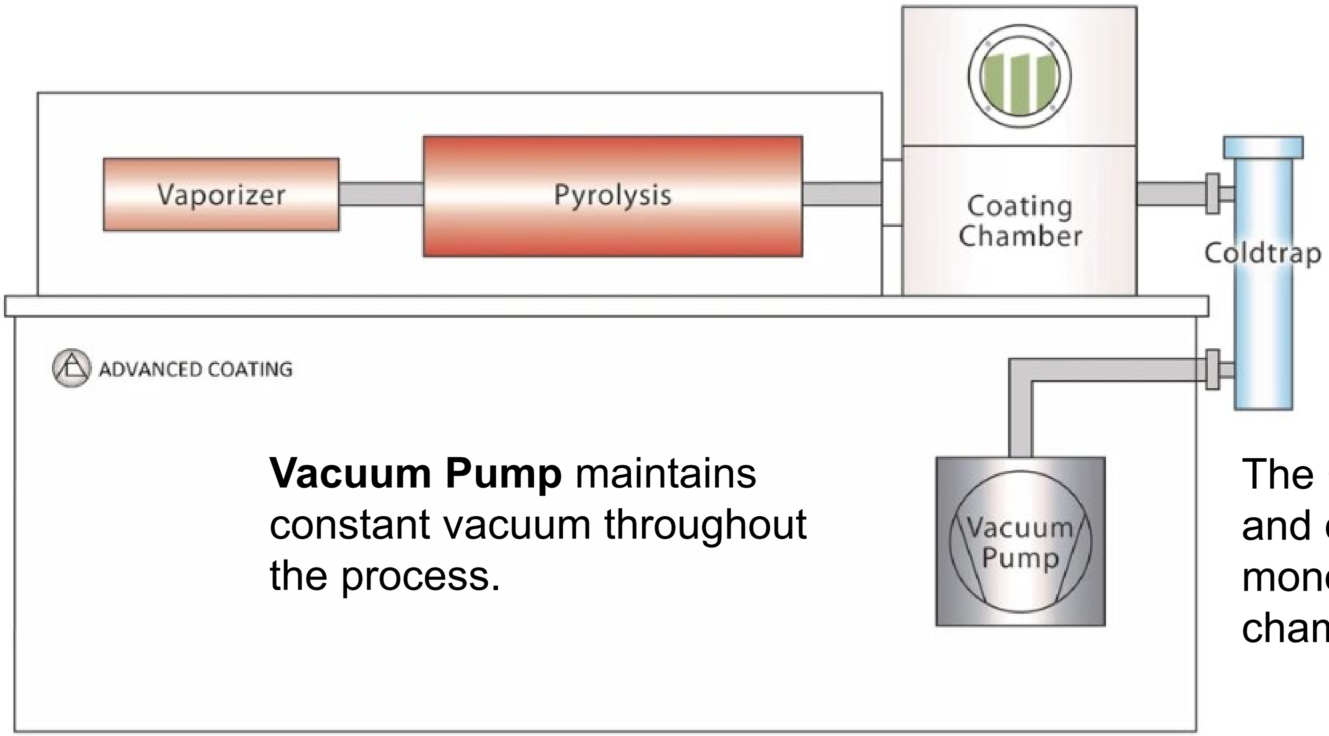
Moisture Barrier Coatings

- Low moisture absorption and permeability
- Processing characteristics and thermal profiles before and after coating
- Adhesion of coating to package
- Avoid cracks, pin holes, interfaces, moisture paths and capillary action
- Coating thickness, density, fillers
- Effect of temperature on coating moisture properties (i.e.Tg)
- Degree of cross linking and polarity of the coating
- Interactions between the coating and the migrating species
- Cleanliness of the applied coating
- Surface cleanliness and texture prior to coat

Parylene

- Vacuum-deposited hydrocarbon coating
- Thicknesses from Angstroms to mils, typically in micron range
- Good combination of electrical and physical properties
- Very low permeability to moisture and volatiles

Parylene Vacuum Deposition Process



Vacuum Pump maintains constant vacuum throughout the process.

The **Cold Trap** collects and condenses excess monomer from vacuum chamber

Source: Advanced Coating (parylene conformal coating specialist) www.advancedcoating.com/depositionprocess

Parylene Vacuum Deposition Process

Phase 1 - Vaporization

The dimer is added to the Vaporizer and is heated to 75-250°C depending on application and Parylene type. The dimer turns from a powder into a vapor.

Phase 2 – Pyrolysis

The Dimer is heated in the furnace at 600 – 700 °C and becomes a monomer.

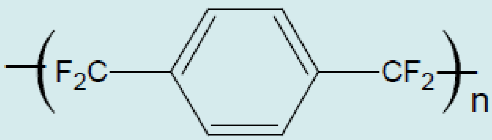
Phase 3 – Deposition

Dimer turns into a polymer that adheres evenly as transparent Parylene film to the components inside the coating chamber at ambient temperature.

The Parylene coating process does not include any liquid phase and there is ***no traditional curing time involved***.

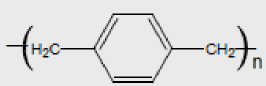
Source: Advanced Coating (parylene conformal coating specialist) www.advancedcoating.com/depositionprocess

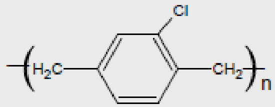
Parylene Vapor Deposition Monomers

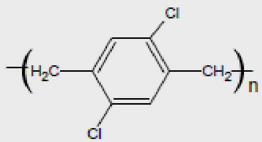


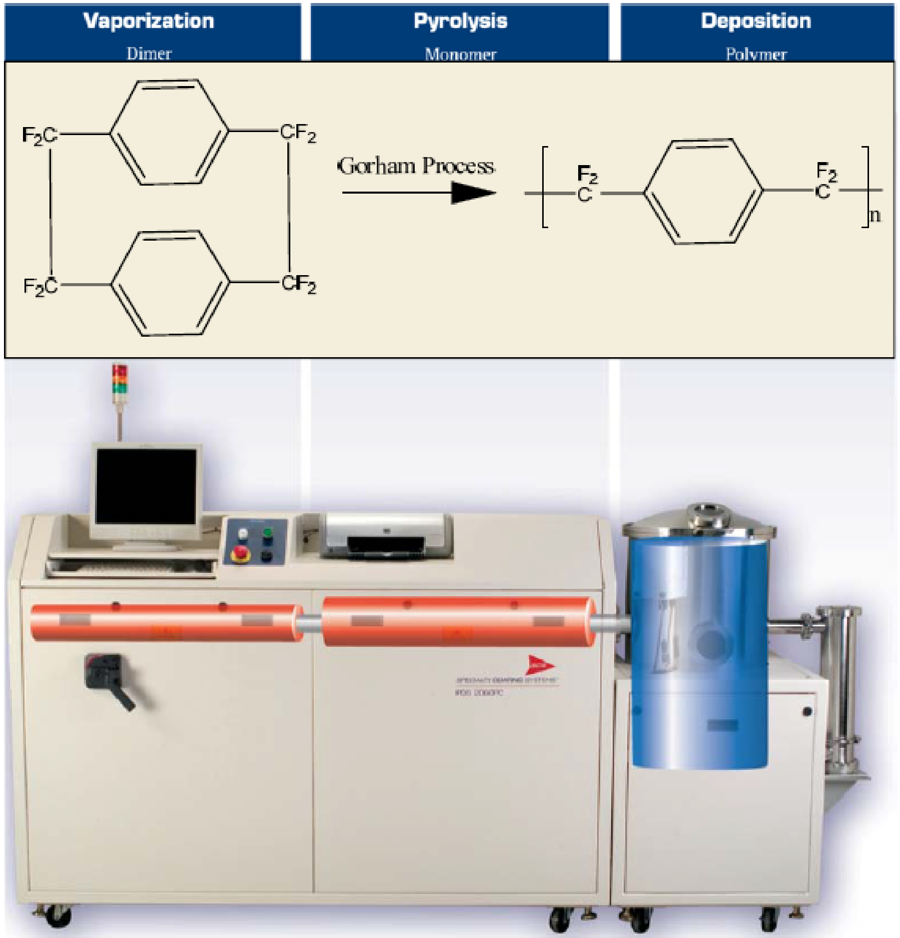
Parylene HT®

High Temperature
Fluorinated Parylene

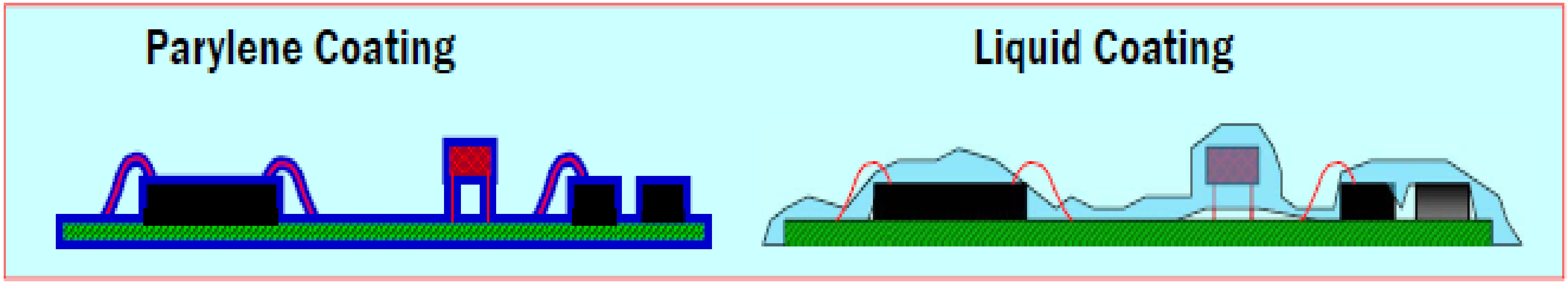
Parylene N 

Parylene C 

Parylene D 



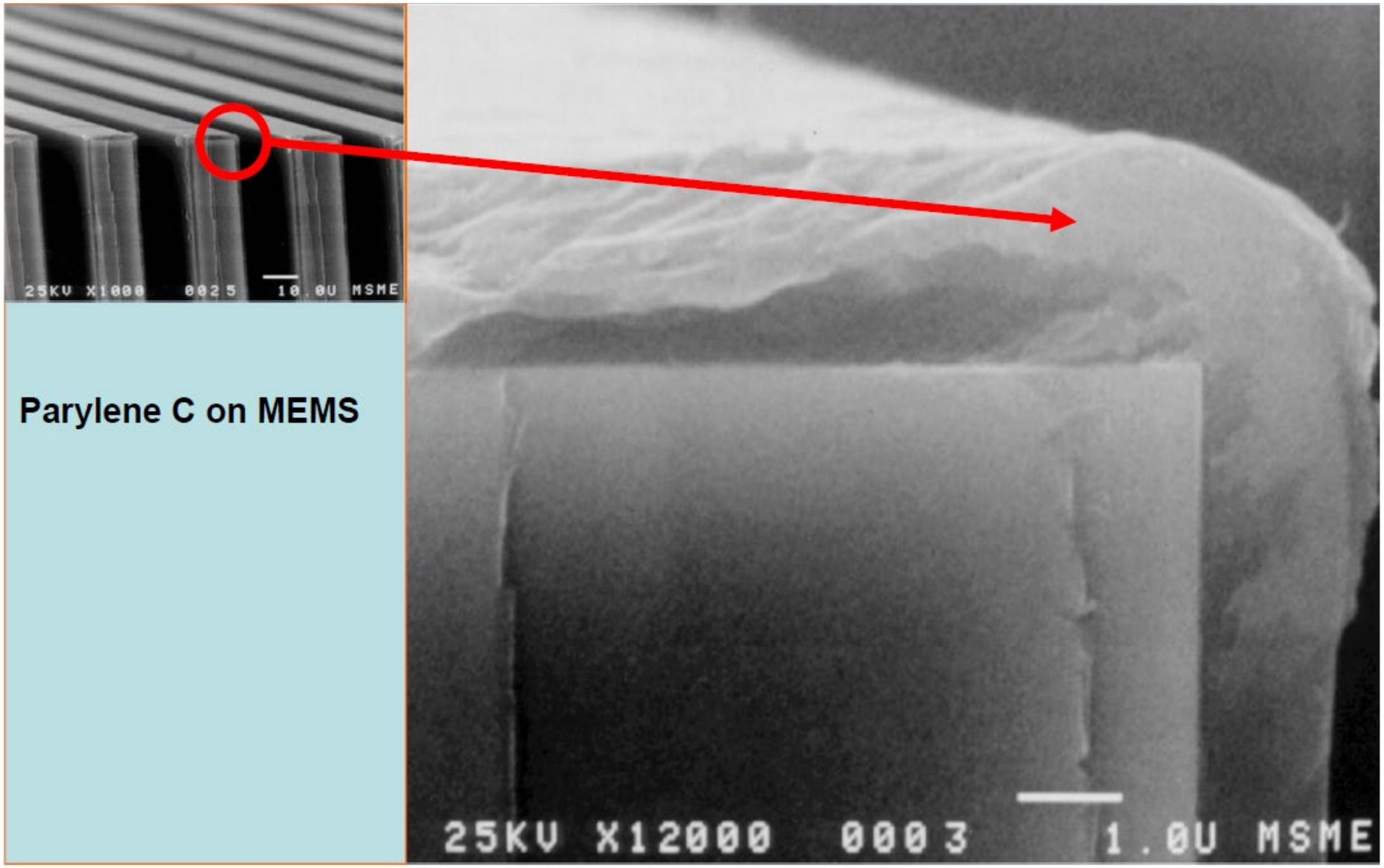
Parylene Coatings



Advantages of Parylene

- Able to coat a variety of substrates
- Uniform with no pooling/voids
- Stress free application
- Low dielectric constant
- Optical clarity/transparency
- Excellent electrical insulation
- Excellent chemical and moisture barrier
- High dry-film lubricity
- Environmentally safe
- Extremely thin
- Pinhole and defect free
- Biostable and biocompatible

Parylene Conformal Coating to 1 micron



Parylene Manufacturing Options

- Commercial services are available to coat product in volume.
- Users can purchase equipment and operate processes themselves.
- Parylene has a good track record and is in common use throughout both the electronics and medical device industries.

Polyimide Film Applications

- **FPC**
  - Cover layer
  - Adhesive
  - Substrate
- **Wire and Cable**
  - Insulation, wire and coil wrapping
- **Motor and Generator**
  - Magnet wire
  - Ground insulation slot liner
- **Pressure sensitive tape**
  - Solder masking tape
  - Thermal insulating tape
- **Specialty Fabricated Products**
  - Speaker coils, barcode labels, gaskets, sensors, transfer belts
- **Solar panel, silicon wafer coating**
- **Flexible heaters**
- **Others**
  - Adhesives
  - Fiber sizing
  - Others

Source: Polyimide Film --- Market Estimates & Trend Analysis Nov 2017 by Grandview Research

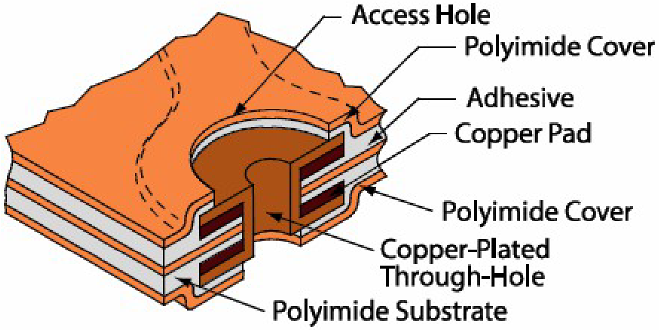
Polyimide Suppliers

- DuPont-Toray (Japan)
- Ube Industries (Japan)
- SKC Kolon PI (South Korea)
- Kaneka Corporation (Japan)
- Taimide Tech Inc. (Taiwan)
- Arakawa Chemicals Industries, Inc. (Japan)
- Shinmax Technology Ltd. (Taiwan)

Double Layer FCCL

Double-layer

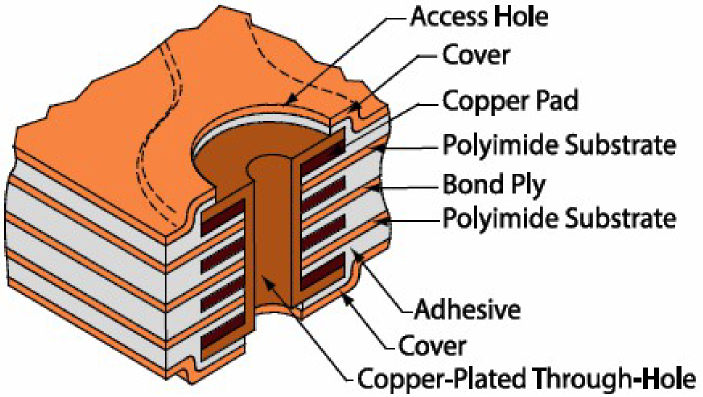
- IPC-6013, MIL-P-50884 - Type 2
- Two conductive layers with an insulating layer between them; outer layers may have covers or exposed pads.
- Plated through-holes provide connection between layers.
- Access holes or exposed pads without covers may be on either or both sides; vias can be covered on both sides.
- Stiffeners, pins, connectors, components are optional.



Multilayer FCCL

Multilayer

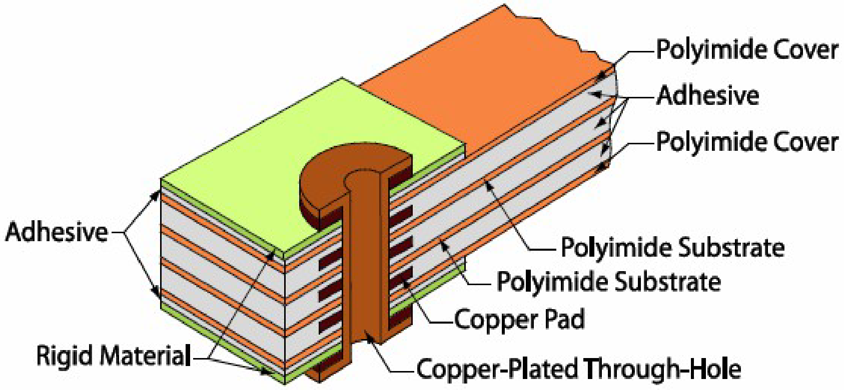
- IPC-6013, MIL-P-50884 - Type 3
- Three or more flexible conductive layers with flexi insulating layers between each one; outer layers may have covers or exposed pads.
- Plated through-holes provide connection between layers.
- Access holes or exposed pads without covers ma be on either or both sides.
- Vias can be blind or buried.
- Stiffeners, pins, connectors, components are optional.



Rigid Flex

Rigid-flex

- IPC-6013, MIL-P-50884 - Type 4
- Two or more conductive layers with either flexible or rigid insulation material as insulators between each one; outer layers may have covers or exposed pads.
- A Rigid-flex has conductors on the rigid layers, which differentiates it from multilayer circuits with stiffeners. Plated through-holes extend through both rigid and flexible layers (with the exception of blind and buried vias). Rigid-flex costs more than a standard circuit with stiffeners.

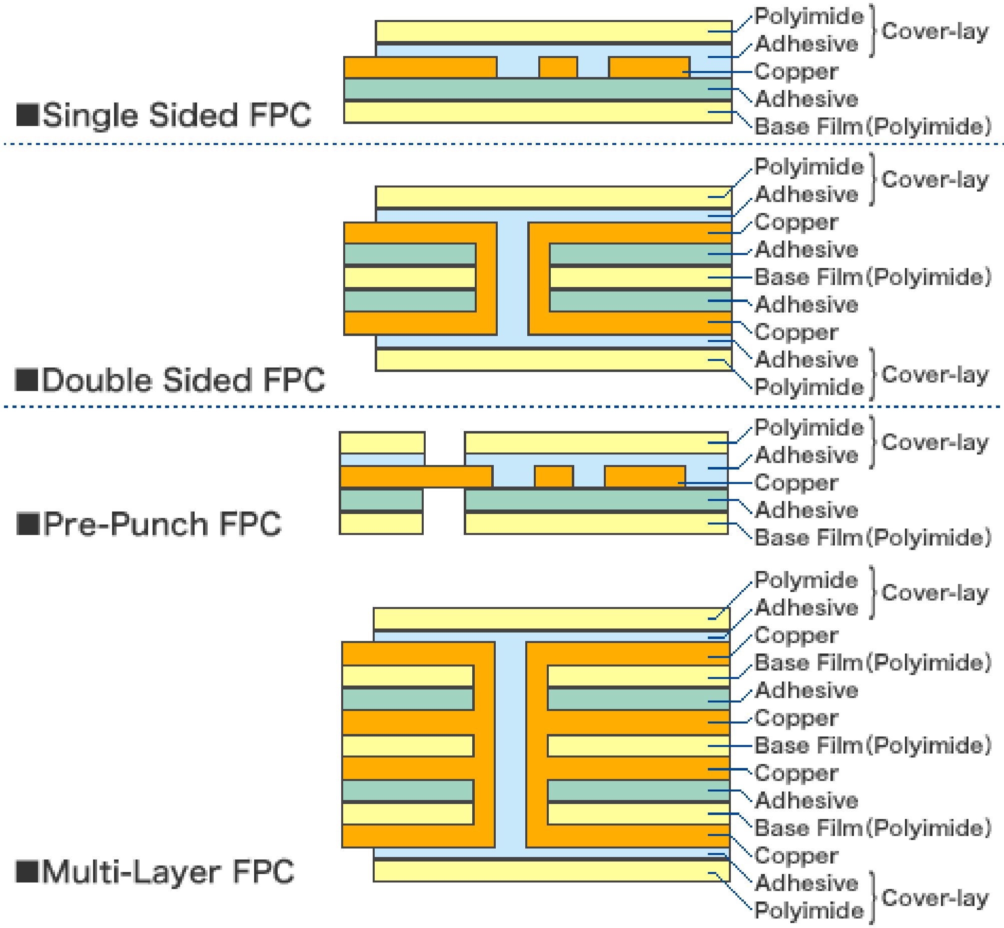


- Access holes or exposed pads without covers may be on either or both sides. Vias or interconnects can be fully covered for maximum insulation.
- Stiffeners, pins, connectors, components, heat sinks, and mounting brackets are optional.
- We also manufacture “flush” rigid-flex, where the top surface of contact areas is level with adjacent adhesive/insulation.
- Minco is capable of sequentially laminating, drilling, and plating circuits, which allows for more flexibility in designing the circuit.

Adhesives Used in Flex

- Acrylic – most common
- Flame retardant epoxy
- Epoxy prepreg
- Polyimide prepreg

Note: looking at stack-ups the adhesive is a key component in the mechanical and thermal performance



All Polyimides are not created alike!

Two types of polyimides:

1. Addition polyimide (this what the PCB mfg’s call high Tg polyimide)
   - Component of BT
   - Isola has a strong presence in high Tg polyimides
   - Available as prepreg and CCL
2. Condensation polyimide (DuPont Kapton™ and Ube Upilex®)
   - Films used in flex circuits
   - Films used in rigid-flex circuits
   - Specialty film applications

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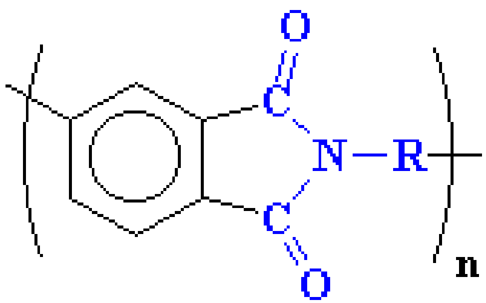
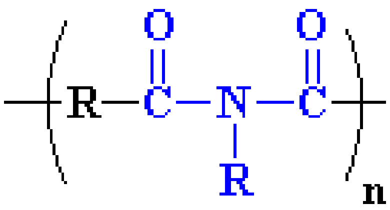
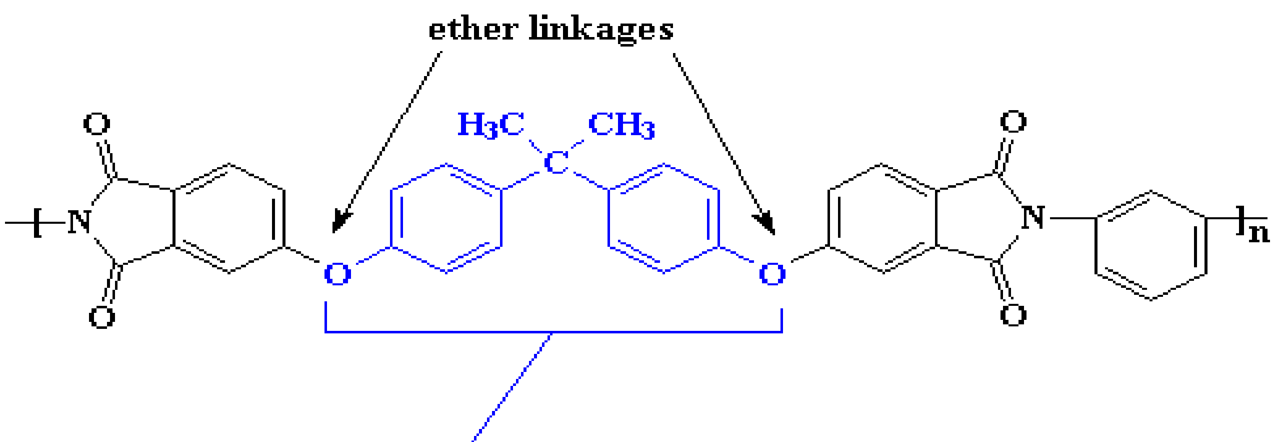
Polyimides



aromatic heterocyclic polyimide

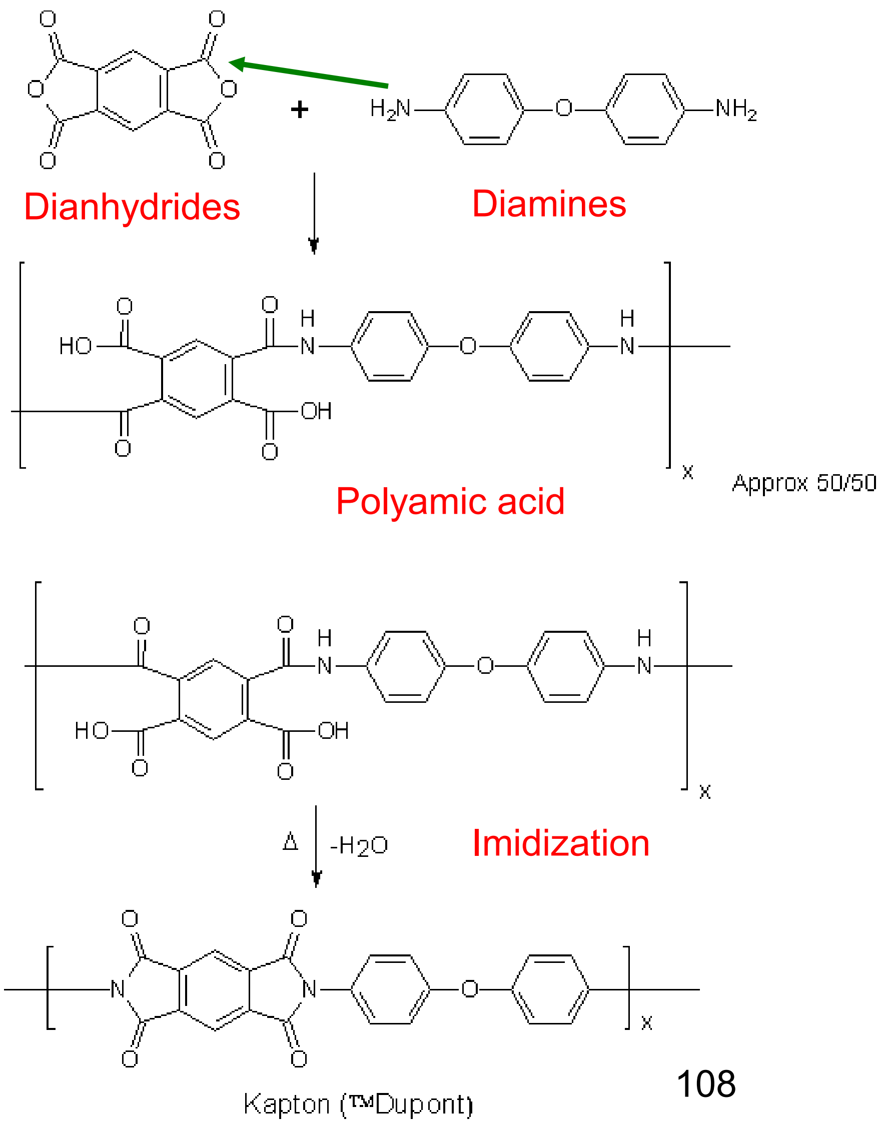


linear polyimide



This **bisphenol-A** linkage and these two ether linkages lend flexability to the polyimide.

Condensation Polyimides

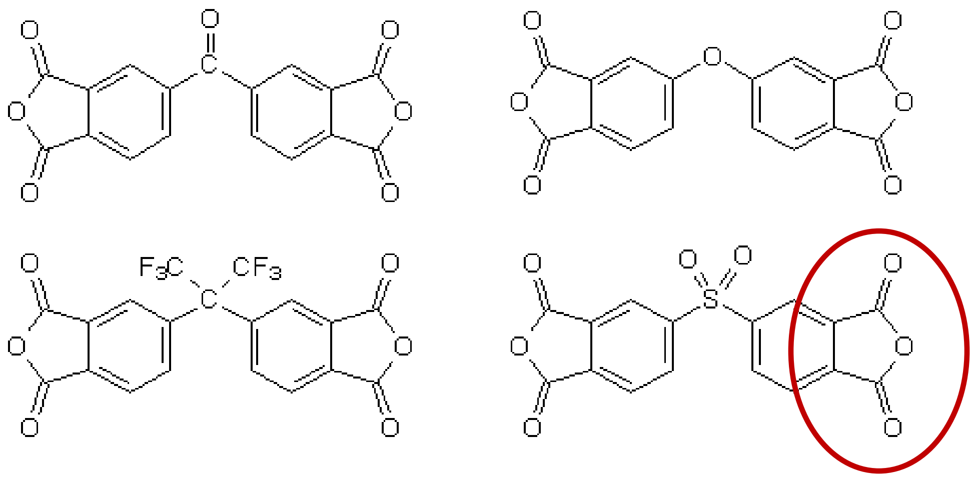


Chemical reaction to form polyamic acid allowing processing (spin coating or casting)

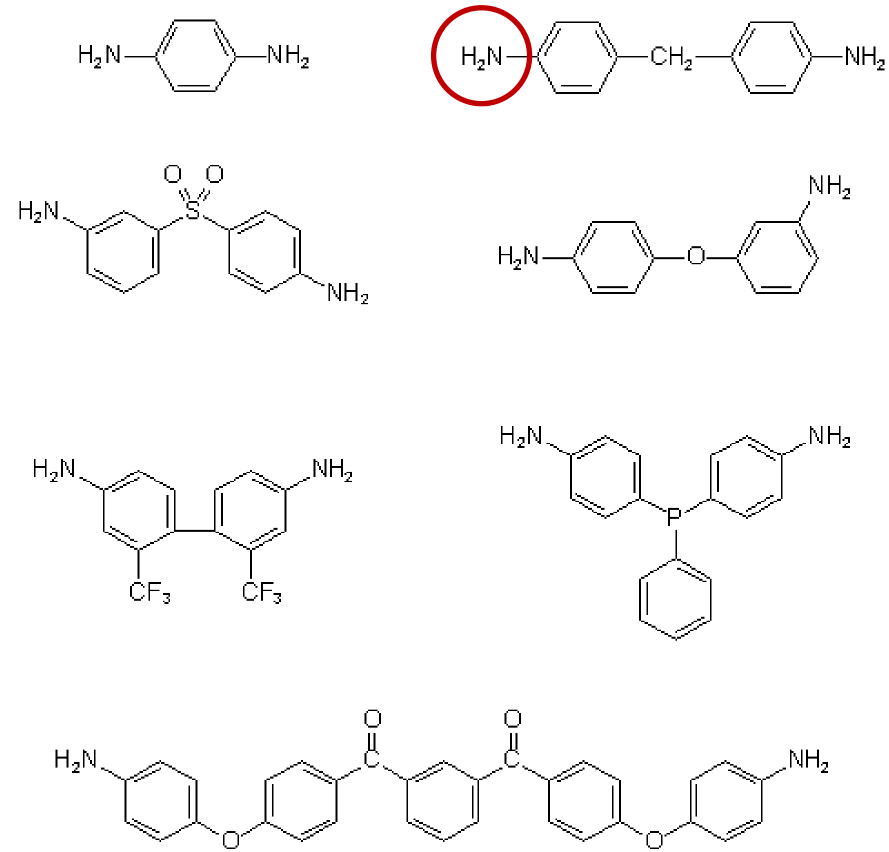
DuPont Kapton™ is PMDA ODA

Chemical reaction to form highly rigid, polyimide films like DuPont Kapton™

Polyimide Chemistry Toolbox



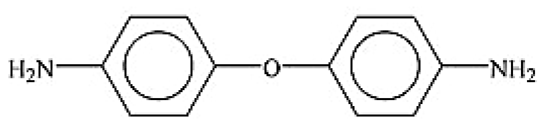
Dianhydrides



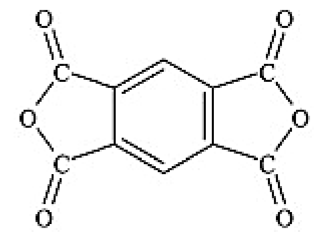
Diamines

DuPont Kapton^{TM} Chemistry

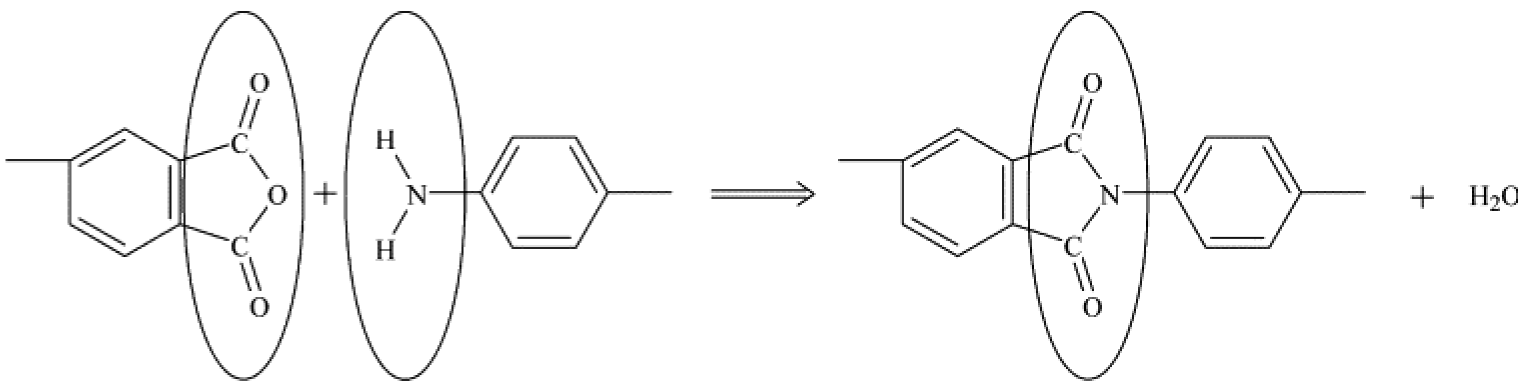
Pyromellitic dianhydride (PMDA)
4,4’ diaminodiphenyl ether oxydianaline (ODA)



4,4'-diaminodiphenyl ether
oxydianiline (ODA)



Pyromellitic Dianhydride (PMDA)



Anhydride Group

Amine Group

Imide Group

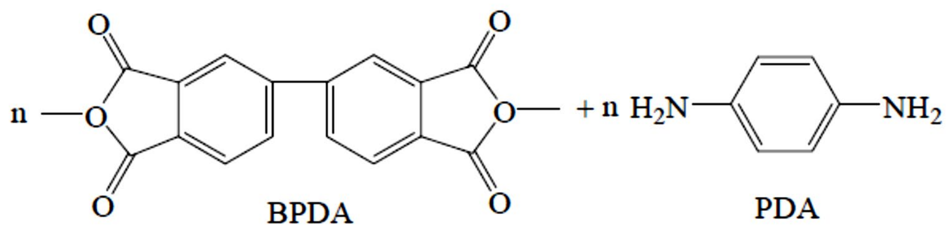
DuPont Kapton^{TM} Films

Kapton polyimide films come in several types, each with unique properties and applications. Commonly used types include:

- **HN:** A general-purpose, transparent polyimide film with a good balance of properties across a wide temperature range.
- **FN:** HN film coated on one or both sides with a fluoropolymer resin, providing heat sealability, a moisture barrier, and enhanced chemical resistance.
- **EN:** A low CTE film designed to match copper's thermal expansion, ideal for flexible printed circuits and high-density interconnects.
- **B:** A matte black film offering exceptional physical, chemical, and electrical properties across a broad temperature range.
- **FPC:** Films with higher dimensional stability and surface modified for improved adhesion.

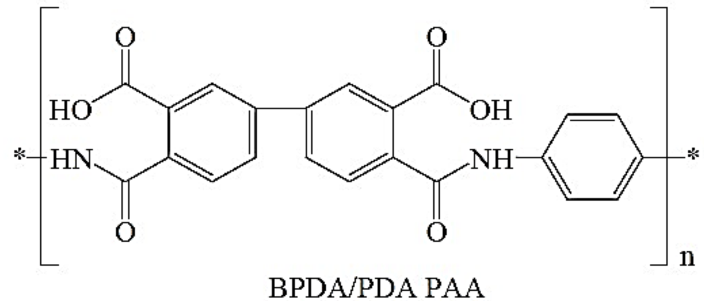
Upilex® Polyimide Chemistry

Upilex uses slightly different starting materials



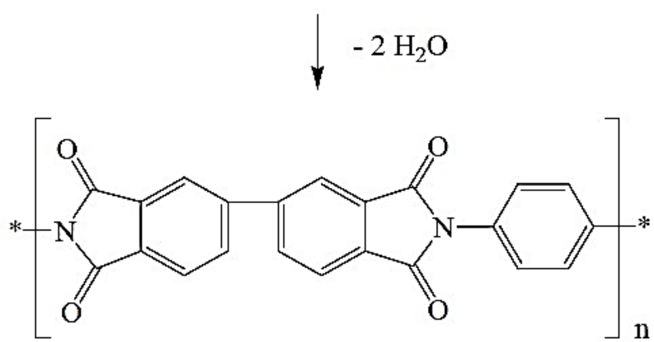
Biphenyltetracarboxylic dianhydride (BPDA)

Phenylenediamine (PDA)



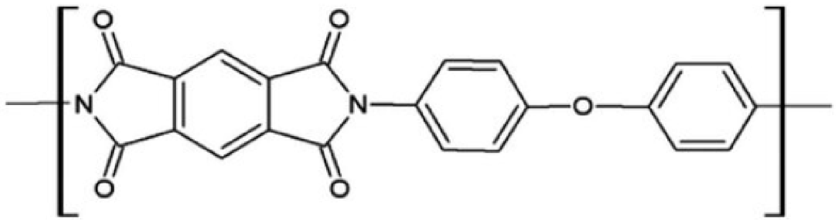
Polyamic Acid

Ring closure with loss of H_2O



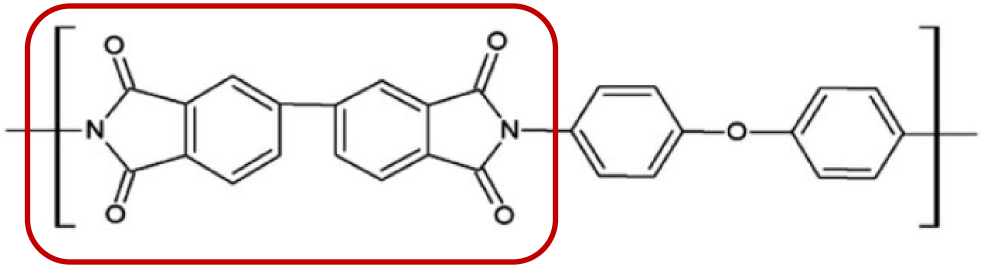
BPDA PDA

Kapton™ and Upilex® Comparison



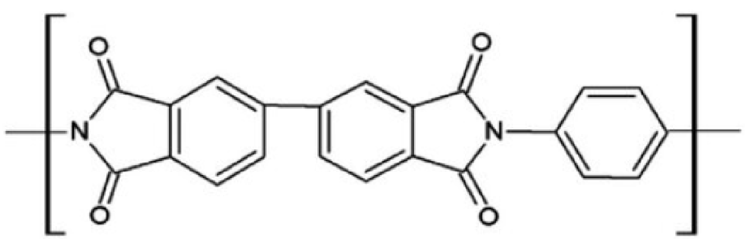
PMDA ODA

Kapton (DuPont)



BPDA ODA

Upilex R (UBE Ind.)



BPDA PDA

Upilex S (UBE Ind.)

Ube Upilex® Films

- Hig heat resistance up to 300C
- Excellent toughness and abrasion resistance
- Used where high strength films are required
- Excellent chemical resistance to organic liquids
- Very good electrical resistance
- Ube's proprietary polyimide film surface layer functionalized to enhance adhesion
- Note: Upilex polyimides have lower atomic oxygen erosion compared with Kapton and thus are potentially more suitable for harsh space environments

Ube Upilex® Films

- Upilex® – S
  - Basic grade
  - High rigidity and heat resistance
  - Low outgassing, excellent surface smoothness, chemical resistance
- Upilex® – VT and Upilex® – NVT
  - Thermally bondable film
  - Thermally bondable polyimide adhesion layer on both surfaces
  - Base polyimide film properties equivalent to Upilex® - S
- Upilex® – SGA
  - Improved adhesion for sputtering and plating
  - Specially treated Upilex® - S

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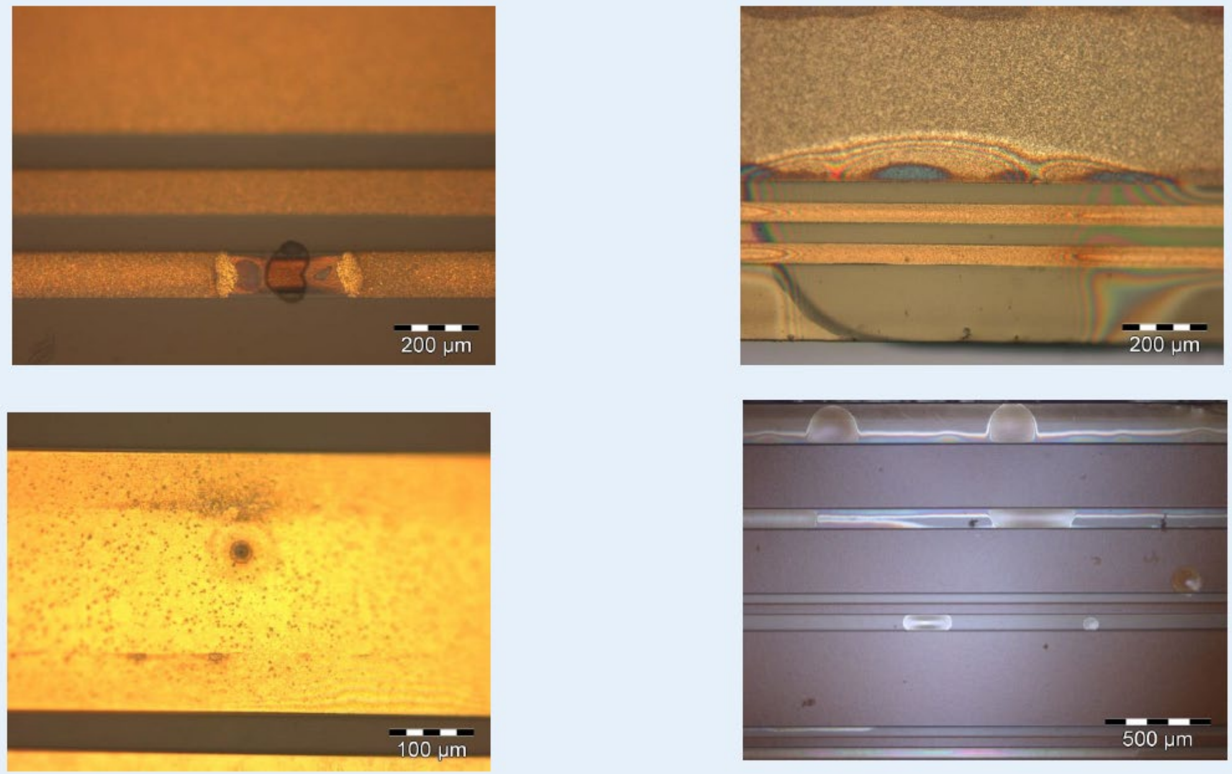
Drawbacks of Polyimides

- High cost (material and process)
  - After spin coating PI films, imidization requires very high temperatures in the range of 300-325°C
  - Typically limited to thin films since water is produced during imidization
- Metal adhesion can be a challenge
  - Tie layer metals for polyimide coatings often include chromium or titanium to improve adhesion between the polyimide and metals like copper and gold.
- Moisture absorption
  - Leads to metal corrosion, package cracking, degradation of dielectric properties
- Susceptible to attack by concentrated acids and alkalis
- Limited impact strength

Kapton^{TM} Film Failure Mechanisms

- Delamination of Kapton as insulative layer or interlevel dielectric from conductive metals, e.g. Ti, Al, Ta, etc., due to aging and fatigue
- Charge transport through the dielectric film, some types more prone to this than others
- “Hard” films on “soft” substrates have difficulty recovering from large deformations and can be prone to fracture…this can apply to metal on Kapton^{TM} or Kapton^{TM} itself on a softer or more pliable substrate

Failure Modes in Flex Connectors



pinholes delaminations

Typical failure modes in Au metal Polyimide Flex after implantation in the body

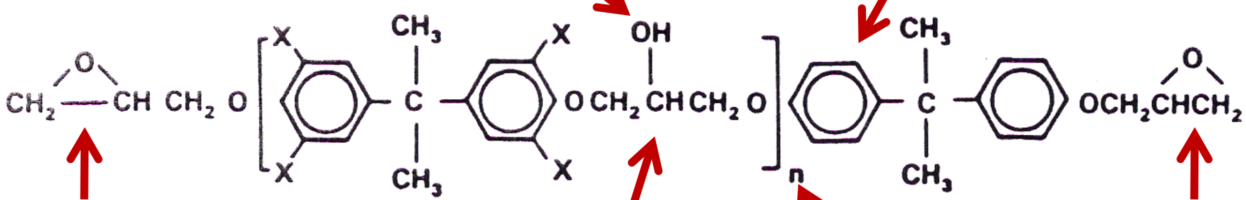
Ref: T. Lebold Retina Implant Minnowbrook Notes 2014

Stress Driven Qualification for Non-Hermetic Packaging

Epoxy is Most Common Thermoset

Adhesion, reactive site, wettability, drawback hydrogen bonds with water molecules

Aromatic rings give high temperature performance and rigidity



Epoxy reactive site

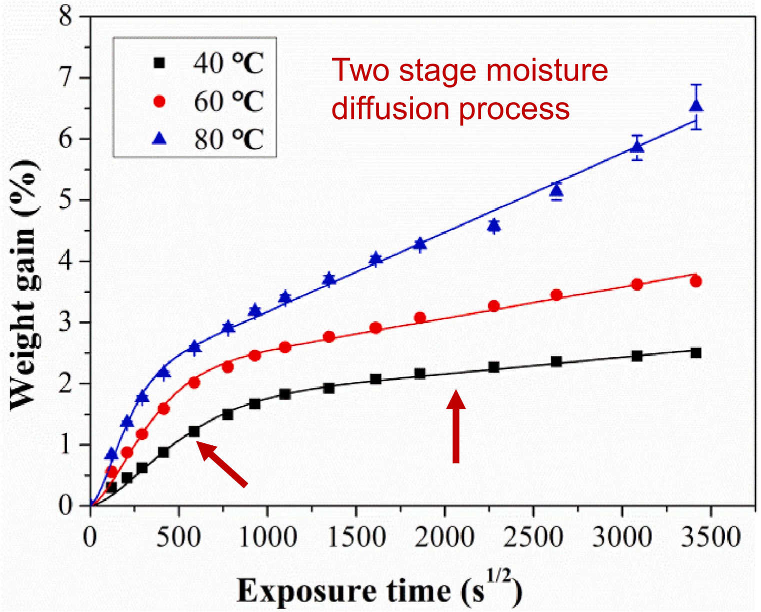
Toughness

Molecular weight

Epoxy reactive site

Bisphenol A epoxy; X=H, for tetrabromobisphenol A; X- Br

Epoxies Absorb Moisture



Bisphenol A epoxy + anhydride hardener
(underfills, coatings, circuit boards etc.)

$$M_t = M_\infty (1 + k\sqrt{t}) \left\{ 1 - \exp\left[-7.3 \left(\frac{Dt}{h^2} \right)^{0.75} \right] \right\}$$

D is the diffusion coefficient

$$D = D_0 \exp\left(-\frac{E_a}{RT} \right)$$

D_0 is a constant and E_a is the activation energy

Source: Xian et. al., Journal of Materials Research and Technology, 31, (2024) 3982 https://doi.org/10.1016/j.jmrt.2024.07.123

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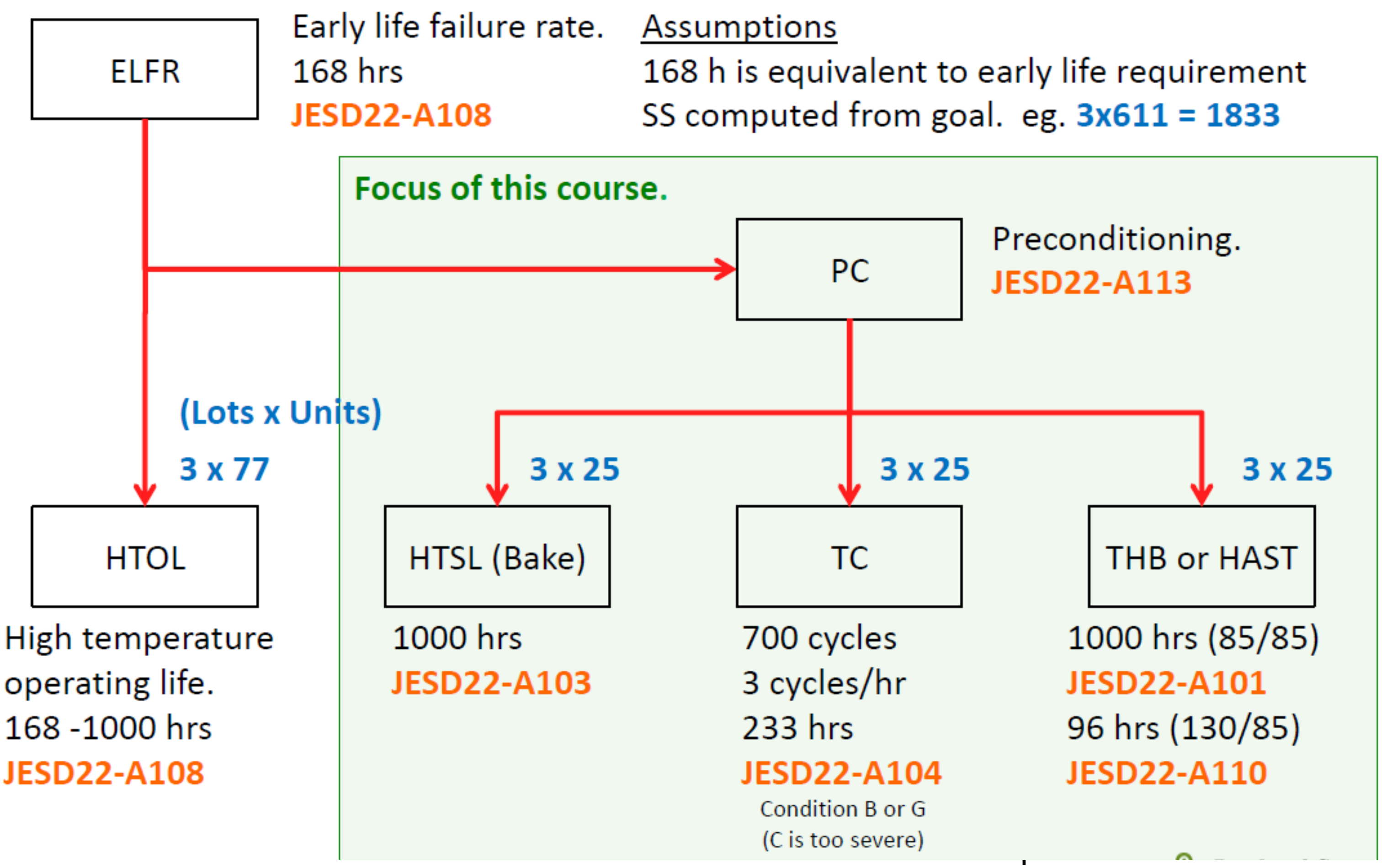
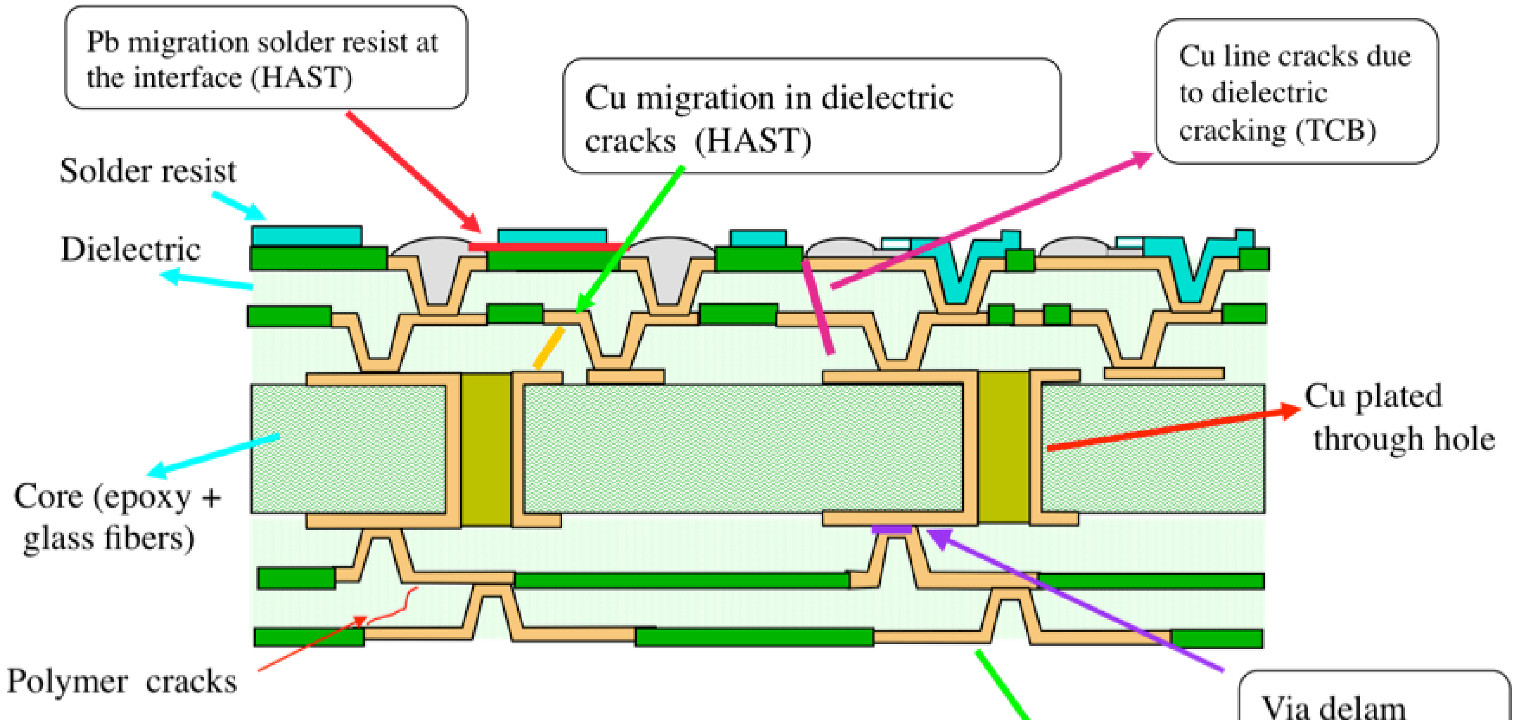
Reliability Testing – Package Level



Typical Failure Modes



- Typical failures include via delamination, barrel cracking, dielectric crack/delam
- SR delam, Cu nodule/migration/corrosion

Reliability Testing – Package Level

Test	Test Condition	Test Conditions
PC Pre-Cond	JEDEC J-STD-020	MSL1 24h bake @ 125°C 192h @ 30°C/60%RH Reflow simulation (3times) with Lead free profile Tmax=260°C
TC Temp. Cycling	JESD22-A104	Ta = -55/+125°C 1000 cycles
HTSL, High Temp. Storage Life	JESD22-A103	Ta=150°C 1000h
THS, Temp Humidity Storage	JESD22-A101	Ta=85°C, 85%RH 1000h without bias
TCoB	JESD22-A103	-40/125C, 500 cycles
Drop Test	JESD22-B111	1500G , 100 drops

L3/260°C

TC on assembled board

assembled board

STATS ChipPAC ECTC 2017

Moisture Sensitivity Level (MSL)

Holy Grail

Most Common

LEVEL	FLOOR LIFE		STANDARD	
	TIME	CONDITION	TIME (hours)	CONDITION
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH
2a	4 weeks	≤30 °C/60% RH	696^2 +5/-0	30 °C/60% RH
3	168 hours	≤30 °C/60% RH	192^2 +5/-0	30 °C/60% RH
4	72 hours	≤30 °C/60% RH	96^2 +2/-0	30 °C/60% RH
5	48 hours	≤30 °C/60% RH	72^2 +2/-0	30 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48^2 +2/-0	30 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH

Moisture Pre-conditioning

MSL Nomenclature:

- Level
- Reflow temperature

Example:
L3 260°C

Source: JEDEC Std-020D.1

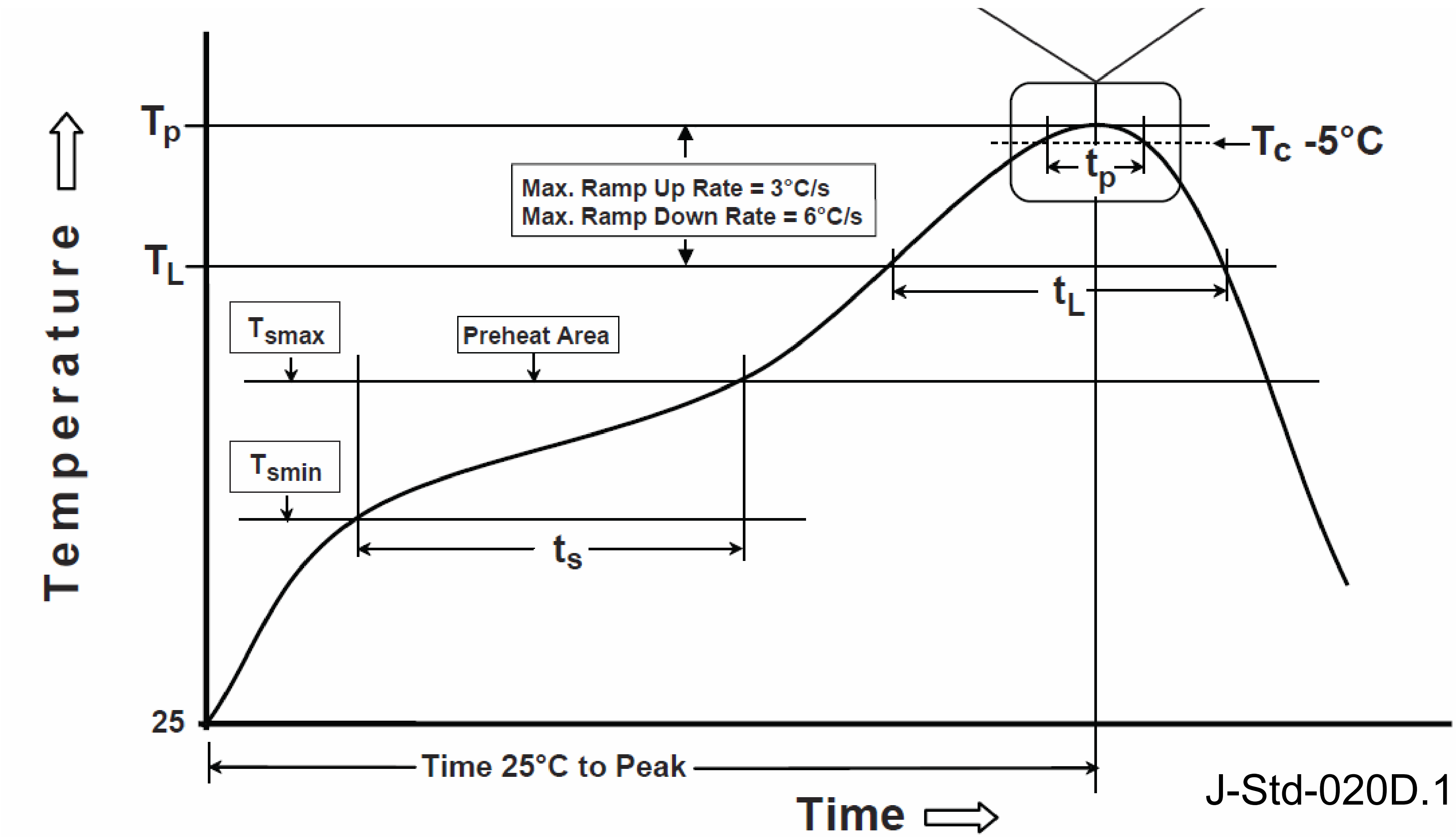
JEDEC STD-020D Reflow Profiles

Condition	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/soak		
Minimum temperature	100°C	150°C
Maximum temperature	150°C	200°C
Time from minimum to maximum	60 to 120 seconds	60 to 120 seconds
Ramp-up rate	3°C per second maximum	3°C per second maximum
Liquidous temperature (T_L)	183°C	217°C
Time held above T_L	60 to 150 seconds	60 to 150 seconds
Peak package body temperature	Between 220°C and 235°C, depending on size and volume	Between 245°C and 260°C, depending on size and volume
Hold time within 5°C of peak temperature	20 seconds	30 seconds
Ramp-down rate	6°C per second maximum	6°C per second maximum
Time from 25°C to peak temperature	6 minutes maximum	8 minutes maximum

Source: Adapted from JEDEC, *IPC/JEDEC J-STD-020D.1, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*, March 2008, table 5-2.

Reflow Profile

T_{peak} = 260°C for lead-free reflow



J-Std-020D.1

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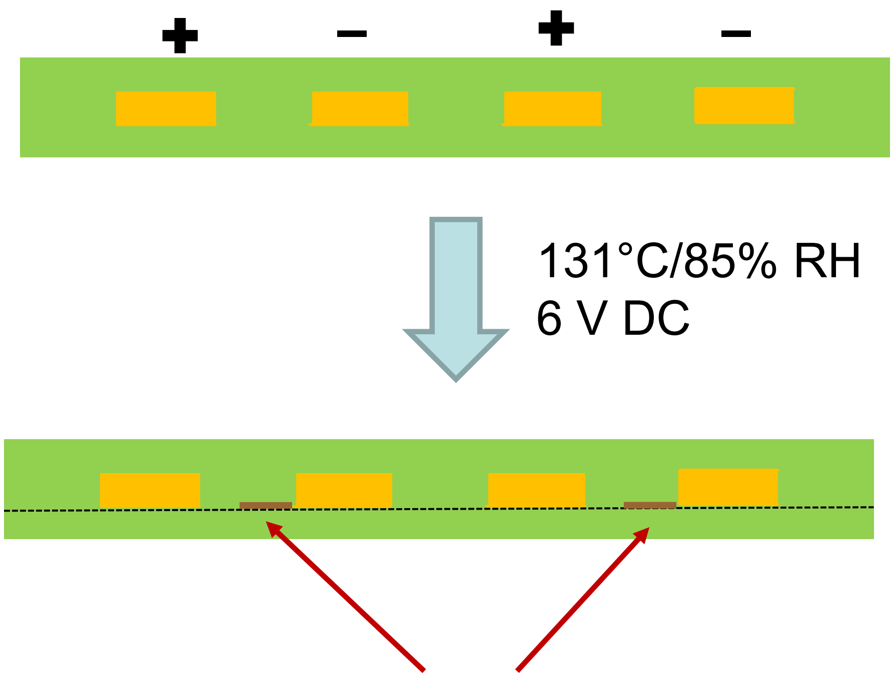
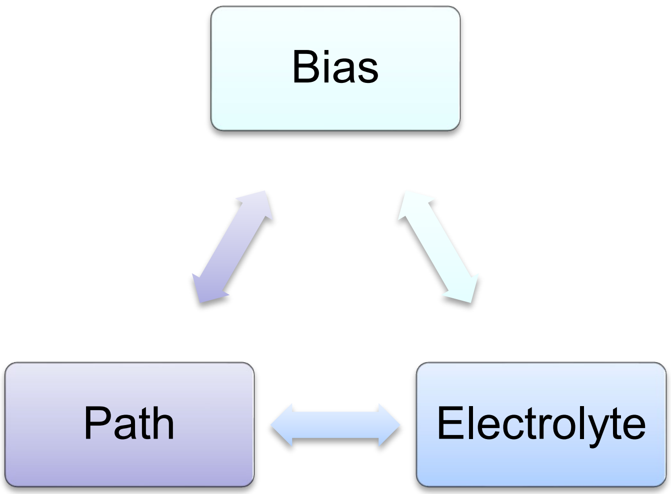
Biased HAST Mechanism

Use comb interdigitated electrode TV

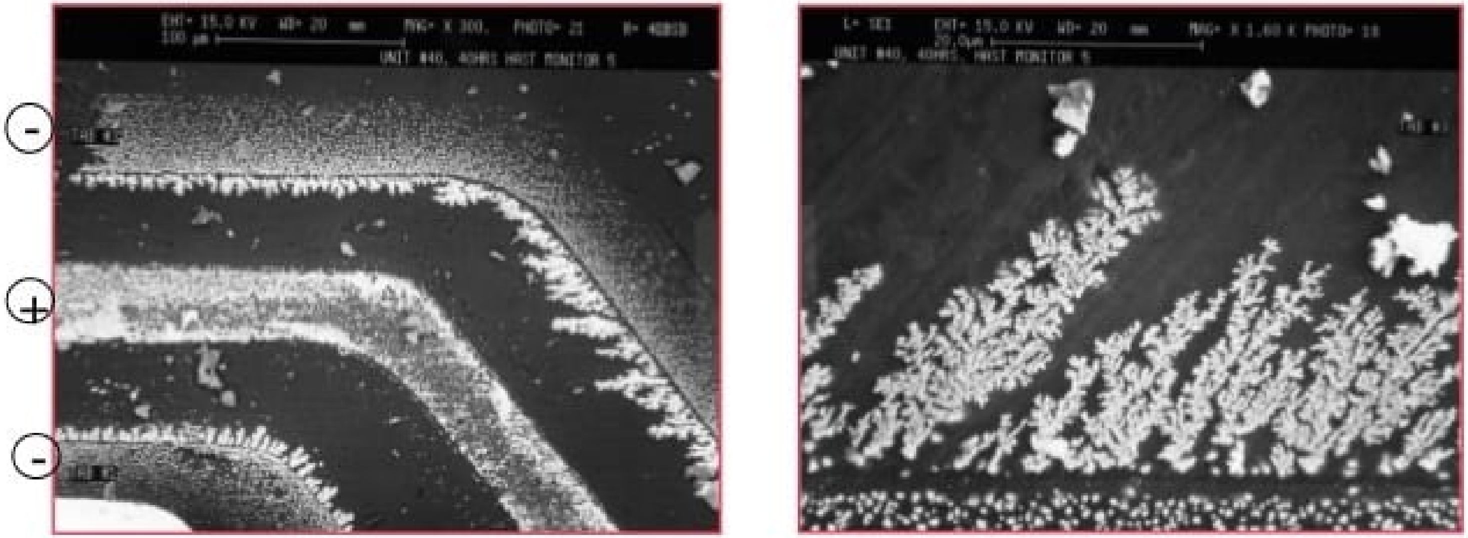




Copper dendrites indicate where weak interfaces exist

Biased HAST Failure Mode

– Accelerated by voltage, temperature and humidity
– Seen as early as 20 hrs 156/85 HAST
– Highly dependent on materials & process



Copper dendrites after 40 hours of biased 156/85 HAST

8/2-4/2011 Plastic Package Reliability 57 Portland State

Glenn Shirley, "Plastic Package Reliability" Portland State Univ. ASQ Short Course, August 2011

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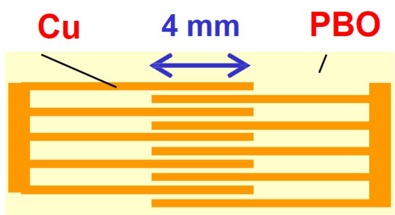
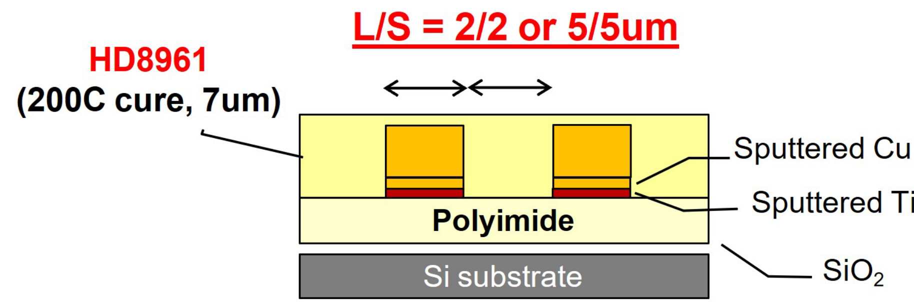
Biased HAST Reliability – Two Layer Fine Pitch

Structure of test vehicle



Top view

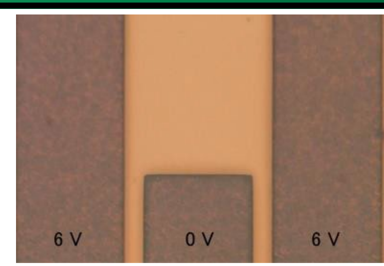


X-sectional view

.

Temp / Humidity: 131 deg.C / 85%RH
Bias voltage : 6 VDC
Time : 500 hrs

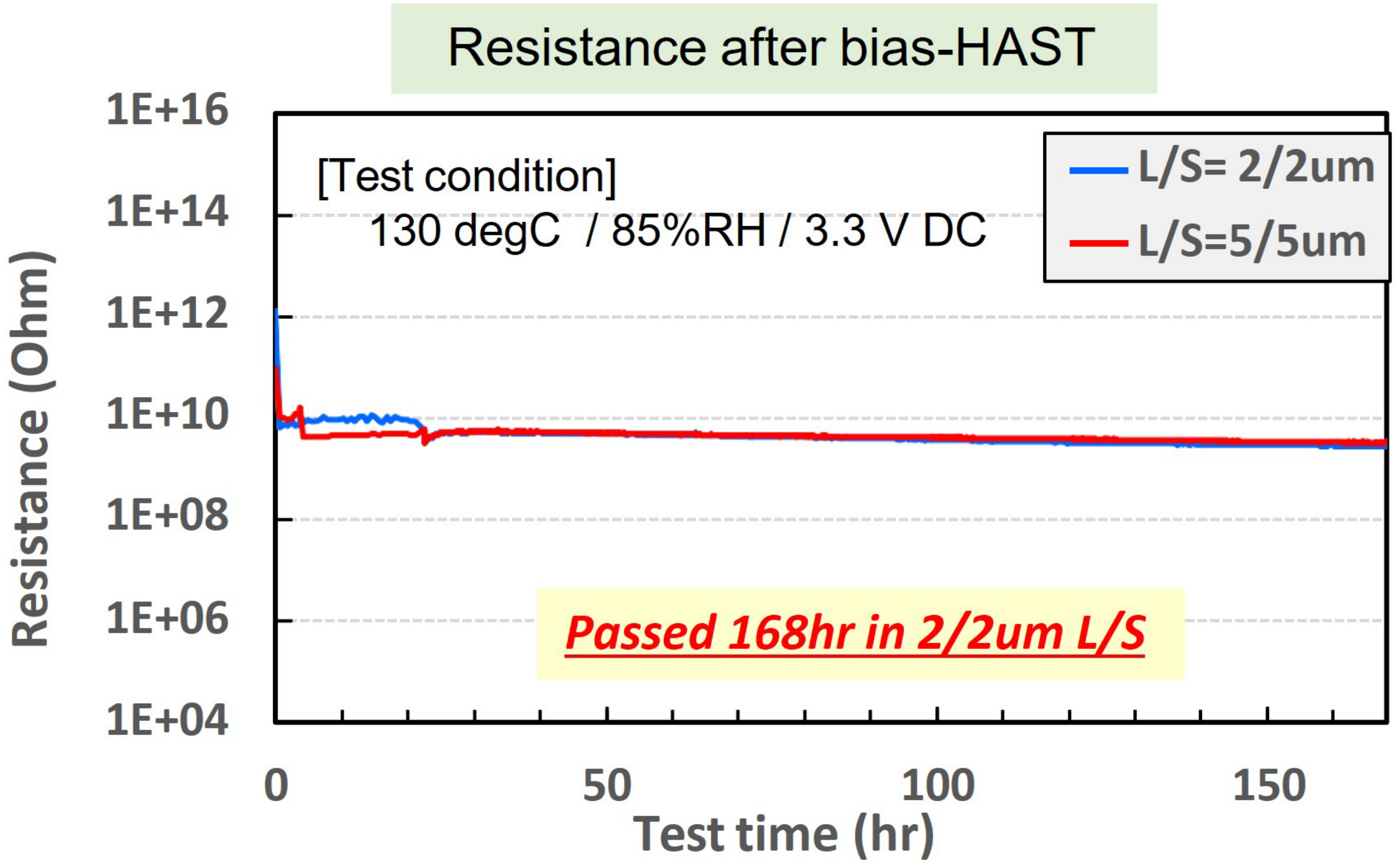
Notice use of sputtered titanium tie layer

Sample	Result	Appearance after HAST
HD8961 (200ºC/1h cure)	No short circuit No dendrite No corrosion No delamination	

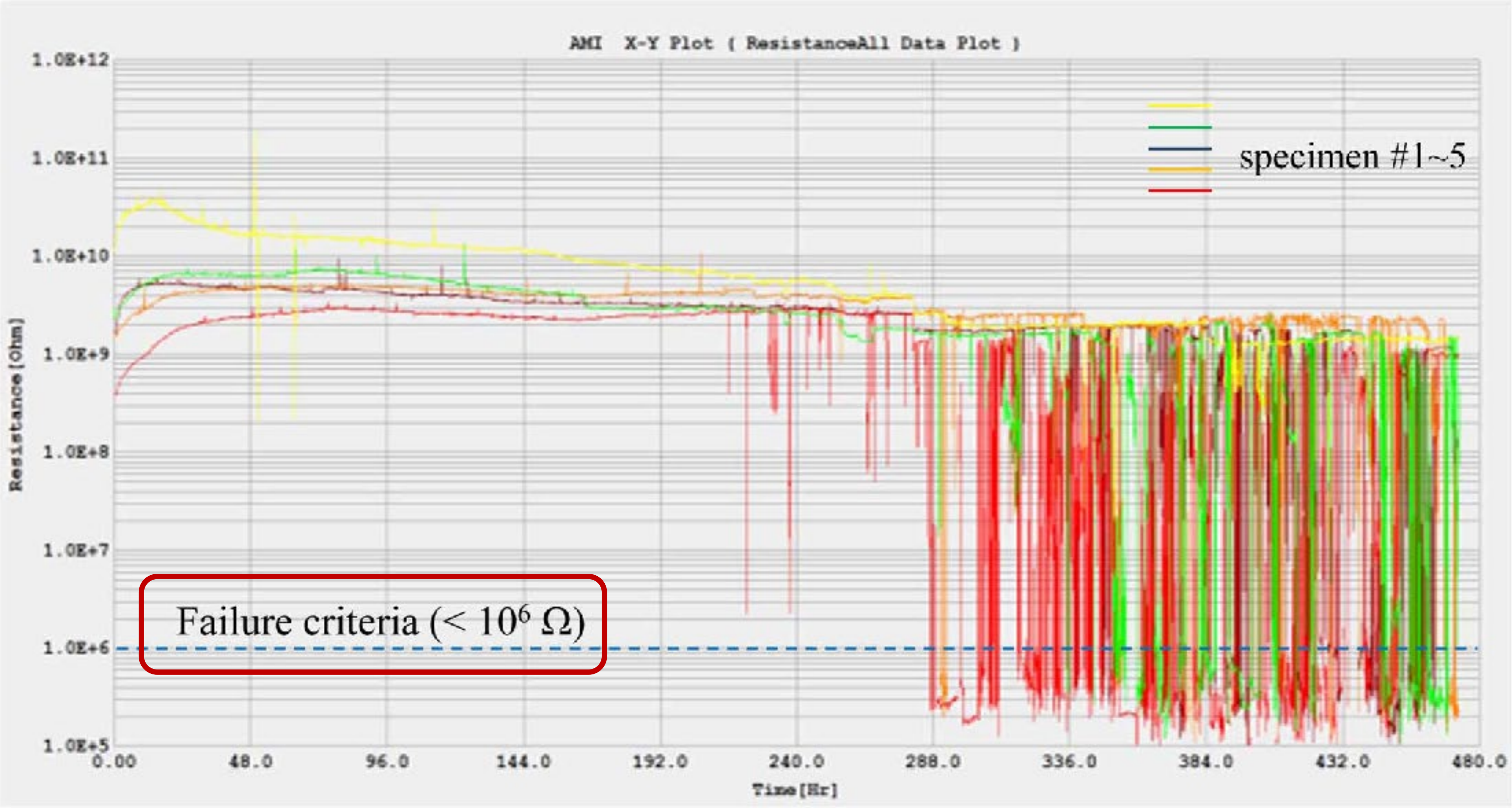
HD8961 PBO

Source: HD Microsystems

Stable Resistance Over Time



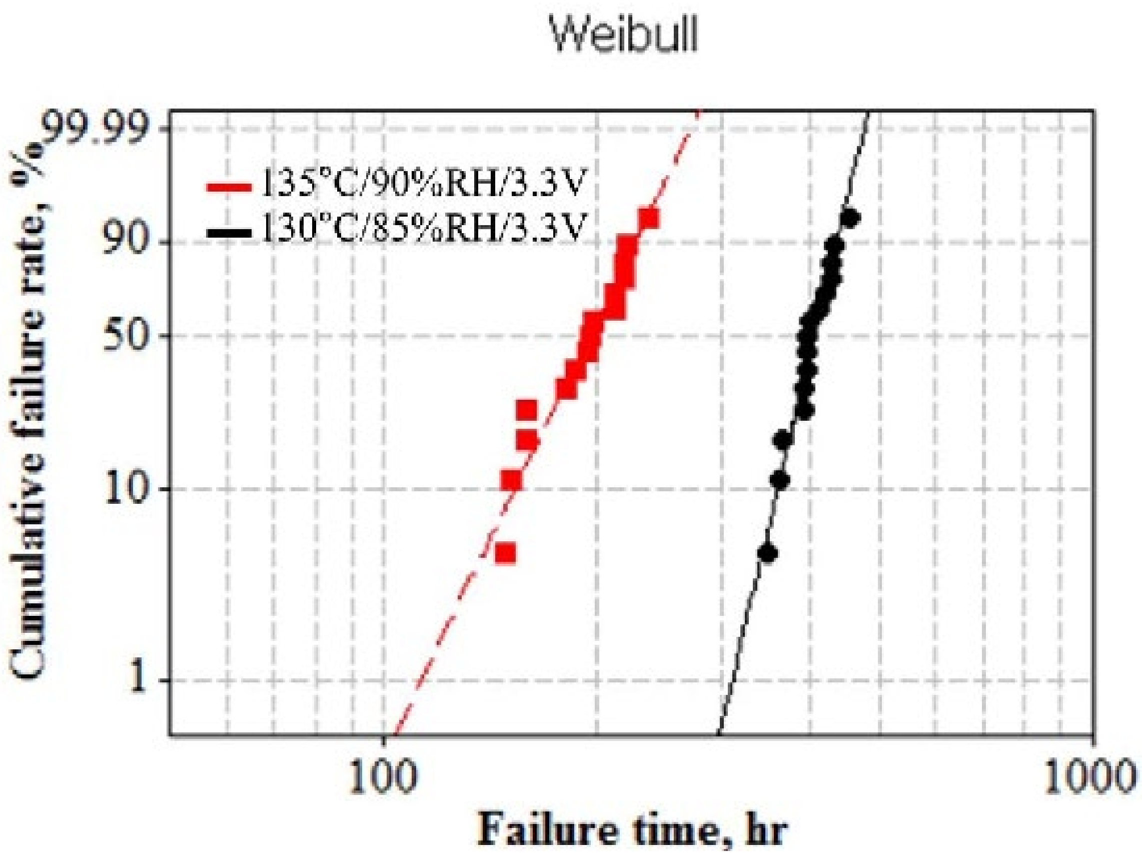
Unstable Resistance versus Time



In-situ resistance plots of 5 specimens at 130°C/85%RH/3.3V (13 μ spacing)

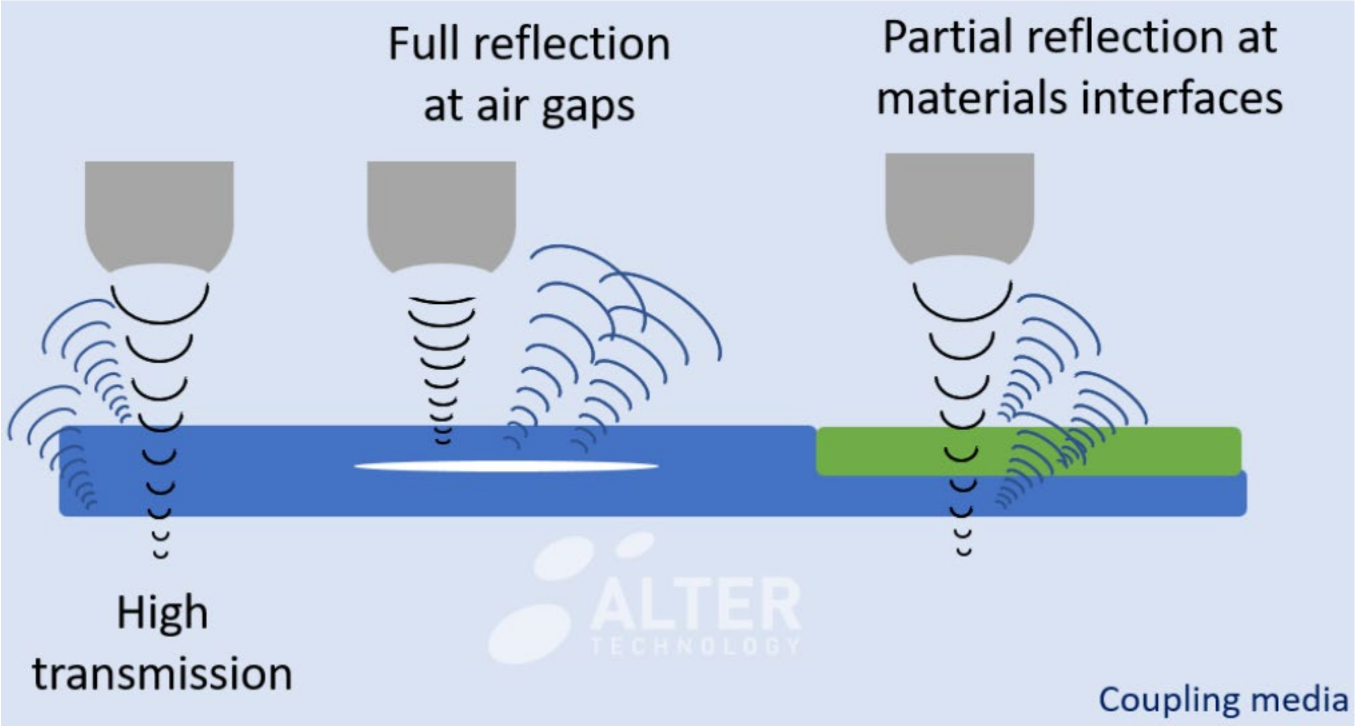
S. Huh, AS Shin, S. Ham, Ion Migration Failure Mechanism for Organic PCB under Biased HAST, DOI:10.6117/KMEPS.2015.22.1.043

Example of HAST Failure Time



S. Huh, AS Shin, S. Ham, Ion Migration Failure Mechanism for Organic PCB under Biased HAST, DOI:10.6117/KMEPS.2015.22.1.043

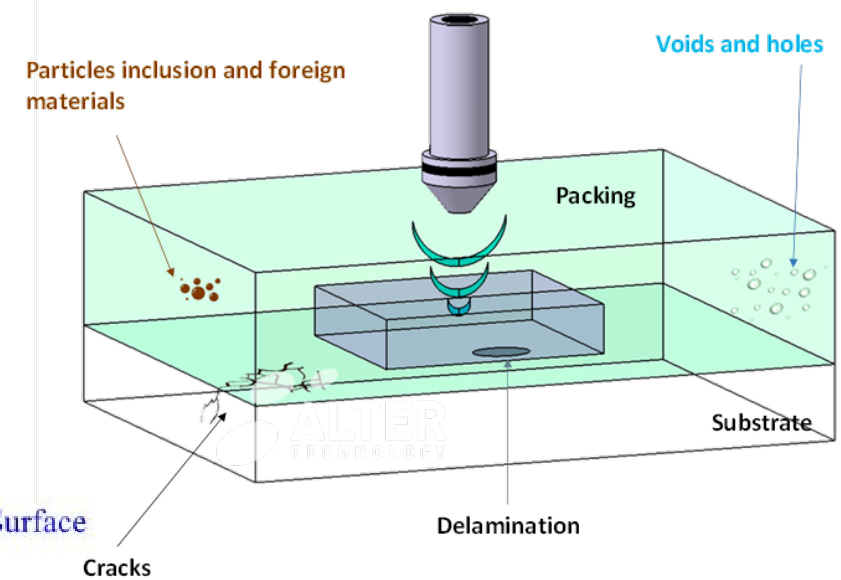
Scanning Acoustic Microscopy



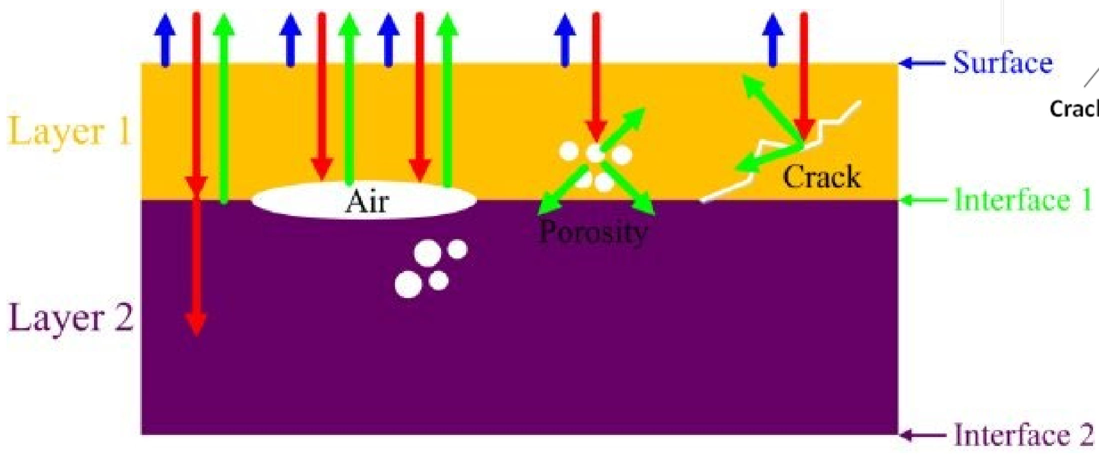
Source: Alter Technology

Confocal Inspection (C-scan)

Used to evaluate air gaps such as voids and delamination

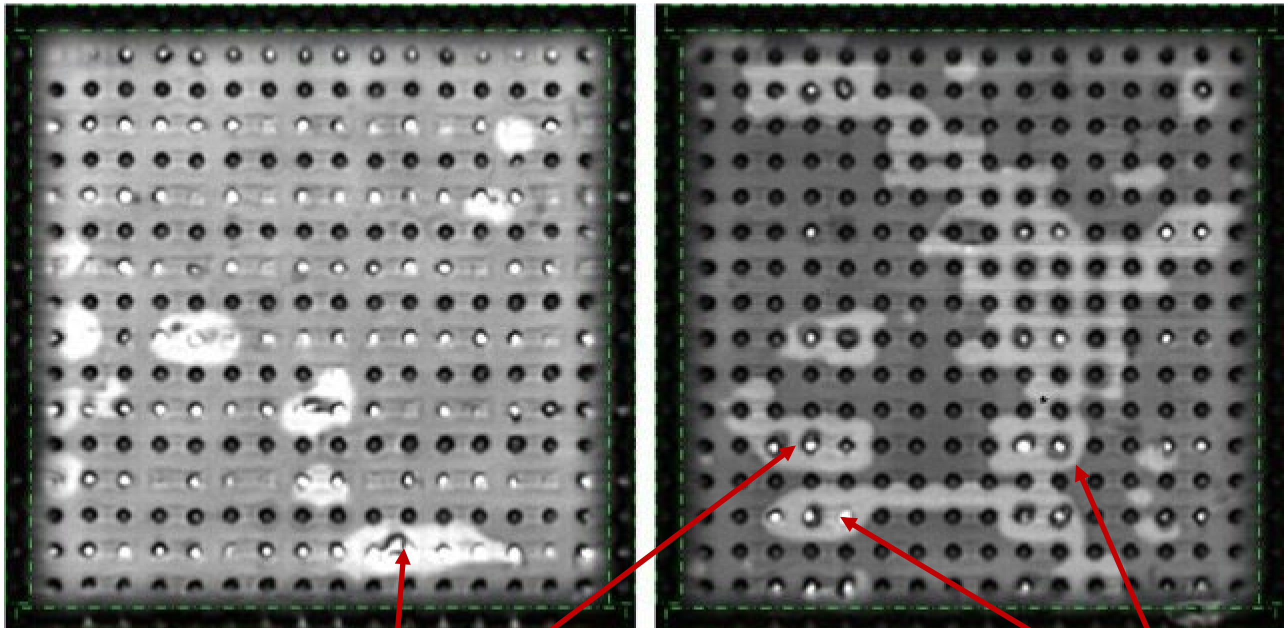


Source: Alter Technology



Lei Su, et. al., Sensors 2013, 13, 16281-16291; doi:10.3390/s131216281

C-SAM of Flip Chip "White Bumps"



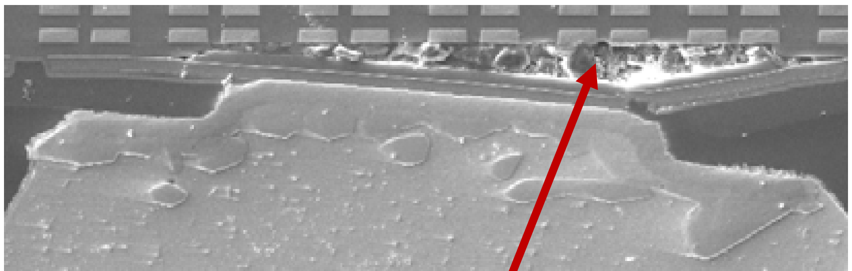
(a) (b)

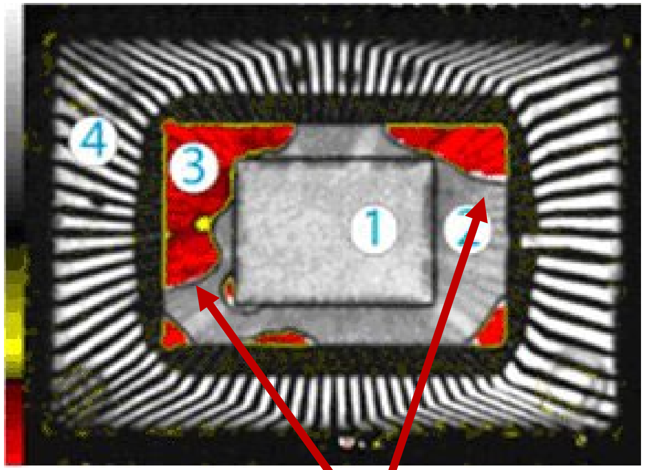
Underfill voids

"white bumps"

Lei Su, et. al., Sensors 2013, 13, 16281-16291; doi:10.3390/s131216281

Delamination Detection Via C-SAM





Delamination in chip dielectric layer causes “white bumps” in C-SAM imaging

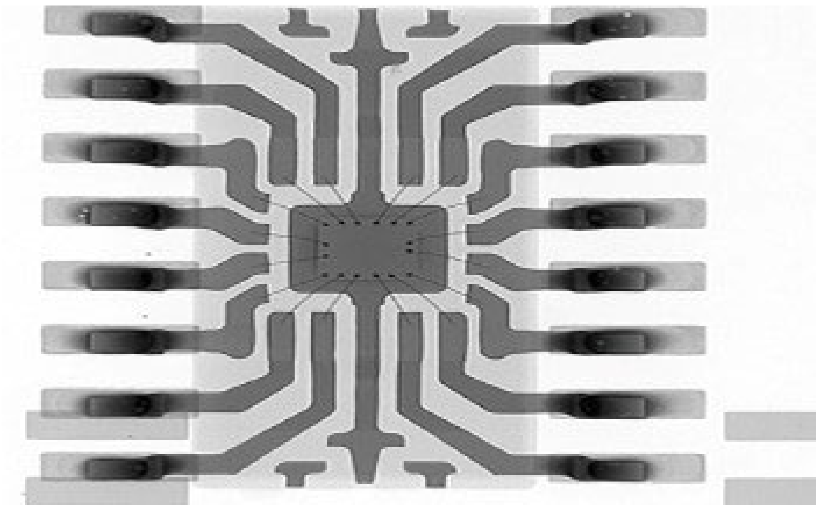
Delamination in between mold compound and die pad shown in C-SAM image

IBM Research Report, The Over-Bump Applied Resin Wafer-Level Underfill Process, RC24851 (W0908-142) August 31, 2009

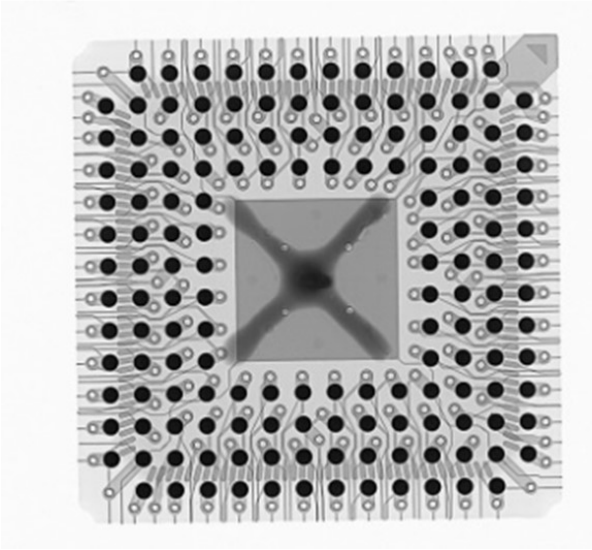
By Sonoscan - Sonoscan, CC BY-SA 3.0, https://commons.wikimedia.org/w/index.php?curid=4360946

Transmission X-ray Inspection

- Imaging of package interior
- Multiple commercial instruments
- Transmission method (no depth discrimination)



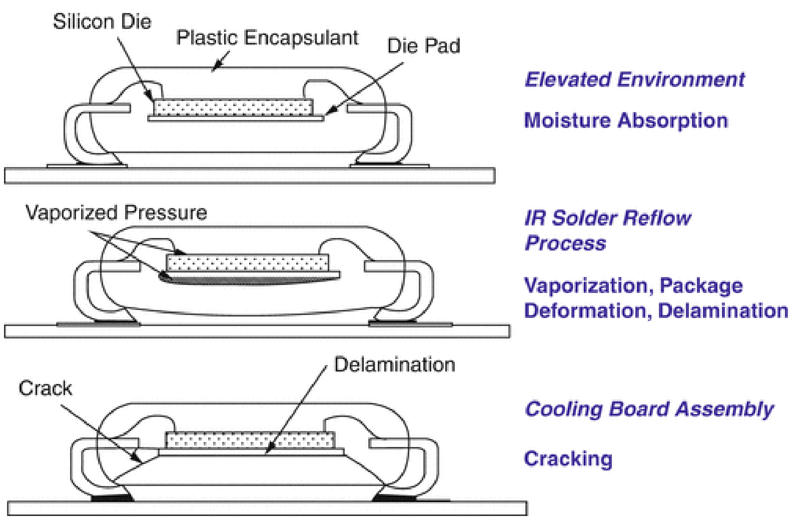
Leadframe package



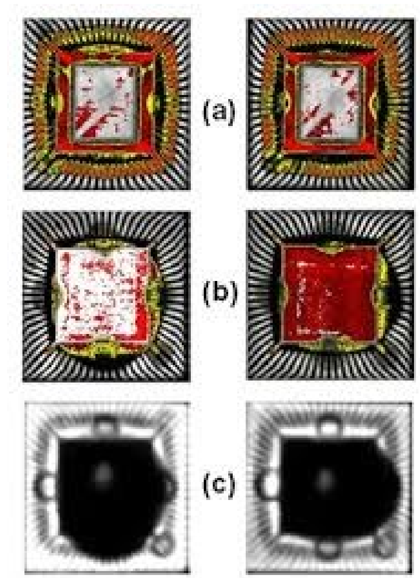
Die bonded PBGA package

After Reflow Inspect Package for Damage

- Popcorning
  - refers to a failure mode where a component, usually a plastic-encapsulated microcircuit, cracks or delaminates due to rapid vaporization of absorbed moisture during the high temperatures of the reflow process



Test Methods
- Visual inspection
- CSAM
- Cross-sectioning
- Electrical test



Scanning Acoustic Microscope (CSAM) images of PBGA after reflow showing delamination (red)

Source: Yi, S. (2014). Hygrothermally Induced Residual Stresses and Failures in Plastic IC Packages During Reflow Process. In: Hetnarski, R.B. (eds) Encyclopedia of Thermal Stresses. Springer, Dordrecht. https://doi.org/10.1007/978-94-007-2739-7_894

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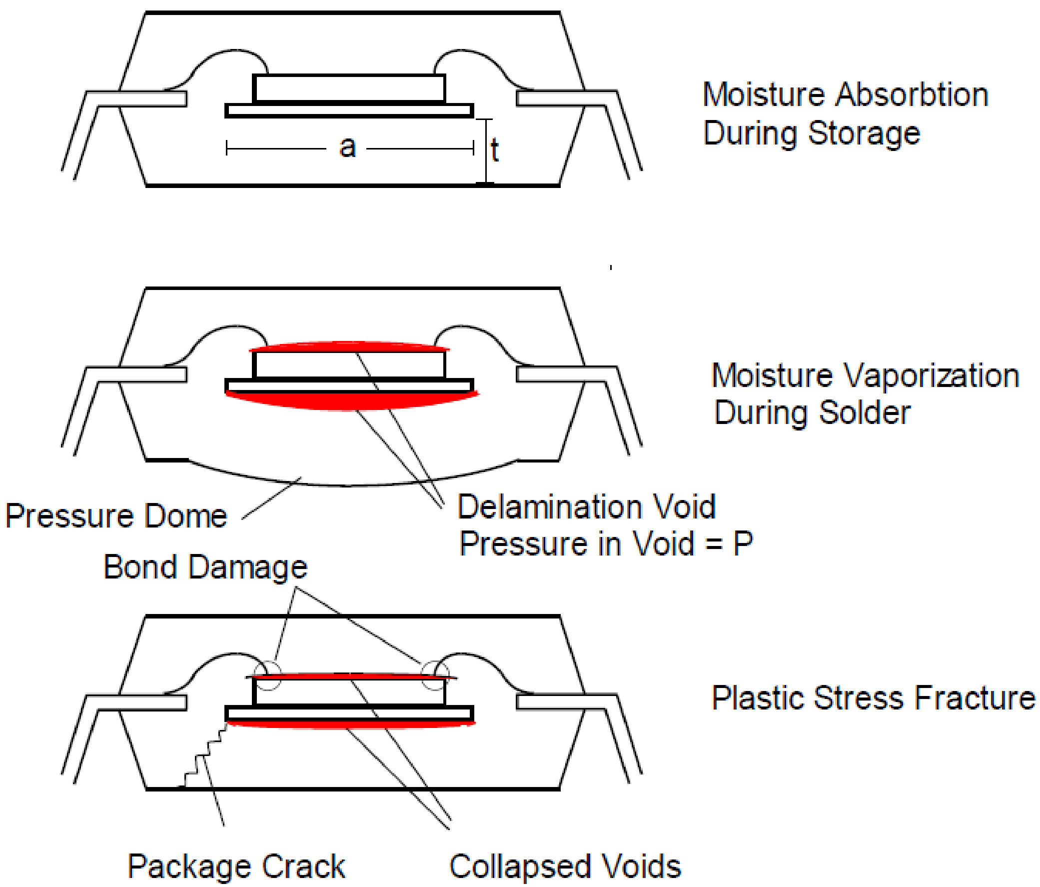
Popcorning in Leadframe Package

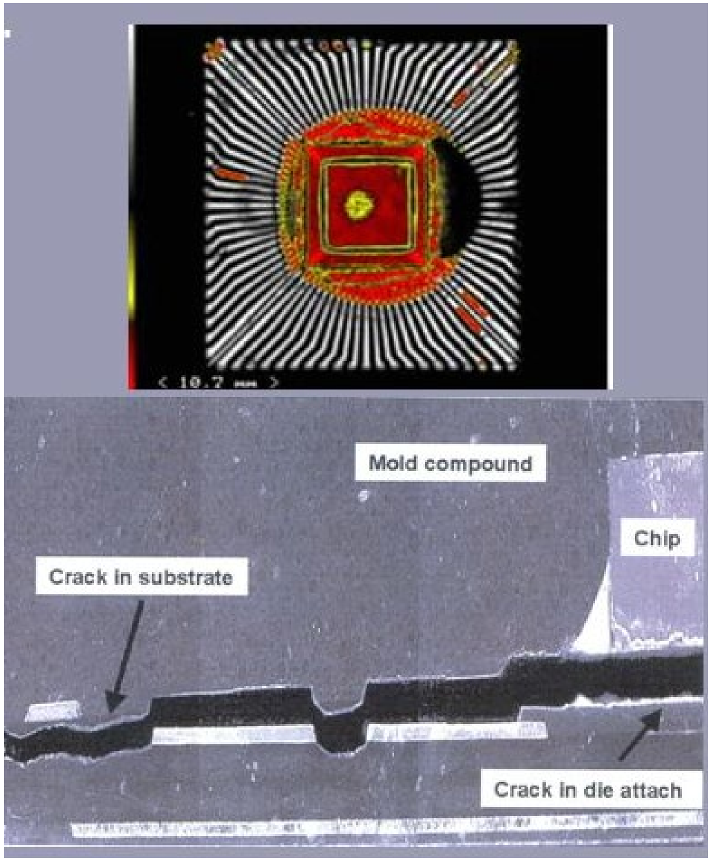


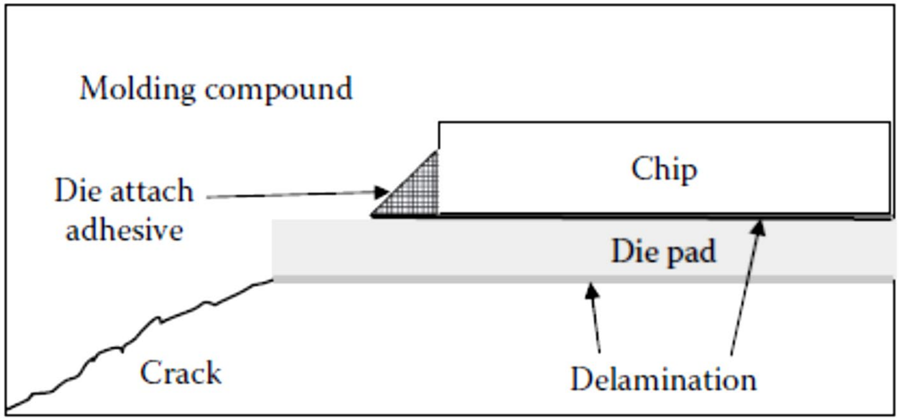
Glenn Shirley, “Plastic Package Reliability” Portland State Univ. ASQ Short Course, August 2011

Factors Affecting Popcorning

- Peak temperature during soldering
- Moisture content of mold compound
- Die paddle dimensions
- Mold compound thickness under die paddle
- Mold compound adhesion to die and/or lead frame
- Mold compound formulation
  - Inherent moisture absorption of the EMC and filler loading

Popcorn Example





Andrea Chen, RandyHsiao-Yu Lo, Semiconductor Packaging, Materials Interaction and Reliability, CRC Press, 2012

Thermal Cycling

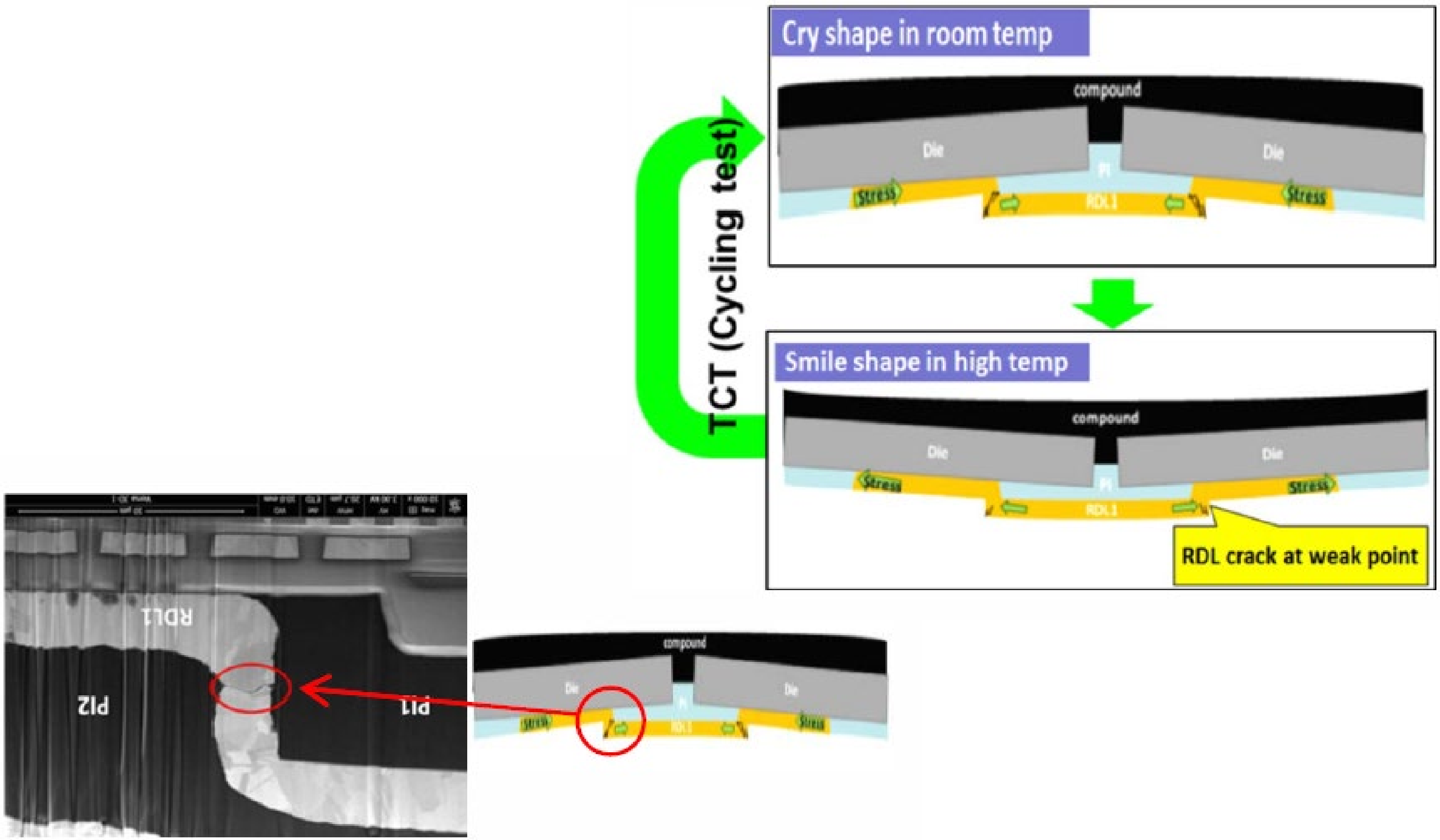
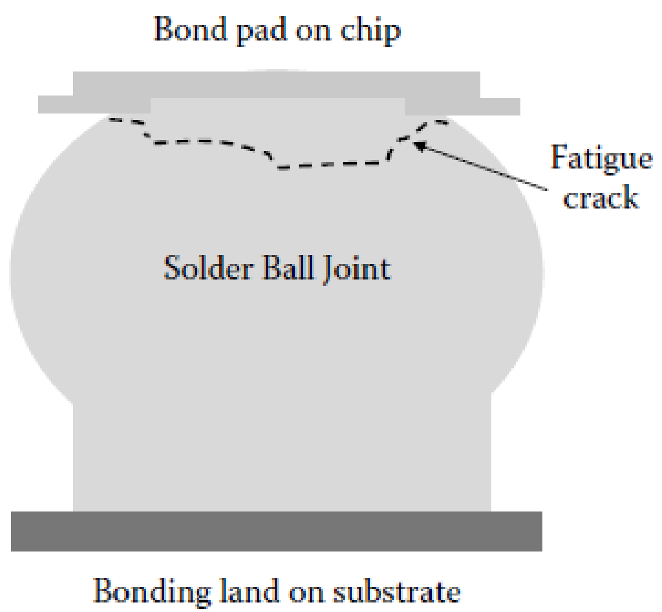


Figure 4. RDL failure after package level TCT.

ASE ECTC 2017

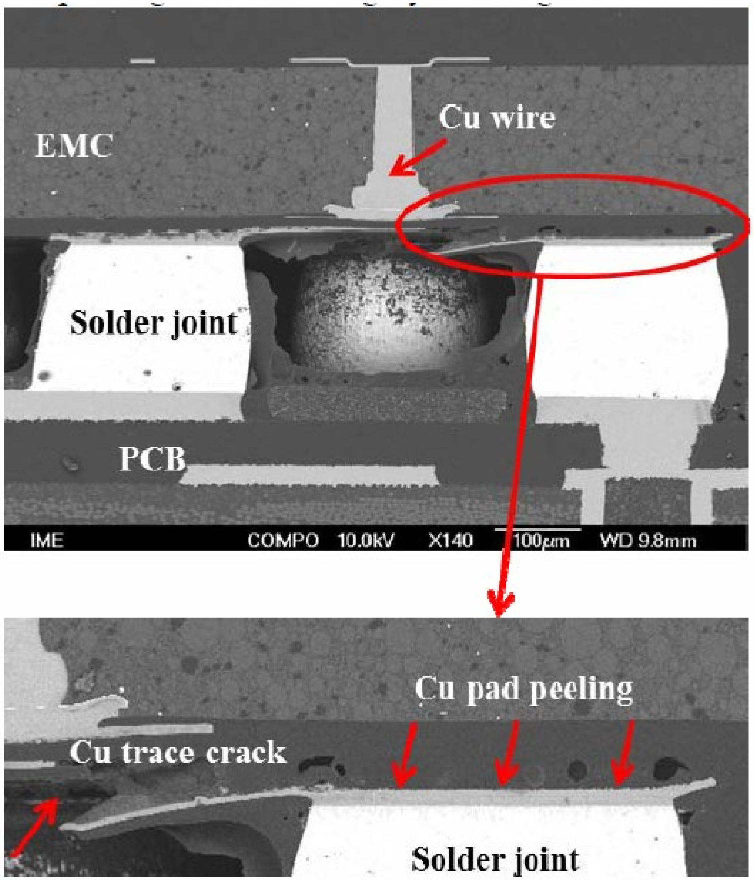
Solder Fatigue-Induced Crack

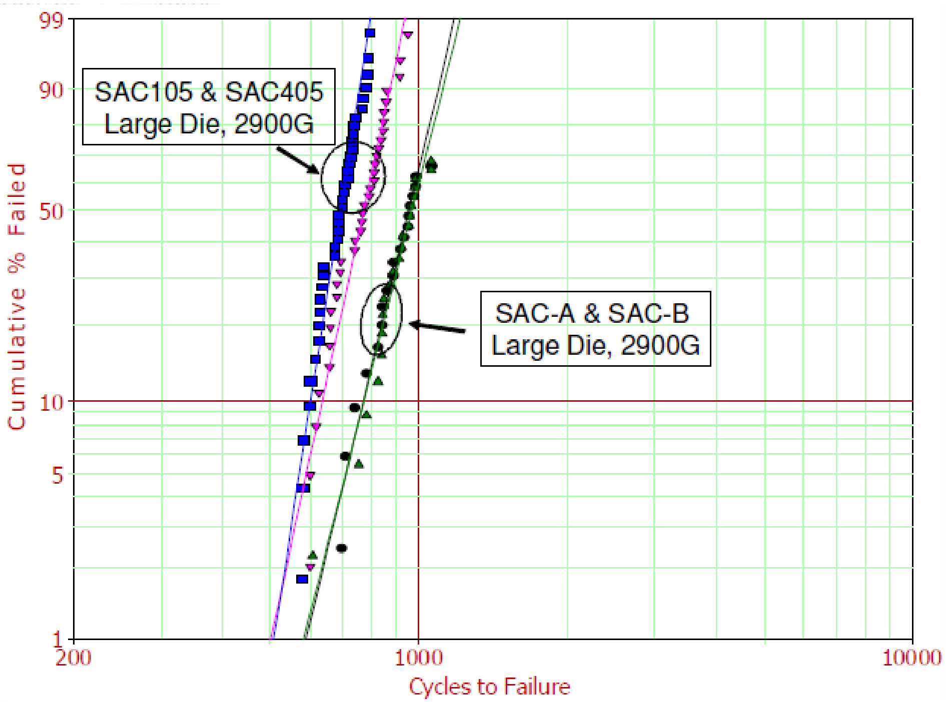


Fatigue crack in solder ball metallurgy, not in polymer

Andrea Chen, RandyHsiao-Yu Lo, Semiconductor Packaging, Materials Interaction and Reliability, CRC Press, 2012

Board Level TC Testing





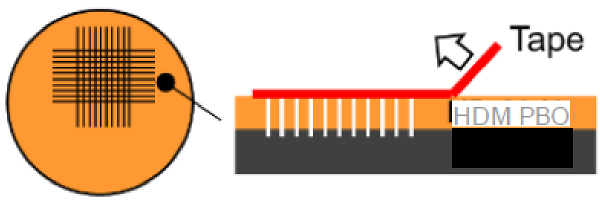
Example of Wiebull plot for different solders

HD Microsystems PBO Adhesion Testing

Cross-section of FOWLP

Cross cut test

Cross cut to dielectric



Condition		Result ※
Pressure Cooker Test	100 h	100/100
	300 h	100/100
	500 h	100/100

※100/100: all pieces remained after the testing (No failure)

Source: SEMICON Taiwan 2014, Masay Toba, Hitachi Chemical Co., Ltd.

Source: HD Microsystems