Critical Developments in TIMs and Thermal Material Characterization Tools

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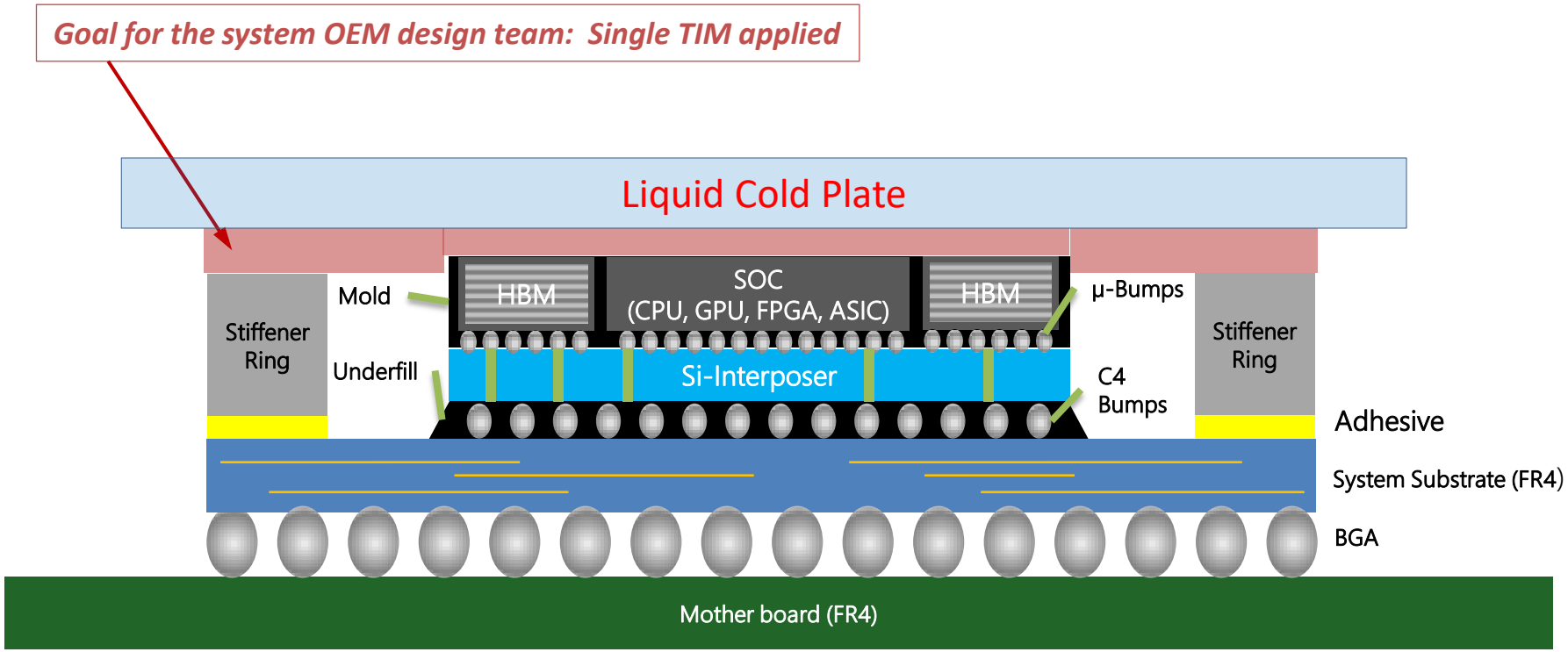
Overview

Presentation purpose:

- IGBT module behavior has significantly impacted thermal interface material (TIM) development:
  - Temperature-induced stresses due to CTE mismatch in an unbalanced system with representative changes ;
  - Increasing power dissipation, heat flux, operating temperatures, and wide range of different characteristics for a different types of TIMs for commercial;
  - Composite material developments assisted in reducing package internal stresses and resulting baseplate cyclical flexing;
  - Challenging TIM requirements for thermal performance and reliability met with patterned phase-change compounds w/high reliability, compliance, adaptable thicknesses
- AI/GPU processor modules now reflect similar characteristics of :
  - Temperature-induced stresses for modules due to CTE mismatch in an unbalanced system;
  - Rapidly increasing power dissipation (1kW → 5.8kW *forecast*)
  - Increasing integration of tightly-packaged large core logic die, combined with highly temperature-sensitive stacked HBM in close proximity on substrates;
  - Large stresses for substrate and die impact and die warpage;
  - Critical TIM requirements for *thermal performance*, *compressibility, compliance, immersion liquid bubble erosion, long-term reliability*.

High Performance IC CPU/GPU/APU Packaging



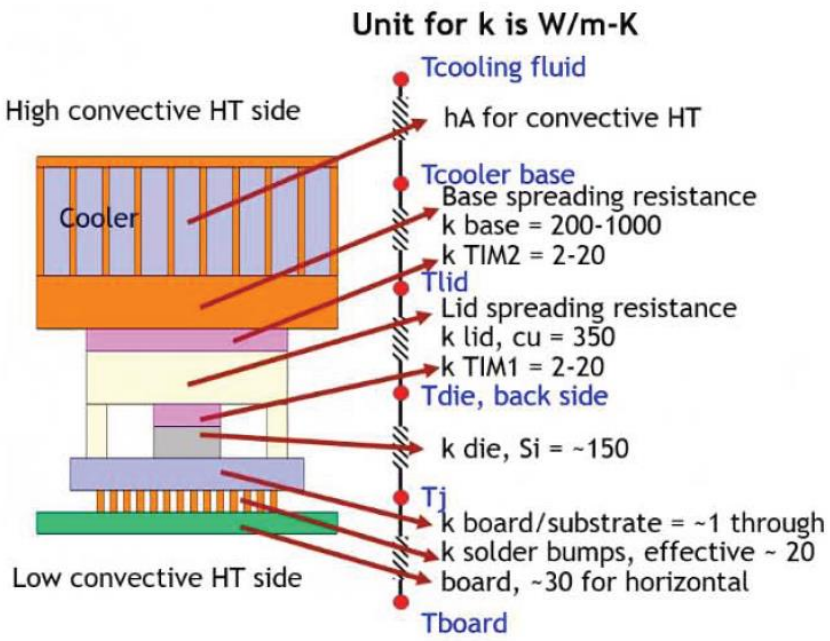
Source: Abo Ras, M., Berliner Nanotest und Design GmbH, "The Unique Role of Thermal Test Vehicles (TTV) for TIM Characterization and Reliability Investigation ," 41st Chemnitz Seminar, Test and Reliability Solutions – New Opportunities for Electronic Components and Systems," Technical University Chemnitz, Chemnitz, Germany, February 14, 2025.

Notes added: DS&A LLC.

High Performance IC CPU/GPU/APU Packaging

What is the *thermal resistance stack* for an IC module?

Resistance	Important Parameters	Increasing Attribute Performance
R_c	Die and package sizes TIM1 Bond line thickness Thermal performance Lid Lid material Lidless Power layout	PSA/Adhesives — PCM/Grease — Direct Attach Plastic — Ceramic — metal — Lidless
R_{TIM}	Bond line thickness Thermal performance Contact area Surface flatness and finish Applied pressure	Bare — Gap Pad — PSA/Adhesives — Pre-form — PCM/Grease — Dir Att 2 psi — 7 — 10 — 20-30 psi
R_{s-a}	Base spreading efficiency Material Thickness Heat exchanging Flow rate Surface area- fin counts, height, length	Al — Cu — HP/VC — Thermo-syphon — Active Liquid — Cold Plate Air — Liquid Stamping — Stand Ext — HA Ratio Ext — Stacked Fins — Fan/HS



Three major sectors where thermal resistance occurs and the major parameters:

R_C (Resistance to case)

R_{TIM} (Resistance through TIM)

R_{S-A} (Resistance sink-to-ambient)

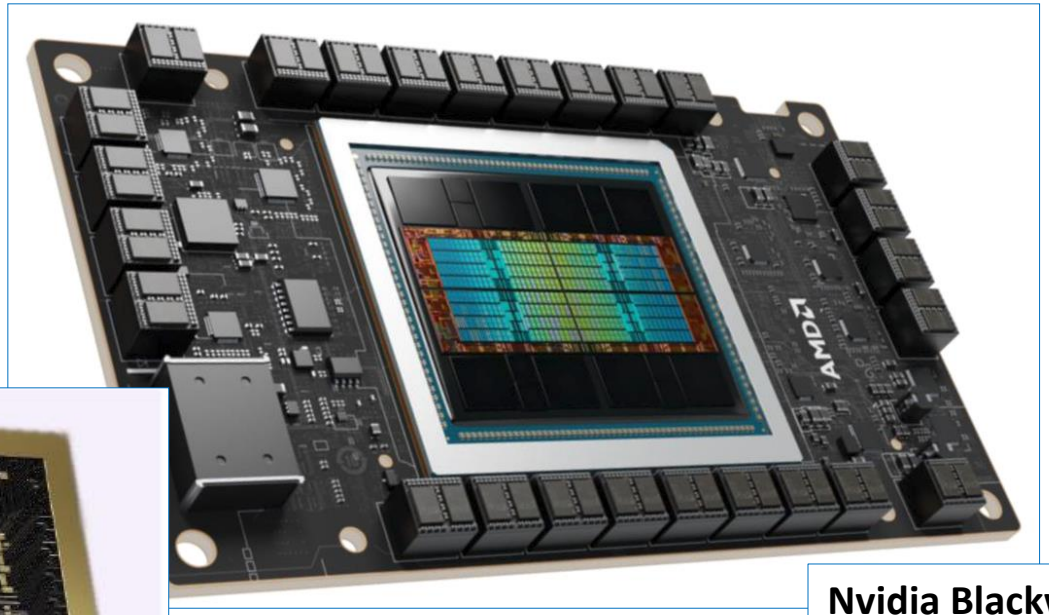
What can the OEM thermal design team most easily and effectively control to limit losses?

1. ***TIM2 selection***
2. ***Heat sink/liquid cold plate design***

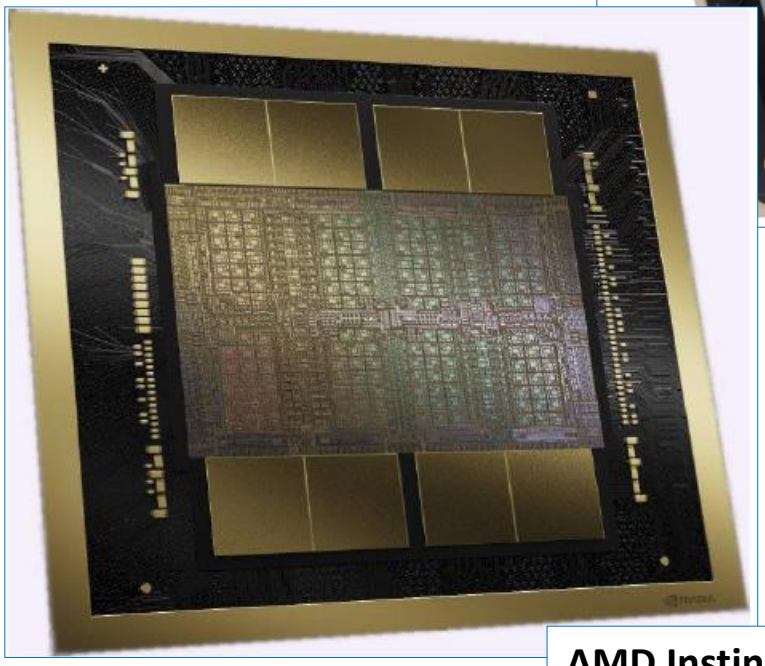
Note that the TIM1 selection is typically not available for change by the OEM thermal design team.

Source: H. Chu, Nvidia, "HIR Packaging Thermal Resistance Path, May 18, 2021. Additional text (in red): DS&A LLC.

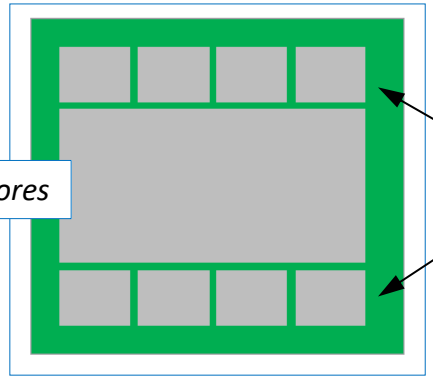
HIR Die and Substrate Warpage



Nvidia Blackwell B200



AMD Instinct MI300X

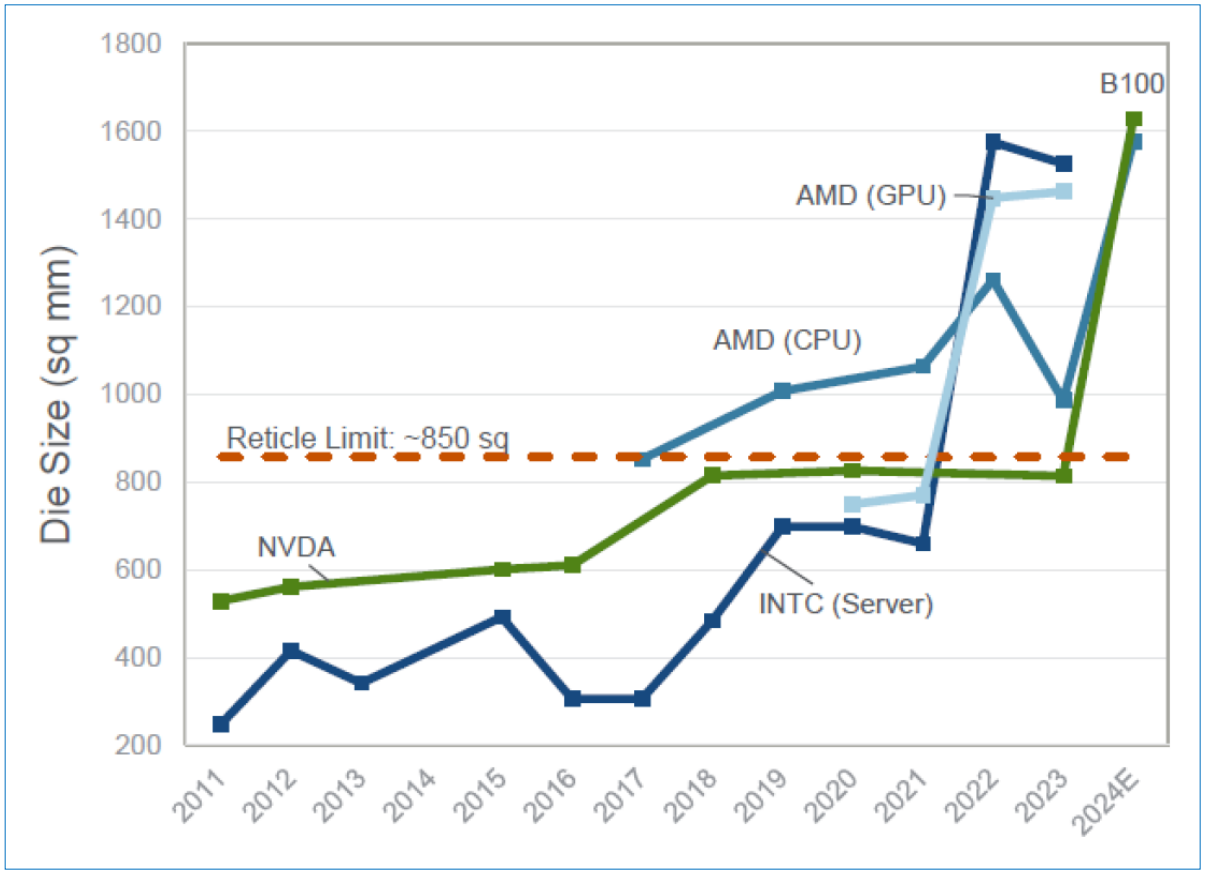


Source: Kini, G., AMD, "Thermal Landscape for Data Center GPUs" Binghamton University/IBM Research/GE Global 35th Electronics Packaging Symposium 2024, Vestal NY USA, September 4-5-2024. See presentation for references to prior sources incorporated.

HIR Die and Substrate Warpage

Die and package warpage for large area HIR processor packaging:

- "Die size" now significantly exceeds reticle size limit;
- Total *potential area for TIM coverage* (as TIM0 or TIM1) now exceeds 1600mm^2.

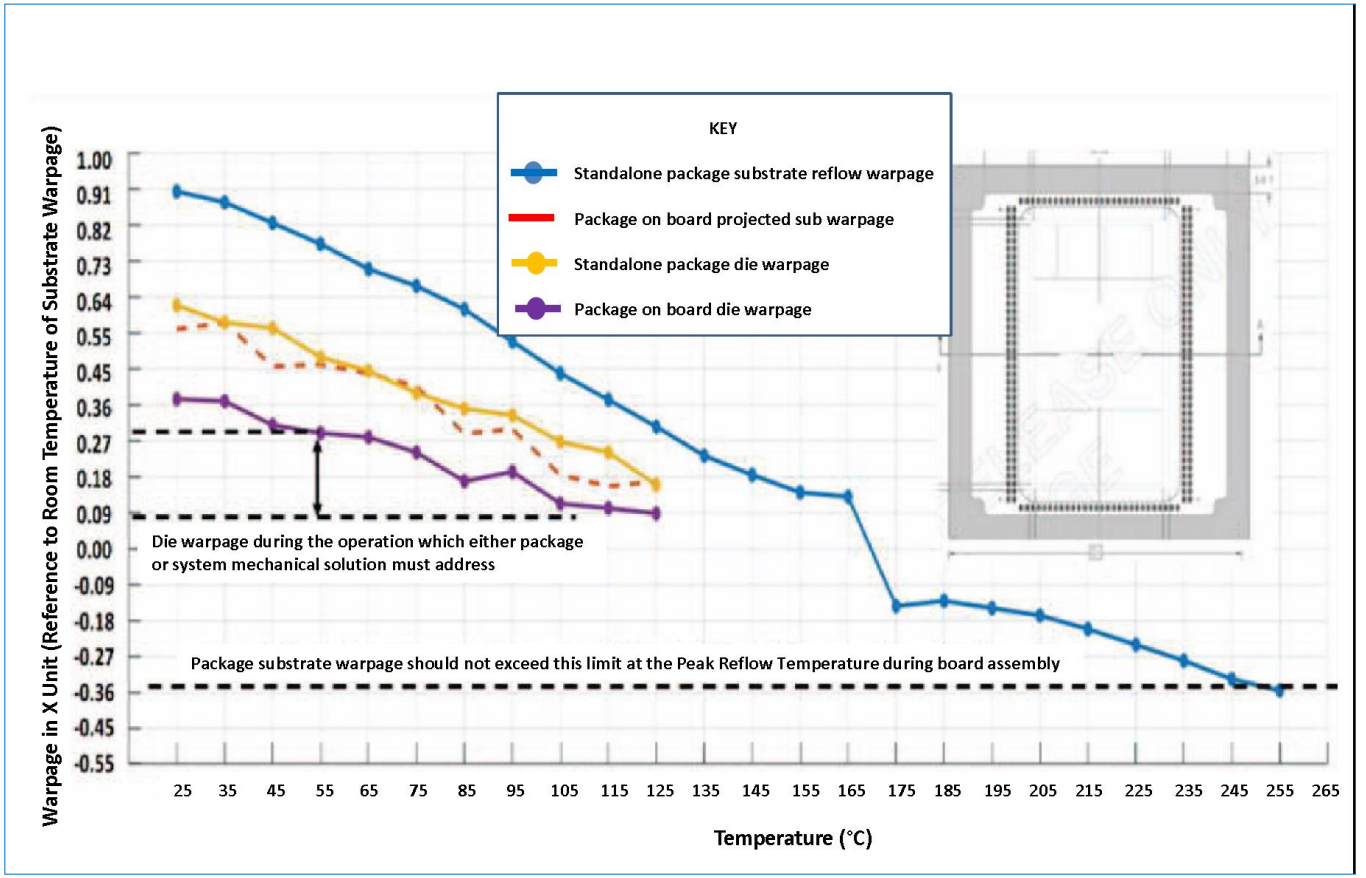


Source: Kini, G., AMD, "Thermal Landscape for Data Center GPUs" Binghamton University/IBM Research/GE Global 35th Electronics Packaging Symposium 2024, Vestal NY USA, September 4-5-2024. See presentation for references to prior sources incorporated.

HIR Die and Substrate Warpage

Die and package warpage for large area HIR processor packaging raises significant challenges for TIM1:

- Coverage of multiple die required
- Bond line thickness post-processing
- Potential die movement due to temperature-induced substrate and die stresses from CTE mismatch.

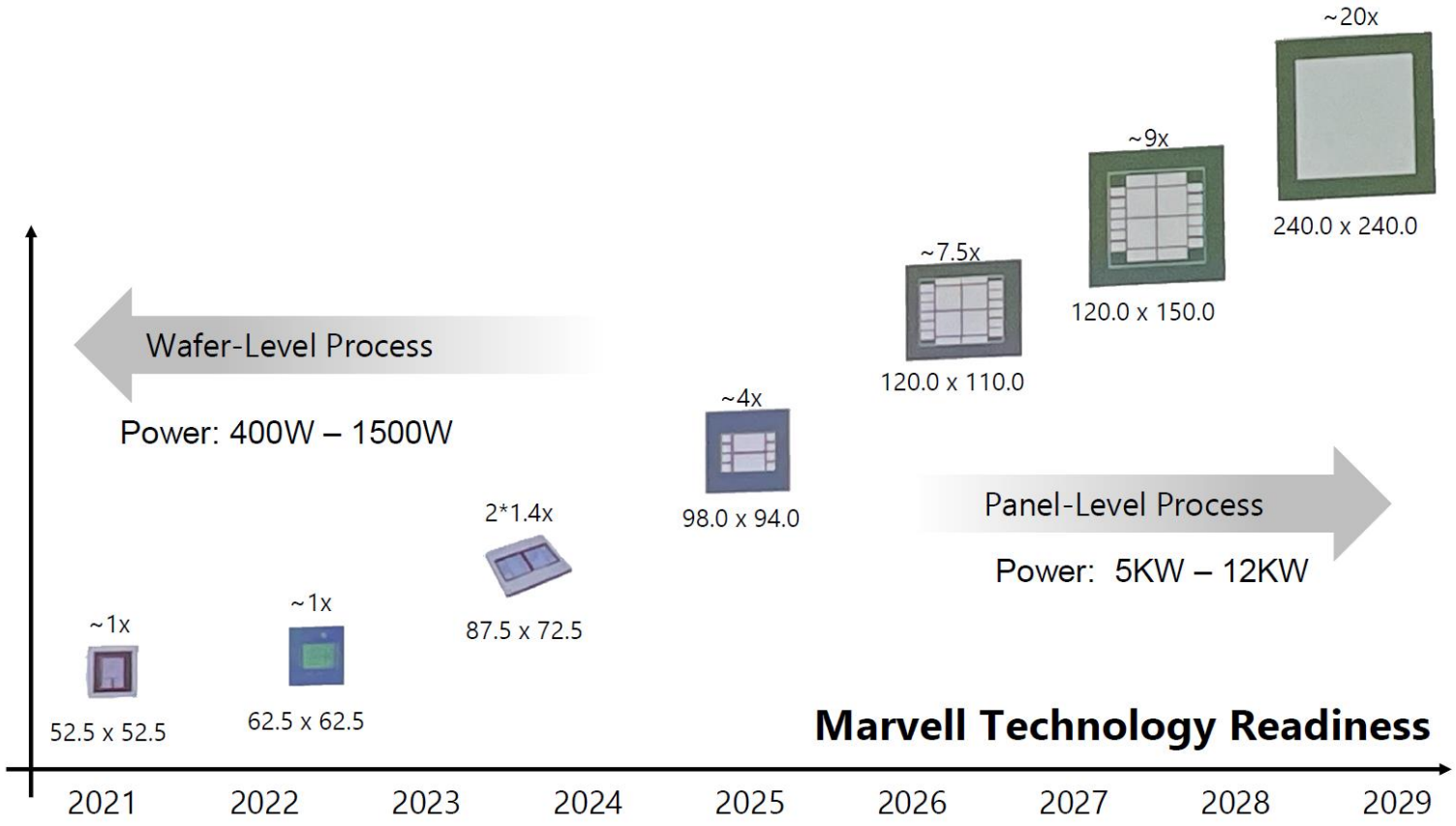


Source: Refai-Ahmed, G.; Do, H.; Islam, M. M.; Strader, J.; Arefeen, Q.; Huttenen, J.; "Roadmap and Challenges on the Next Generation of Thermal Interface Material for High Warpage Heterogeneous Package," 2022 IEEE 24th Electronics Packaging Technology Conference , Singapore, December 7-9, 2022.

HIR Die and Substrate Warpage

IC die and substrate forecast dimensional map, example:

- Marvell Technology
- Illustrates forecast growth in total die area per module

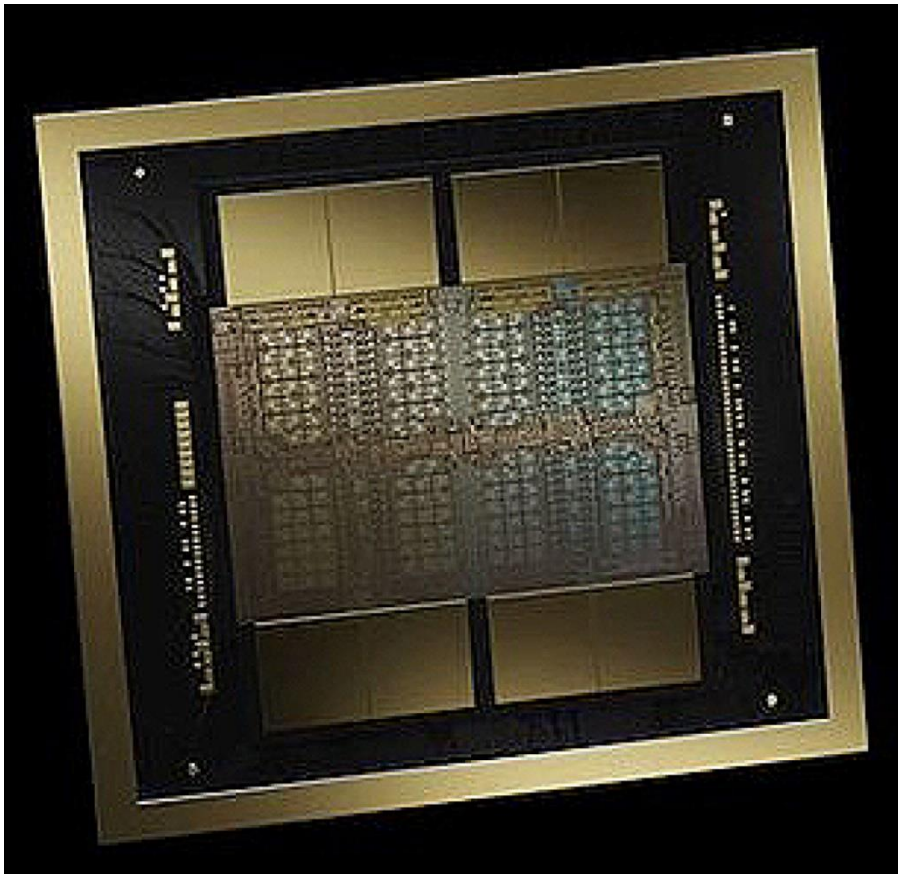


Source: Marvell Technology, Virk, P., IMAPS, 22nd International Conference on Device Packaging, Phoenix AZ USA, March 2026

HIR Die and Substrate Warpage

TSMC is expected in 2025 to:

- Introduce a 6X reticle-size “super carrier”
- Interposer may reach 5148 mm^2
- 9X reticle packages planned for 2027.



Source: Nvidia “Blackwell” Multi-reticle module. 3D-InCites, “Artificial Intelligence is Driving Panel Level Packaging,” March 11, 2024. Web: https://www.3dincites.com/2025/03/artificial-intelligence-is-driving-panel-level-packaging/

HIR Die and Substrate Warpage

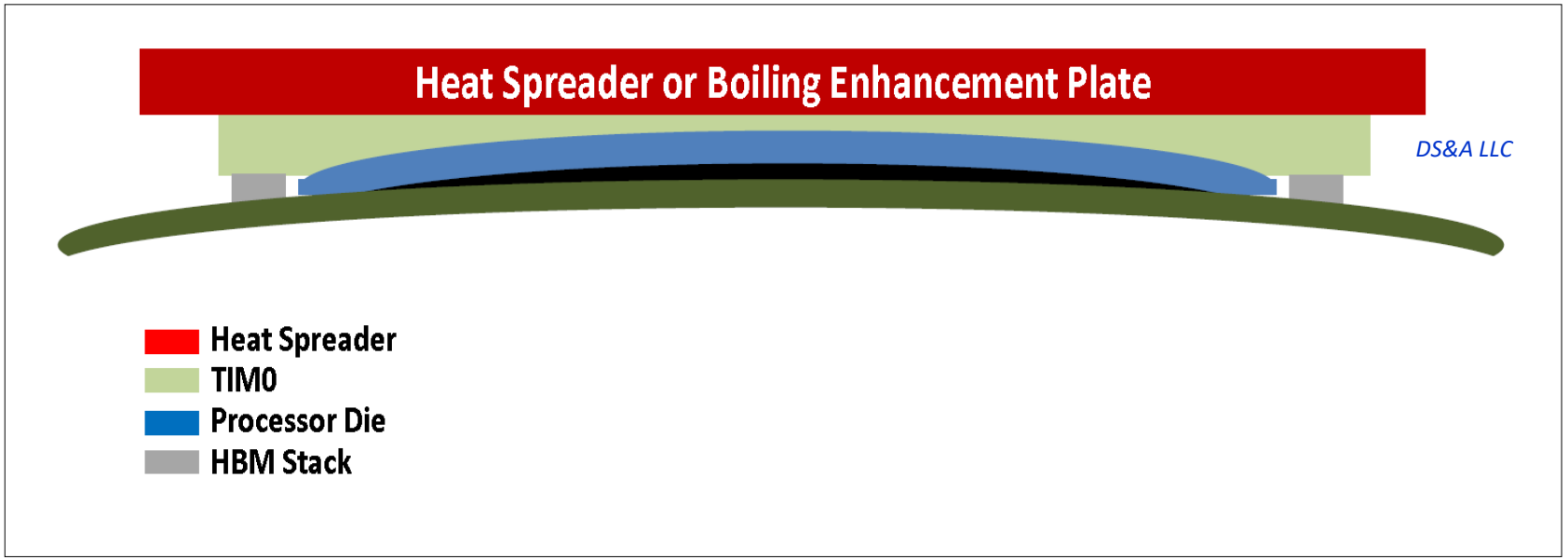
Die and package warpage for large area HIR processor packaging raises significant challenges for TIM1:

- Bond line thickness post-processing and resulting clamping force dramatically impacted by increasing die warpage values;
- Adequate TIM coverage of multiple die is increasingly difficult across entire area;
- Potential die movement due to temperature-induced substrate and die stress due to CTE mismatch, creating mechanical pumping action for polymeric TIMs;
- Liquid immersion systems pose identified immersion fluid contamination issues;
- *Newly identified phenomena: Two-phase liquid immersion fluid bubble erosion* eliminates applicability of many polymeric TIMs, for system long-term reliability.

Source: Kini, G., AMD, "Thermal Landscape for Data Center GPUs" Binghamton University/IBM Research/GE Global 35th Electronics Packaging Symposium 2024, Vestal NY USA, September 4-5-2024. See presentation for references to prior sources incorporated.

HIR Die and Substrate Warpage

Die and package warpage for large area HIR processor packaging raises significant challenges for TIM0:

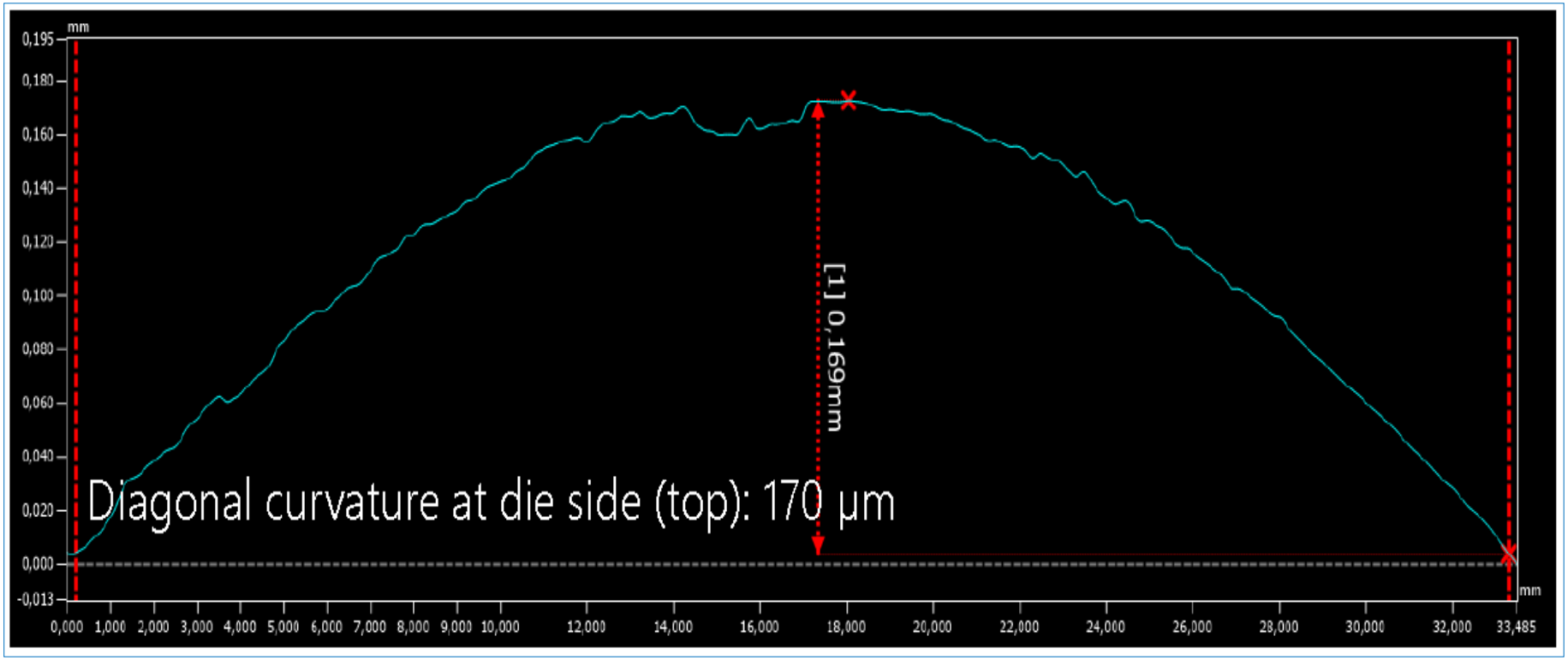


- A large-die TTV is a very useful tool for evaluating TIM performance at specific die temperatures at selected points across the die under test.

Source: Refai-Ahmed, G.; Do, H.; Islam, M. M.; Strader, J.; Arefeen, Q.; Huttenen, J.; "Roadmap and Challenges on the Next Generation of Thermal Interface Material for High Warpage Heterogeneous Package," 2022 IEEE 24th Electronics Packaging Technology Conference , Singapore, December 7-9, 2022.

HIR Die and Substrate Warpage

Example, measured die warpage (diagonal) for large area HIR processor package:



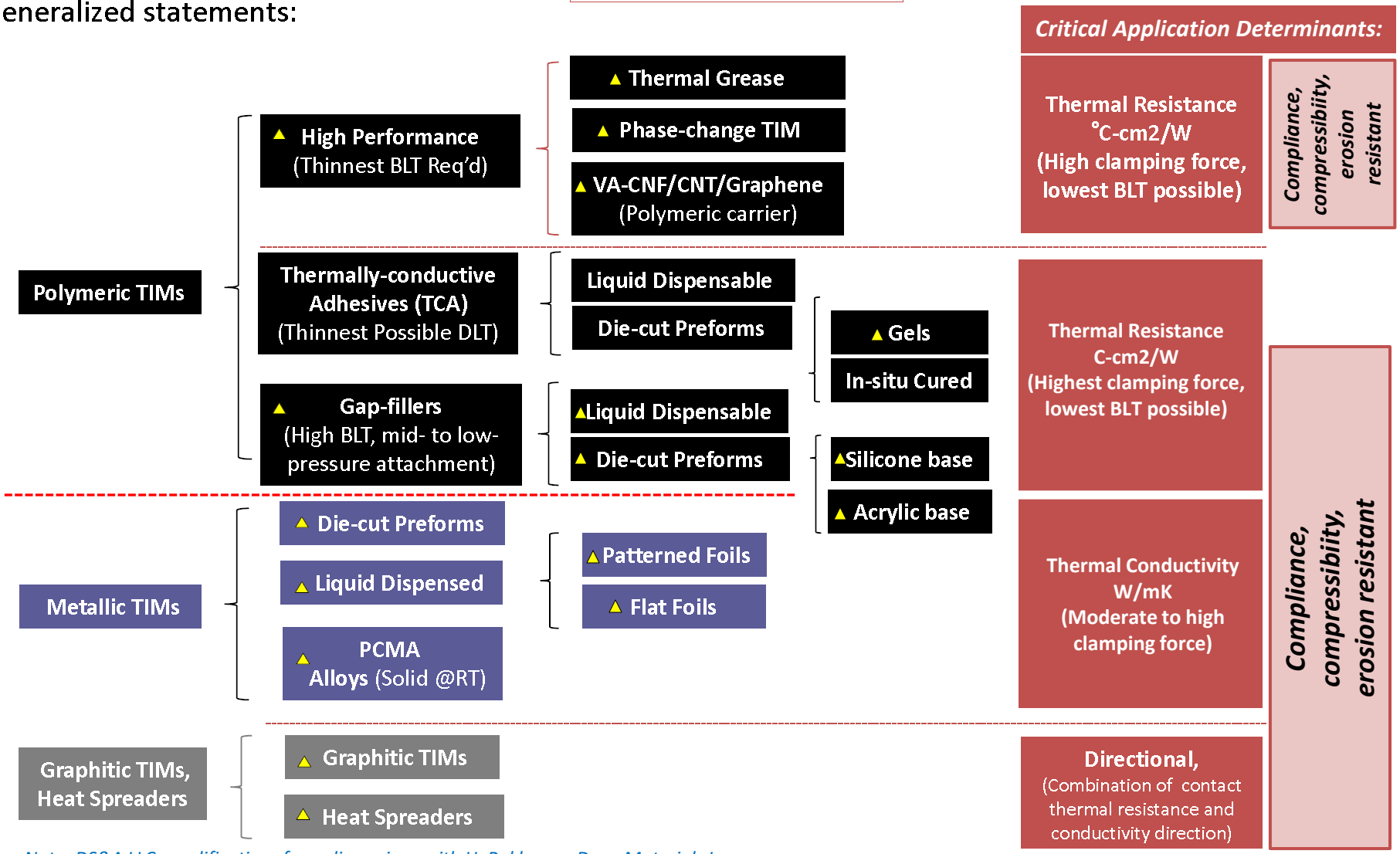
Some reported warpage values: ≥ 300µm

Sources: Abo Ras, M., "Thermal Test Vehicle for Investigation of Thermal Path in Large Die Area Packages by Thermal Transient Impedance Analysis" SEMI-THERM 40 Symposium, San Jose CA USA, March 2024.
Maximum reported warpage values: DS&A LLC, March 2025.

Thermal Interface Material Categories

Key
△ Mechanical Clamping Required

Generalized statements:



Note: DS&A LLC, modifications from discussions with H. Pokharna, Deep Materials Inc..

Thermal Interface Material Categories – Development Areas

General Categories of Thermal Interface Materials

Thermally-conductive adhesives (TCA) and pressure-sensitive TCA (PSA)
Die-attach adhesives (DA) – Used as TIM1
Gap-fillers
- Die-cut preforms (traditional format)
- Liquid-dispensed cure-in-place (most recent developments)

Graphite sheets and films (as heat spreaders and TIMs)
Elastomeric sheets
Electrically-isolating die-cut preforms
Thermal greases (Compounds, dispensed or die-cut preforms) and gels (dispensed)
- Silicone-based
- Non-silicone based

Phase-change compound (PCM, dispensed) and die-cut and sheet-form free-standing films (FSF)
Metallic die-cut pre-forms and die-cut pre-forms with thixotropic compound coatings
Liquid metals and variants
- **Solder thermal interface material (STIM) – Reflowed low-melting solders, used as TIM 1**
- **Liquid Metal Alloys (LMA)** *and* **Phase-Change Metal Alloys (PCMA)**
- **Hybrid Liquid Metal (HLM)**
- **Solid/Liquid Hybrids (SLH)**
- **Liquid Metal Embedded Elastomers (LMEE),** *somewhat similar to* **Liquid metal alloy gel**

Vertically-aligned carbon fibers (VA-CNF)
Vertically-aligned carbon nanotubes (VA-CNT)
Vertically-aligned graphite plates

Areas of greatest current development by TIM manufacturers highlighted in bold

Metallic TIM types

Graphitic/CNF/CNT TIM types

Note: TIM types shown in bold type are the primary applicable materials.

Thermal Interface Material Categories – Development Areas

Examples -- Relative bulk thermal conductivity values for development metallic TIMs of different types:

Bulk Thermal Conductivity Values – Metallic TIMs			
Basis[1]	**Category**	**Type (Typical Intended Usage)**	**Value (W/mK, Typ.)**
Indium Based	Solid	Solder TIM (TIM1)	70-86
		Compressible TIMs (Patterned, TIM2)	86
	Phase-Change	Phase-change metal alloy TIMs (TIM2)	40-50
Indium/Gallium[2]	Hybrid Liquid Metal	Indium® m2TIM™ (TIM1)	40-50
		Liquid metal pastes (TIM0, TIM1, TIM)	15-25
Gallium Based[2]	Liquid	Liquid metal TIMs (TIM0, TIM1)	20-45

- Bulk thermal conductivity is a useful indicator for initial selection for evaluation, but the primary determinant for performance is *in-situ thermal resistance* with specific application conditions for flatness, parallelism, force applied, operating environment.

Notes: 1. Primary metal by percentage.
2. Generalized statements regarding intended usages shown in parentheses. Multiple materials available from suppliers.
Source: Adapted from: Miloš Lazić, Indium Corporation, "Advanced Gallium-Based Thermal Interface Materials," IMAPS New England Symposium 49, Boxborough Massachusetts USA, May 2, 2023.

Current TIM Developments: Liquid Metals and Composites

Substantial materials developments are underway currently for solid-liquid hybrids using indium/gallium combinations, dispensed, and reflowed indium solders as TIMs:

Metallic TIM Types: Current Development			
Metallic TIM Type	**Primary Application Suitability**	**Advantages**	**Disadvantages**
Liquid Gallium Mixtures (Including LMA)	TIM0, TIM1, TIM2	Low interfacial resistance Excellent surface wetting Good bulk thermal conductivity	Retention dam required Gallium corrosion protection required for metal contact surfaces Thermal cycling degradation
Liquid Non-Gallium Mixtures (PCMA)	TIM0, TIM1, TIM2	Low interfacial resistance Excellent surface wetting Good bulk thermal conductivity	May require application-specific films and formats for production, handling, application process
Solid/Liquid Hybrid	TIM0, TIM1	Improved performance over liquid Excellent surface wetting	Thermal cycling challenges HVM challenges: process development
Amalgam	TIM0, TIM1	Final structure is a solid Some mechanical adhesion due to expansion	Requires phase change Solid interface can be brittle

Note: Modifications by DS&A: Shading indicates development materials. Grey shading indicates statements by DS&A from industry sources. Blue shading indicates statements from source documents listed below. Metallization for protection from corrosion is necessary; LMAs should not contact aluminum surfaces.

Source documents: 1. Jensen, T., "Metal TIM Innovations for High Performance Computing Applications," IMAPS UK-IEEE EPS Joint Thermal Management Workshop (Virtual), November 25, 2020; 2. Jensen, T., "Liquid Metal Innovations for High Performance TIMs," Semitherm Symposium 35, March 2019.

Current TIM Developments: Liquid Metals and Composites

Bulk thermal conductivity and suggested maximum operating temperatures for metallic TIMs:

Maximum Bulk Thermal Conductivity and Suggested Operating Temperature for Metallic TIMs		
Metallic TIM Composition	**Bulk Thermal Conductivity (W/mK)**	**Suggested Maximum Operating Temperature (°C)**
52In/48Sn Indalloy 1E	34	100
80 In/20 Sn	53	110
Indium Corporation Heat-Spring® (100 In)	86	125
Indium Corporation Heat-Spring® (In/Al Clad)	-	125
Sn, "Sn+"	73	200
100 Pb	35	250
100 Cu	395	750

- Table shows suggested values for selected metals and alloys; other alloys available.
- Characteristics of interface surfaces may affect maximum temperature.

*Note: Notes: * "Indalloy", "Sn+" are Indium Corporation products. Data Source: R. Jarrett, Indium Corporation , Utica NY USA; Bulk conductivity values, G. Wilson, Indium Corporation, Milton Keynes UK.*

Current TIM Developments: Liquid Metals and Composites

Metallic TIMs have been in volume production for decades for semiconductor and module applications in hundreds of millions of units with proven wide market acceptance:

Metallic TIM Types: Current Production			
Metallic TIM Type	**Primary Application Suitability**	**Advantages**	**Disadvantages**
Compressible w/Thixotropic Compound	TIM2	Low interfacial resistance Excellent surface wetting Range of metals, metal thicknesses, compounds, phase temperatures, and compound thicknesses (one-side, two-side) available; typically non-silicone	Traditional pre-form Phase-Change TIMs: PCM Coating on Al foil carrier Tooling, documentation, P/N Certain vendor compound formulas have poor thixotropicity
Compressible	TIM2	Long life and reliability, including for cryogenics and liquid immersion cooling No pump-out, bleed-out, run-out Range of metals and alloys available	Requires mechanical fastening Relatively high thicknesses
Reflowed Indium Solder (STIM)	TIM1	High performance, high bulk conductivity CTE-matching function Mechanical joining Many alloys available	Requires metallization (BSM, lid) Requires flux Requires one-time reflow process and reflow temperatures
Liquid Metal Alloy (LMA); Phase-Change Metal Alloy (PCMA)	TIM0 TIM1 TIM2	Low interfacial resistance Excellent surface wetting Applied as a liquid (LMA) or solid (PCMA)	Requires containment (dam) system Potentially subject to pump-out Thermal cycling degradation

Source: DS&A LLC.

TIM Characterization Methods

Thermal Interface Material Test Methodologies		
Performance Property	**Property Parameter**	**Method/Value**
Thermal Resistance	Through-plane (primary) bulk + (2) contact resistance values = total thermal resistance	**ASTM D 5470-17 (Steady-state, unidirectional controlled heat flow)** JEDEC JESD 51-14 (In-situ, Transient with structure function calculations from electrical resistances) **Thermal Test Vehicle (TTV, in-situ)**
Thermal Conductivity	Homogeneous, bulk (isotropic)	**ASTM D5470-17 (Steady-state)** JEDEC JESD 51-14 (Transient) Laser flash (Homogeneous materials) 3Ω Characterization
	Non-homogeneous, bulk (through-plane)	**ASTM D5470-17 (Steady-state, unidirectional flow)** **JEDEC JESD 51-14 (Transient)** 3Ω Characterization
	Non-homogeneous, bulk (in-plane)	**Berliner Nanotest LaTIMA™ (Steady-state, in-plane flow)** Scanning pulsed laser

Note: Not all test methods (such as laser flash) are suitable for testing certain categories of TIMs, such as anisotropic and/or non-homogeneous structures. Examples of non-homogeneous structures are TIM compounds coated on a dielectric carrier or metal foil and multilayer TIMs.)

TIM Characterization Methods

Method	Steady-State	Transient/Structure Function
Designation	**ASTM D 5470-17 industry-wide standard**	**JEDEC JESD 51-14 semiconductor industry**
Purpose	Highly-defined test data generated under specific controlled, known unidirectional flow conditions • Primary industry standard for comparative performance	Data is generated under application-specific ("in-situ") conditions • Structure function knowledge required
Benefit	• Enables independent test lab data comparisons across multiple labs, test stands • Multiple types of tests, including mechanical reliability • All types of TIM and thermal materials, including adhesives • Multiple types of data generated: • Thermal conductivity • Thermal resistance vs. pressure range (0-140 PSI, typical)	• Requires specific package type and die, to generate useful in-situ test data • Characterizes internal package electrical and thermal performance • Results can be imported to CFD models for that one specific package and one set of conditions.
Data Output Types	• Known: Power, pressure, surfaces, heat flow • Application-dependent variables removed • Generate data sheet values under known conditions – *vital for TIM manufacturers and for material-to-material comparisons* • Ideal for *materials down selection* prior to test and evaluation	• Results will *not* necessarily correspond to ASTM D 5470-17 data – *by definition* • Results will be tightly aligned to a specific package type, only
Ideal User	• TIM and thermal material developers and manufacturers • Industry OEM mechanical engineers • Selecting TIMs for system design	Universities, semiconductor manufacturers

Note: Not all test methods (such as laser flash) are suitable for testing certain categories of TIMs such as anisotropic and/or non-homogeneous structures.

TIM Characterization Tools: ASTM D 5470-17 Test Stands

Thermal test per ASTM D-5470-17:

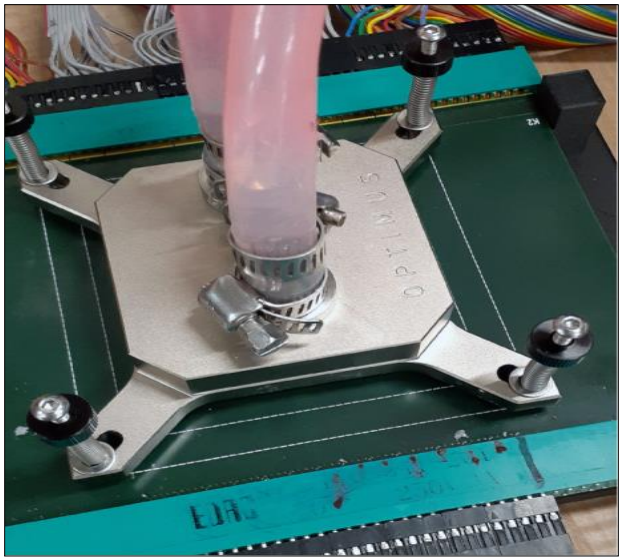
- Test stands available off the shelf from three suppliers
- Use of standardized lab-conditions testing is ideal for TIM vs. TIM comparison
- Goal is to arrive at down selection of a small (i.e., 2) materials to test in-situ
- System example: Berliner Nanotest TIMA6
  - Newly released in March 2026, upgrade from industry-standard TIMA5
  - 500W power to upper (heater) test head (versus 80-100)
  - Test head sizes 10mmx10mm to 38mmx38mm (versus 25x25mm)
  - Higher force applied capability (to 120PSI w/38x38mm test head set
  - Improved resolution and user GUI

Source:

TIM Characterization Tools: TTVs

Thermal test vehicles (TTVs) have become *critical for evaluation of multiple characteristics of TIM performance* in-situ with test packages given two industry-critical trends for integrated circuits:

- Heterogeneous integration (HIR) modules incorporate multiple processor, HBM memory, and support ICs on a *single complex substrate*;
- Placement of multiple processor die with minimum (<10µ) spatial separation;
- "Single-die processor" may refer to two to six (or more) AI/GPU, ASIC, or processor die placed on single substrate;
- Temperature-sensitive stacked HBM and control modules placed at periphery;
- Total die area is therefore termed as "multi-reticle"
- *HBM, other die: dissimilar die heights*
- TTV testing: temperature mapping capability across the *entire die area*
- Useful for developing temperature mapping to assess die warpage impact.

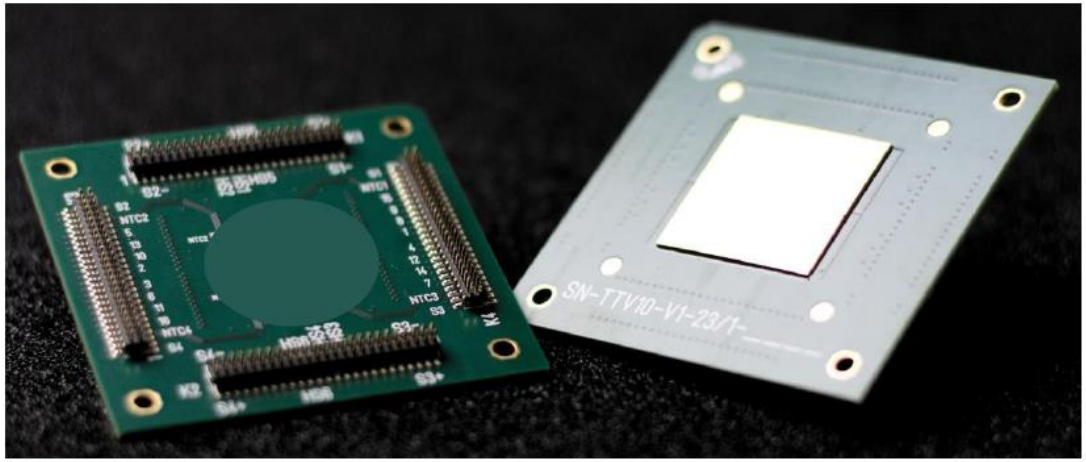


Source: Liquid cold plate applied to bare die TTV on engineering test board (ETB). (Photograph, DS&A LLC, January 16, 2024.)

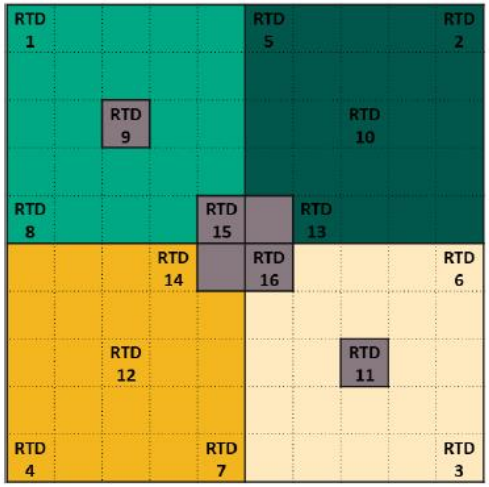
TIM Characterization Tools: TTVs

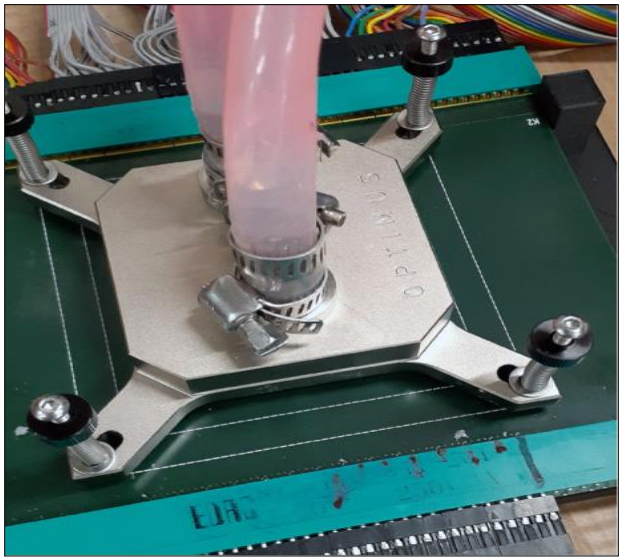
Thermal test vehicles and companion engineering test boards (ETB):

- Examples from Berliner Nanotest und design GmbH:



Electronic test board for TTV (adapter board with sense current and MUX)



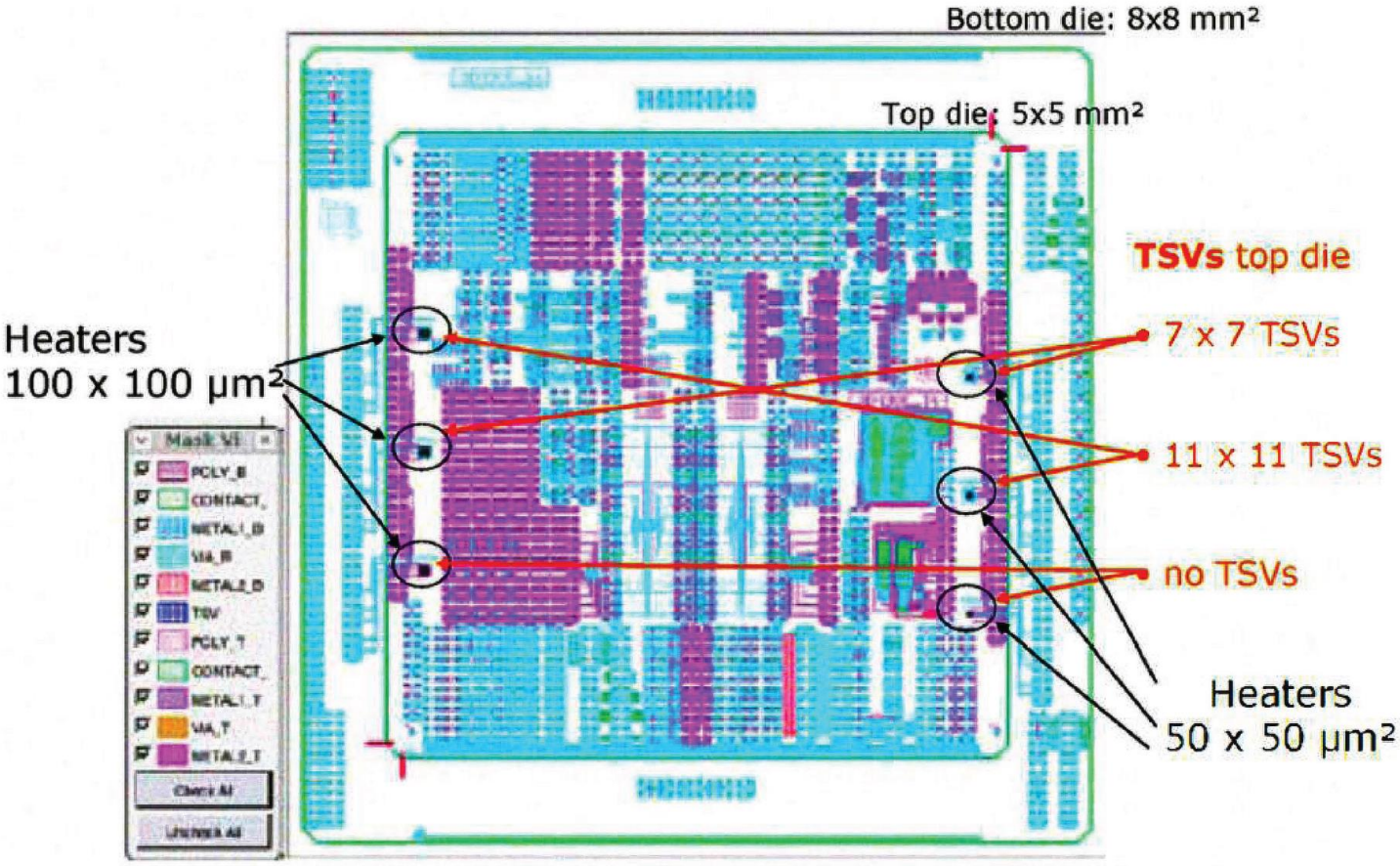


Sources: (Above) Nanotest; (right) Photograph, DS&A LLC, January 16, 2024.)

TIM Characterization Tools: TTVs

Example of a TTV designed for characterizing and evaluating CPU die hot spots:

- Design layout of the die stack of the thermal test chip with the thermal test structures



Source: IMEC, Oprins H., Cherman, V., Torregiani, C., Stucchi, M., Vandevelde, B., Beyne, E.; "Thermal Test Vehicle for the Valiation of Thermal Modeling of Hot Spot Dissipation in 3D Stacked ICs," IEEE Electronic Systems Technology Conference ,August 31, 2010. https://doe.org/10.1109/estc.2010.5642955

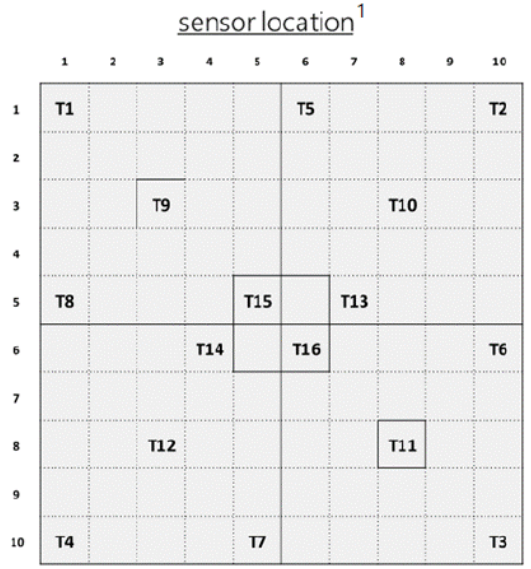
TIM Characterization Tools: TTVs

Simplified statement of thermal test vehicle output as reported by Jain, S., Arieca:

- Reference describes development of *controlled warpage TTV* capabilities for addressing die warpage
  - Targeting 150µ warpage in described assembly

- Cold Plate Temperature = Monitored through the thermocouple drilled to the center of the heat sink.
- Average Die Temperature = Derived from the mean values of 16 temperature sensors
- Temperature Differential (ΔT) = Average die temperature – Cold Plate temperature
- Rth = Computed using ΔT and Power

[1] Nanotest

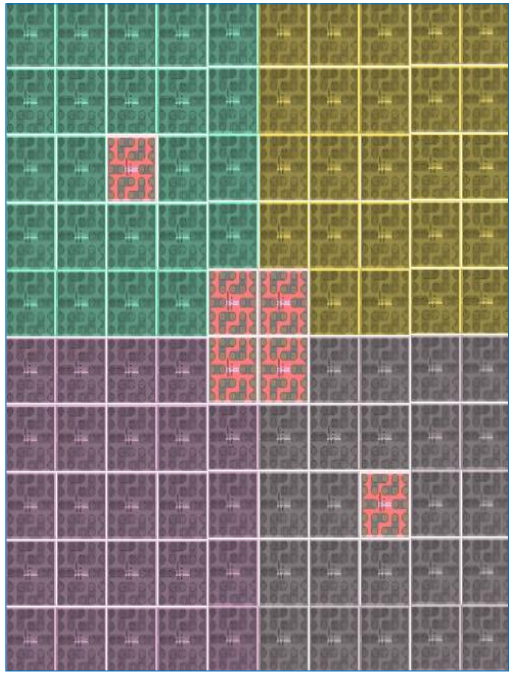


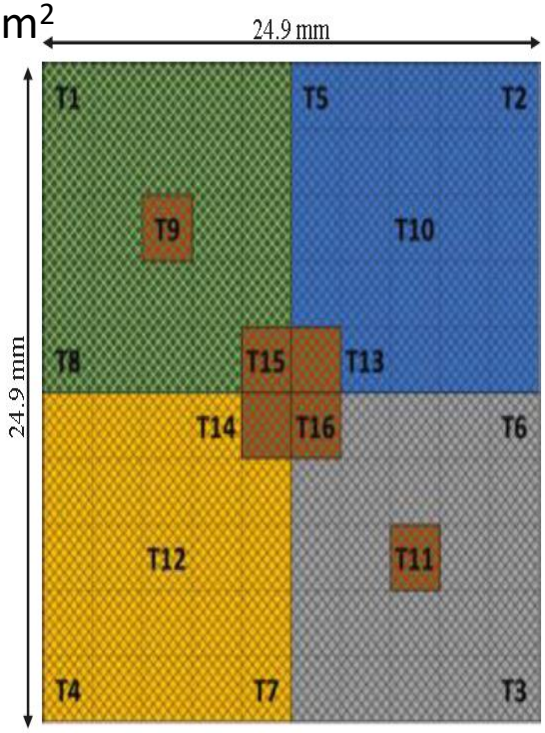
Source: Qnity, Jain, S., et. Al, "Thermal Performance Evaluation of TIM 1.5 Under Large TTV Warpage," SEMI-THERM 42 Symposium, March 9-12, 2026, San Jose CA USA.

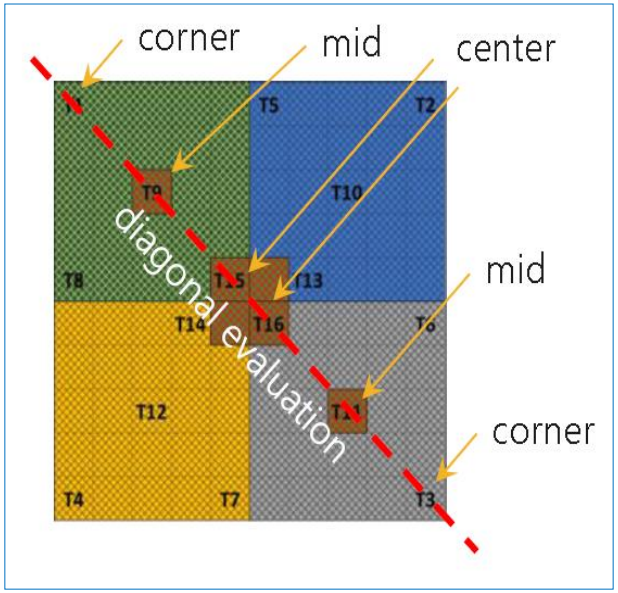
TIM Characterization Tools: TTVs

Large-die TTV construction:

- 10x10 cells in 24.9 x 24.9mm (620mm^2) die area
- 60x60 maximum substrate area
- (4) heater zones, (16) RTDs
- Power density to 10W/mm^2





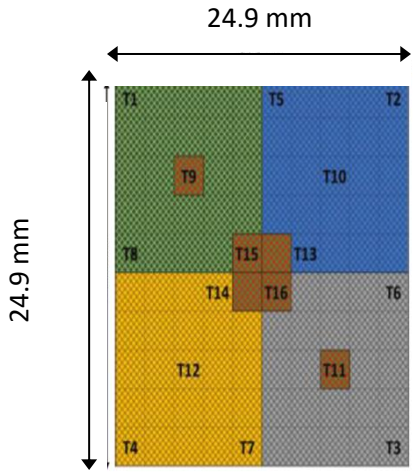


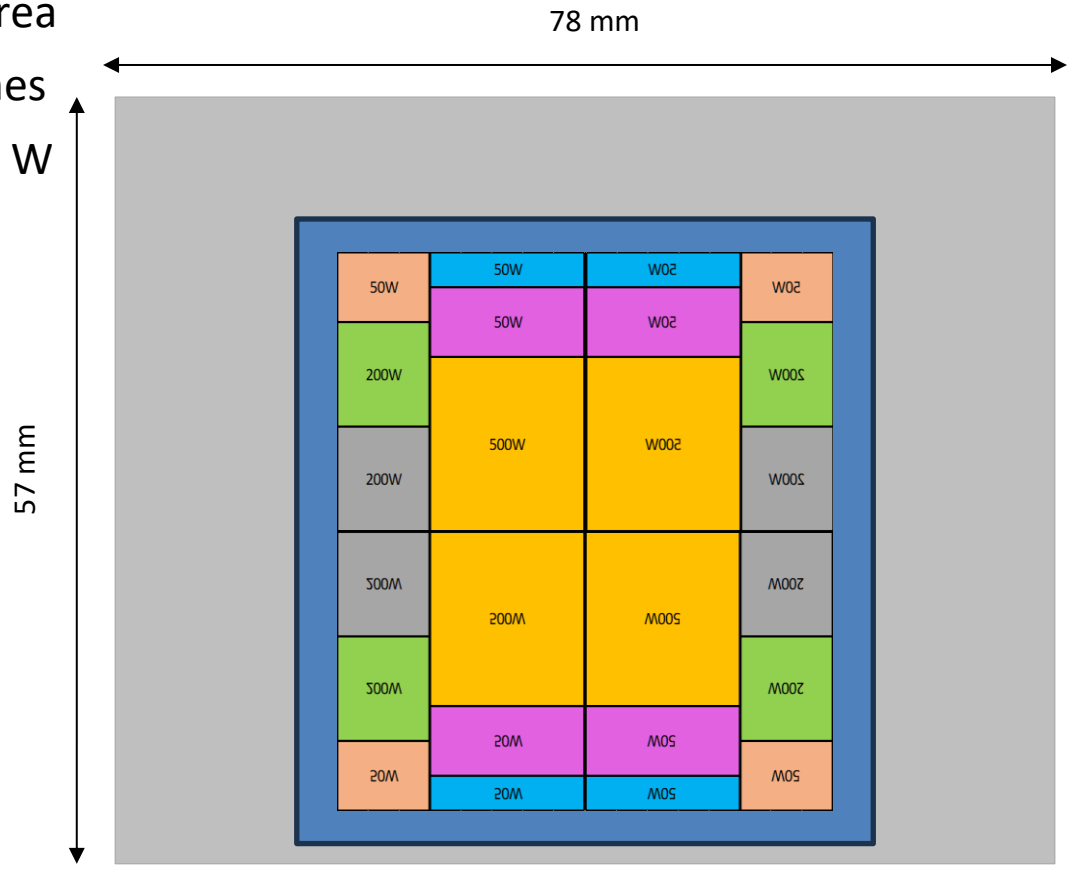
Source: Abo Ras, M., "Thermal Test Vehicle for Investigation of Thermal Path in Large Die Area Packages by Thermal Transient Impedance Analysis" SEMI-THERM 40 Symposium, San Jose CA USA, March 2024.

TIM Characterization Tools: TTVs

Next large-die TTV construction (in development):

- 39.9mm x 39.9mm (1592mm^2) die area
- 78mm x 57mm substrate area
- 24 Independent heater zones
- Total package power: 4000 W





Source: Abo Ras, M., "Thermal Test Vehicle for Investigation of Thermal Path in Large Die Area Packages by Thermal Transient Impedance Analysis" SEMI-THERM 40 Symposium, San Jose CA USA, March 2024. Abo Ras, M., Berliner Nanotest und Design GmbH, "The Unique Role of Thermal Test Vehicles (TTV) for TIM Characterization and Reliability Investigation ," 41st Chemnitz Seminar, Test and Reliability Solutions – New Opportunities for Electronic Components and Systems," Technical University Chemnitz, Chemnitz, Germany, February 14, 2025.

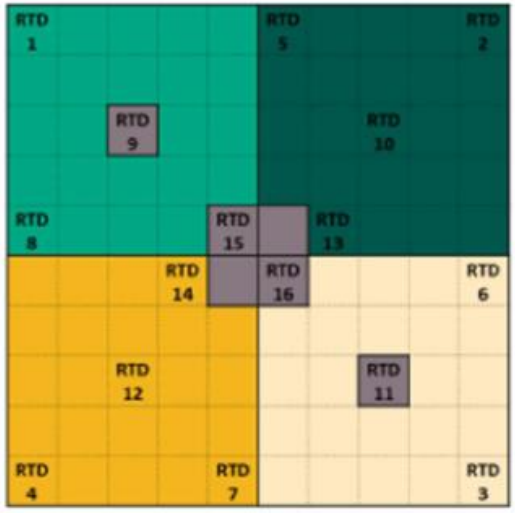
TIM Characterization Tools: TTVs

Latest new TTV releases:

- 10x10 to 20x20 cells – even more powerful
- Increasing number of cells with heaters and temperature sensors

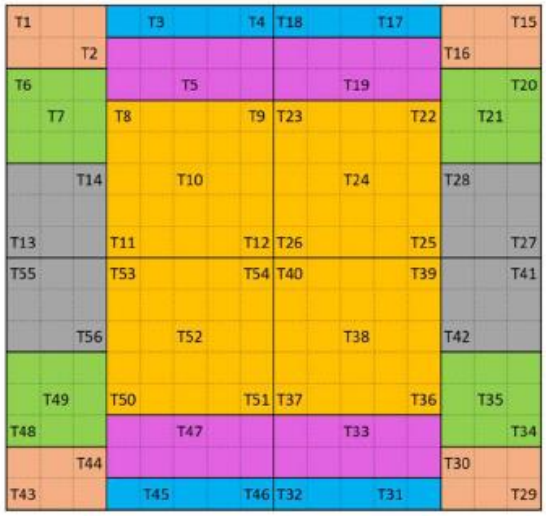
TTV10

10x10 cells



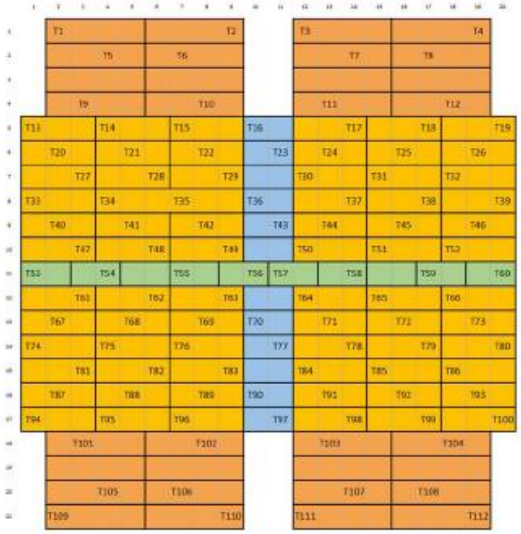
TTV16

16x16 cells



TTV200

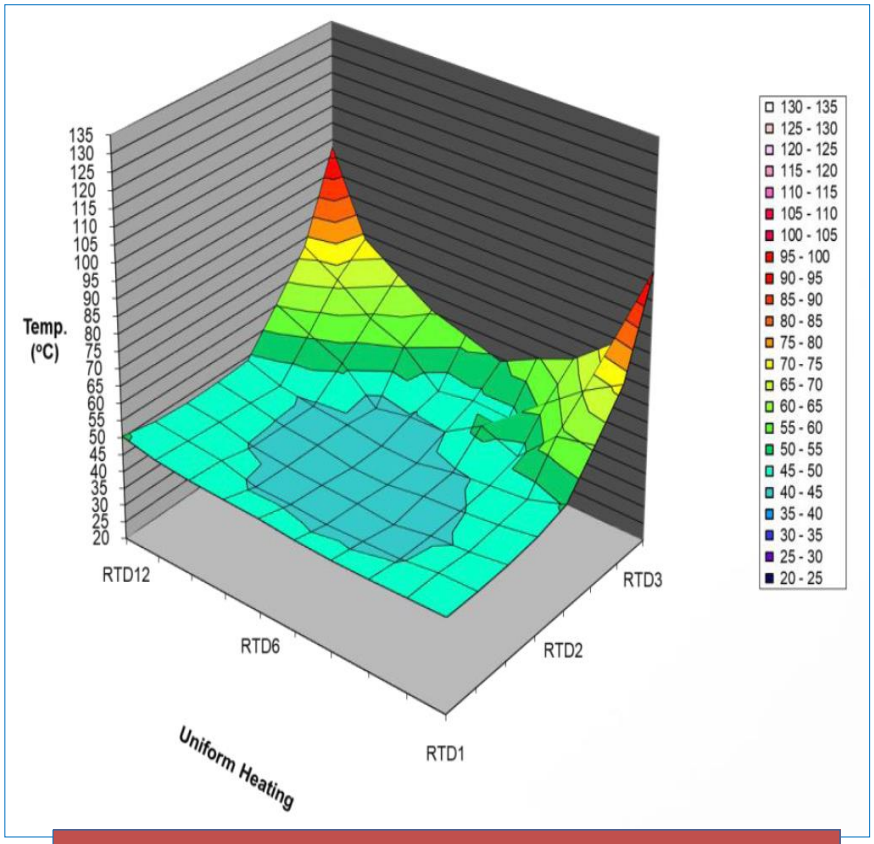
20x20 cells



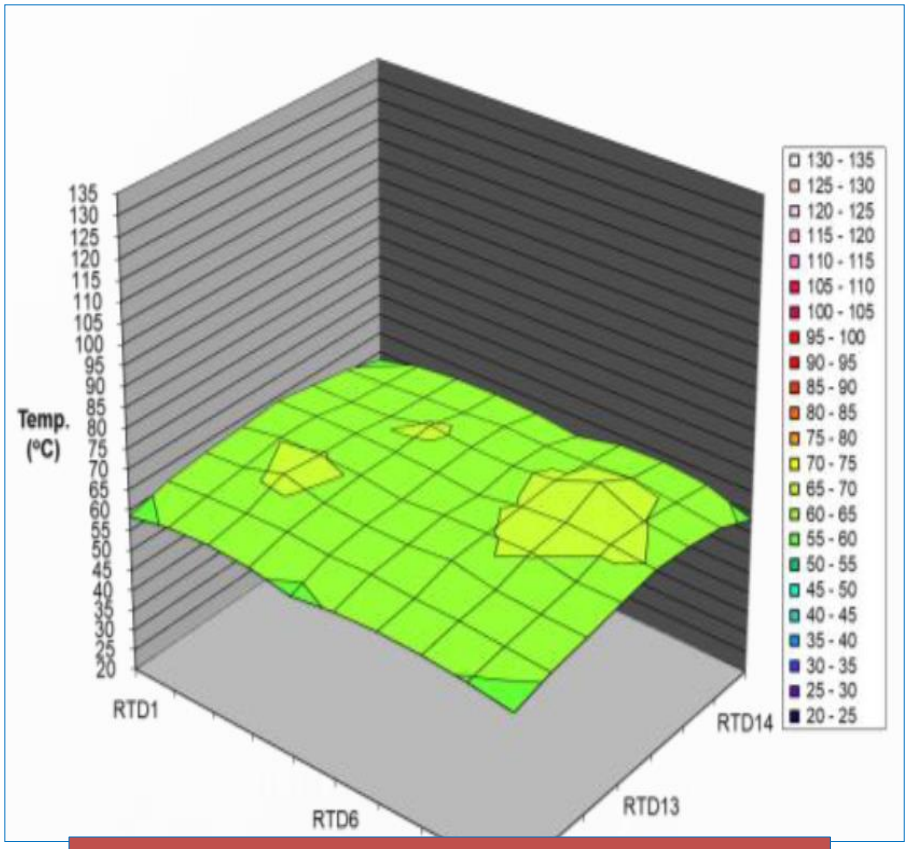
Source: J. Haseloff, M. Sternberg, D. Wargulski, M. Abo Ras, "Power Cycling Test Methodolog to Investigate TIM Degradation Under Varying Interface Configurations for High-Performance Computing Using Thermal Test Vehicles," IMAPS France Thermal and Micropackaging Workshop 19, La Rochelle, France, March 24-27, 2026.

TIM Characterization Tools: TTVs

Large-die TTV comparative sector performance testing of selected TIM0/TIM1:



High-performance silicone thermal grease



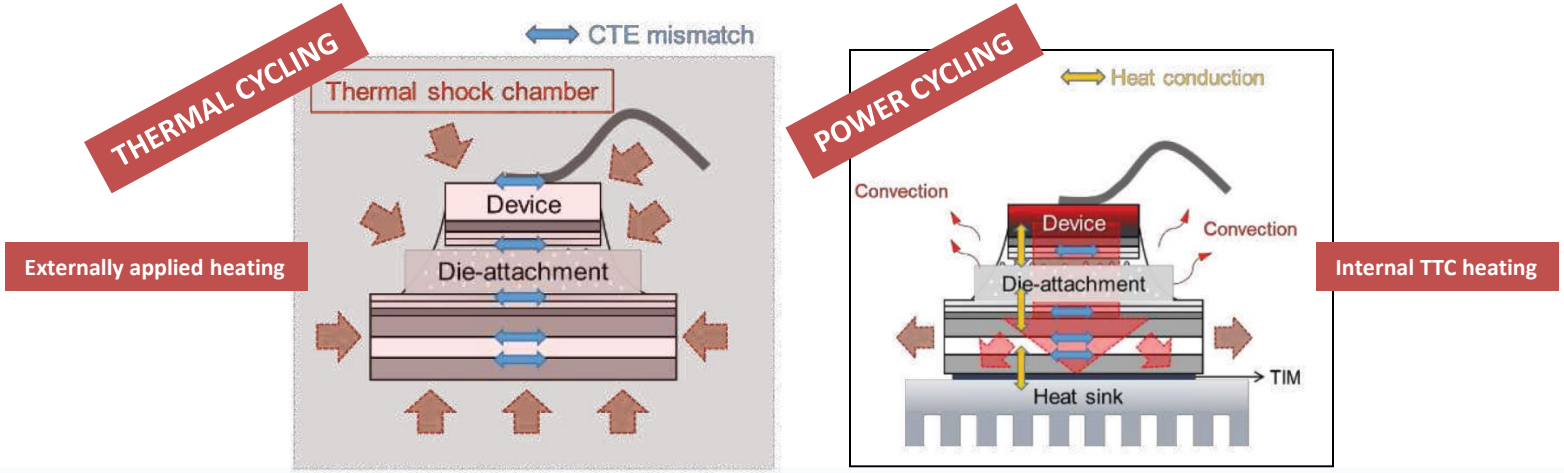
Development Phase-change Metal Alloy

Sources: Jensen, T., "Metal TIMs for High Performance BGA Packages, SEMI-THERM 40 Symposium, San Jose CA USA, March 2024; Jensen, T., "Metal TIMs for Bare Die Applications" IMAPS Symposium 2024, Boston MA USA, September 30 – October 2, 2024.

TIM Characterization Tools: TTVs

Function of thermal test vehicle (TTV) for TIM testing:

- Primary: Device package similar to planned production (commercial) package;
- Important additional function is internal heating capability (versus externally-applied heating), especially with multiple heat sources and temperature sensors:
  - Within a single die, capable of on-die high heat flux point source of heating
  - Within a single die or multi-die package, evaluation of internal package stresses.
- Typically a second-level test method employed in a sequence of tests, such as:
  1. ASTM D 5470-17 for TIM down-select;
  2. TTV for package and die analysis;
  3. Thermal cycling, power cycling, HAST, thermal shock for reliability testing.



Source Reference: Kim, D; Yamamoto, Y.; Nagao, S.; Wakasugi, N.; Chen, C.; Suganuma, K.; "Measurement of Heat Dissipation and Thermal-Stability of Power Modules on DBC Substrates with Various Ceramics by SiC Micro-Heater Chip System and Ag Sinter Joining", DOI: 10.3390/mi10110745.

TIM Characterization Tools: Other Methodologies

Other test methods available:

Thermal imaging:

- Very common for gross temperature measurement of a device or assembly
- Emissivity coating(s) are critical for useful results.
  Laser flash (LFA): Widely known for rapid testing for basic data. Primarily suitable for testing homogeneous materials. Heterogeneous thermal materials may result in no useful test results or misleading test data.
- An excellent examination of the use of LFA specific to gap-filler materials (thermal performance, performance degradation with temperature, reliability is found in reference (a): Vinh Khuu, University of Maryland, 2009).
- Modified hot wire (MHW) following ISO 8894 or ASTM C 1113.

HotDisk:

- Not well known or frequently used. See reference (b): Developers Gustavsson and Gustafsson (original manuscript, anisotropic materials).

Source references:
a. Khuu, V. "Evaluation of Thermal Interface Mateirals and the Laser Flash Method", Thesis, Doctor of Philosophy, University of Maryland, USA. 2009. Online: https://drum.lib.umd.edu/handle/1903/9873

b. Gustavsson, M.; Gustafsson, S.E.; "On the Use of Transient Plane Source Sensors for Studying Materials with Direction Dependent Properties", Chalmers University of Technology, IEEE ITCC 26, 2001.

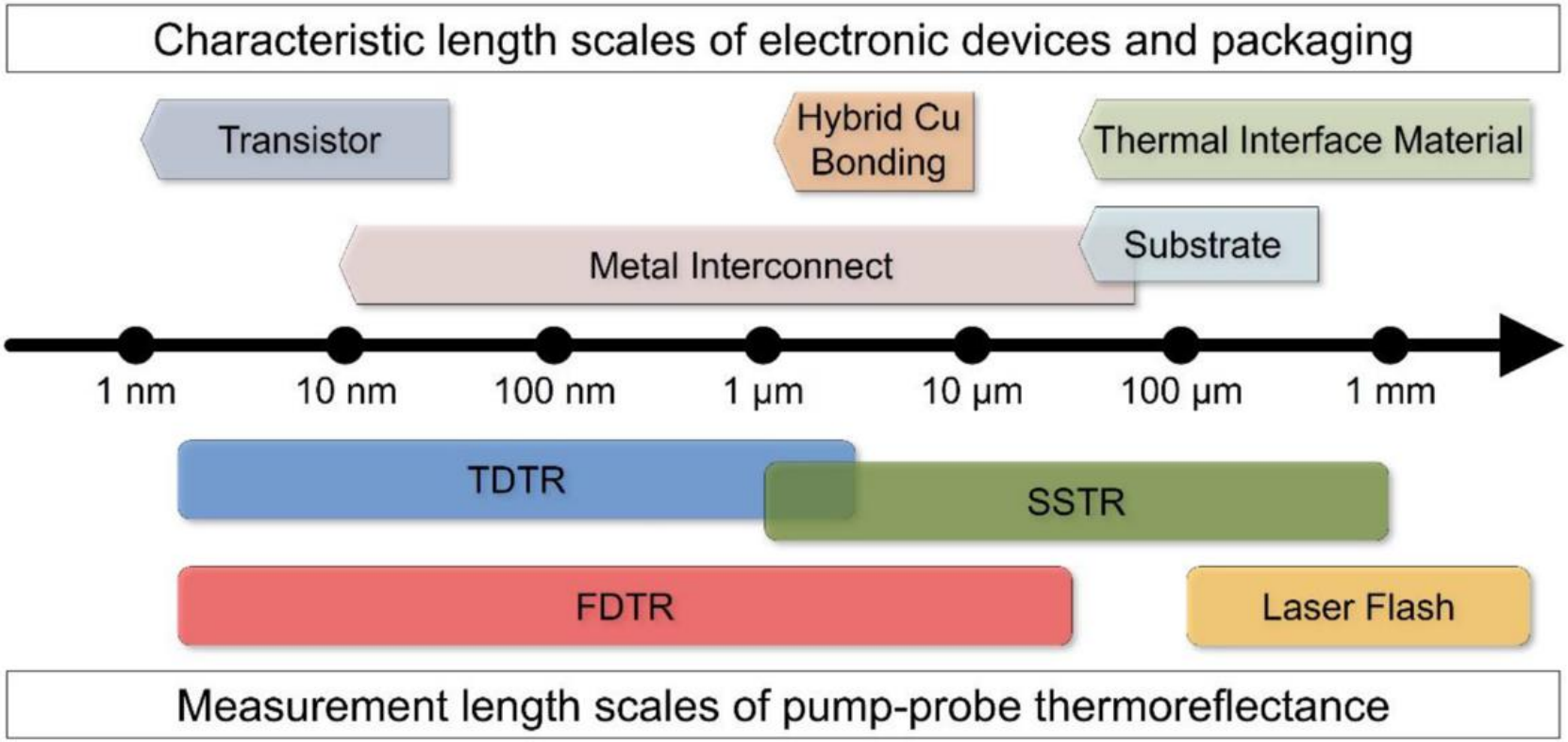
Thermal Characterization and Failure Analysis Tools

Thermoreflectance characterization methods – very concise overview of three principal methodologies and comparative statements for usefulness:

	Time-Domain Thermoreflectance	Frequency-Domain Thermoreflectance	Steady-State Thermoreflectance
Measured Property	k, TBC, C	k, TBC, C	k, TBC
References	Number: Target (Measured property) [211,212]: TIMs (k) [213,214]: Cu-Cu bonding (TBC)	Number: Target (Measured property) [208,217]: Buried interface: Si-Si bonding (TBC) [215,216]: Buried interface: GaN-Diamond bonding (TBC) [218–221]: TIMs (k, TBC, C)	Number: Target (Measured property) [222]: Buried Ga_2O_3-SiC bonding (TBC) [223]: Buried layer (k)
Advantages	- Nanometer-scale depth resolution - High measurement sensitivity near the sample surface - Capability to capture non-equilibrium dynamics	- Nanometer-scale depth resolution - Broader probing depths: from near surface to buried layers - Capability for high-throughput multi-frequency thermal imaging - Cost and size	- Capability to measure k without knowledge of C - Capability to measure the properties of thermally buried layers and interfaces - Cost and size
Disadvantages	- Cost and size (ultrafast pulsed laser, mechanical delay stage, EOM) - Typically require C for extracting k and TBC	- Incapable of capturing non-equilibrium phenomena dynamics - Typically require C for extracting k and TBC	- Incapable of capturing non-equilibrium phenomena - Calibration is required for every experiment

Source: Park, J-H, et. Al, "A Review of the Thermo-mechanical analysis framework for microelectronics packaging: Mechanics, Material Property Determination, and Structural Considerations. J. Materials Science in Semiconductor Processing, 12-10-2025. DOI: doi.org/10.1016/j.mssp.2025.110321.

Thermal Characterization and Failure Analysis Tools



Source reference: Khuu, V., University of Maryland, "Evaluation of Thermal Interface Materials and the Laser Flash Method", Thesis, Doctor of Philosophy, University of Maryland, USA. 2009. Online: https://drum.lib.umd.edu/handle/1903/9873

TIM Characterization and Performance Drivers

General statements determining performance for selecting a well-performing thermal interface material:

- Clamping force uniformly applied must achieve maximized surface wetting;
- *Achieving thinnest possible thickness with highest clamping pressure is critical to minimizing thermal resistance.*
- Degree of surface wetting achieved is critical to overall performance to minimize contact thermal resistance at each of two contact surfaces.
  - *Contact resistance dominates TIM bulk resistance for polymeric TIMs.*
- Excellent bulk Z-direction thermal conductivity is necessary when limited clamping force (e.g., $\leq$ 30PSI) is available for polymeric TIMs.
- For liquid immersion applications, ideal TIM needs:
  - Do *not* contaminate immersion fluid
  - Are compatible with immersion fluid chemistries
  - *Are not subject to erosion* by bubble action in two-phase immersion.

HIR Die Warpage Developing Solutions: What is Needed

Developments needed to address bare-die HIR IC module warpage issues:

- Implement a module lid incorporating accompanying TIM1:
  - *Places warpage control and TIM responsibility on the semiconductor manufacturer*, resulting in improved control of TIM application, enabling use of solder TIMs (STIMs), and correcting retention and reliability;
- Implement improved mechanical fastening hardware with *balanced (uniform) pressure capability with engineered minimum pressure*
- Development of new high thermal conductivity substrates
- Focus on improvements in CTE matching throughout the materials stack to reduce warpage
- Continuing development of additional new forms of metallic or graphitic TIMs not subject to bubble action erosion in two-phase immersion systems.
- For TIM1, transition to application of liquid metal TIMs with retention barriers or PCMAs.

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