High-throughput Additive Manufacturing of Microelectronics including Passive & Active Components for 3D HI, Legacy Electronics and Advanced Packaging

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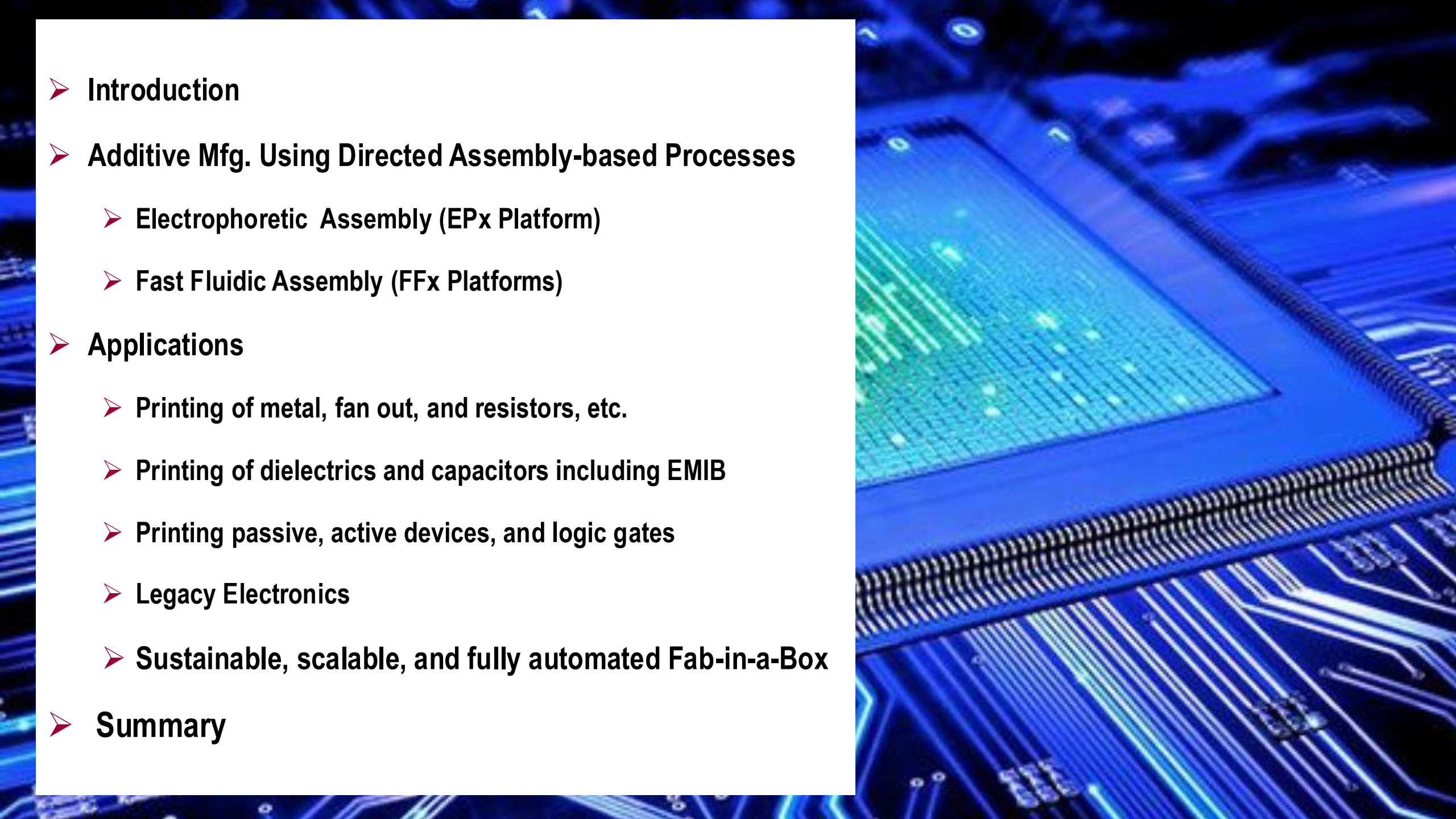
www.nanomanufacturing.us, www.nano-ops.us



- Introduction
- Additive Mfg. Using Directed Assembly-based Processes
  - Electrophoretic Assembly (EPx Platform)
  - Fast Fluidic Assembly (FFx Platforms)
- Applications
  - Printing of metal, fan out, and resistors, etc.
  - Printing of dielectrics and capacitors including EMIB
  - Printing passive, active devices, and logic gates
  - Legacy Electronics
  - Sustainable, scalable, and fully automated Fab-in-a-Box
- Summary

What if we A Sustainable Semiconductor Foundry in a Box

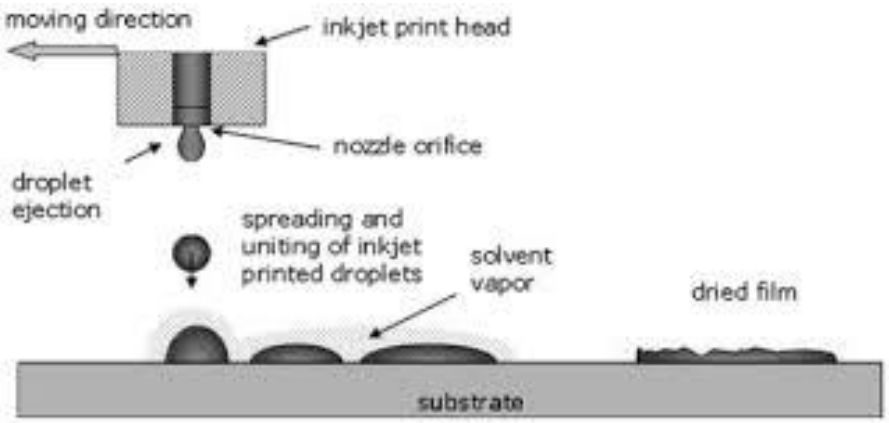
- On-demand chips, interposers, or packages in a few hours
- Multi-material, monolithic, quick turnaround, low cost fab
- No etching, chemical reactions, or vacuum
- 100 times faster than conventional fabrication
- 1000 times faster than 3D printing
- 25 nm to 1000 microns feature size demonstrated
- Modular, automated ~10 m^2 system footprint
- Up to a 1000 times reduction in materials use
- Reduces carbon footprint by more than an order of magnitude

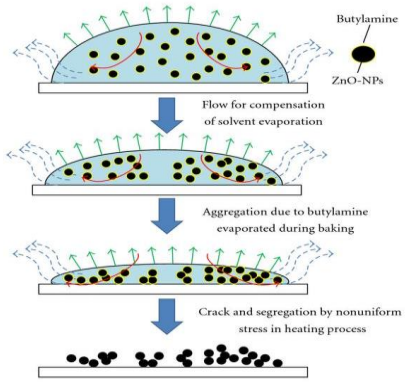
Semiconductor Foundry in a Box

Patented new technology (directed assembly-based printing) to print circuits at the nano and microscale funded by NSF and DoD.

How does directed assembly-based printing work?

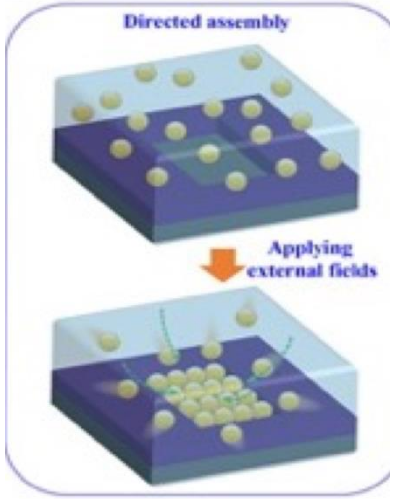
Inkjet printing

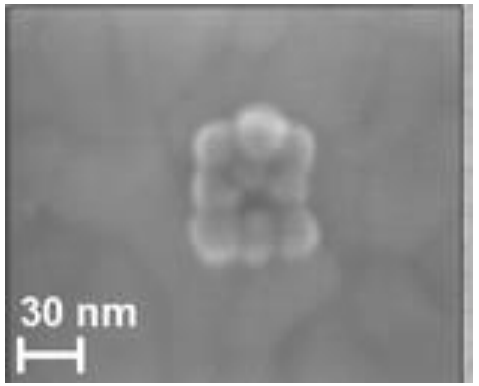




- **Directs a droplet** toward a substrate to form a pattern using many (dots) limiting pattern resolution and fidelity.
- Inherently relies on mechanical accuracy.
- Materials limited to organics and metals

Directed assembly-based printing





- **Directs each nanoparticle** (down to 3nm in size) toward a substrate to form a nanopattern.
- Prints 1000 times faster & smaller patterns than inkjets
- Prints one circuit layer per minute

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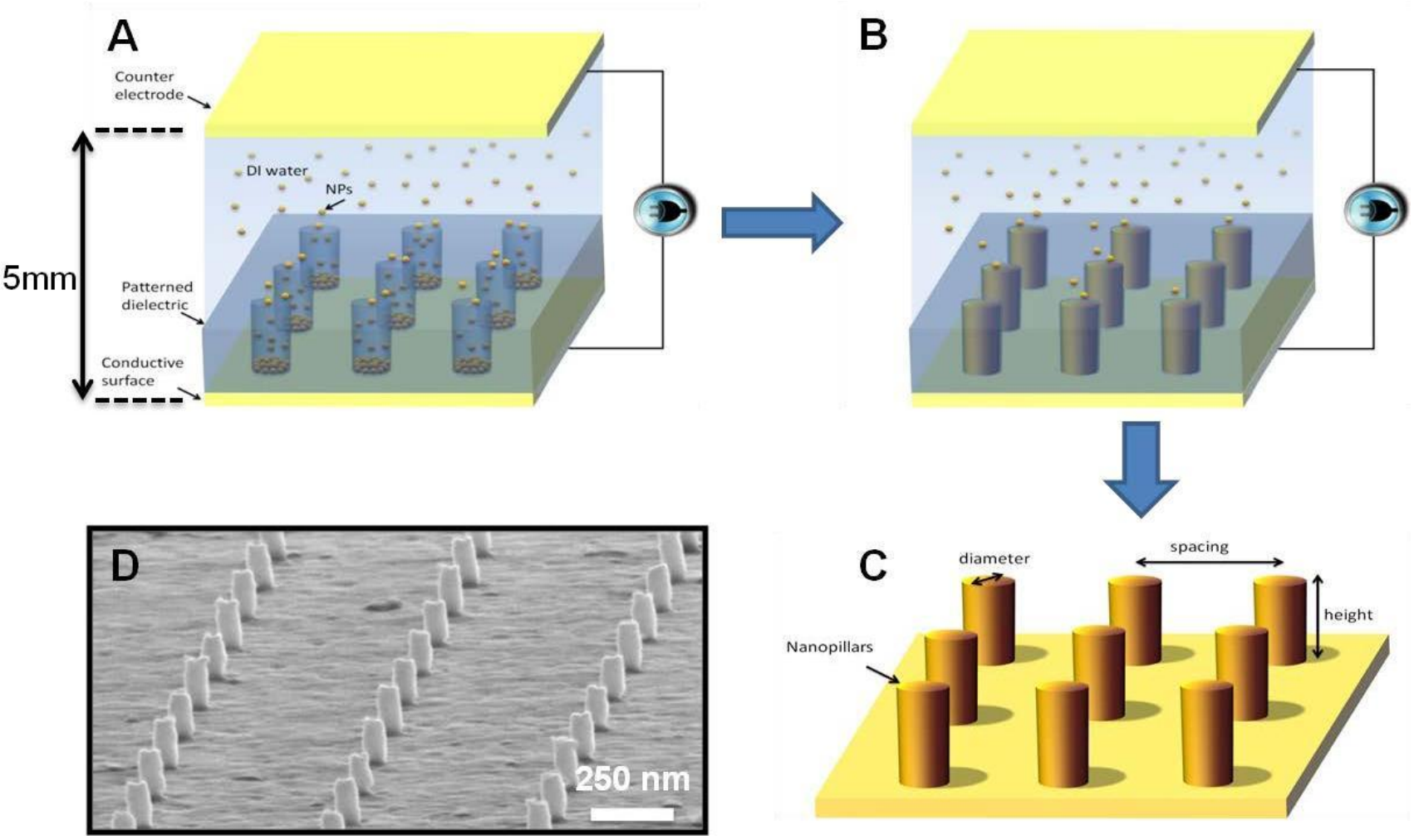
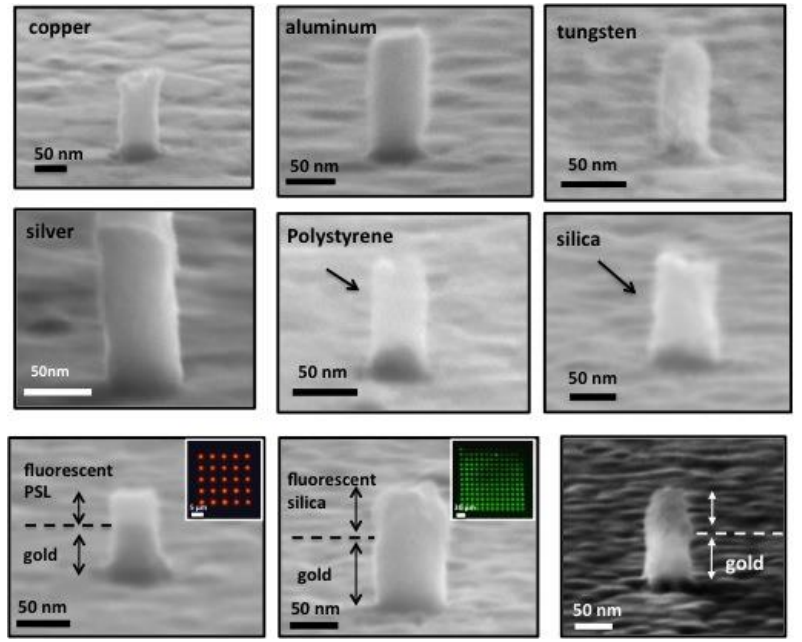
Electrophoretic Directed Assembly– EPx Platform

Assembled Interconnects

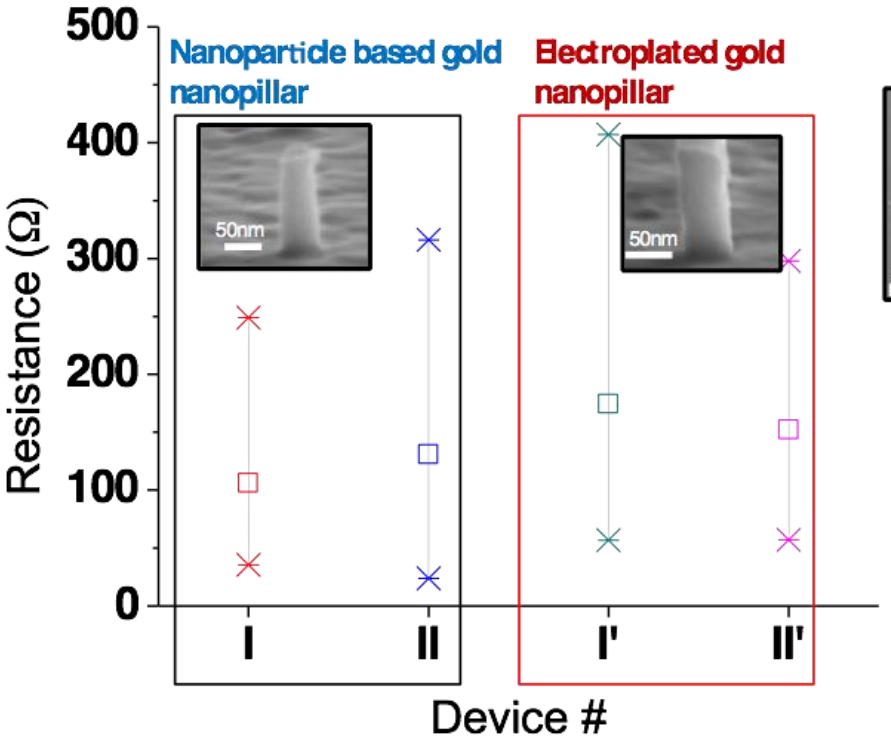


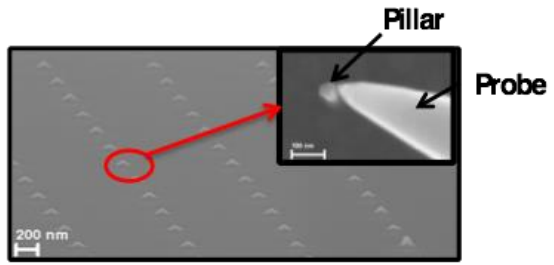


All assembled Nanoparticles are completely fused insitu.

ACS Nano, 8 (5), 2014.

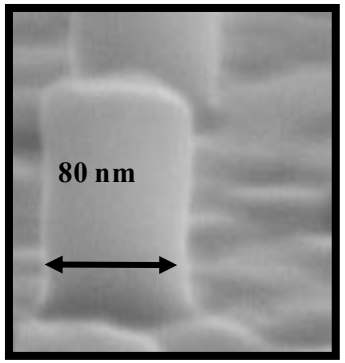
Interconnects Properties

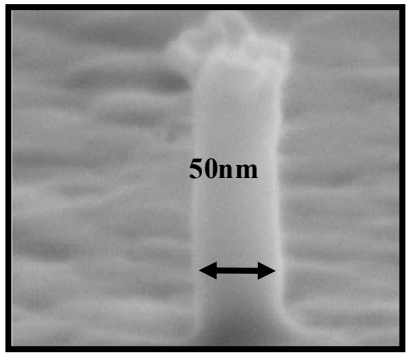


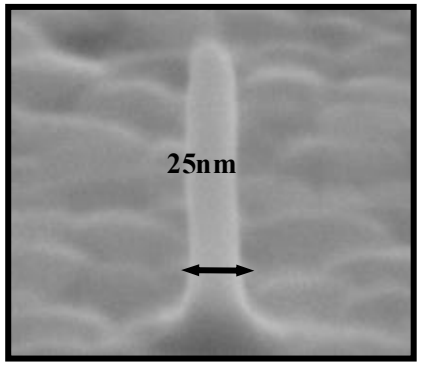


Resistance of assembled interconnects is the same as bulk (electroplated interconnects).

Crystalline Au Pillars





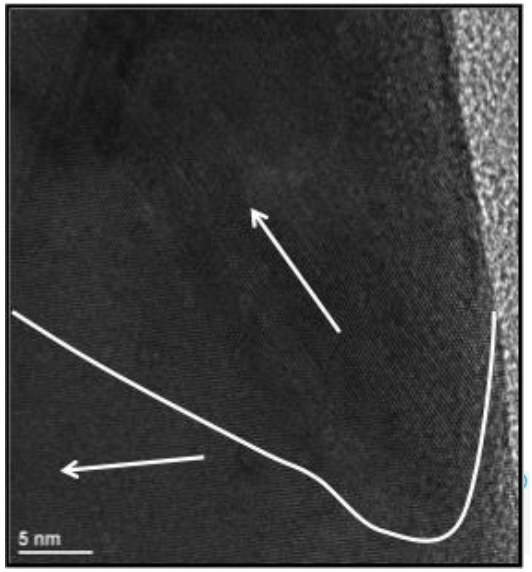


Directly assembled structures properties are equivalent to electroplating, CVD and PVD fabrication.

Directly assembled metallic structures (Cu, Ag, Al, Au, and W, etc.) in addition to semiconductors and dielectrics were demonstrated.

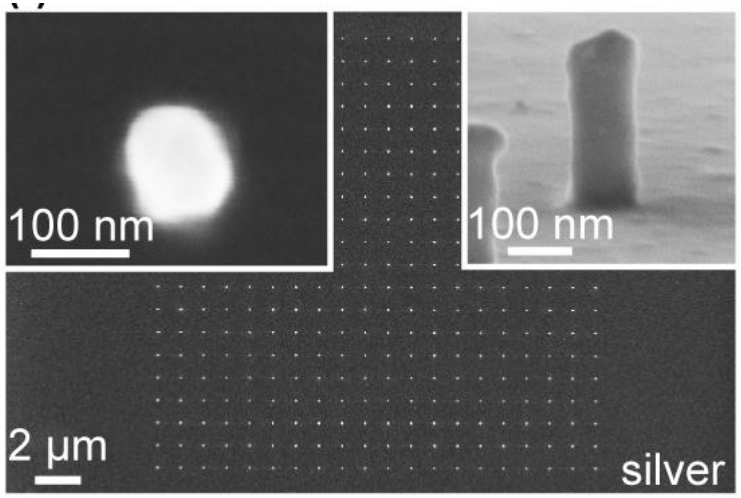
- TEM shows that NPs completely fuse without any voids at room temperature.
- Nanopillars have polycrystalline nature.

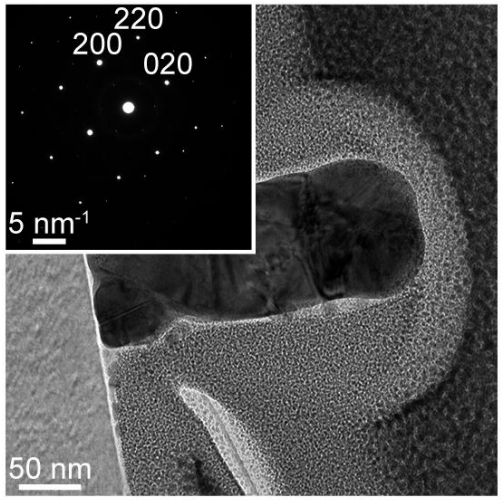
ACS Nano, 8 (5), 2014.

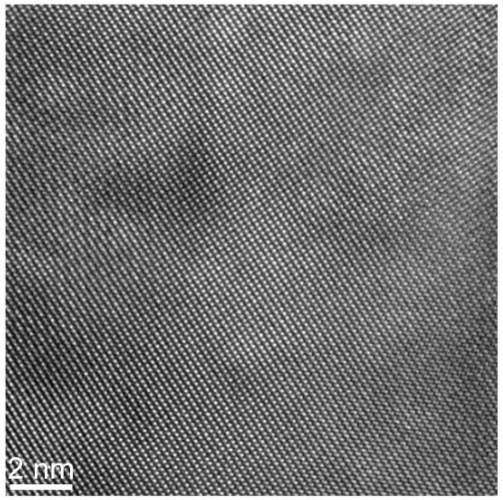


Wafer-scale Additively Manufacturing Single Crystal Semiconductor and Metal

Interfacial convective directed assembly





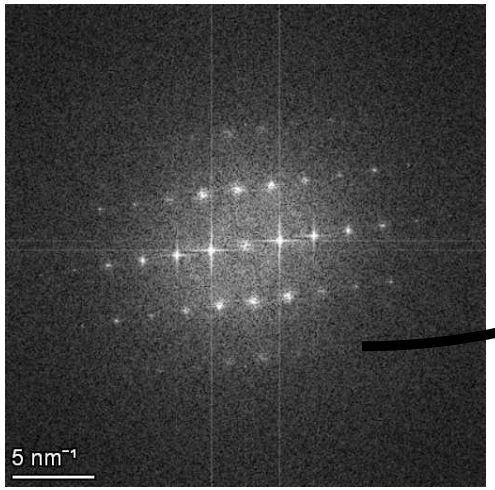


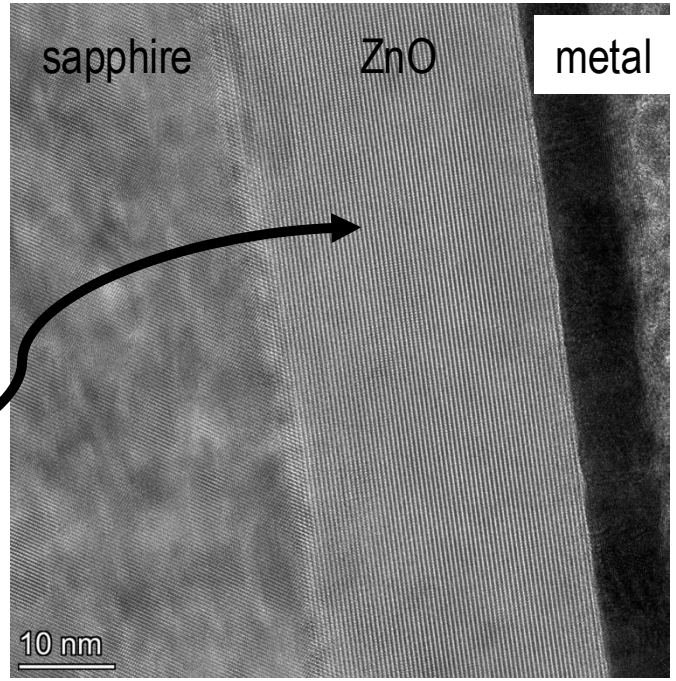
Advanced Materials, 2020.

Room temperature Directed assembly of Ag nanoparticles (5-10 nm) yields single-crystal metal (Ag) nanopillars

Fast Fluidic directed assembly

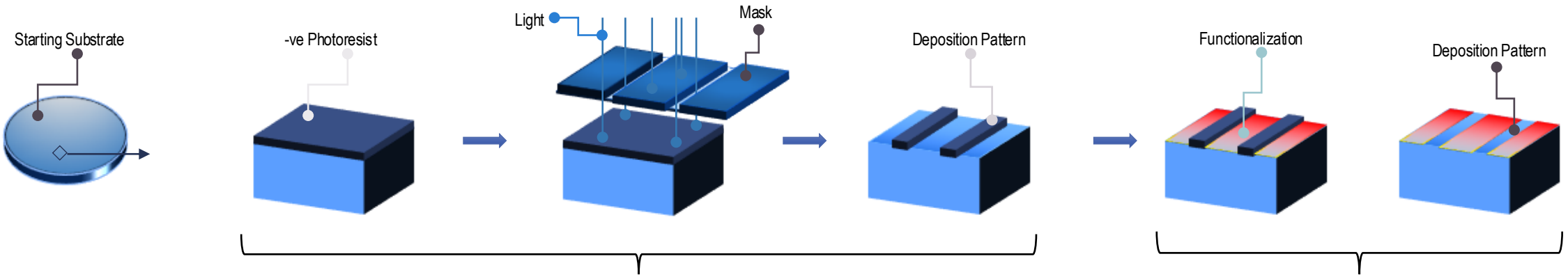
Large area Single Crystal ZnO after sintering of the ZnO nanoparticles

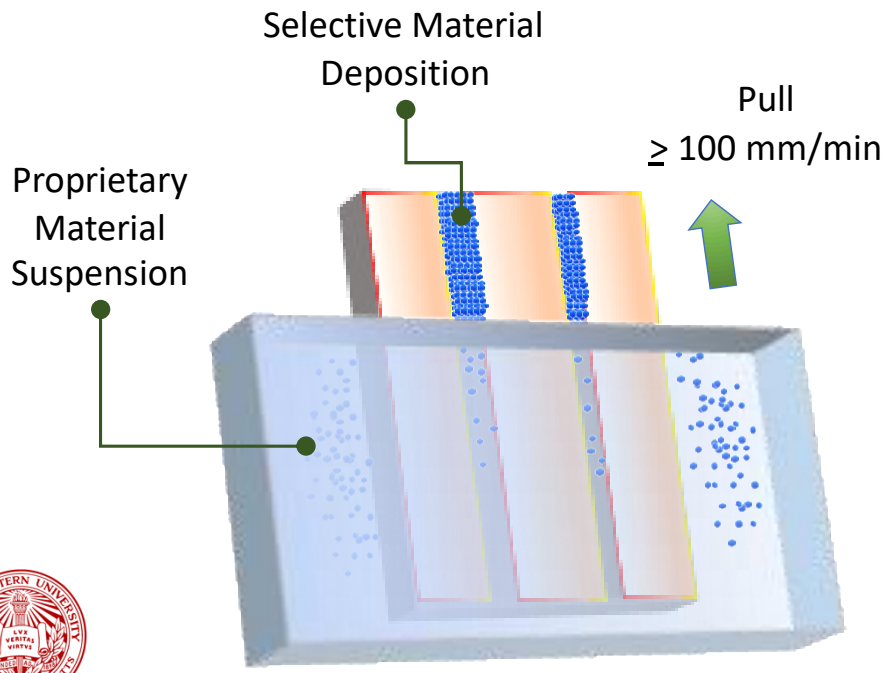




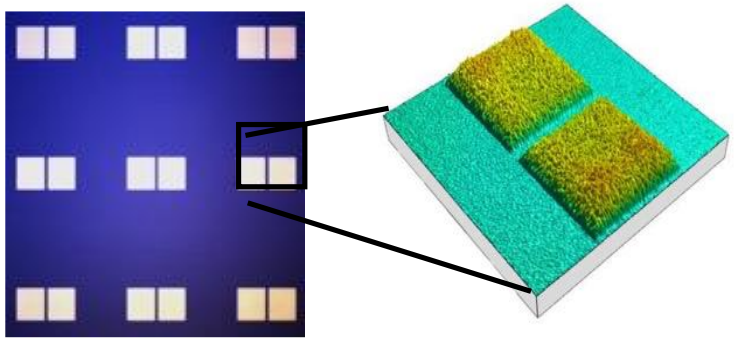
RTP sintering (1000 C for 2 min) of II-VI nanoparticles (50-100 nm) on sapphire yields a single crystal structure throughout.

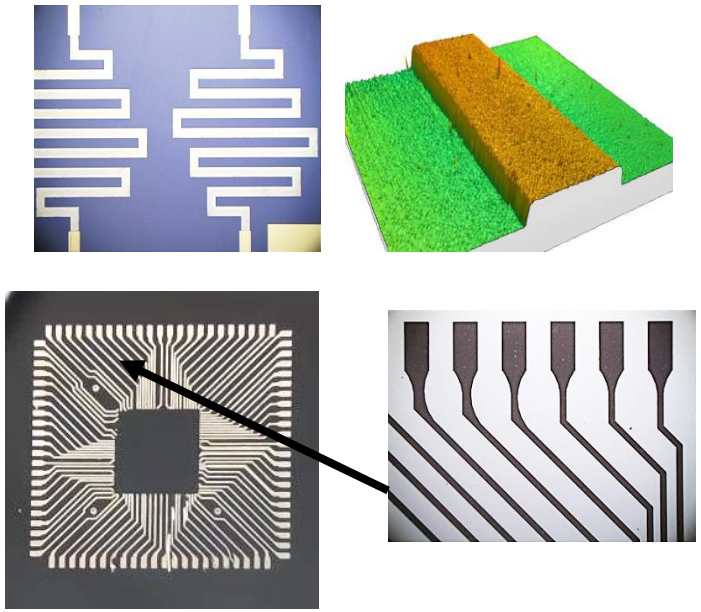
Fast Fluidic Assembly Process– FFx Platform





SiO_2 substrate – 10 µm spacing





Fast Fluidic Assembly Process

What inorganic materials were additively manufactured and utilized?

Material Type	Material	Made nano & micro structures	Sintered at room temp	Sintered at High temp	Devices made & tested
Conductor	silver	yes	yes	yes	passive & active
	copper	yes	yes	yes	passive & active
	gold	yes	yes	yes	passive & active
	platnium	yes	no	yes	passive
	alumnium	yes	yes	no	no
	Tungesten	yes	yes	no	no
Semiconductor	Silicon	yes	yes	yes	active
	ZnO	yes	no	yes	active
	ZnSe	yes	yes	yes	active
	InP	yes	no	yes	no
	GaAs	yes	no	no	no
	GaN	yes	no	no	no
	In2O3	yes	no	yes	active
Dielectric	SiO2	yes	yes	yes	passive & active
	Alumina	yes	yes	yes	passive & active
	HfO2	yes	yes	yes	passive & active
dopants	B+	yes	no	yes	passive & active
	P-	yes	no	yes	passive & active

Room-temperature sintering, yielding single-crystal or polycrystalline structures, requires the assembly of nanoparticles of 5-20 nm.

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Review Article on Directed Assembly for Making Nanoscale Devices

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Review

Directed Assembly of Nanomaterials for Making Nanoscale Devices and Structures: Mechanisms and Applications

Zhimin Chai, Anthony Childress, and Ahmed A. Busnaina*

Cite This: https://doi.org/10.1021/acsnano.2c07910

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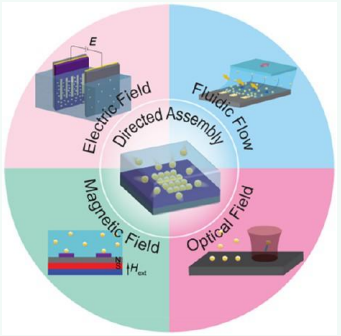
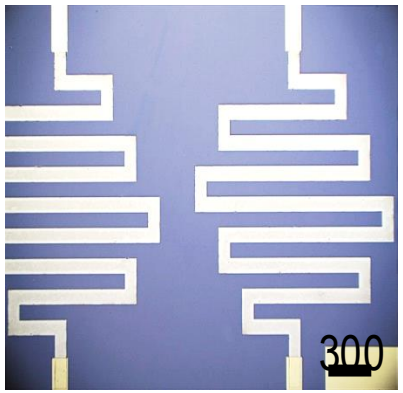
ABSTRACT: Nanofabrication has been utilized to manufacture one-, two-, and three-dimensional functional nanostructures for applications such as electronics, sensors, and photonic devices. Although conventional silicon-based nanofabrication (top-down approach) has developed into a technique with extremely high precision and integration density, nanofabrication based on directed assembly (bottom-up approach) is attracting more interest recently owing to its low cost and the advantages of additive manufacturing. Directed assembly is a process that utilizes external fields to directly interact with nanoelements (nanoparticles, 2D nanomaterials, nanotubes, nanowires, etc.) and drive the nanoelements to site-selectively assemble in patterned areas on substrates to form functional structures. Directed assembly processes can be divided into four different categories depending on the external fields: electric field-directed assembly, fluidic flow-directed assembly, magnetic field-directed assembly, and optical field-directed assembly. In this review, we summarize recent progress utilizing these four processes and address how these directed assembly processes harness the external fields, the underlying mechanism of how the external fields interact with the nanoelements, and the advantages and drawbacks of utilizing each method. Finally, we discuss applications made using directed assembly and provide a perspective on the future developments and challenges.

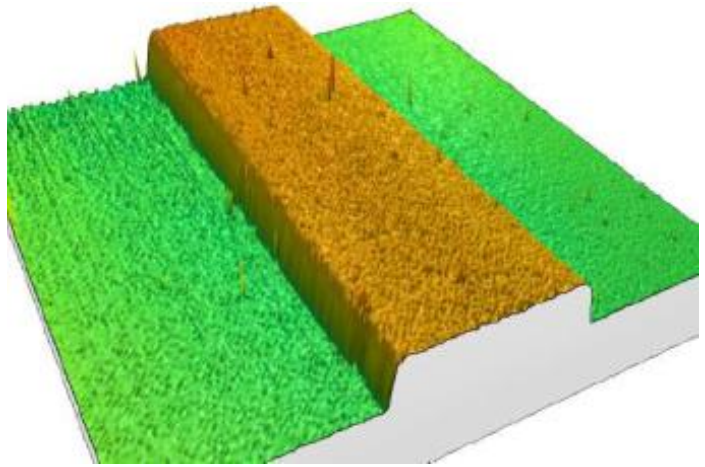


KEYWORDS: *directed assembly, bottom-up fabrication, nanomaterials, nanotechnology, nanoelectronics, microelectronics, electrophoresis, dielectrophoresis, magnetophoresis, fluidic assembly*

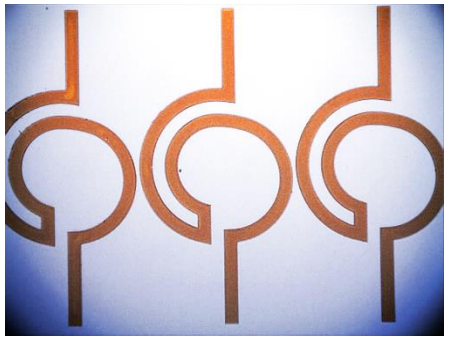
Additively Manufactured Metal Resistors

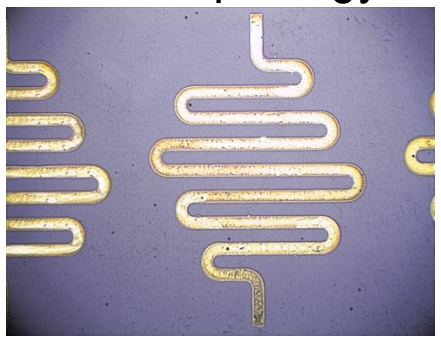
- Confocal microscope measurements show an average platinum thickness of 250 nm after sintering.

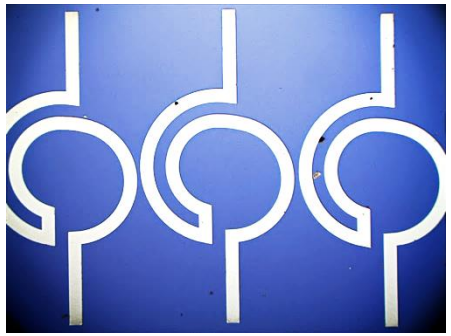


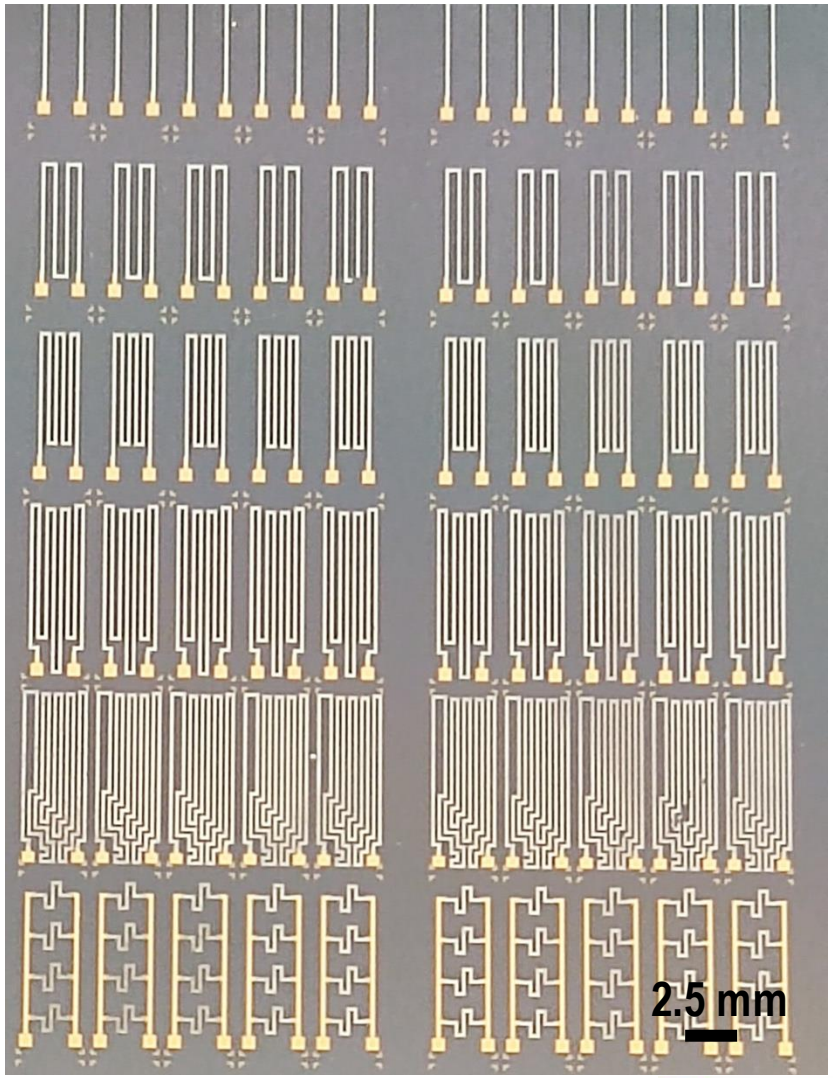


The printed Platinum shows uniform and homogeneous surface morphology.


Copper


Gold


Platinum



50 Ω

100 Ω

250 Ω

550 Ω

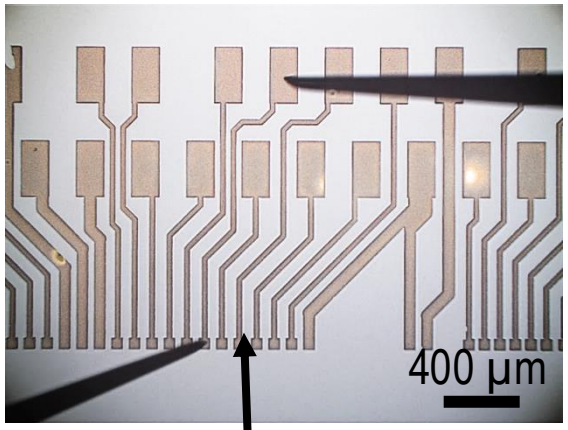
800 Ω

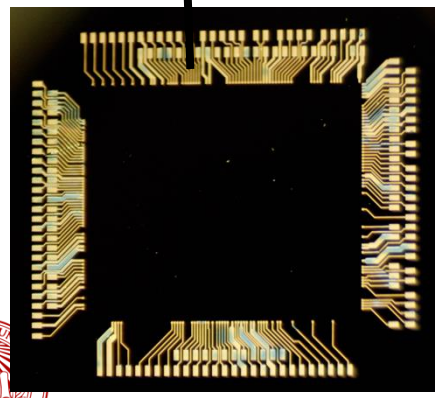
30 Ω

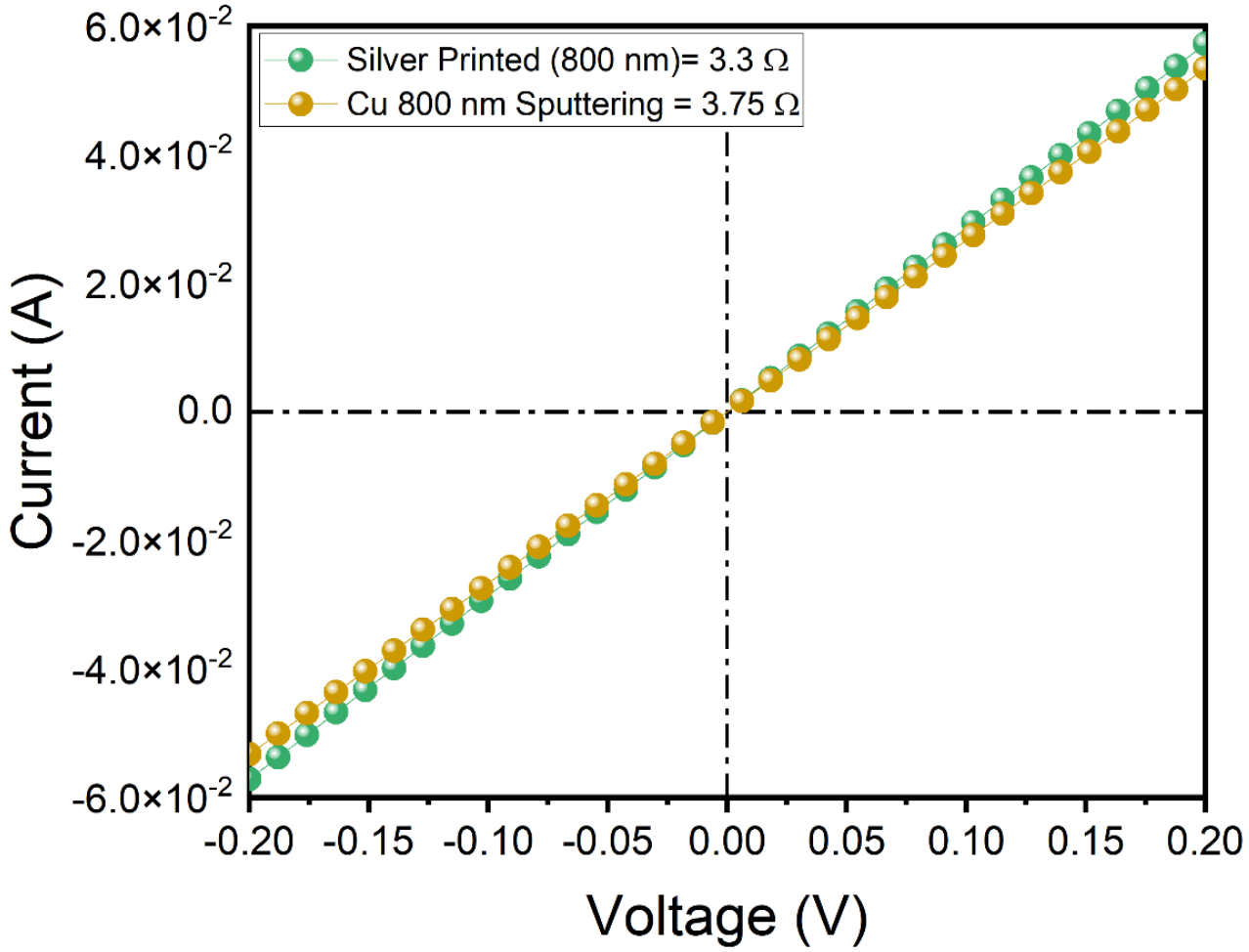
Additively Manufactured Silver vs Sputtered Copper

- Fan out Flip chip pattern was made using silver (internal pads < 40 microns)
- The trace's conductivity is equivalent to sputtered copper at the same thickness.

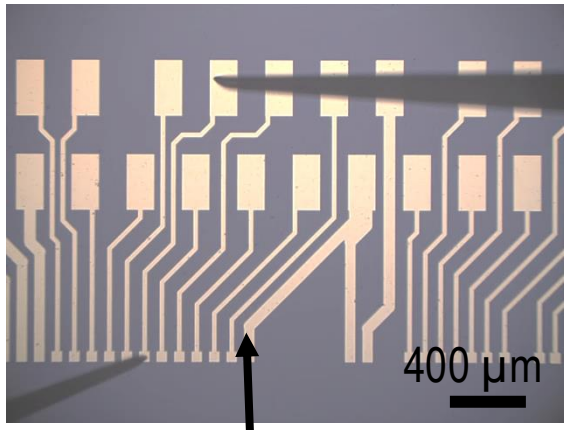
Silver

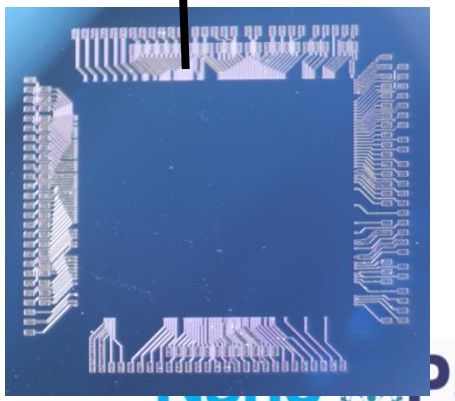






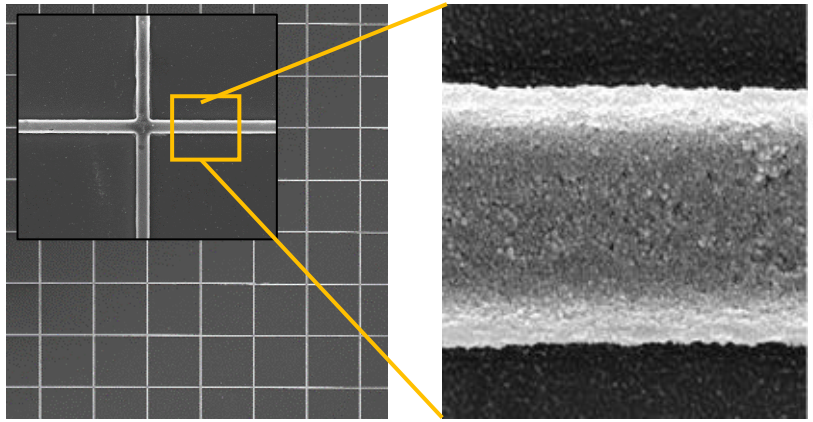
Copper (sputtered)

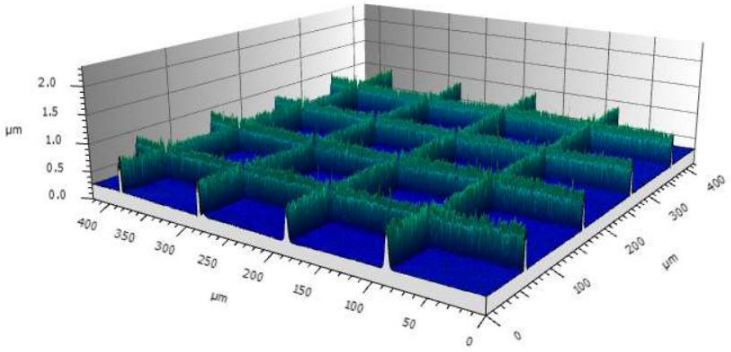




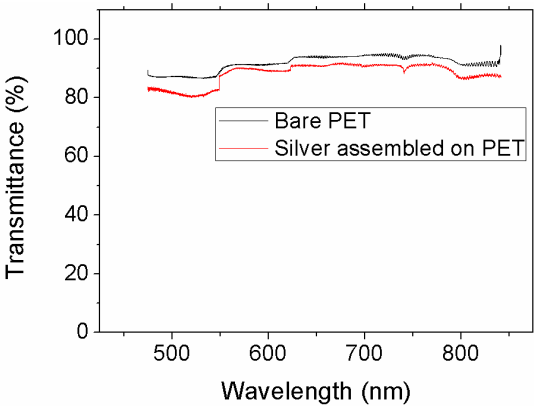
Additively Manufactured Touch Display at the Micro and Nanoscale

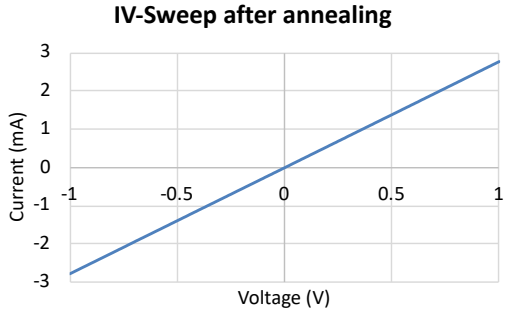
Ag grids for touch display applications

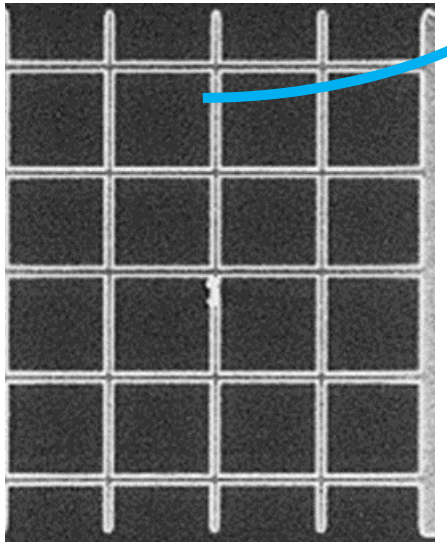




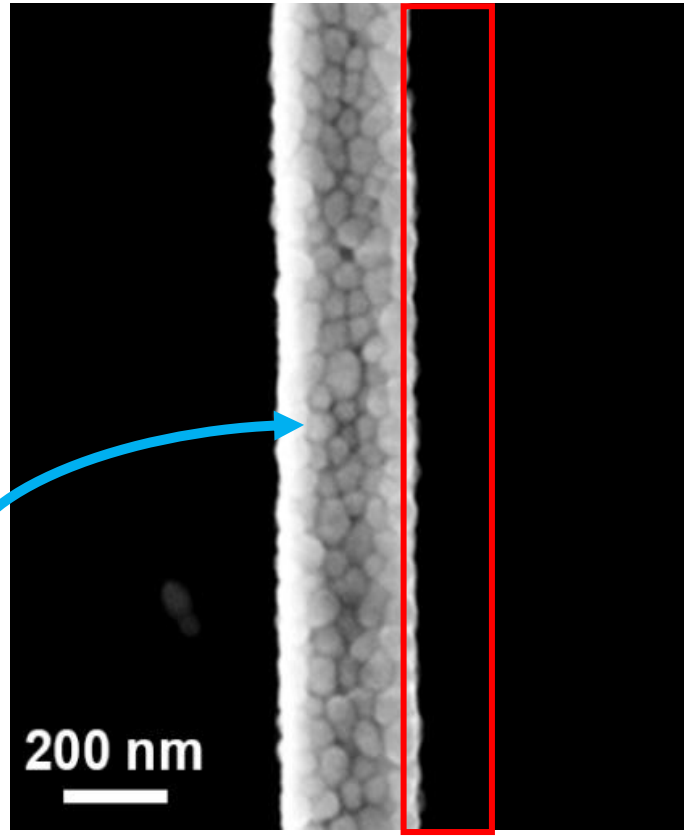
Line width 2 um







Line width 300 nm



Excellent Line edge roughness
3.7 nm
Using large nanoparticles

COMMUNICATION

Transparent Electrodes

ADVANCED MATERIALS INTERFACES
www.advmatinterfaces.de

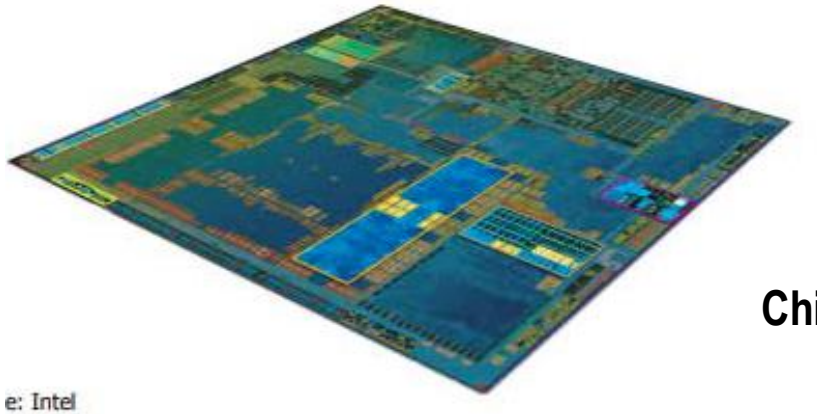
Scalable Printing of High-Resolution Flexible Transparent Grid Electrodes Using Directed Assembly of Silver Nanoparticles

*Salman A. Abbasi, Zhimin Chai, and Ahmed Busnaina**

NanoOPS©

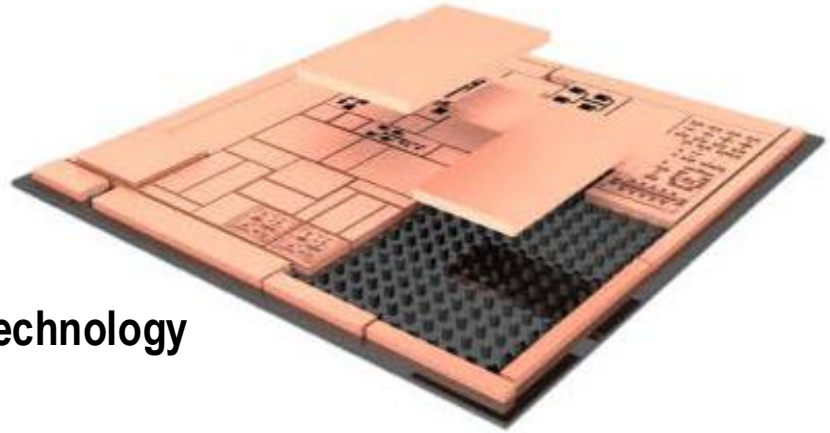
Advanced Packaging for Heterogeneous Integration
for chiplet technology for integrating multiple dies in a package or system

Today – Monolithic



e: Intel

Tomorrow – Modular

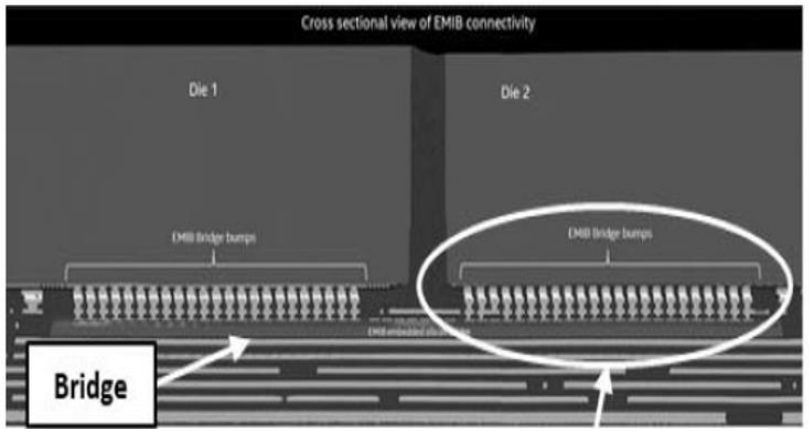


Chiplet Technology

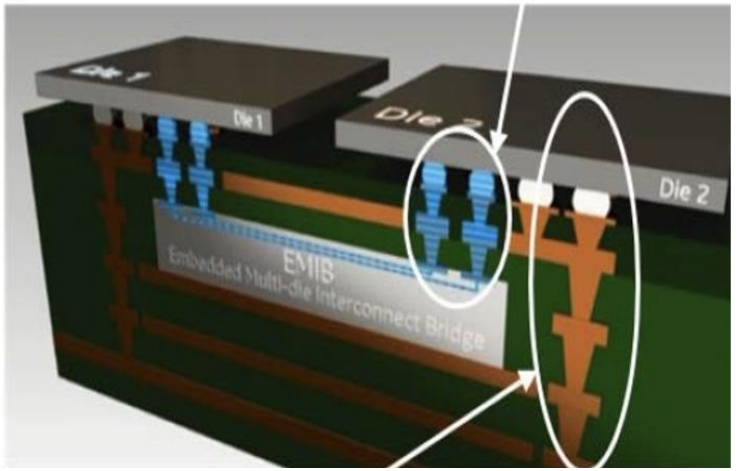
- **Conventional packaging approaches can not meet the resolution and density requirements with feature size and pitch at 2 microns or less.**
- **Currently, It can only be done at conventional fabs now.**

Additively Manufactured EMIB-Like Structures

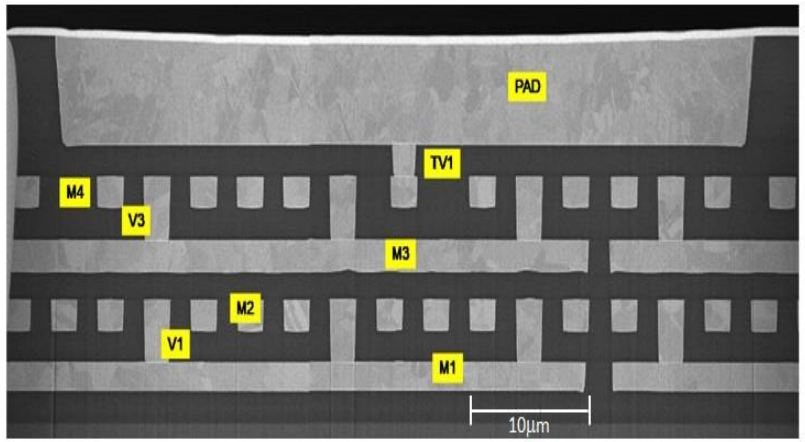
- Intel's Embedded Multi-die Interconnected Bridge (EMIB) is an advanced chip packaging technique connects multiple heterogeneous dies or chiplets within a single package.
  - More compact than a large silicon interposer



Localized Fine Pitch Interconnects used for die-to-die interconnects

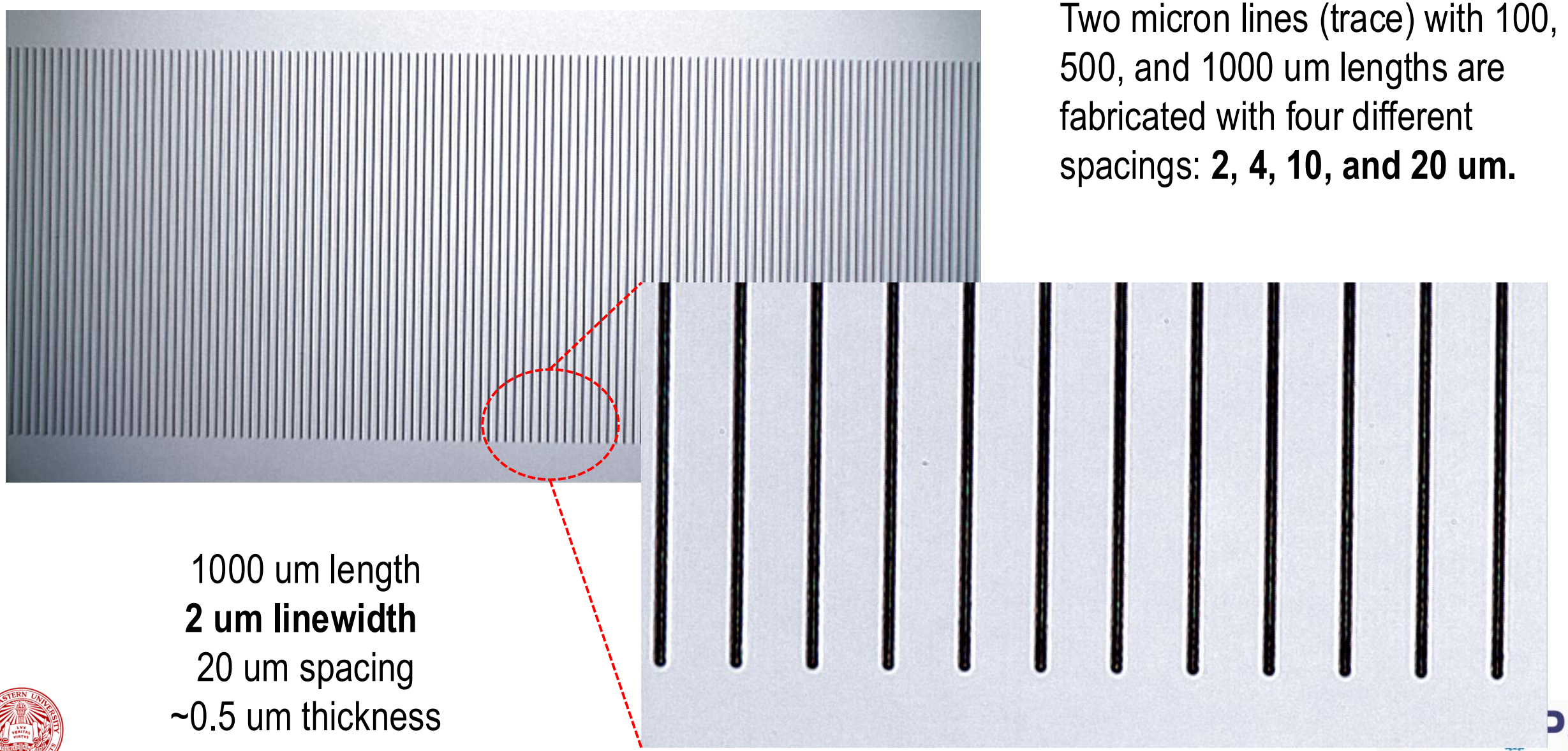


Package interconnects outside of the bridge region are unaffected



Bridge Cross-Section showing 4 Metal layers with 2 µm Lines/Spaces/vias.

Additively Manufactured EMIB-Like Structures

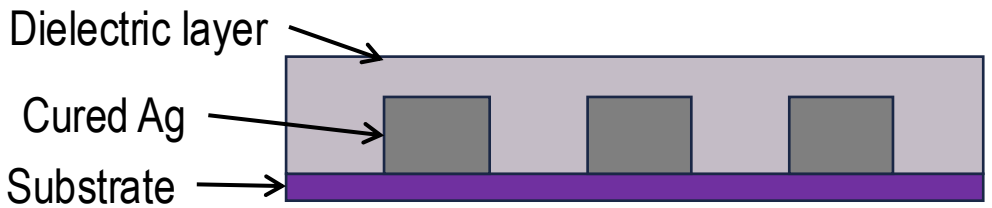


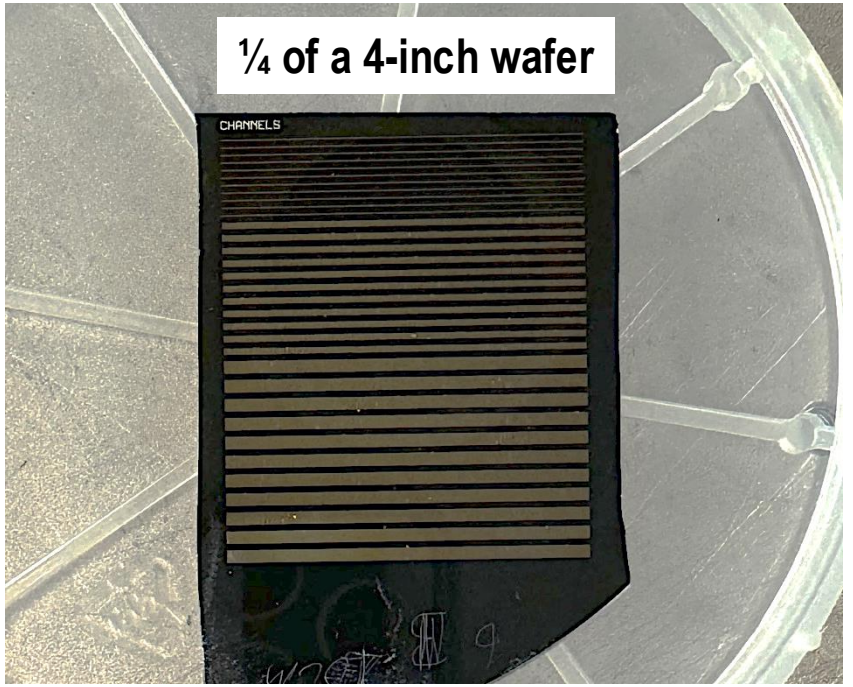
Two micron lines (trace) with 100, 500, and 1000 um lengths are fabricated with four different spacings: **2, 4, 10, and 20 um.**

1000 um length
2 um linewidth
20 um spacing
~0.5 um thickness

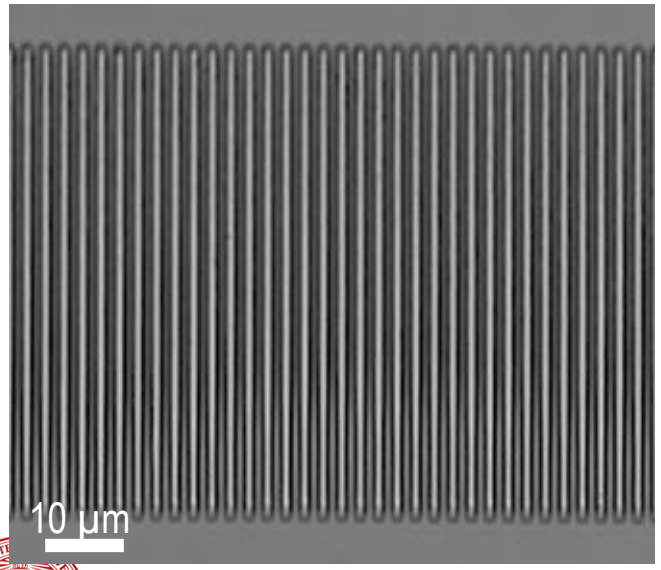
Additively Manufactured EMIB-Like Structures

- **Printed pitch: 4, 7, 12, and 22 µm**
- The width of each line is 2 µm
- Three-different lengths: 100, 500, & 1000 µm

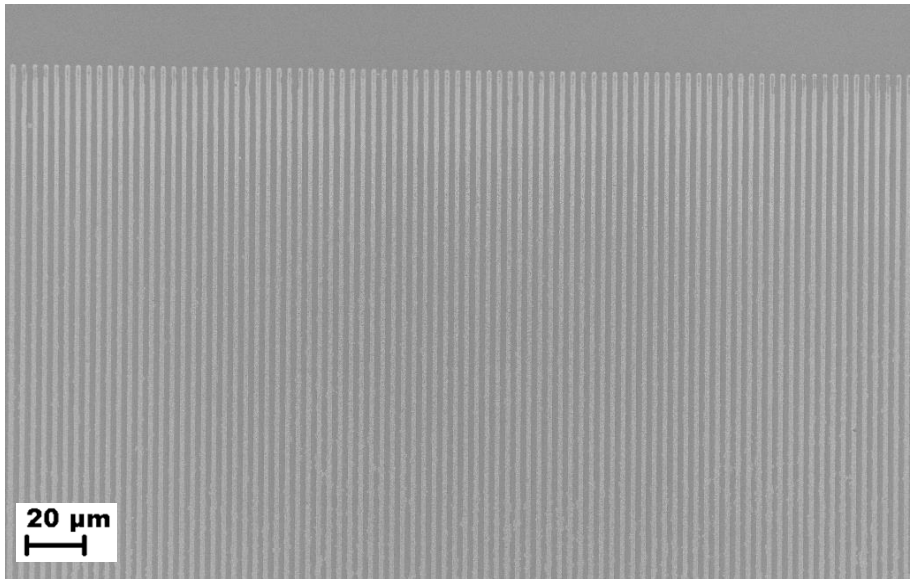




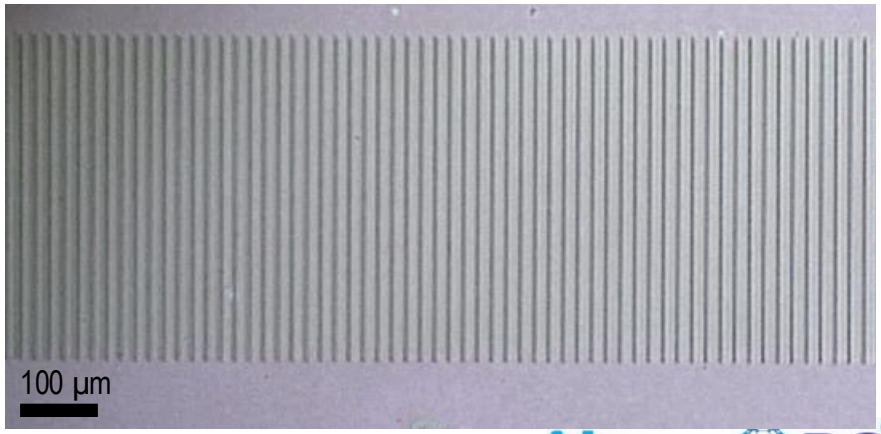
50 length-to-width aspect ratio



500 length-to-width aspect ratio with **4 µm pitch**

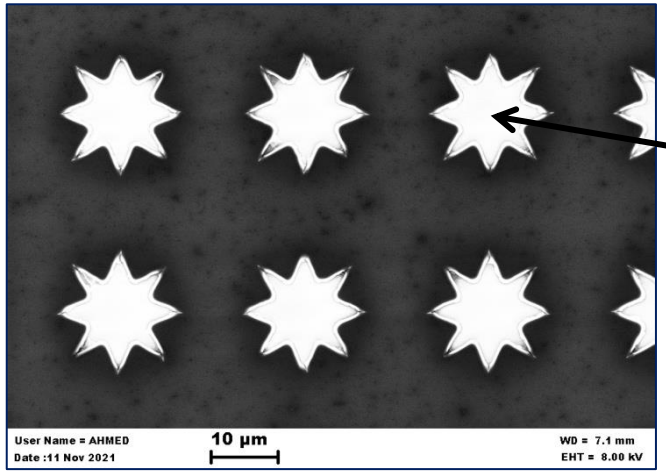


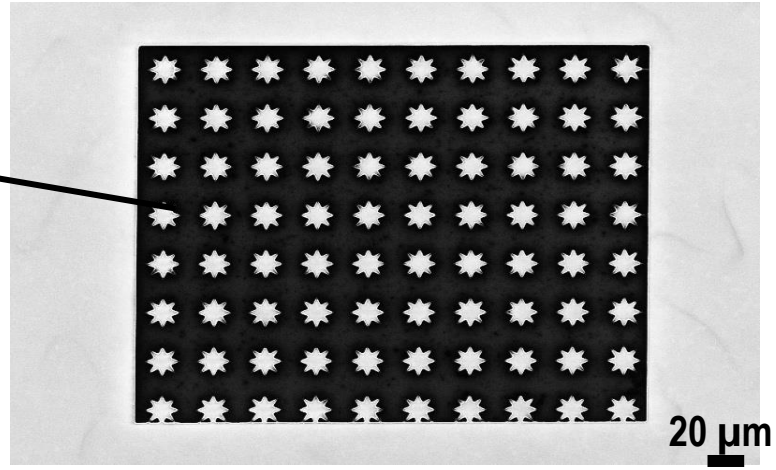
250 length-to-width aspect ratio



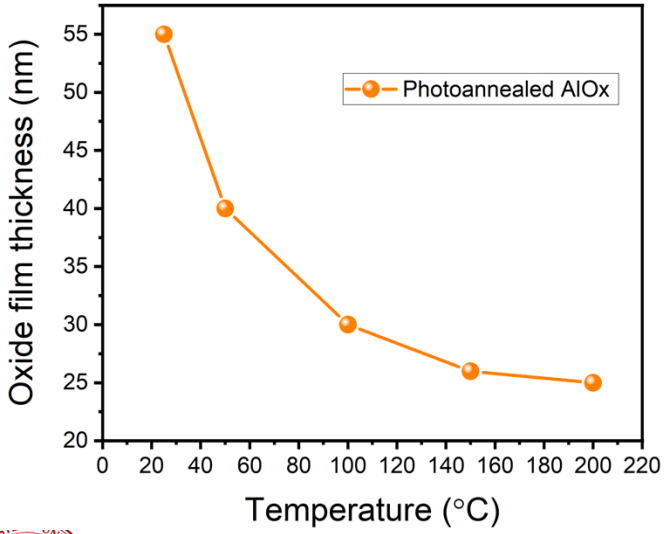
Additively Manufactured Dielectrics

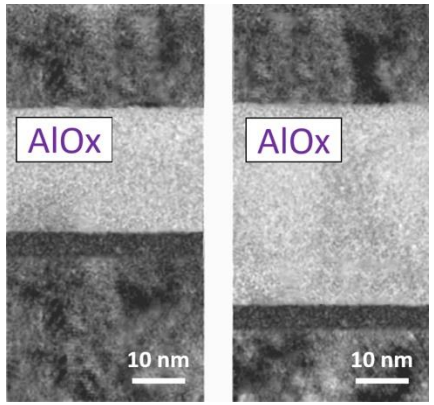
The SEM images below shows Al_2O_3 micropatterns prepared by directed fluidic assembly with a dielectric constant that matches that obtained by CVD or ALD ($\varepsilon_d = 7.2$).

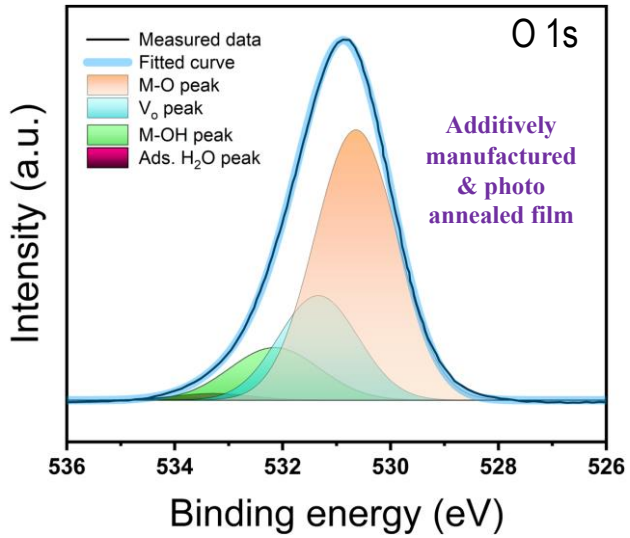


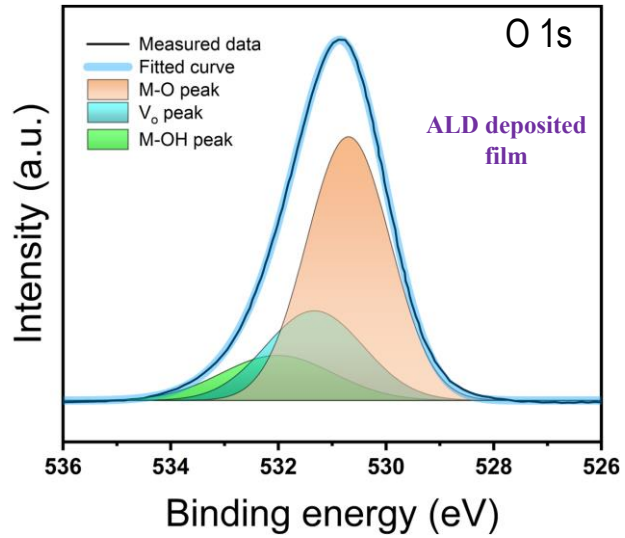


X-ray Photoelectron Spectroscopy (XPS) characterization of the Dielectric Layer shows agreement in between ALD and printed films in terms of peak intensities and composition ratios.



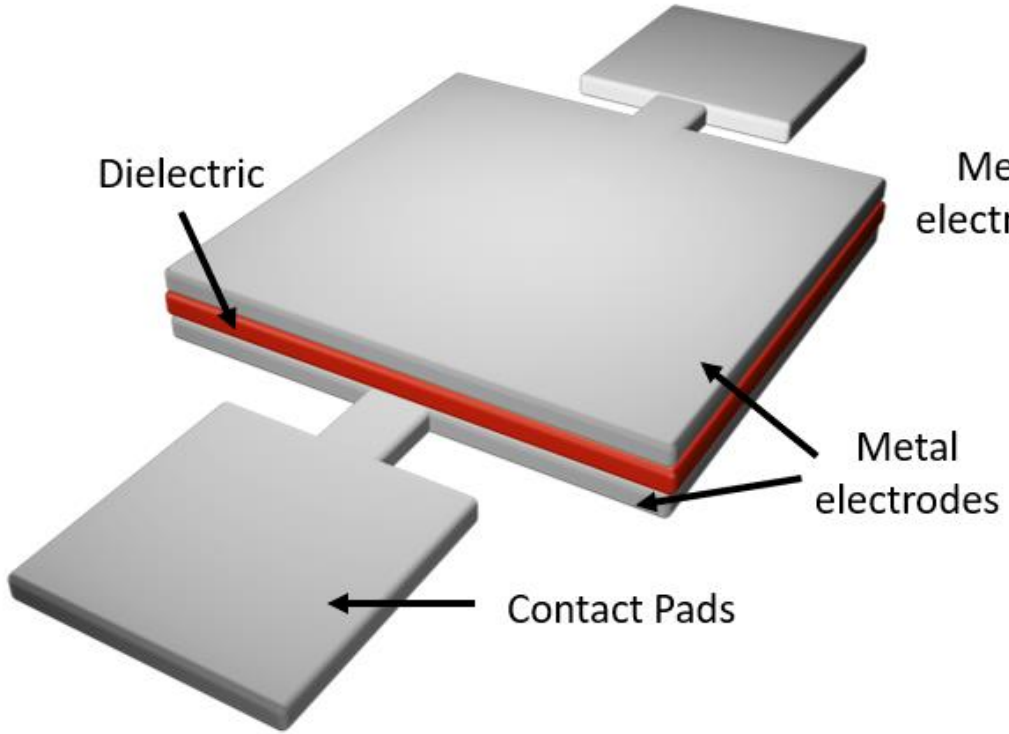


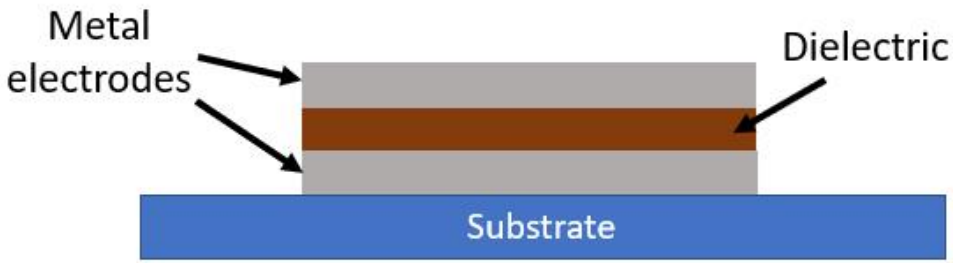


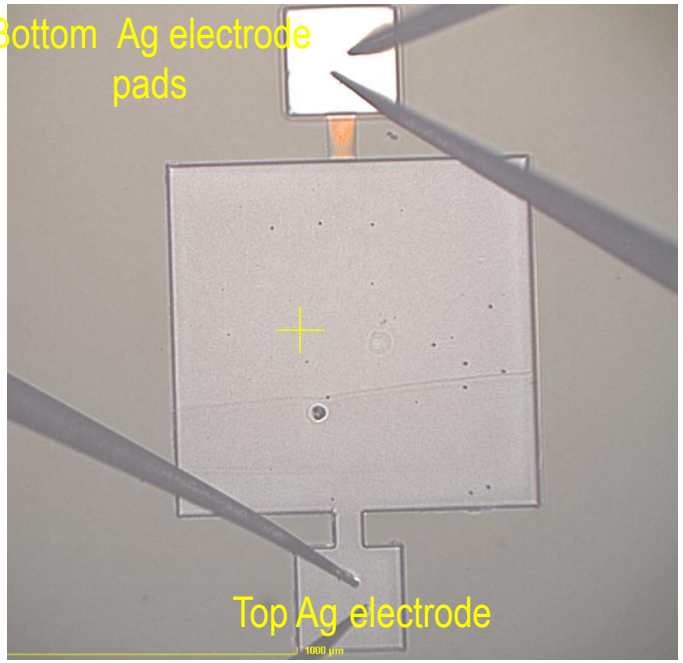


- Higher temperature densification and better dielectric properties for the film.
- Cross-sectional shows the oxide film thickness variation between 50 °C and 200 °C annealing.

Additive Manufacturing of Capacitors



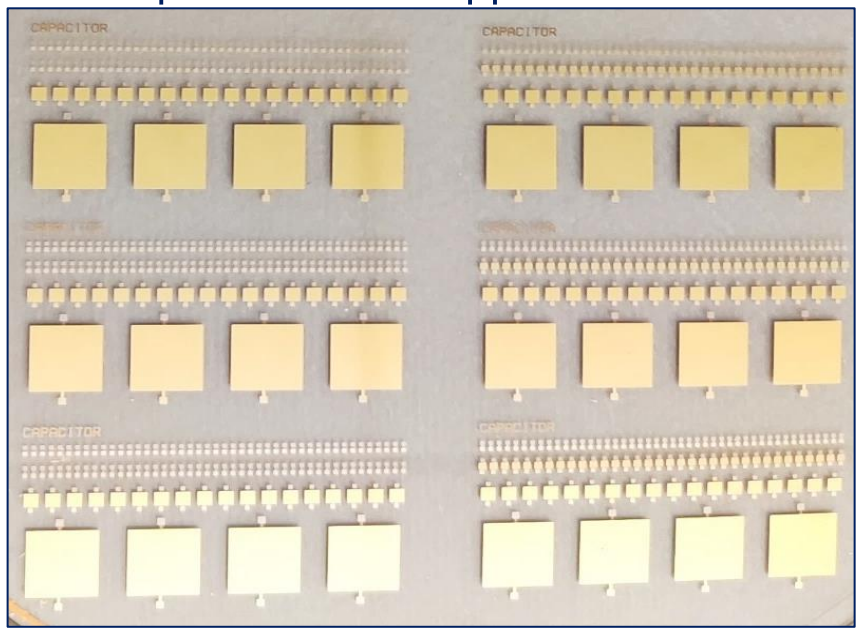




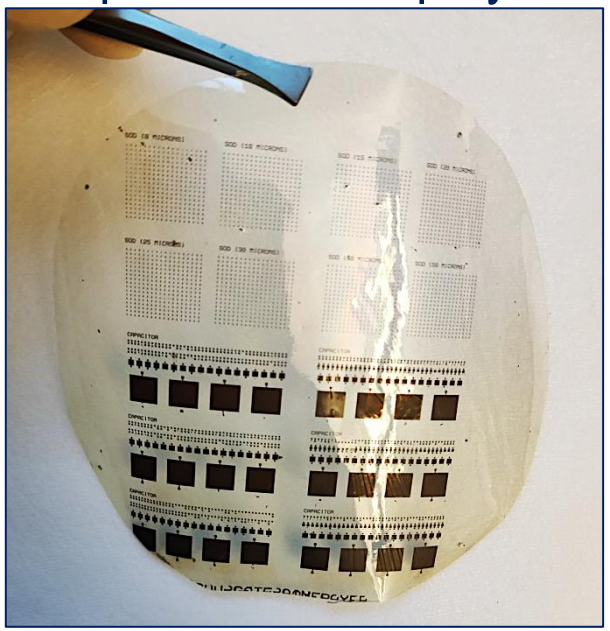
Additively Manufactured Capacitors on Rigid and Flexible Substrates

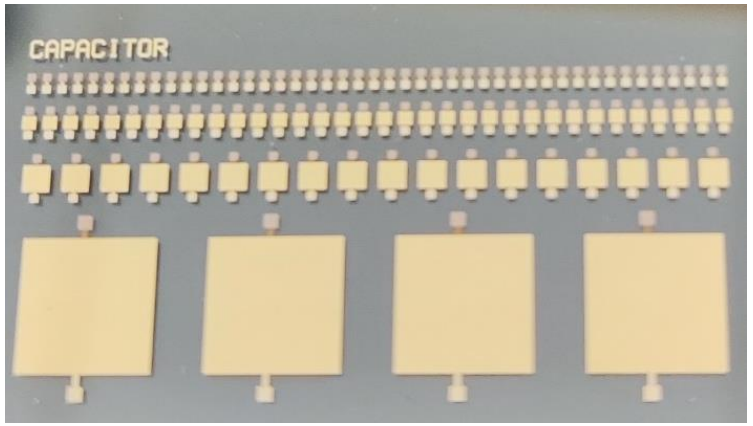
- Large-scale fabricated capacitors with a dielectric layer onto sapphire or polymer substrates.
- Each substrate has 640 capacitors with different surface areas of side lengths 20, 50, 100, 500, 1000, and 5000 µm.
- Metal: **Silver**
- Dielectrics: **Al_2O_3, SiO_2, HfO_2**

Capacitors on a sapphire substrate

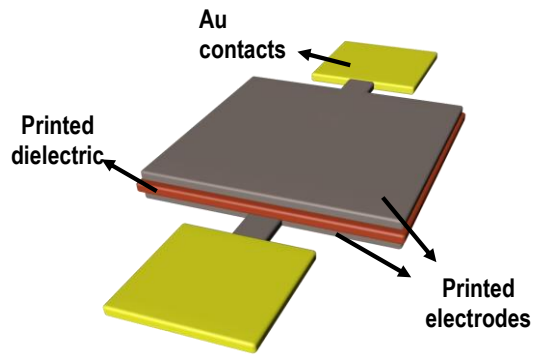


Capacitors on a polymer





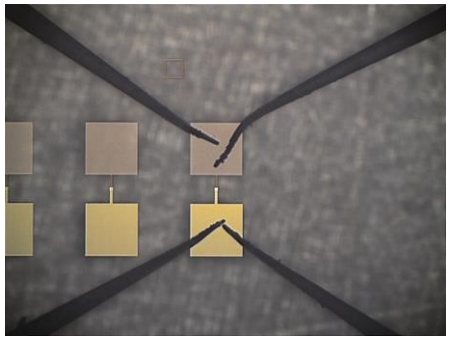
Capacitors on silicon



NanoOPS©

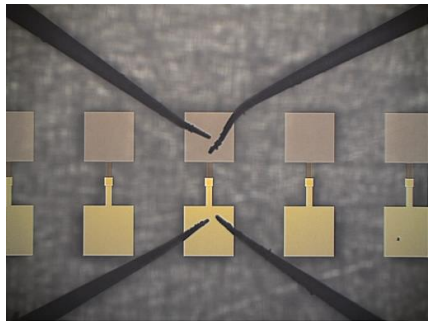
Characterization of Additively Manufactured Capacitors

- For high-frequency applications, the capacitors need to show reliable performance under high frequency.
- The curve shows the capacitance variation versus different frequencies up to 1 MHz.



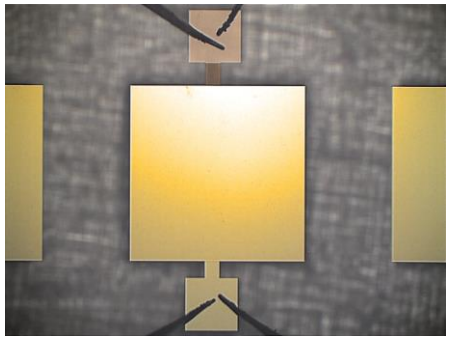
20x20 µm

C= 857 fF



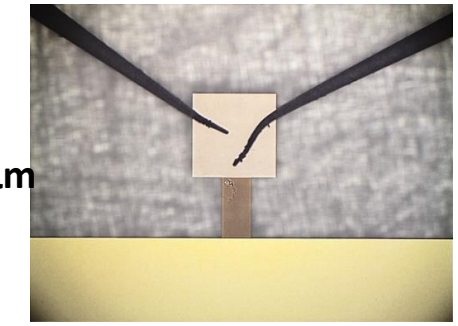
50x50 µm

C= 4.3 pF



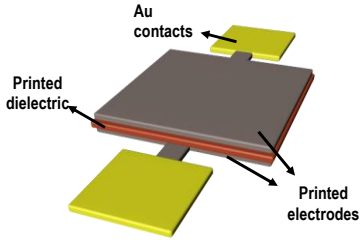
1000x1000 µm

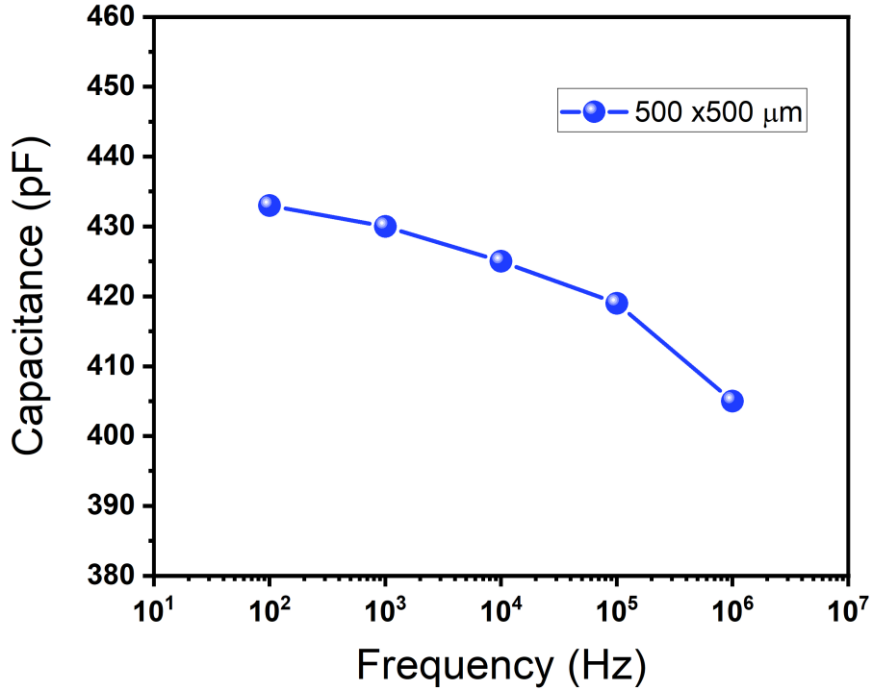
C= 1.6 nF

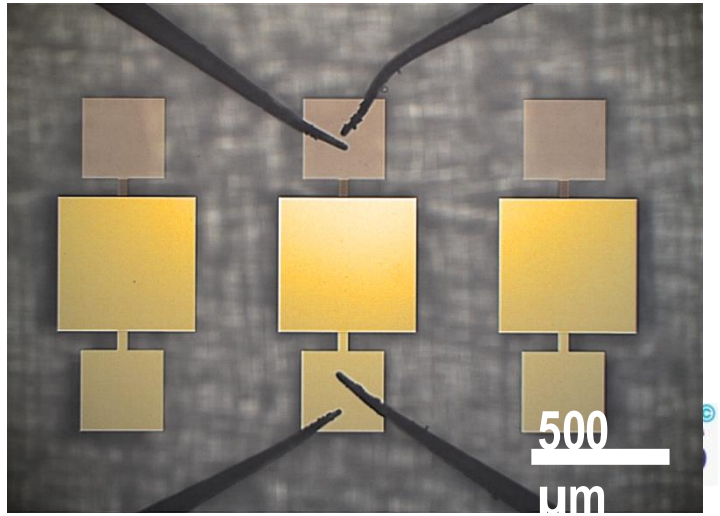


5000x5000 µm

C= 5.68 nF





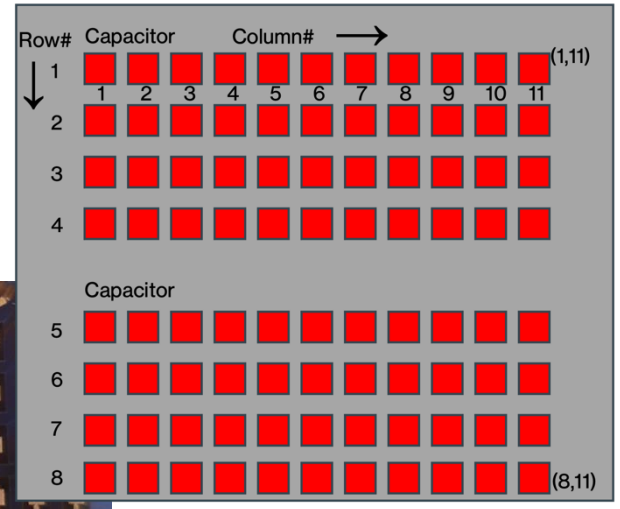


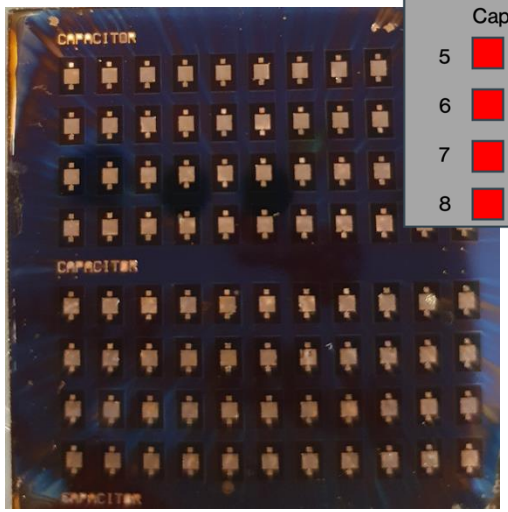
Characterization of Additively Manufactured Capacitors

Section	Row	Column	Capacitance(F)	Dissipation Factor
Left, Top	1	1	2.40E-11	0.029166
	1	2	2.40E-11	0.027735
	2	1	2.43E-11	0.029309
	2	2	2.36E-11	0.029016
Left, Bottom	7	1	2.51E-11	0.033264
	7	2	2.40E-11	0.030501
	7	3	2.40E-11	0.035232
	8	1	2.79E-11	0.130963
Right, Top	1	10	2.39E-11	0.026566
	1	11	2.39E-11	0.027482
	2	10	2.36E-11	0.026815
	2	11	2.38E-11	0.029224
Right, Bottom	7	10	2.39E-11	0.030106
	7	11	2.43E-11	0.029147
	8	10	2.46E-11	0.029886
	8	11	2.92E-11	0.038304
Center	4	5	2.26E-11	0.031084
	4	7	1.66E-11	0.033057
	5	5	2.24E-11	0.03135
	5	6	2.30E-11	0.031123

88 capacitors in the shown sample were characterized at 1 kHz frequency. **The average capacitance is 2.39×10^{-11} F with a standard deviation of 2.35×10^{-12} F and a low dissipation factor of an average of 0.0354665.**

Yield = 100%





Reliability of Additively Manufactured Capacitors

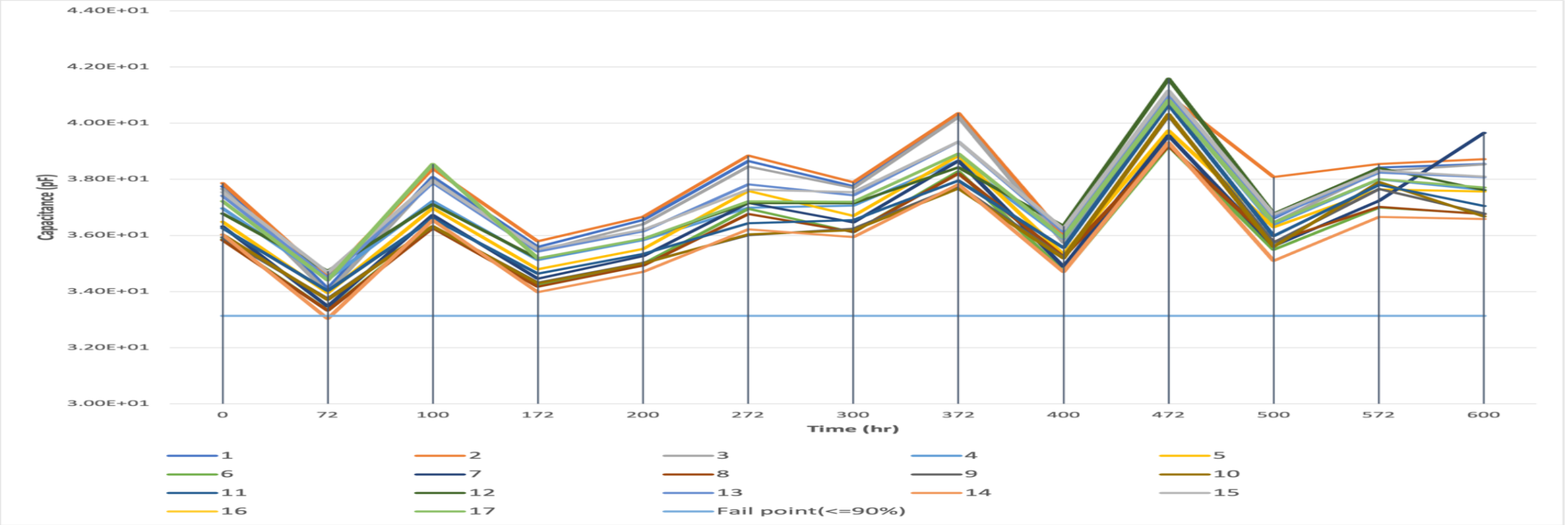
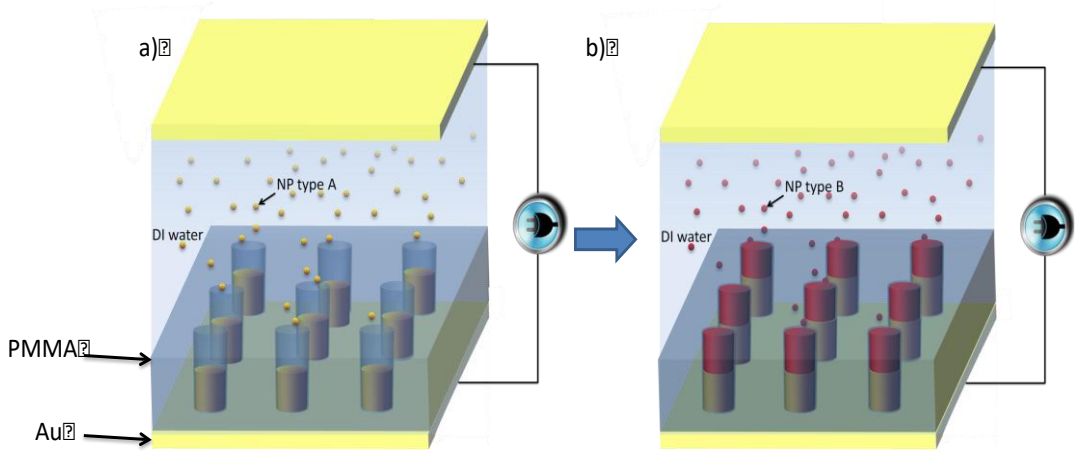
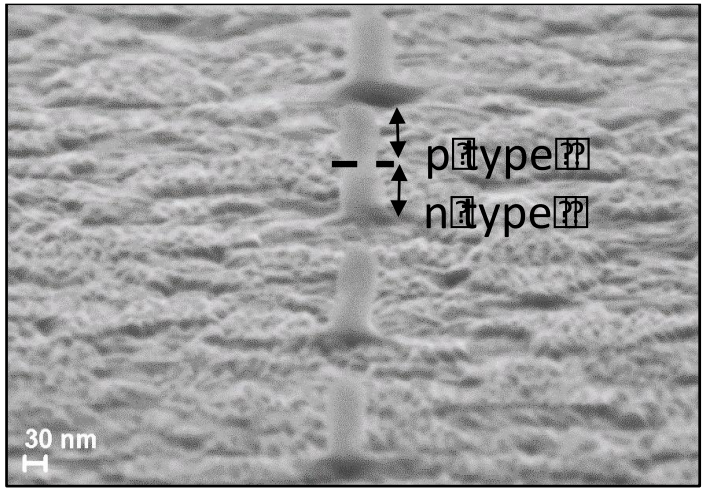


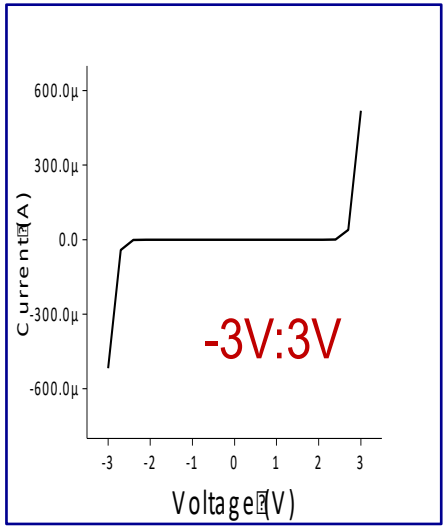
Figure 19D summarizes the capacitance and dissipation factor reliability data at 125°C after 72, 100, 172, 200, 272, 300, 372, 400, 472, 500, 572, and 600 hours. A capacitor is considered failed when the capacitance decreases to 90% or lower of the initial capacitance. The results show that none of the additively manufactured capacitors using a polymer dielectric failed when heated to 125C which is typically higher than typical testing temperatures for capacitance with organic polymers.

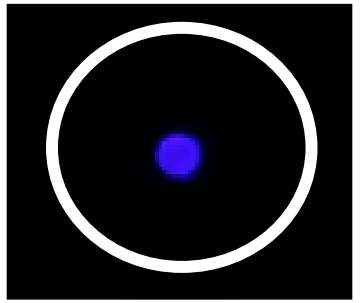
Printed Nano LEDs

Printed 50 nm diodes (P-N junctions) using directed assembly-based printing





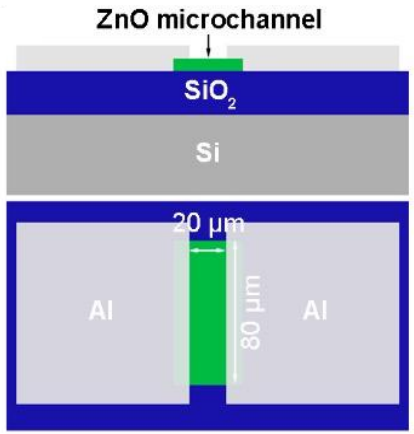


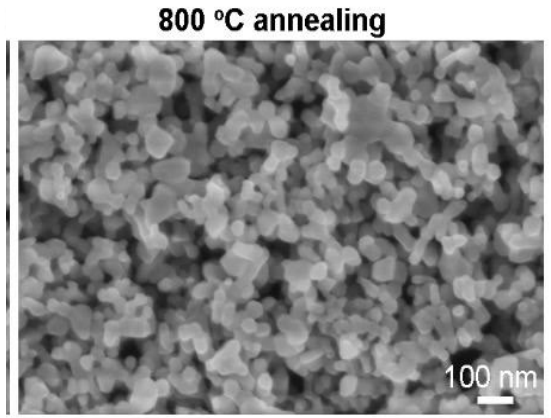


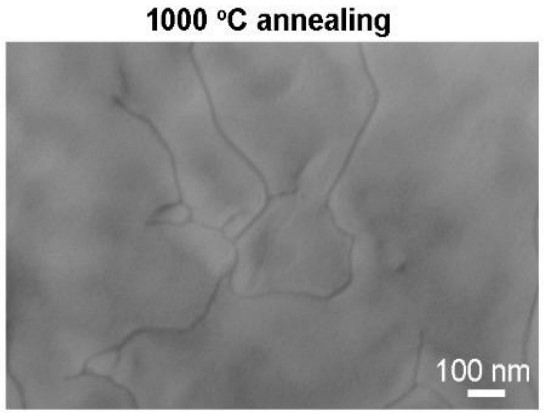
Printing N-doped and P-doped II-VI semiconducting particles that are self annealed insitu during the directed assembly-printing process to yield printed blue LEDs.

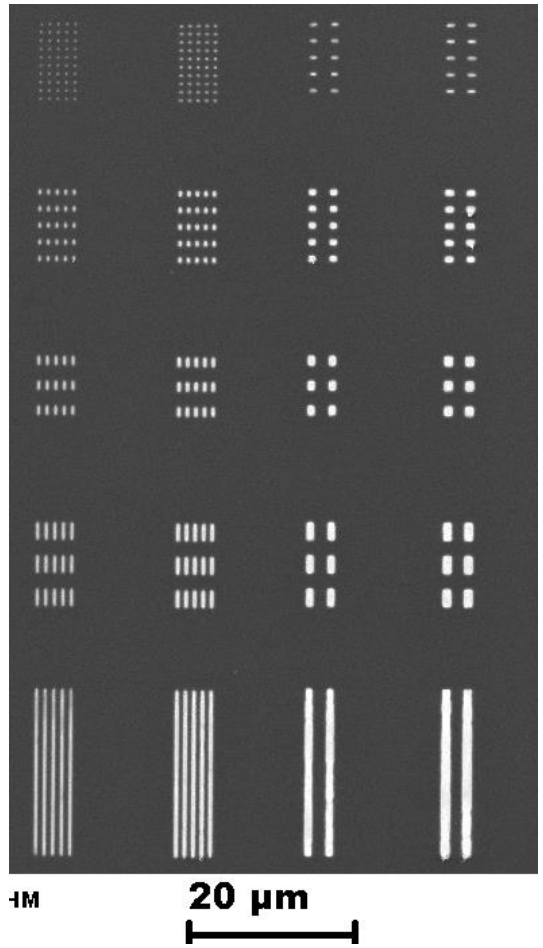
Color	Wavelength (nm)	Voltage (ΔV)
Blue	450 < λ < 500	2.48 < ΔV < 3.7

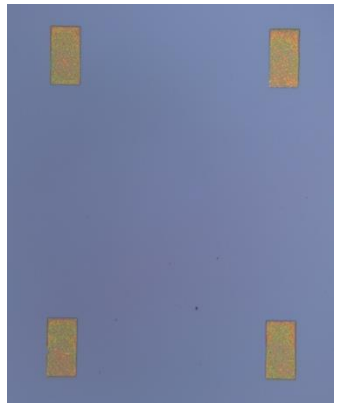
Field Effect Transistor (FET) Using II-VI Semiconductors (NMOS)



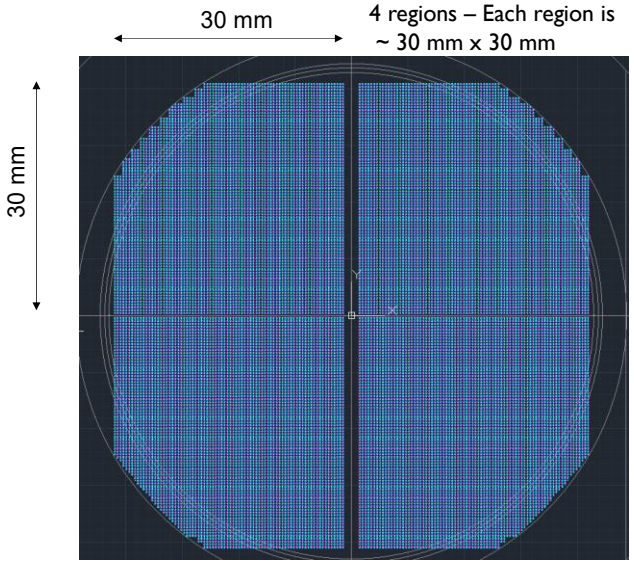


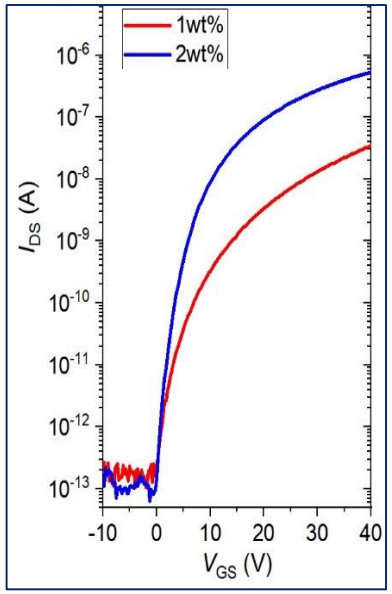






Channel width varied from 100 nm to 2 um, length varied from 100 nm to 20 um





Wafer-level manufacturing of 37,000 transistors exhibiting an on/off ratio higher than 10^6 after annealing.

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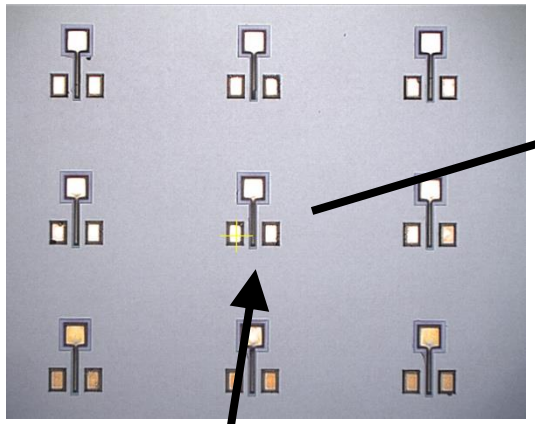
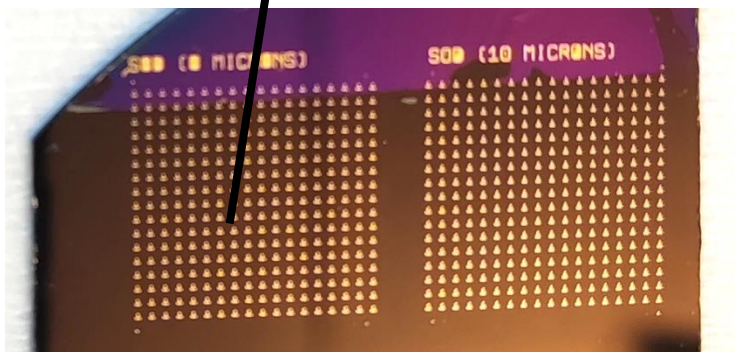
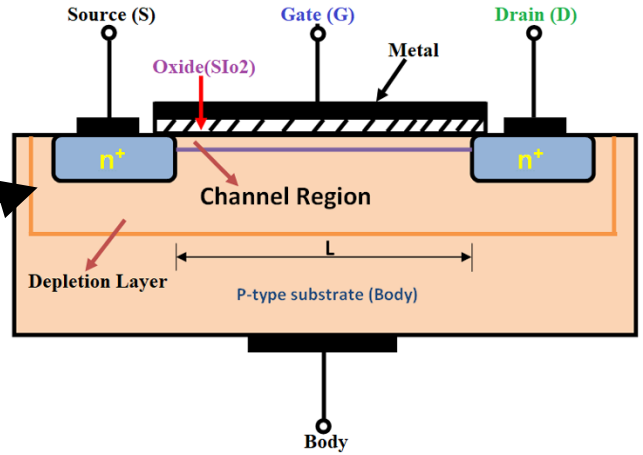
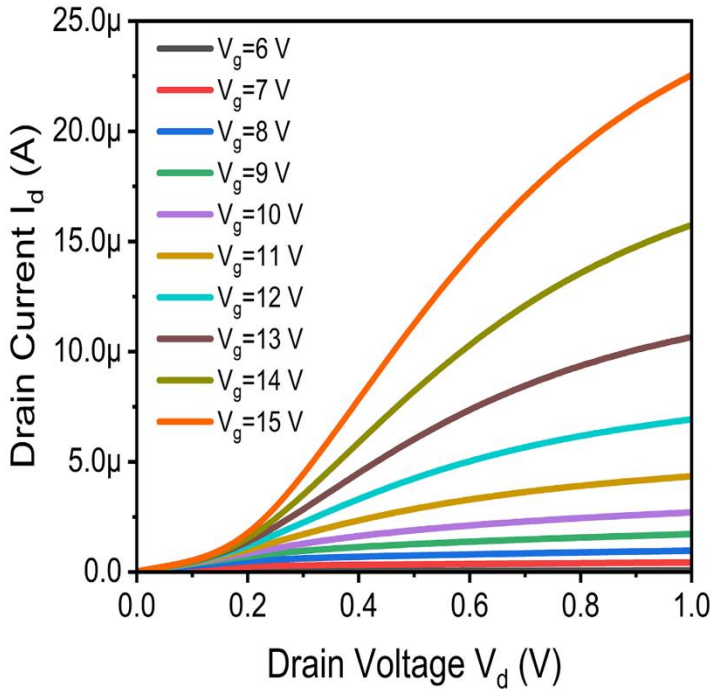
Additively Manufactured Silicon Transistors (MOSFETs)

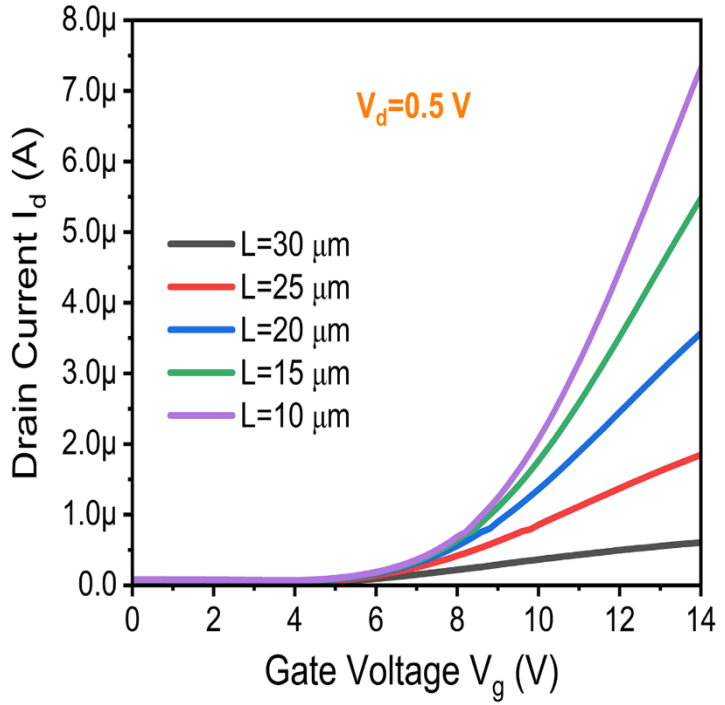




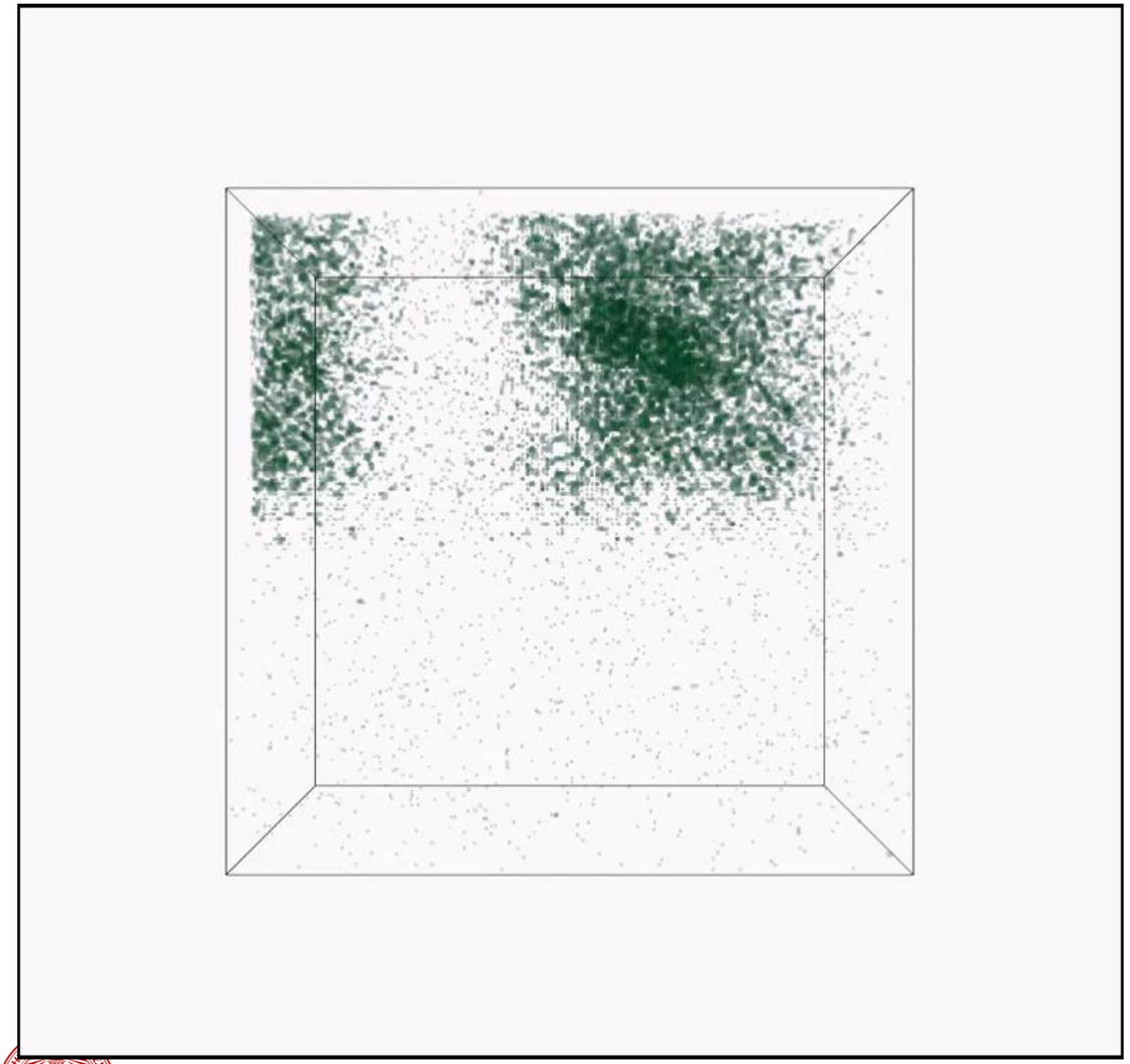


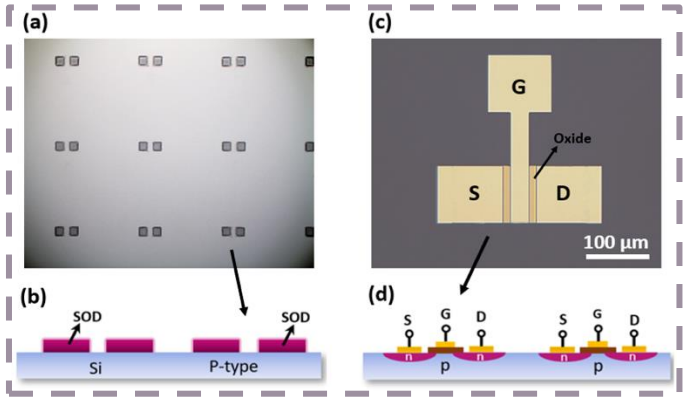
A fully additive liquid-based process process to manufacture MOSFETs using dopants inks to make NMOS.

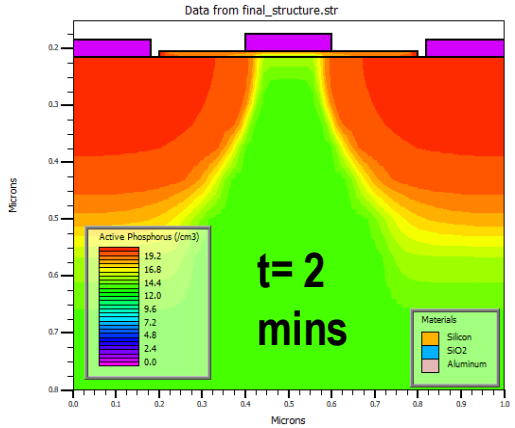


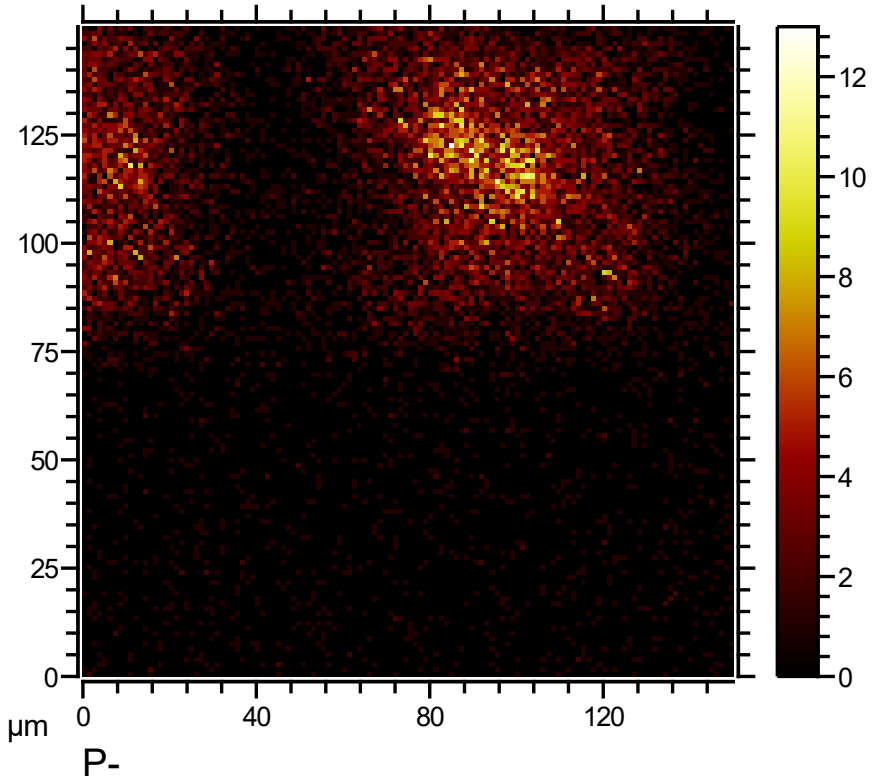


Phosphorous 3D doping profile (TOF-SIMS)



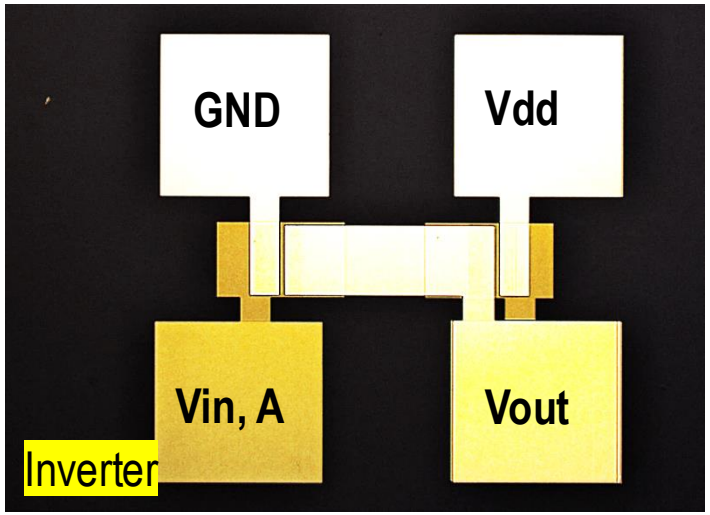


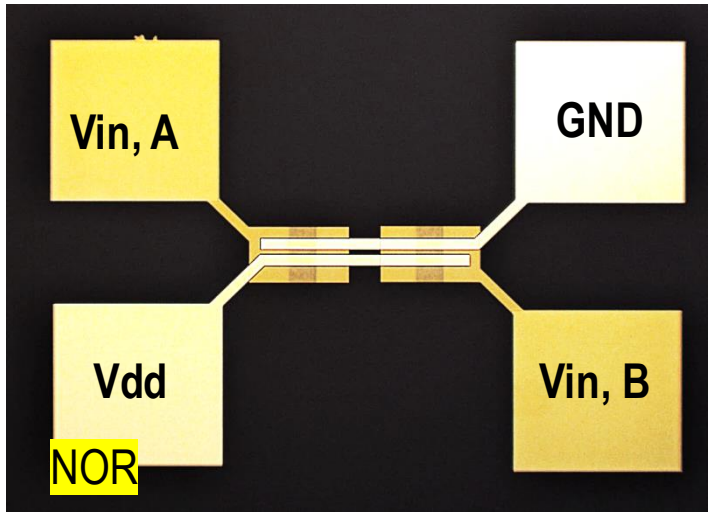


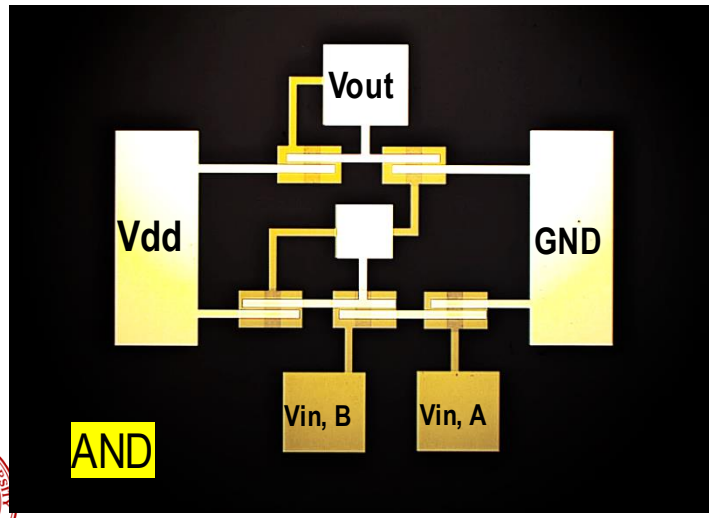


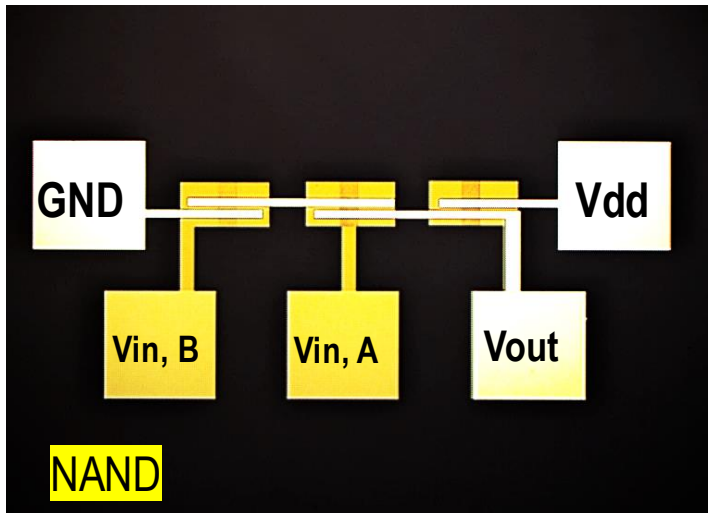
Additively Manufactured Logic Gate Electronics

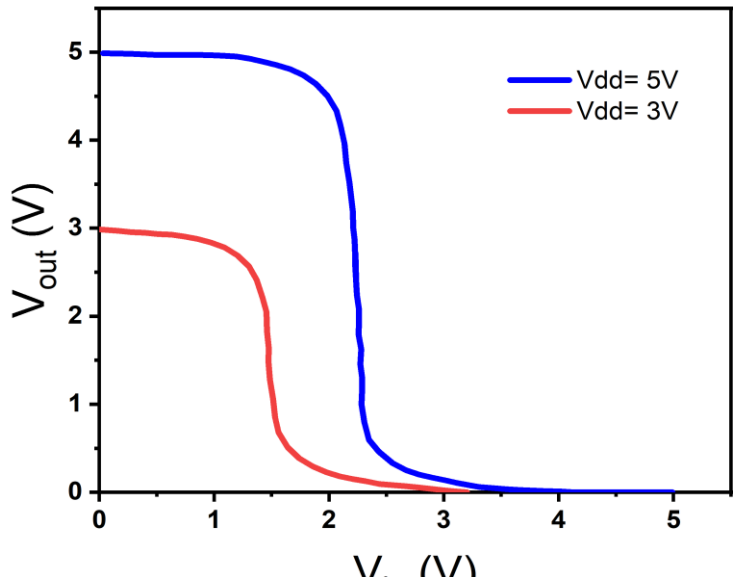
- Logic gates such as Inverters, AND, NAND, and NOR were printed
- The figures below show the fabricated logic circuits (using PMOS)

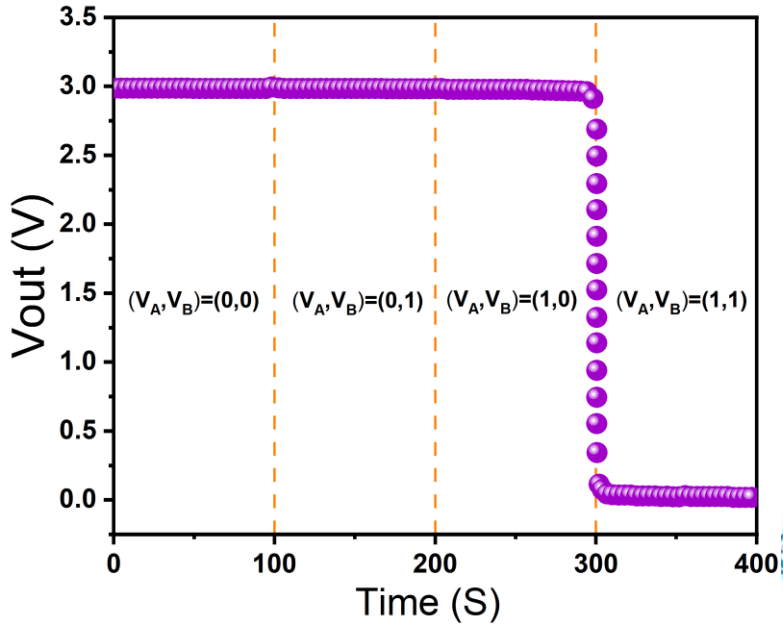




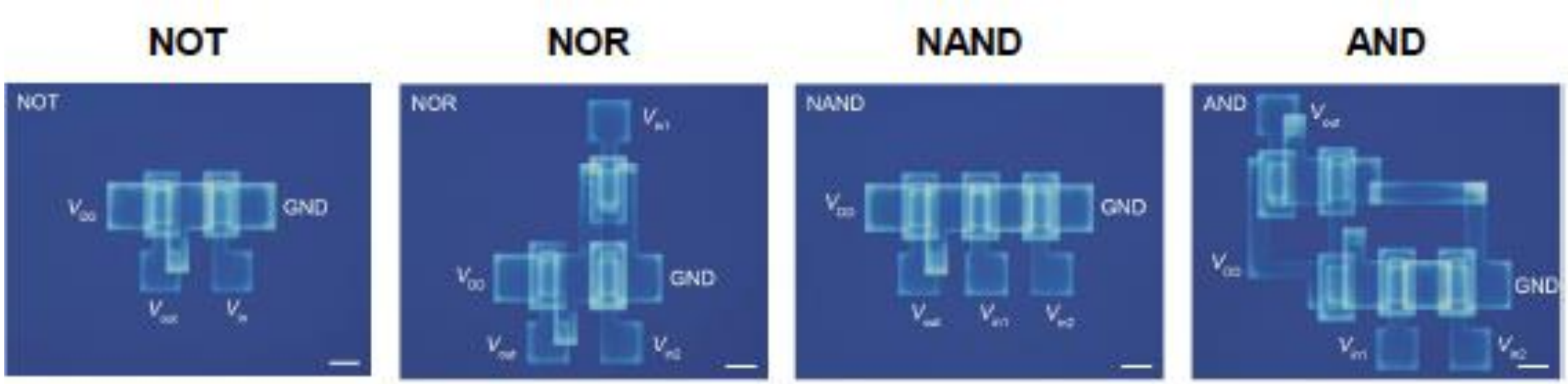


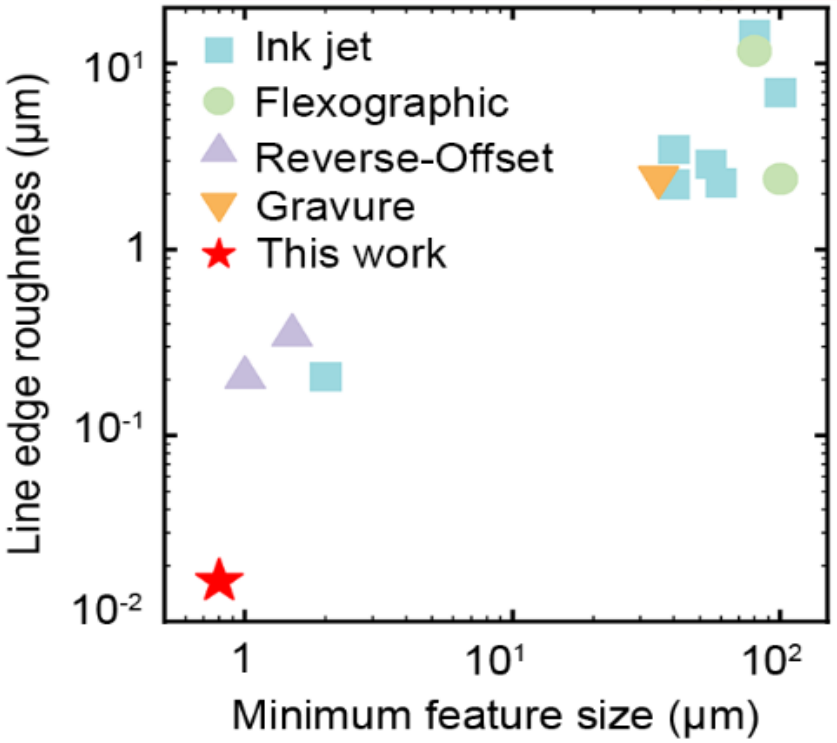


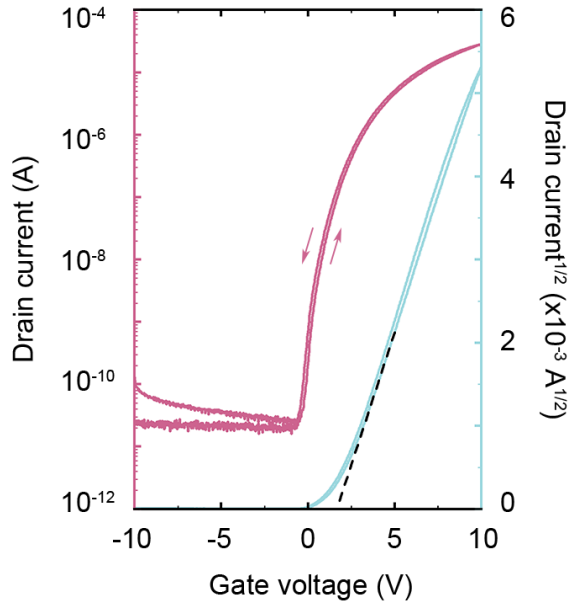


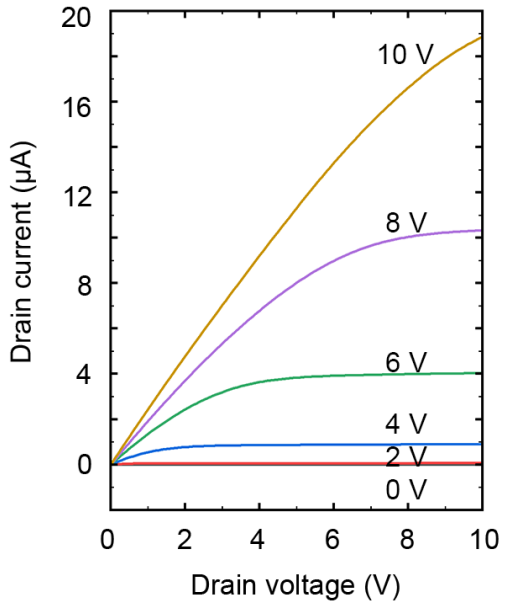


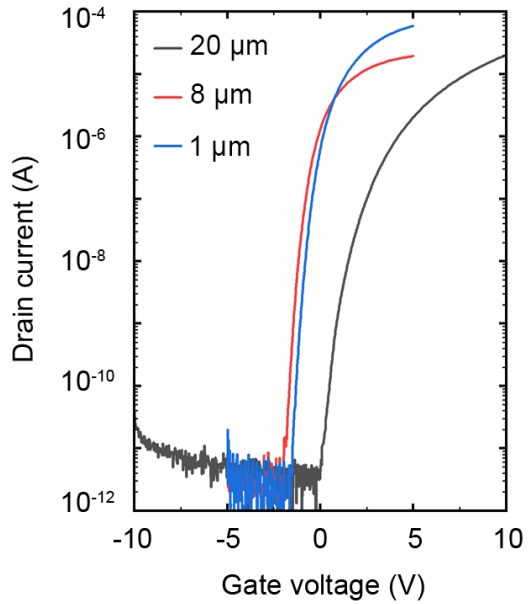
Additively Manufactured Logic Gate Electronics using Indium Oxide (NMOS)





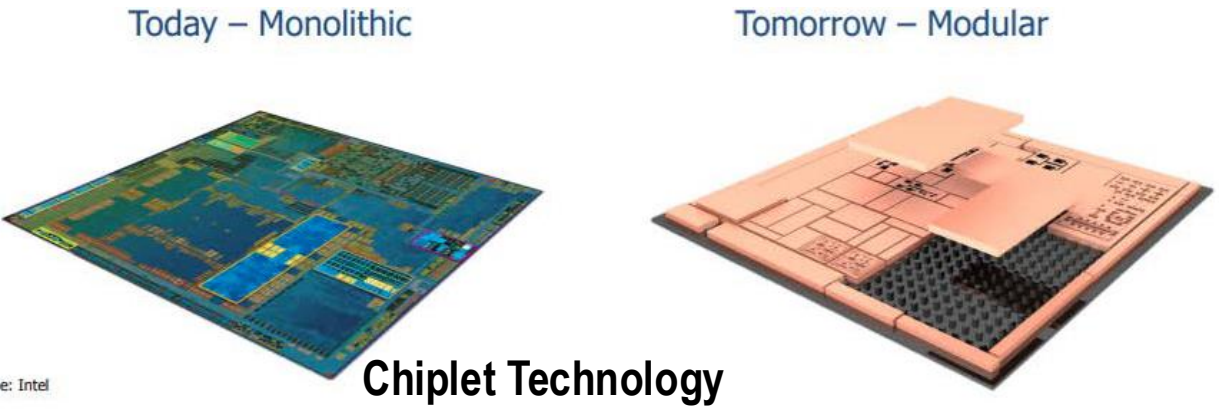






ACS nano, Vol. 18, 2024.

Advanced Packaging for Heterogeneous Integration
for chiplet technology for integrating multiple dies in a package or system



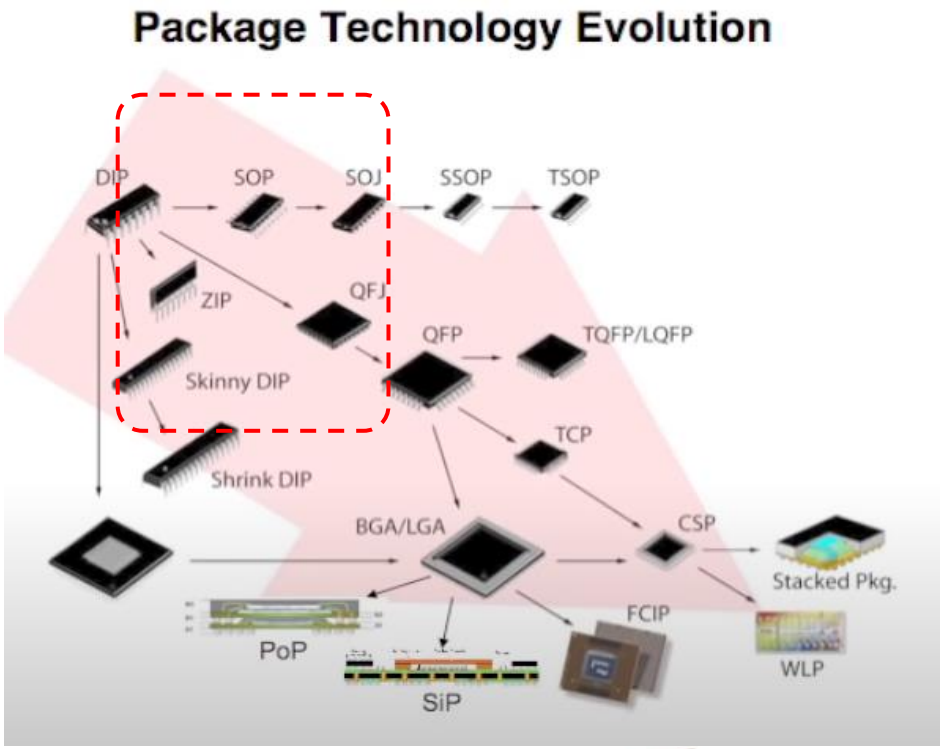
Chiplet Technology

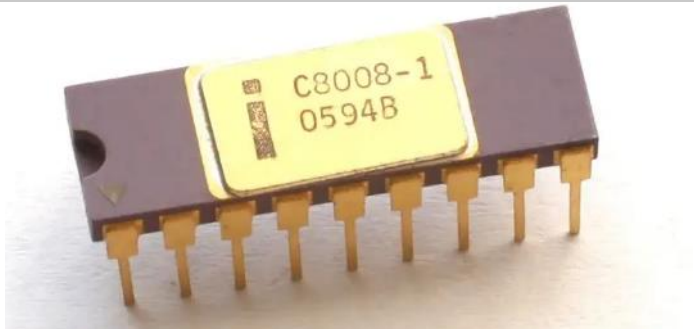
- Conventional packaging approaches can not meet the resolution and density requirements.
- It can only be done at conventional fabs now.

Fully automated and cyber enabled system

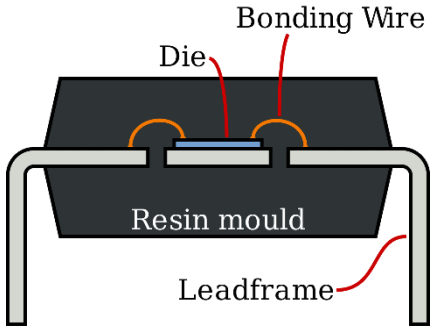
- Submit DXF or GDS files and load ink, wafers, etc.
- Additively Manufacture:
  - micro and submicron interconnects.
  - passive components
  - onto silicon, glass or organic substrates (interposers)

Packaging of On-demand Additive Manufacturing of Legacy Components and Chips



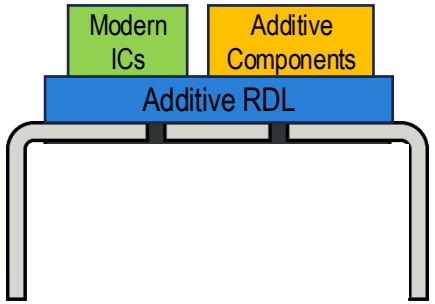


DIP Packaging (1964-1980s)
[Intel 8008]



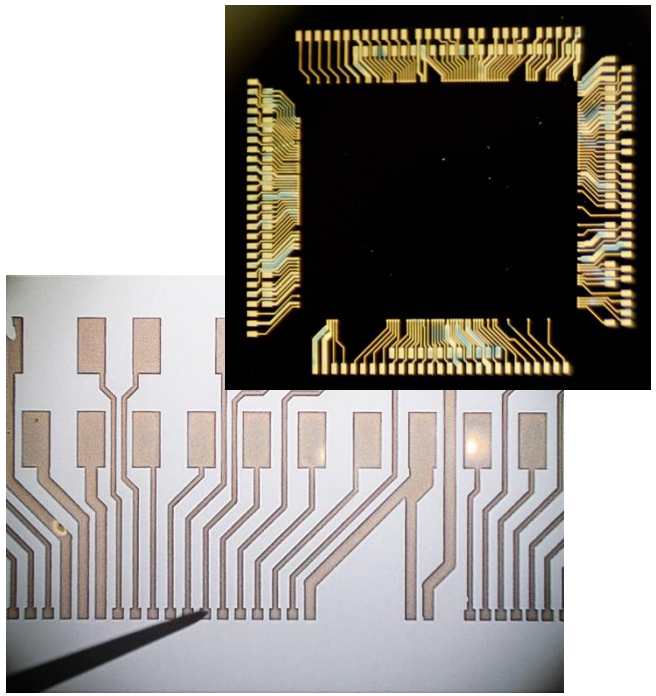
Legacy dual in-line packaging (DIP)

On-demand Additive Manufacturing of Component

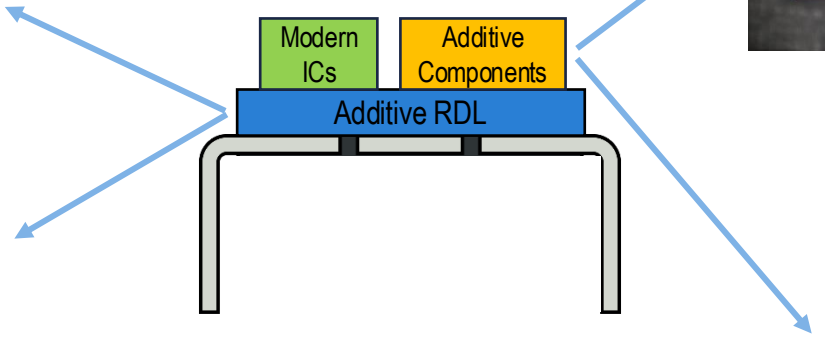


- Passive Components
- Digital
- Analog
- Hybrid (Analog/Digital + Passives)
- Level converters (voltage level matching)

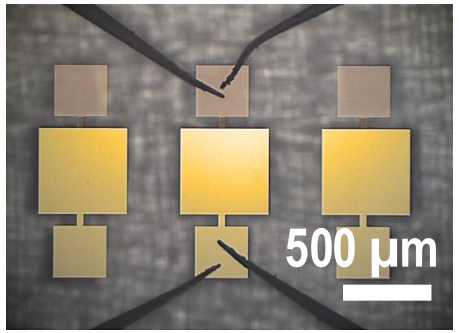
Hybrid Additive Manufacturing Approach for Legacy Components

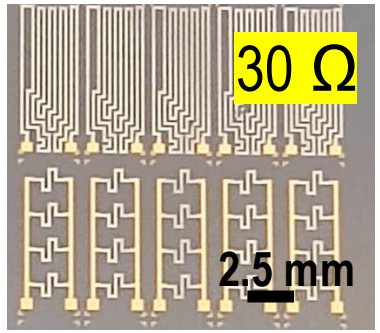


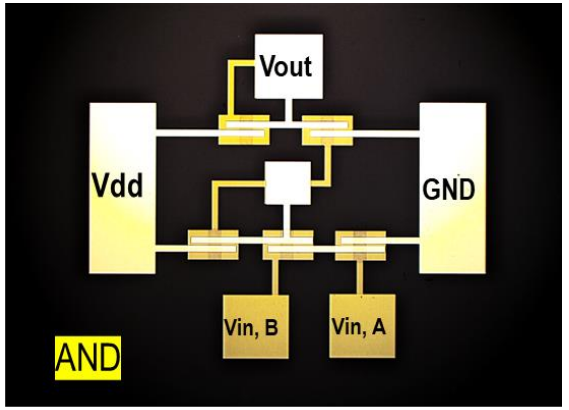
On-demand Additive Manufacturing of Component



Direct Assembly Printing (NanoOPS)







- Multilayer RDL and FANOUT for dies (FPGA, …) and components
- High integration density or fixed footprint (component embedding and chip stacking)

- Printed high-quality active components and networks
- Direct integration of active devices
- High-resolution RDL for direct bare die and interposer integration (advanced packaging enabler)

The Future of Electronics Manufacturing

Any Material
Any Substrate

Minimum Feature Size
20 nm

High throughput
10 – 100x Faster

Cheaper 10 – 100x

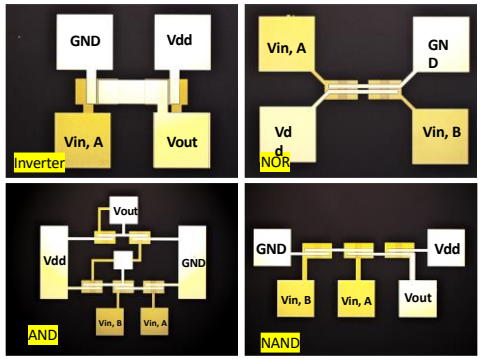
Fab-in-a-Tool: A Fully Automated Nanoscale Electronics Manufacturing Platform

https://www.youtube.com/watch?v=QpbDfAJzXDU&t=7s

On Demand Microelectronics Manufacturing: Semiconductor Fab-in-a-Box

Challenges

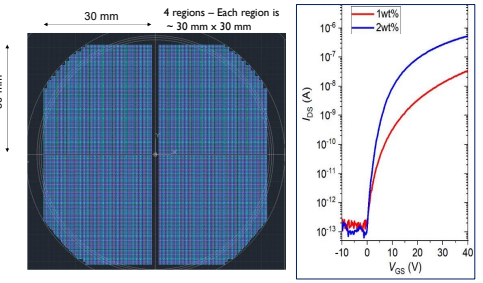
- Offshore, centralized mega-fabs
- High cost and long timelines
- Supply-chain vulnerability
- Limited secure production
- Obsolete component shortages



Printed logic gate electronics

Technical Approach

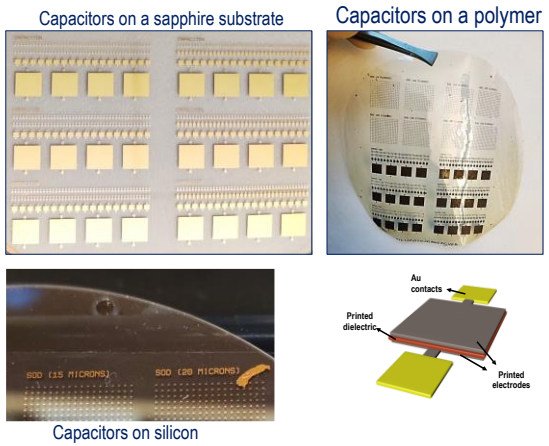
- Directed assembly
- Ambient processing
- Multi-material printing
- Single tool: Fab in a Box from a GDS file to a finished product.
- High-throughput and Wafer-scale capability



37,000 printed transistors with an on/off ratio higher than 10^6.

Benefits and Impact

- **Multi-material, monolithic, quick turn, low-cost fab**
- Trusted manufacturing
- Rapid deployment Modular, automated ~10 m² footprint
- Legacy sustainment
- Supply-chain resilience



Summary:

- One layer per minute
- 300 nm feature size ready
- Inorganic semiconductor and Dielectrics.
- Cu, Ag., Au, Pt and W deposition
- Can deposit new materials
- Fully automated

Nano & Micro Printing Platform

Nano OPS©

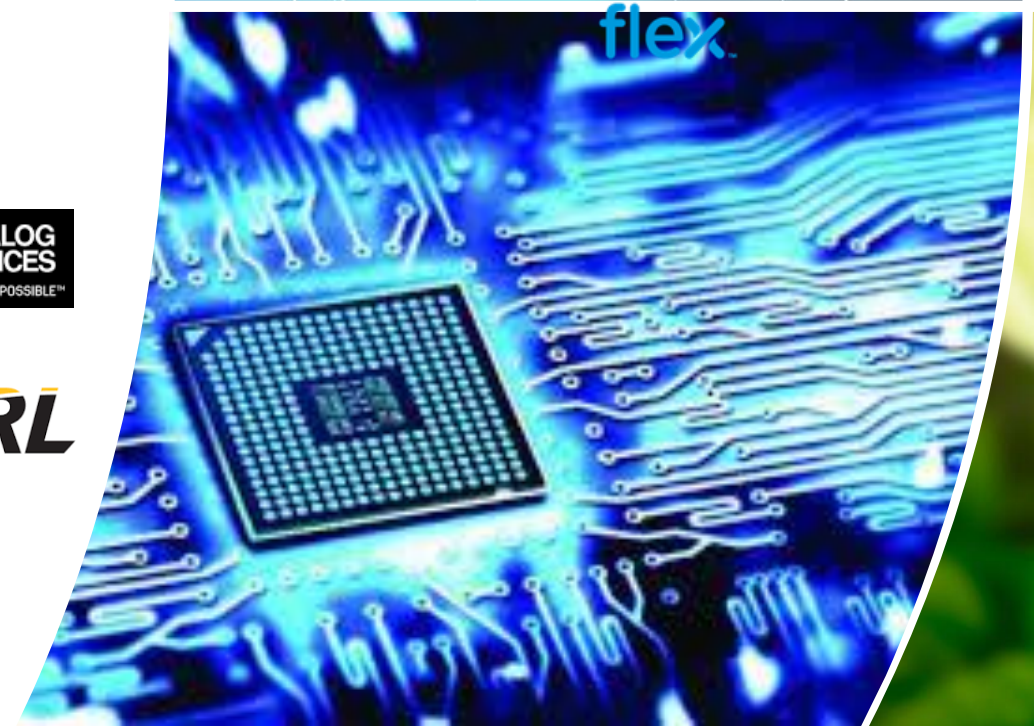
Nano OPS©

On-demand Additive Manufacturing of Microelectronic Component and Legacy Components and Chips (ICs)

- Capable of fully printing passives such as capacitors and resistors using metals and inorganic high K dielectrics (HfO2, Al_2O_3), and low K dielectrics (SiO2).
- The Fab-in-a-Box on-demand turnkey device fabrication provides a reduction in manufacturing cost of 10-100 times and a throughput 10 to 100 times higher compared to current technology.
- Such manufactured components can replace legacy components or the IC, the packaging needs to be equivalent to the legacy components and that will need a first-level printed package that is either PTH or SMT of the printed device.
- Another immediate option for legacy ICs or chips, a small FPGA can be packaged using printed packaging equivalent to the legacy chip. These FPGAs can be digital or analog and have a wide voltage range (~1-5.5 V).
- All traces and packages will be designed and printed to match the actual size and connections of the legacy chip.
- Nano OPS, Inc. have the facilities to prototype on-demand replacement for legacy components and ICs.

Technological Impact

- Adv. Packaging on demand
- Passive and Active components on demand
- Fast prototyping and development cycle
- Security
- Sustainable
- Material innovation



NSF Raytheon ANALOG DEVICES AHEAD OF WHAT'S POSSIBLE™ MASSACHUSETTS TECHNOLOGY COLLABORATIVE NASA ARL DRAPER NEXTFLEX DARPA UNITED STATES AIR FORCE GE ROGERS CORPORATION

Acknowledgment

Raytheon
BOEING
ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™
NASA
DARPA
UNITED STATES AIR FORCE
BAE SYSTEMS
GE
NSF
UNITED STATES ARMY
MASSACHUSETTS TECHNOLOGY COLLABORATIVE
ROGERS CORPORATION
DRAPER
nbmc Nano Bio Manufacturing Consortium
NEXTFLEX®
flex
MILARA

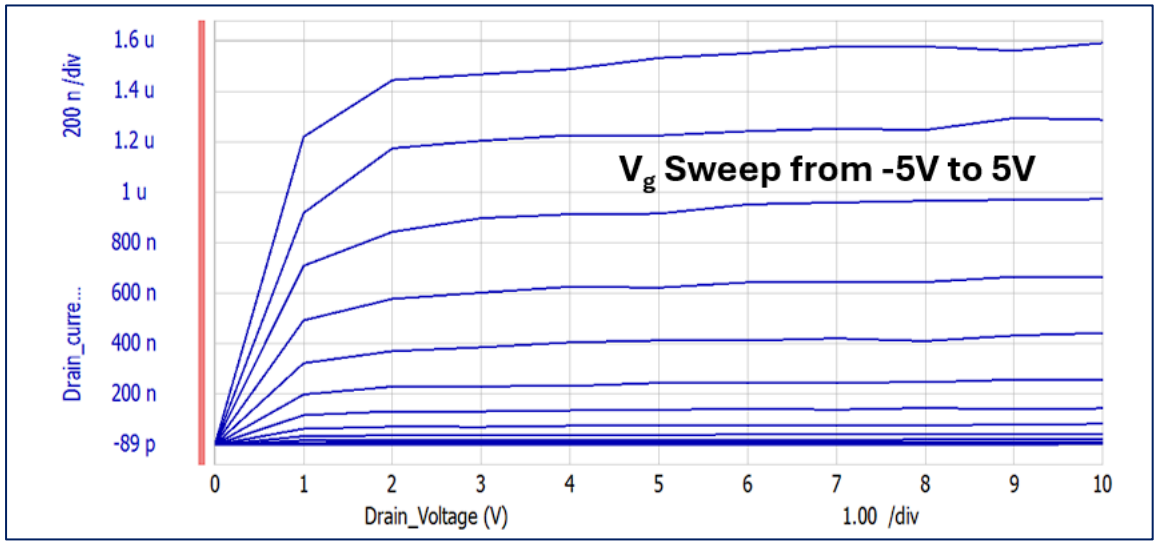
CTO@nano-ops.net

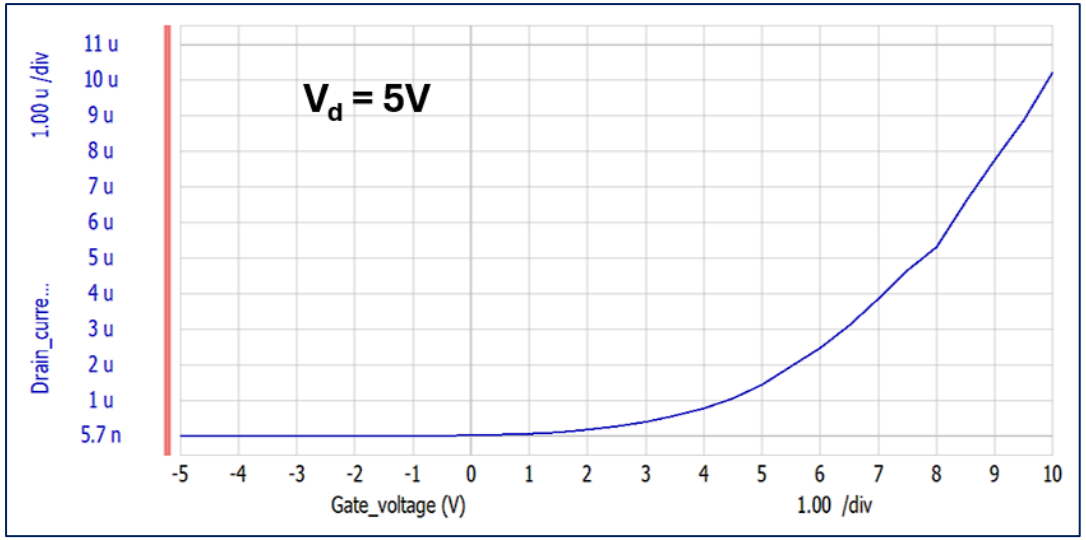
To learn more: www.nano-ops.net

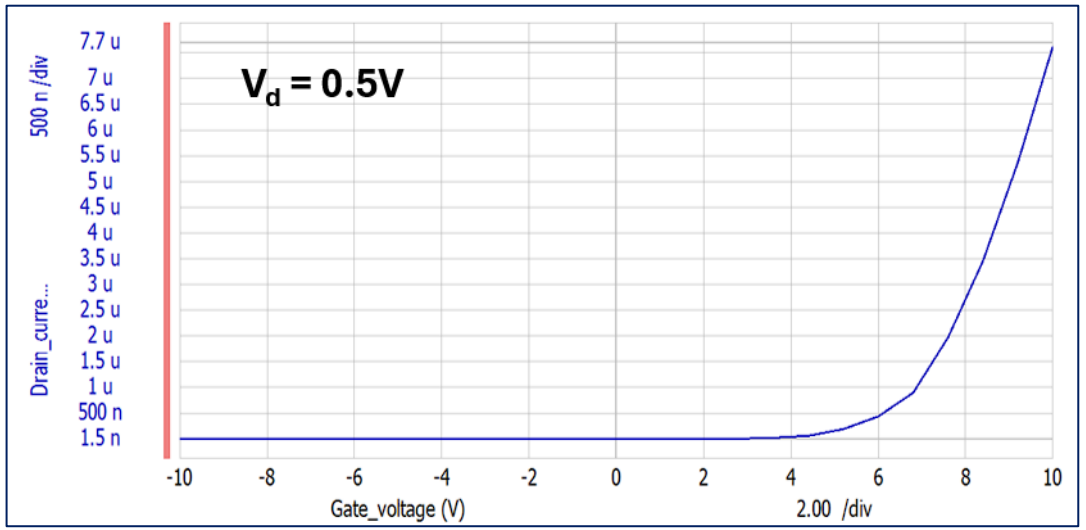
Nano OPS©

Additively Manufactured Silicon Transistors (MOSFETs)

A fully additive liquid-based process process to manufacture MOSFETs using dopants inks. NMOS characterization curves.

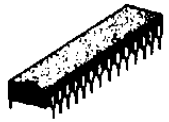
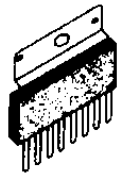
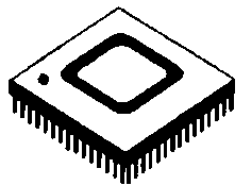




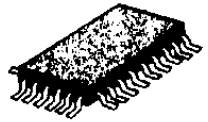
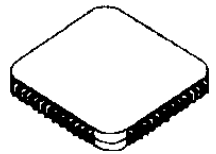
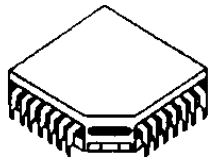
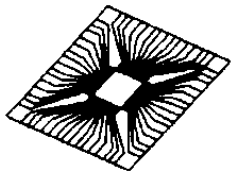


Types of First Level Packages

Through Hole Package

a		DIP (Dual In-line Package)
b		SH-DIP (Shrink DIP)
c		SK-DIP, SL-DIP (Skinny DIP, Slim DIP)
d		SIP (Single In-line Package)
e		ZIP (Zig-zag In-line Package)
f		PGA (Pin Grid Array) or Column Package

Surface Mounted Package

g		SO or SOP (Small Out-line Package)
h		QFP (Quad Flat Package)
i		LCC (Leadless Chip Carrier)
j		PLCC, SOJ (Plastic Leaded Chip Carrier with Butt Leads)
k		BGA (Ball Grid Array)
l		TAB (Tape Automated Bonding)
m		CSP (Chip Scale Package)