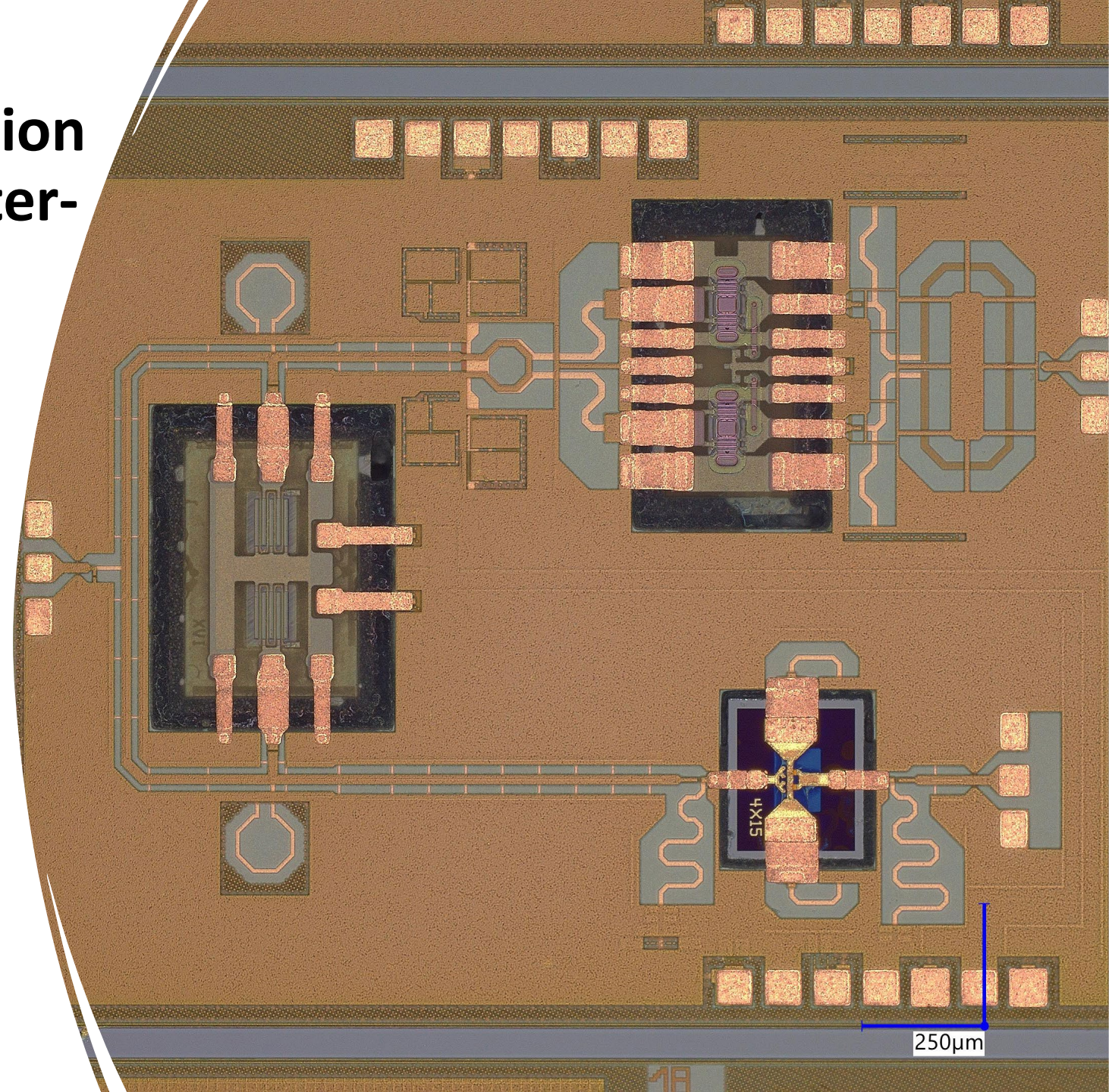
# GaN and InP Chiplet Integration in CMOS Wafers for Millimeter-Wave Front-Ends

PseudolithIC

**Florian Herrault** | *CEO*

*April 30th, 2025*



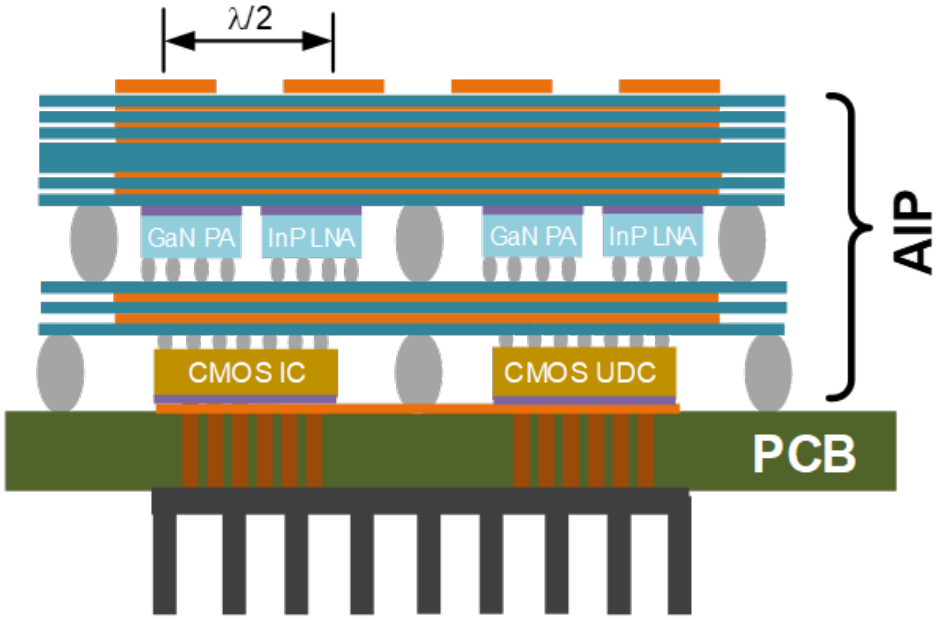

CMSE 2025 - The 28th Annual Components for Military & Space Electronics Conference & Exhibition

# Outline

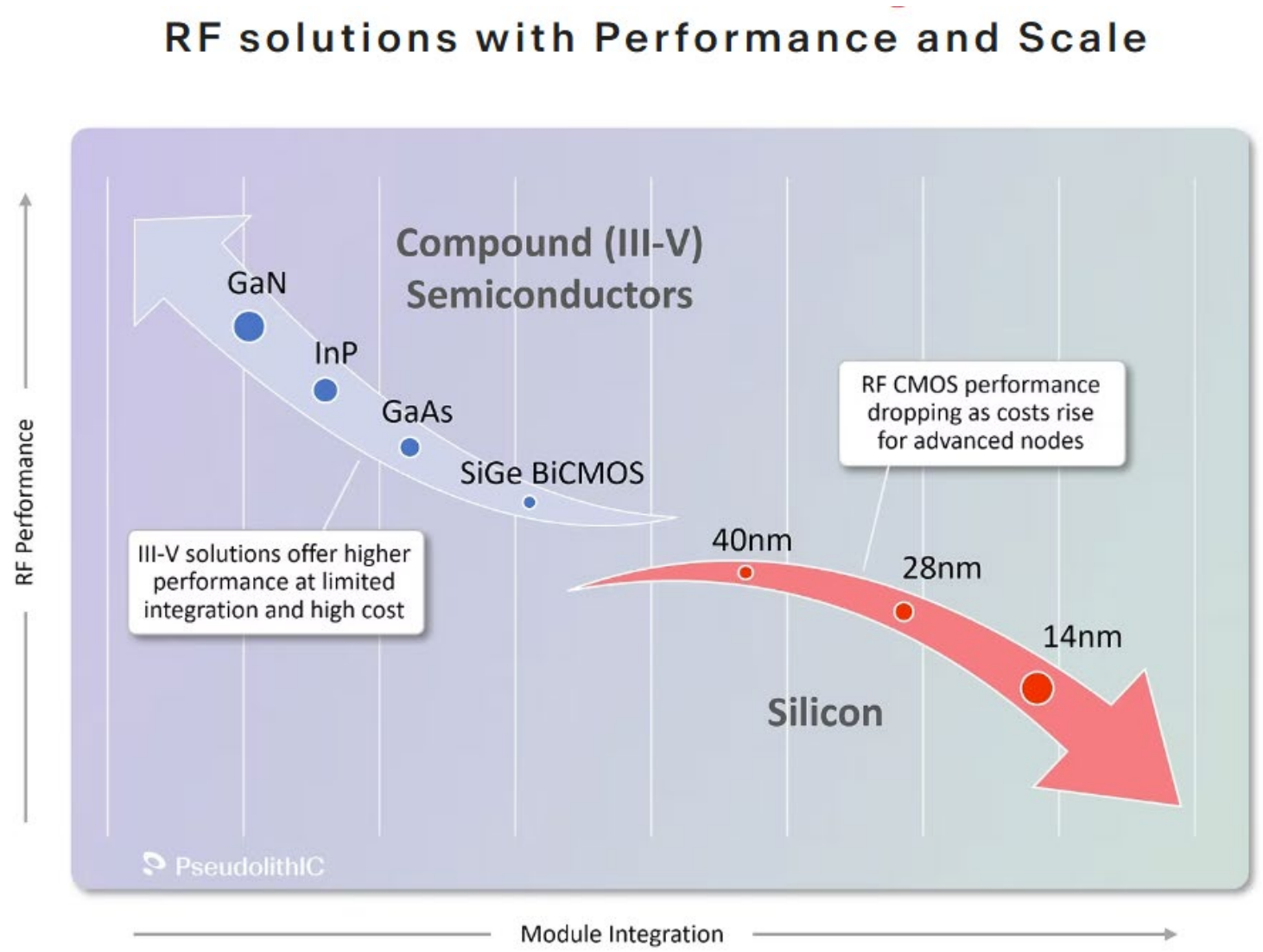
- Motivation & Technology Introduction
- Manufacturing Advantages of a III-V Chiplet / Si Integration Platform
- Design Examples and Measurement Results
- X+ CMOS as a Key Differentiation
- Conclusions

# Commercial Phased Arrays

- A tale of two cost structures:
  - Beamforming ICs have been pushed to commodity pricing: 10 cents/channel
  - III-V front end modules have been unmoved in cost and volume (but are needed for Phased Array Performance)
- Millimeter-wave probably won't work commercially until something changes.

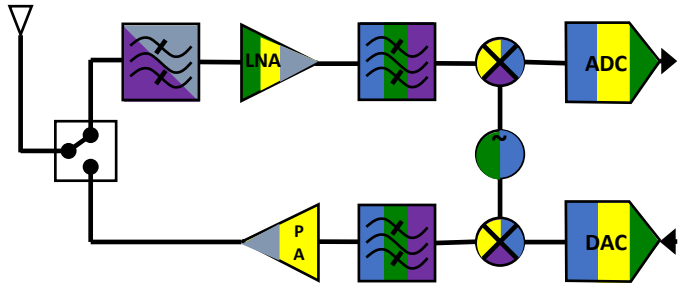


# What is the Technical Challenge?



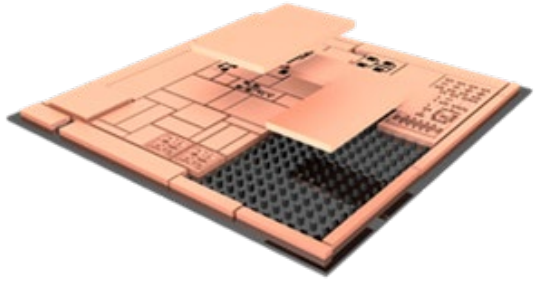
# Why Heterogeneous Integration?

Component



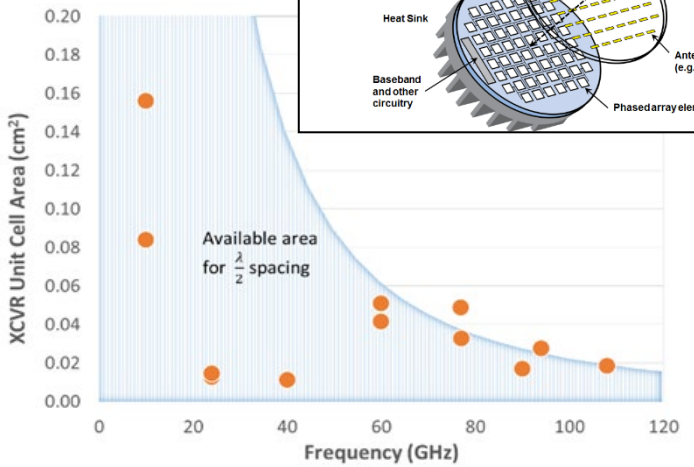

Best of breed technology

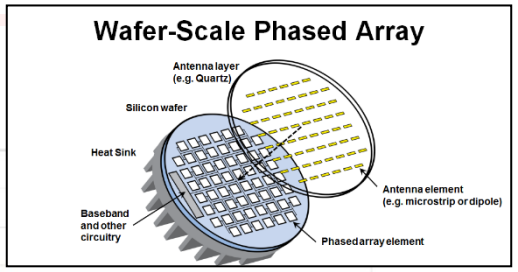
Si CMOS/SiGe BiCMOS
InP HBTs/HEMTs
GaN HEMTs
RF MEMS/High-Q passives



Modular design

Density of integration




System

Performance — Value Proposition — Cost

Customer 1 | Customer 2

Sources: DARPA, UCSD

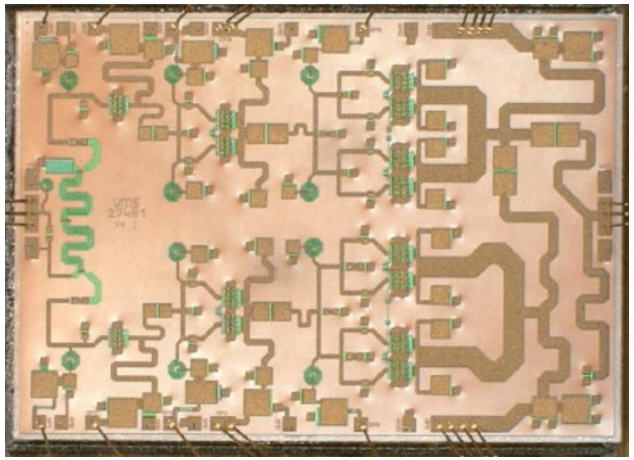
→ Rather than making expensive investments into expensive monolithic process development, heterogeneous integration offers pathway to quickly customize solutions to customer's needs.

# And Opportunities in III-V Manufacturing

- High-performance GaN, InP wafers and other emerging technologies are limited to 4” diameter

- Transistor area per chip is typically less than 10%
- 90% of the area is used for passive elements

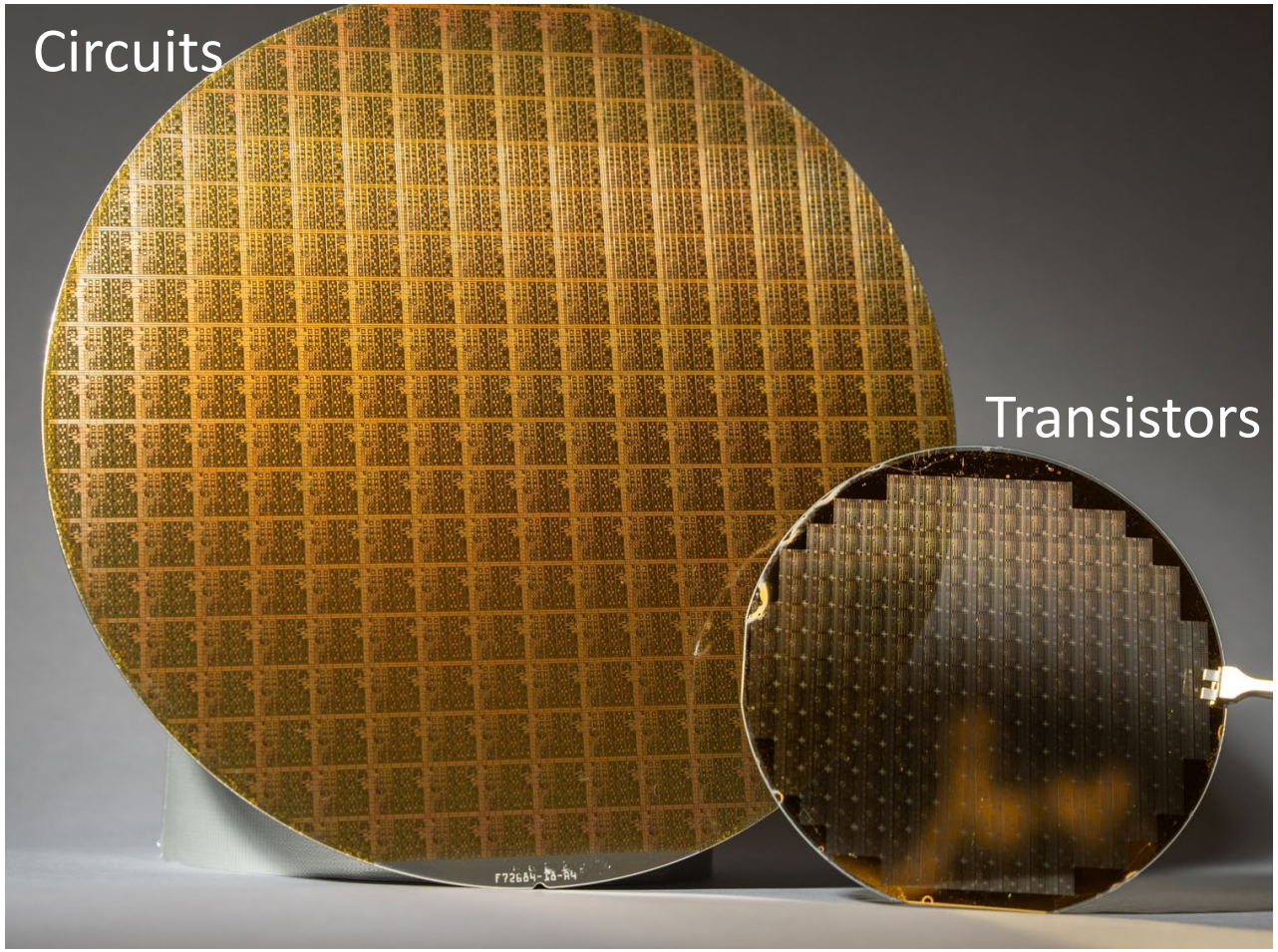
- SoA III-V transistors are typically developed in high-mix low-volume fabs (extends cycle time, reduces yield)



Source: Google image

# The PseudolithIC Solution

**Silicon Foundry:**
RF CMOS
SiGe BiCMOS

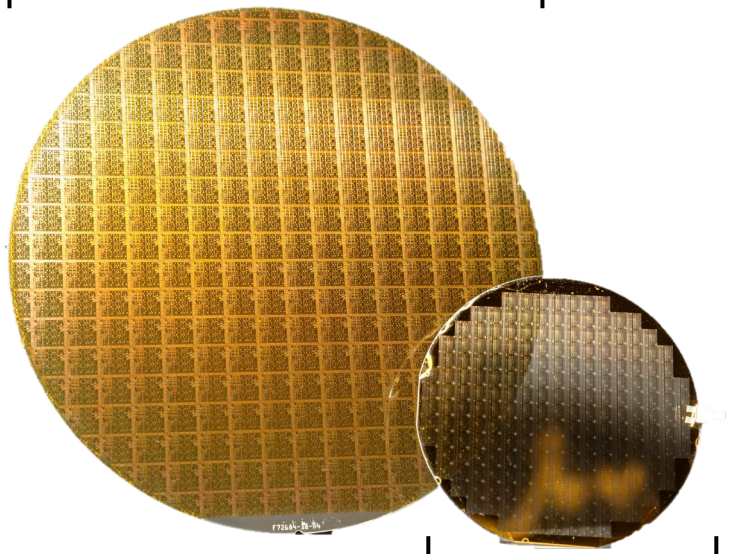



**Compound Semiconductor Foundry:**
GaN
InP
GaAs

Let Foundries excel at making transistors!

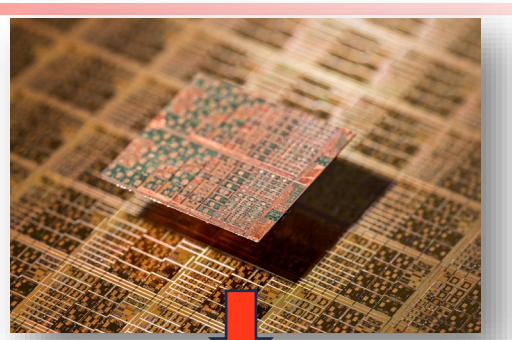
# Integrate III-V into Si Wafers

*200-mm Si CMOS wafer*



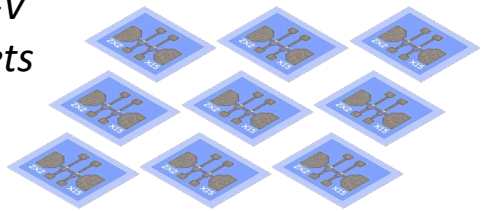
*4'' III-V wafer*

*Custom Si interposer with 100s of designs comprising passives and/or CMOS*

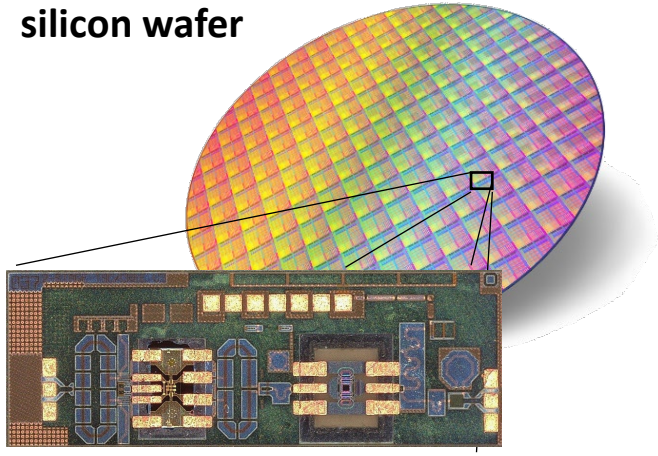


**Automated Wafer Scale Chiplet Integration @ PseudolithIC**

*100,000s of III-V µm-scale chiplets*



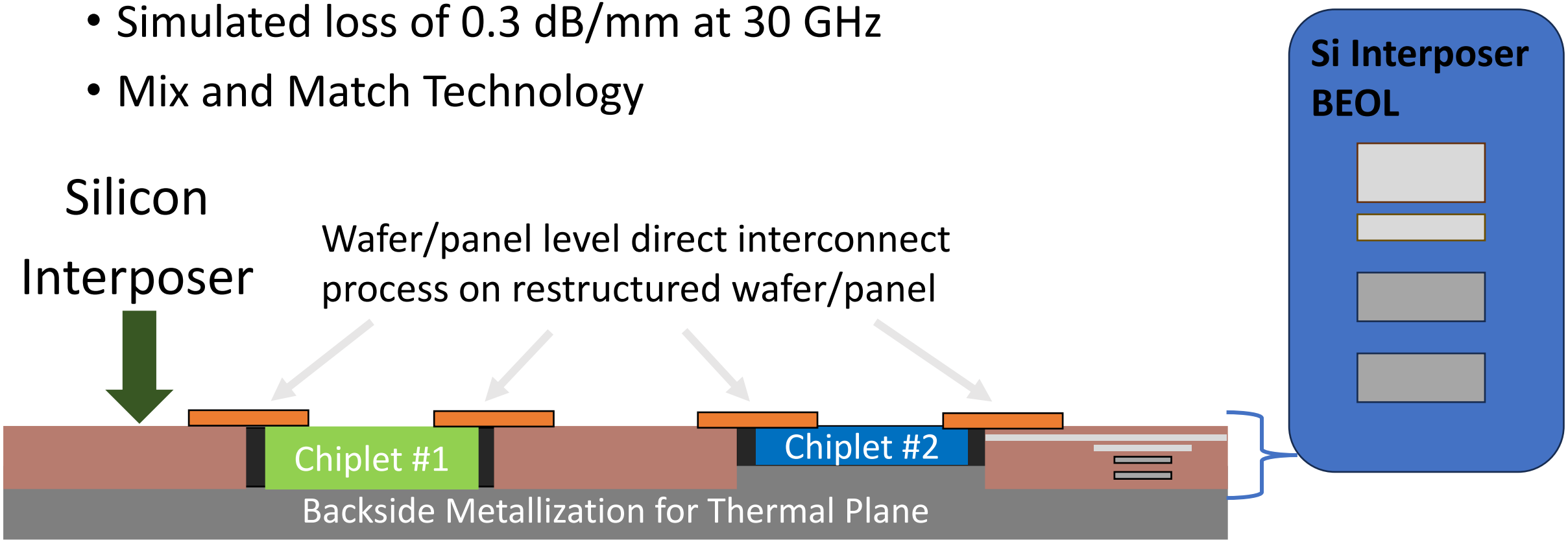
**PSEUDOLITHIC**
**Reconstructed compound semiconductor device-in-silicon wafer**



**World's 1st mm-Wave Mixed Technology InP + GaN Amplifier**

# Pseudolithic Cross Section

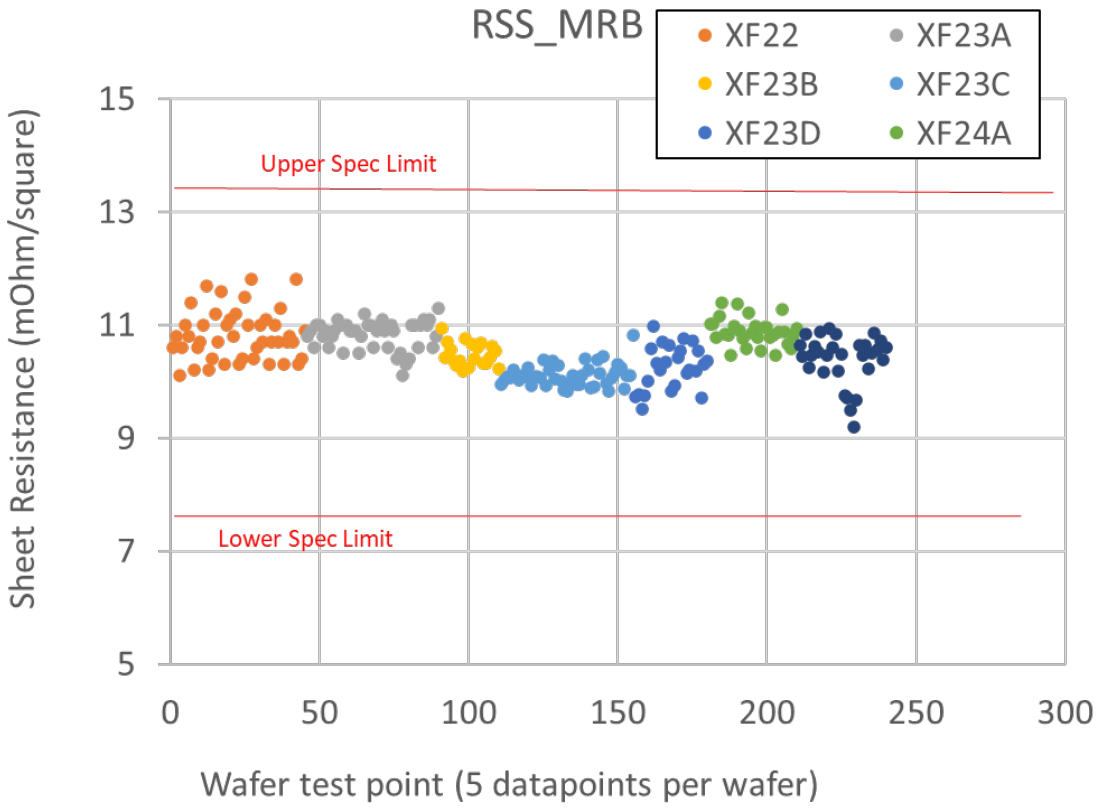
- Reconstructed Wafer with III-V transistor Chips
- Capable of 5um gaps between interconnects
- Simulated loss of 0.3 dB/mm at 30 GHz
- Mix and Match Technology



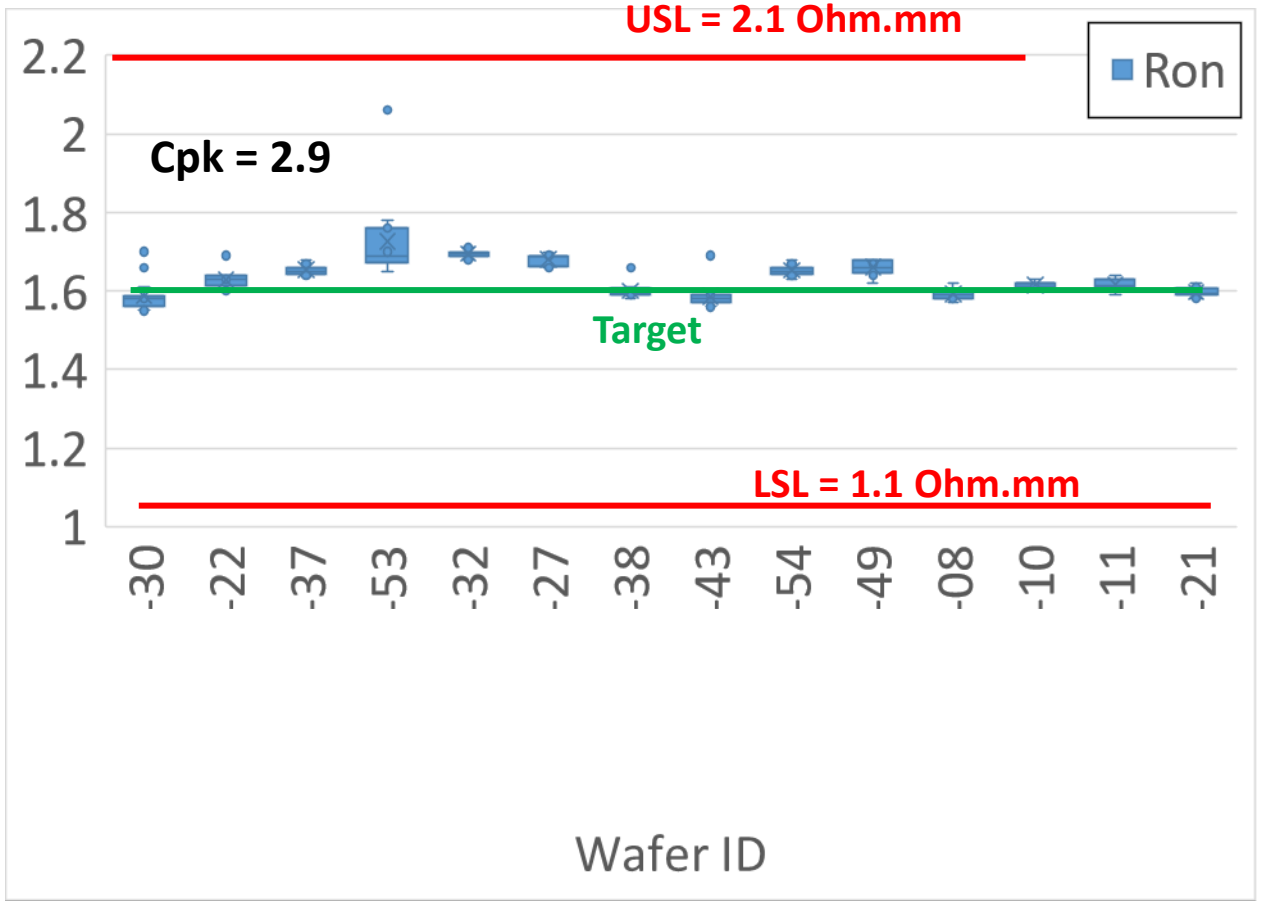
# Manufacturing Advantages of a III-V Chiplet / Si Integration Platform

# Increasing Yield Through HI

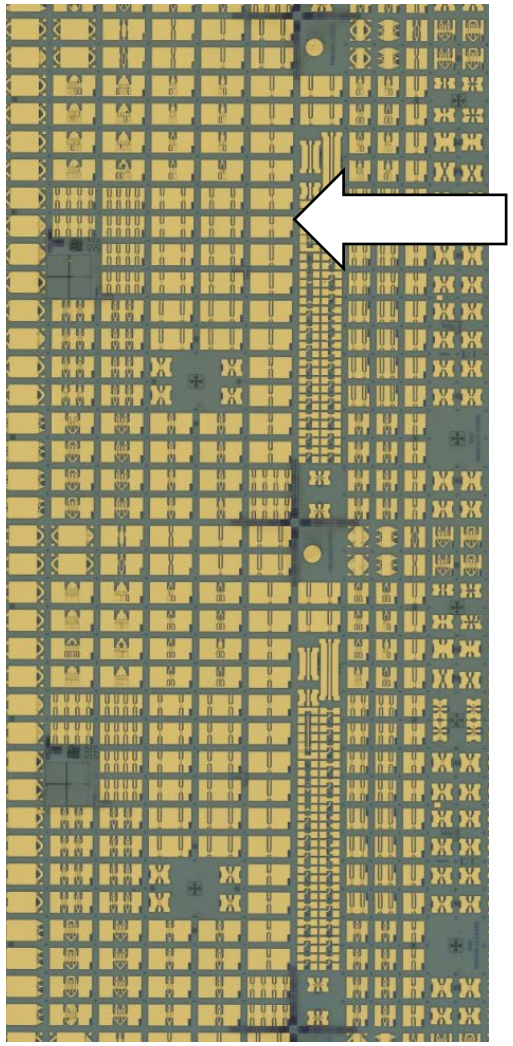
## Silicon Wafer Components – Cpk > 2




## GaN Transistor Ron (Ohm.mm)

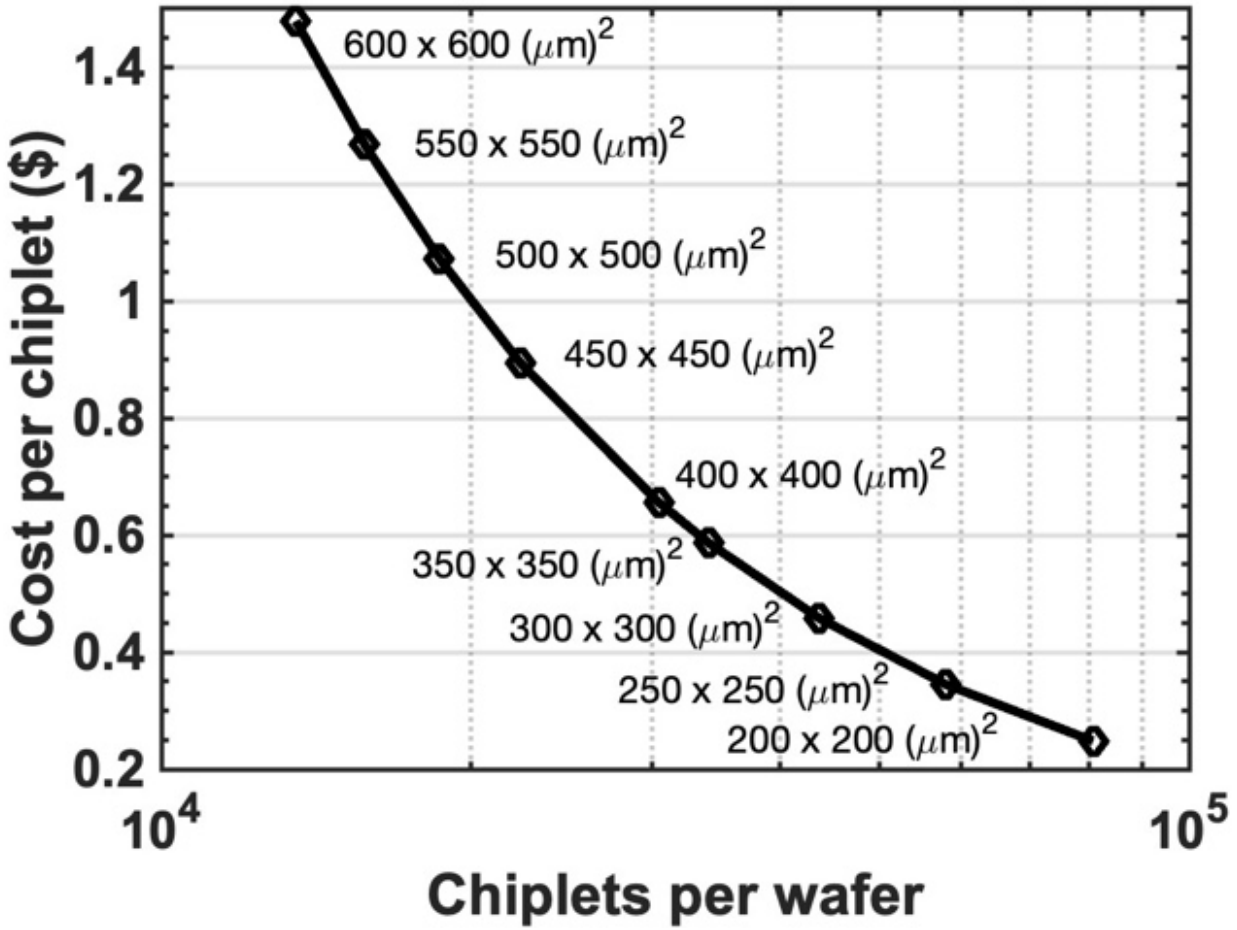


# Driving Down the Cost of Transistors

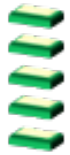
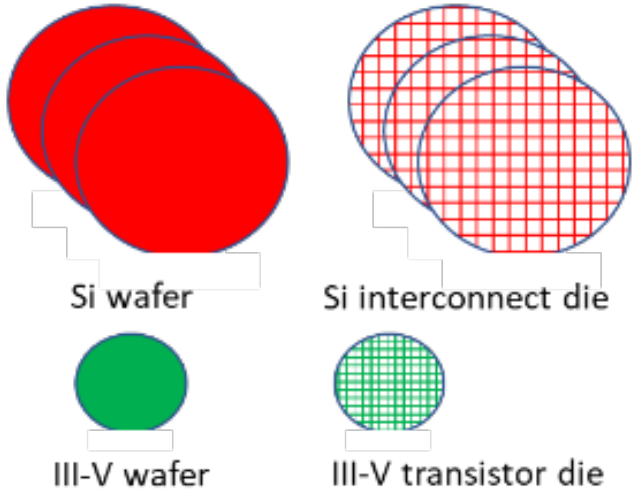
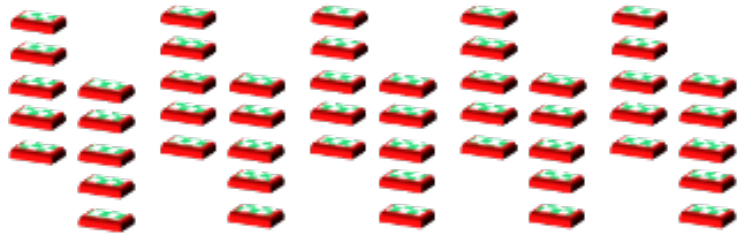


Entire III-V wafer is used to produce chiplets.

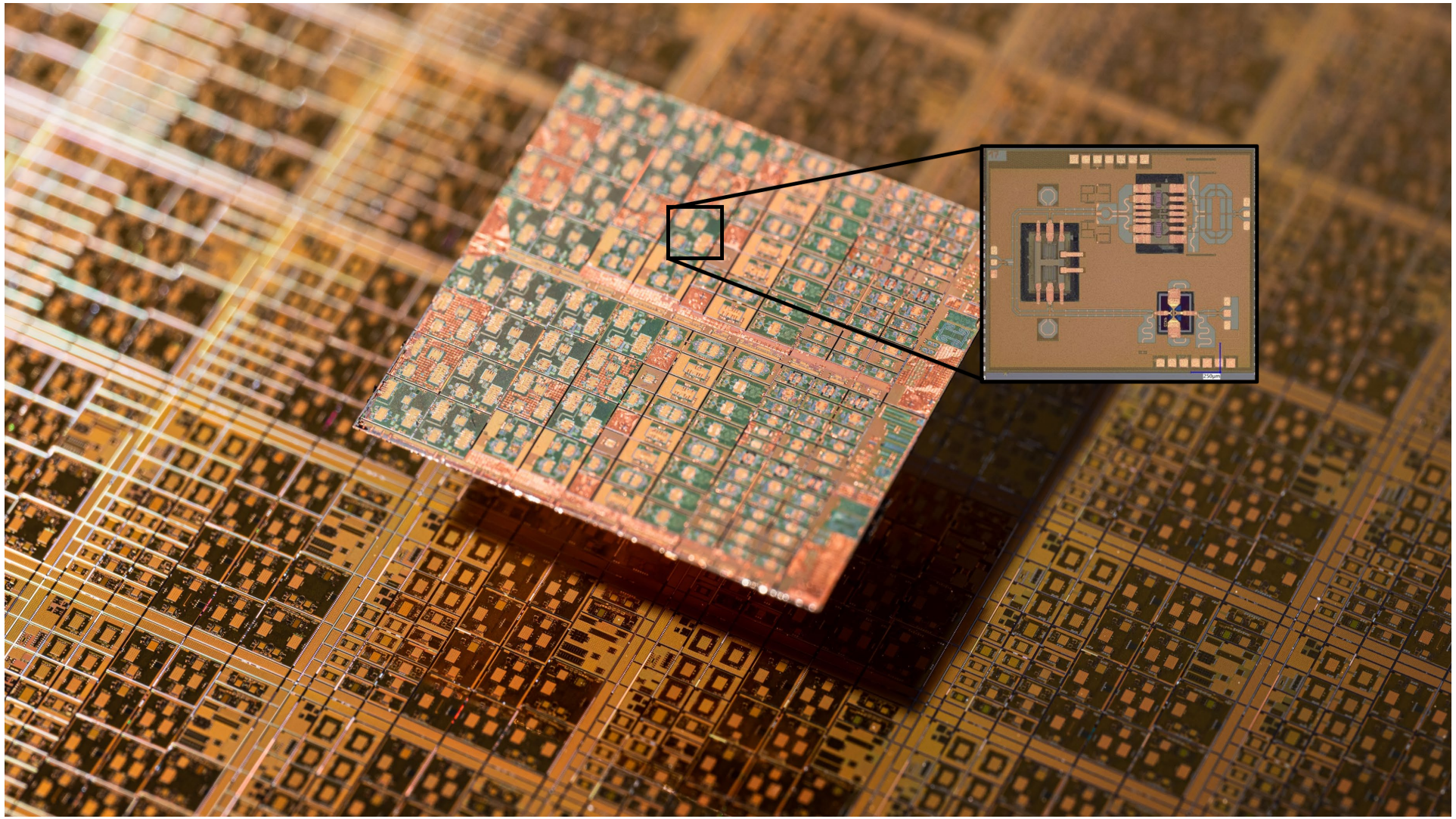
The more chiplets produced per wafer, the lower the cost per transistor cells.



# Driving Up the Quantities of Chips

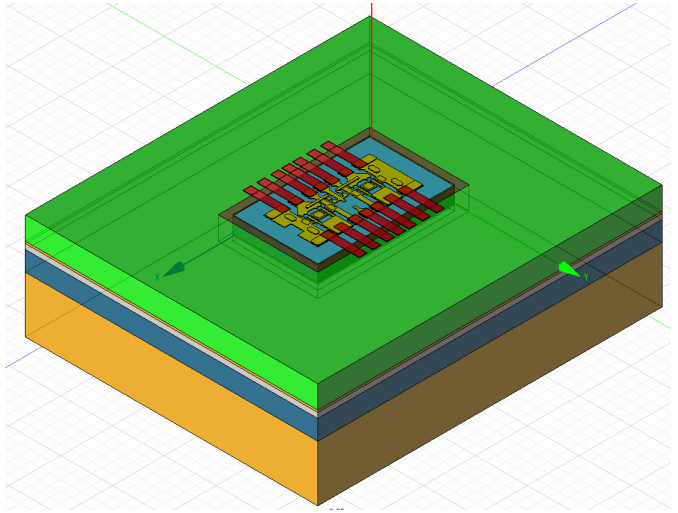
| | Semiconductor Process Wafers | Microwave Die |
|---|---|---|
| III-V MMIC |   |  |
| Pseudolithic PLIC |   |  ~10X Product per III-V wafer<br>80% cost reduction<br>75% cycle time reduction<br>Enables Heterogeneous Integration |

# A Pseudolithic Chip looks like a Silicon Chip

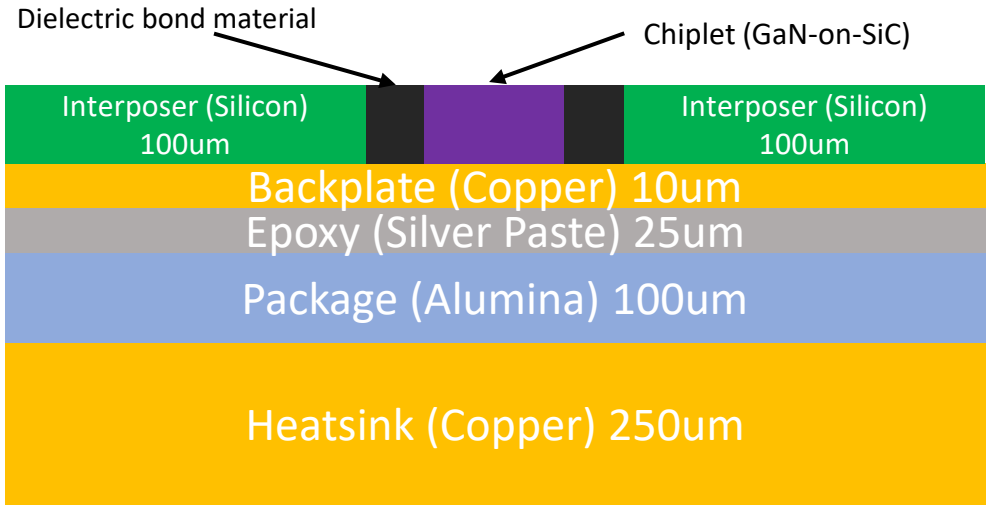


# Comparing PLIC with GaN on Silicon

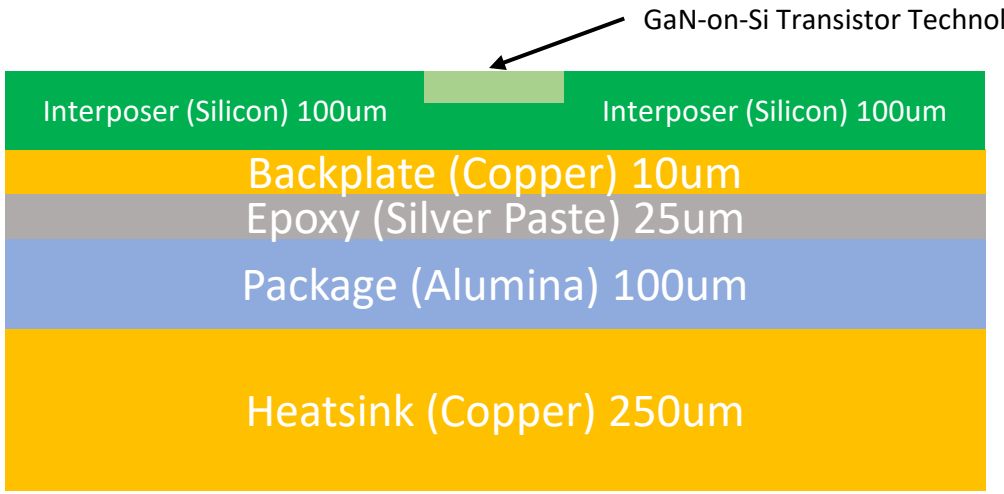
- Simulate the effect of silicon substrate below GaN chiplet instead of typical Silicon Carbide (SiC)
- Power dissipation is 1W, 2W, 5W, and 10W
  - 8 fingers, (125mW, 250mW, 625mW, and 1250mW per finger)
- Base temperature a bottom of heatsink is 26°C
- 3D Model, chiplet includes device pattern and PLI connections



Chiplet Model

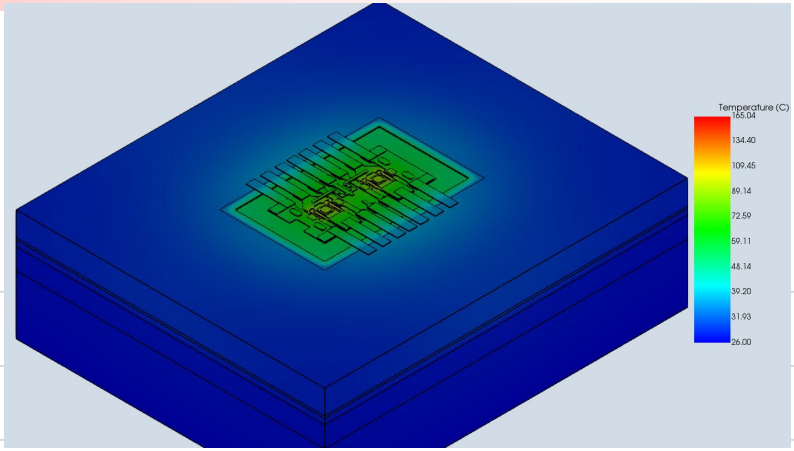


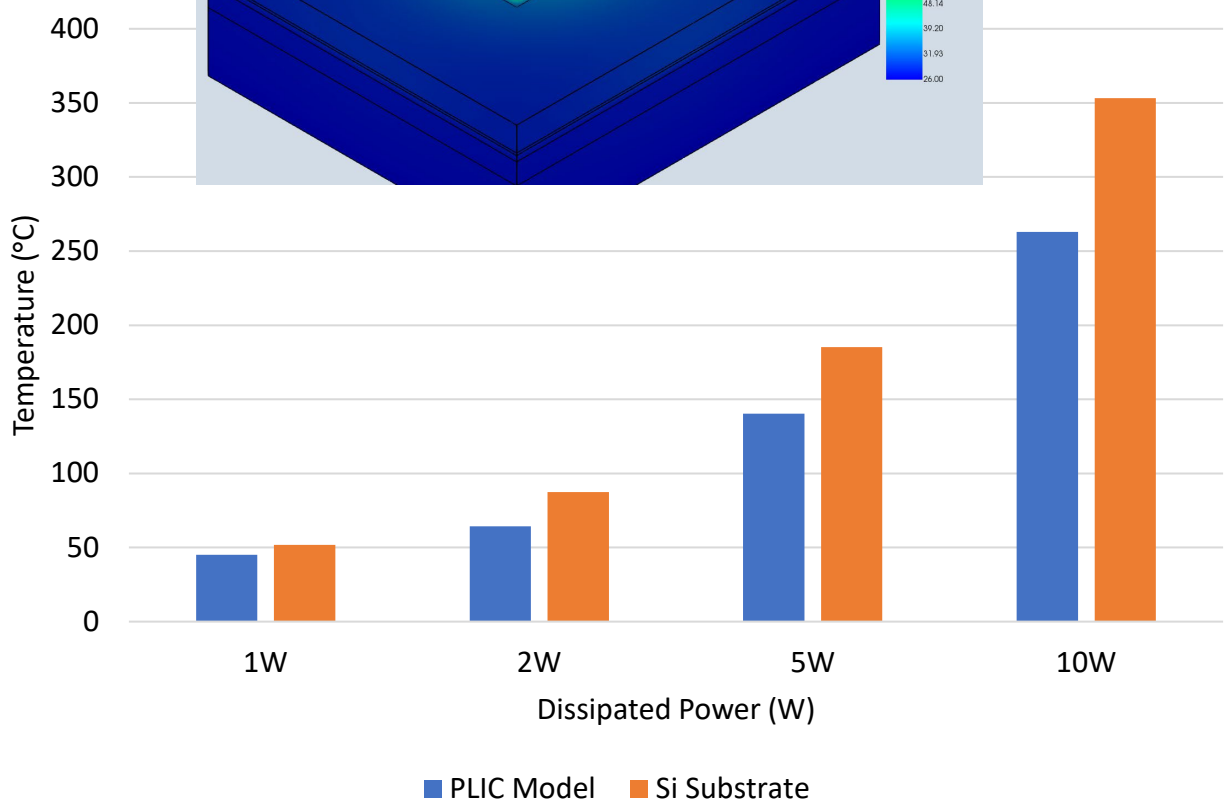

Silicon Based Model



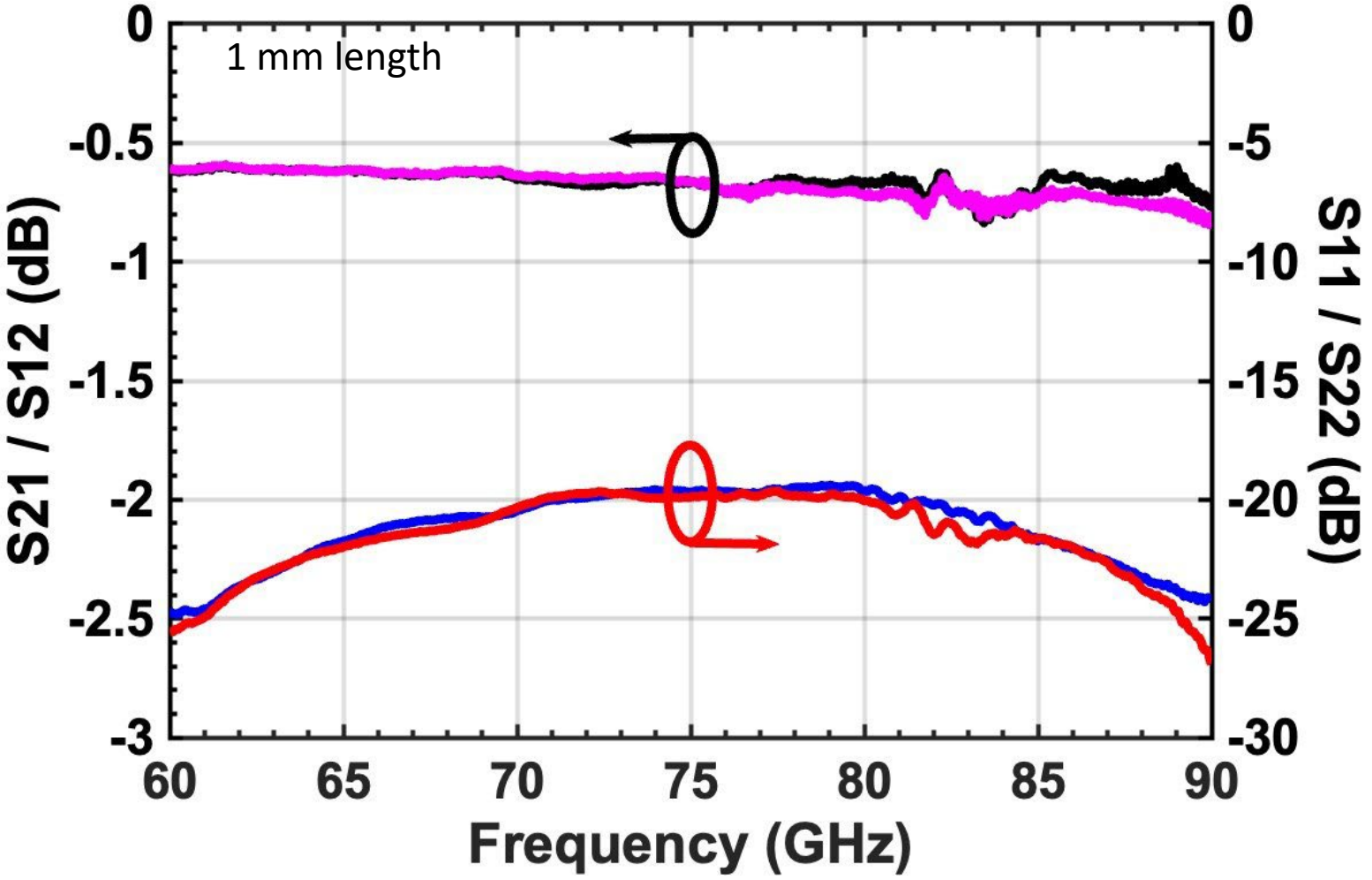
# PLIC Transistors outperform GaN-on-Si

- Temperature spread widens as dissipated power increases
- Reported temperature is average temperature along the hottest gate finger
- 75um Substrate Difference
- 1W Pdiss - ~10 °C Difference
- 10W Pdiss - ~100 °C Difference



# Interposer Transmission Line is Low Loss



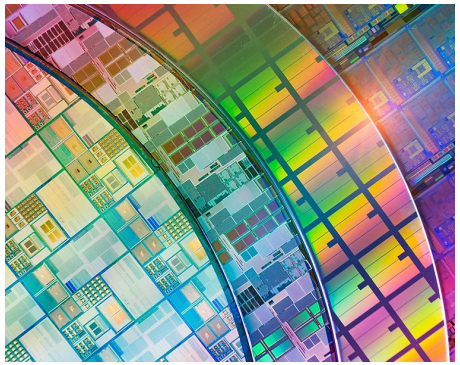
# Comparing against Other Manufacturing Approaches

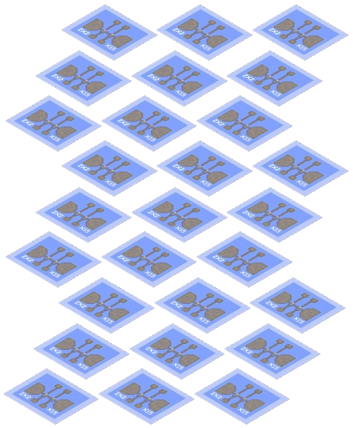
| | Design Flexibility | Mix and Match Technologies (Chiplet availability) | Thermal Management | Prototyping Cost |
|---|---|---|---|---|
| Wafer Bonding | Low | Low | Poor | Extremely High |
| Flip Chip | High | High | Poor | Medium |
| Micro-Transfer Printing | High | Medium | Poor | High |
| PseudolithIC | High | High | Great | Low |

# Design Examples and Measurement Results

# Unprecedented RF/MMIC Design Flexibility

From 1 or 2 chiplet runs:



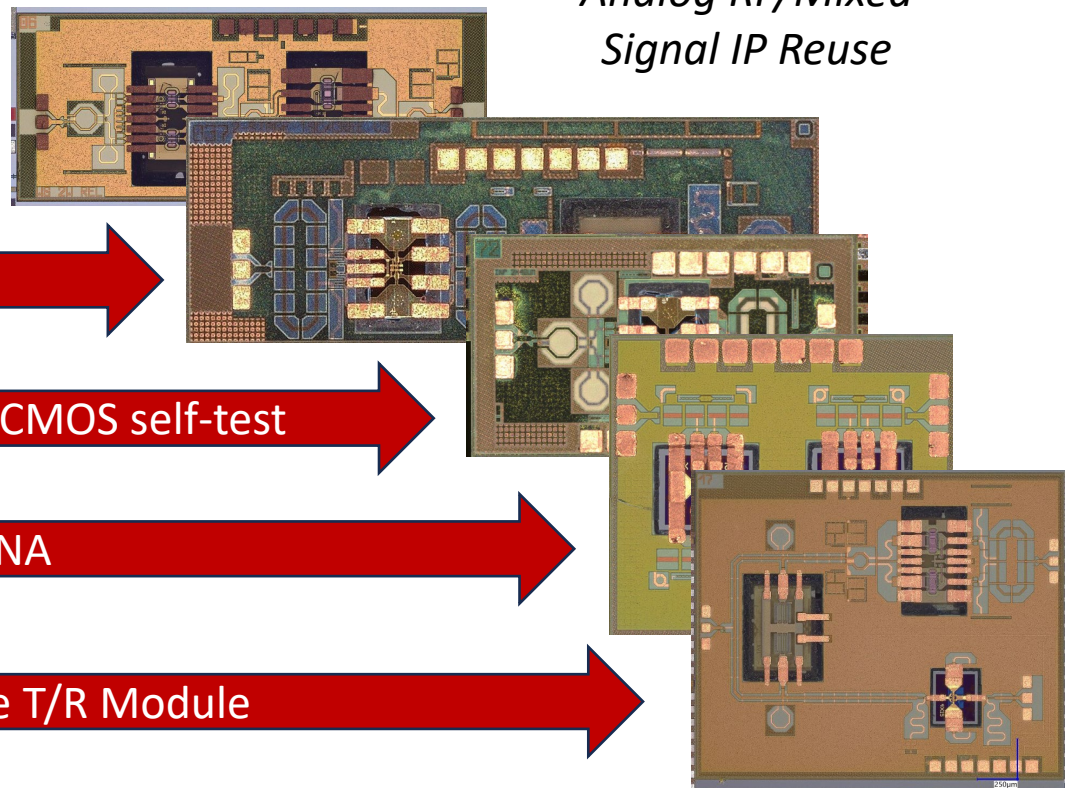


*10,000s of III-V µm-scale chiplets from a single run*

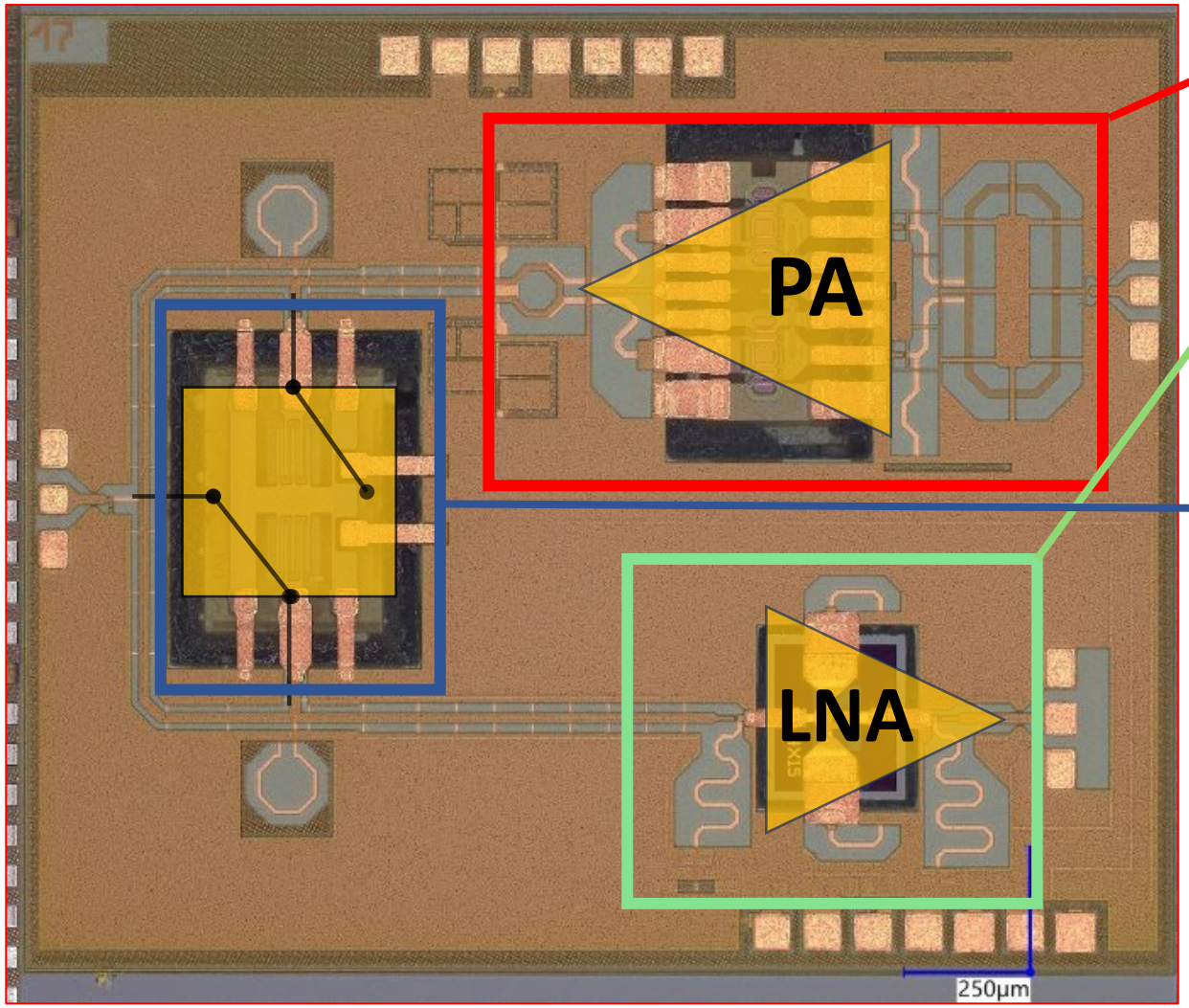
Dozens of different circuit topologies:

*Analog RF/Mixed Signal IP Reuse*

- 2W Two-stage GaN Power Amplifier
- First ever InP + GaN Two Stage Amplifier
- Ultra low noise InP amplifier with built-in CMOS self-test
- Two-stage InP HEMT LNA
- First ever InP + GaN Complete T/R Module



# High-performance T/R for Low-cost Phased Arrays



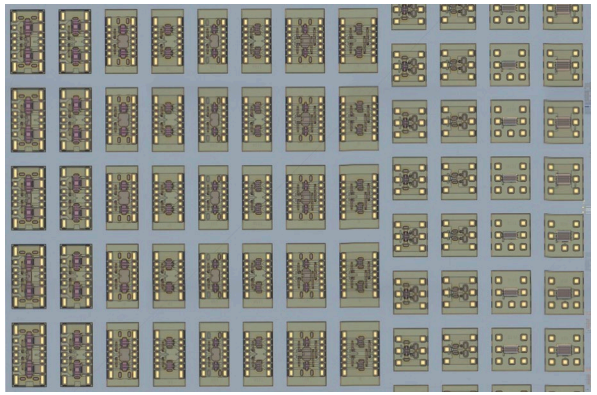

- 150nm GaN HEMT
- 90nm GaN HEMT

- 100nm InP HEMT
- 90nm GaN HEMT
- CMOS SOI

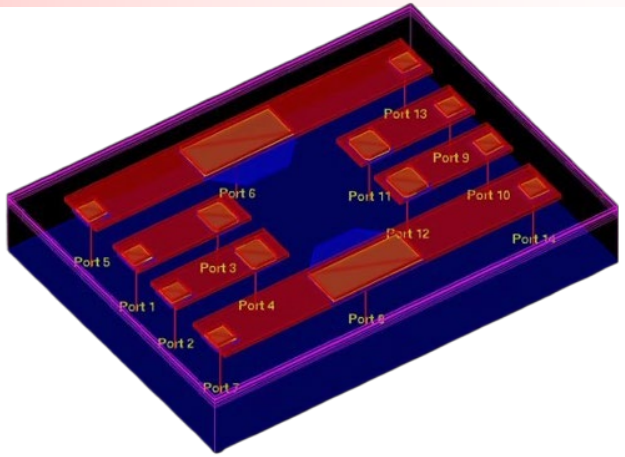
- 90nm GaN HEMT
- CMOS SOI

- Upgrades with CMOS SOI
  - SPI Interfaces
  - Power management
  - Multiple channels on one die
  - Compatibility with flipchip packaging

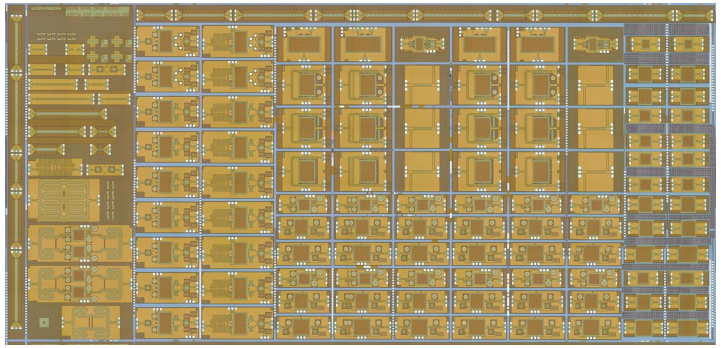
# PseudolithIC Design Flow



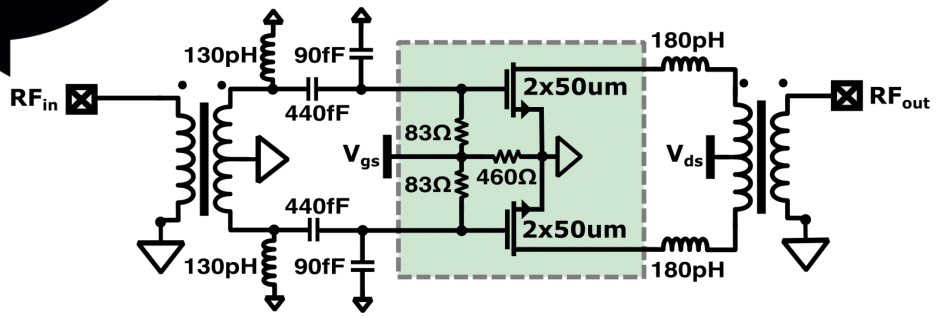
Chiplet Design




Interconnect Design



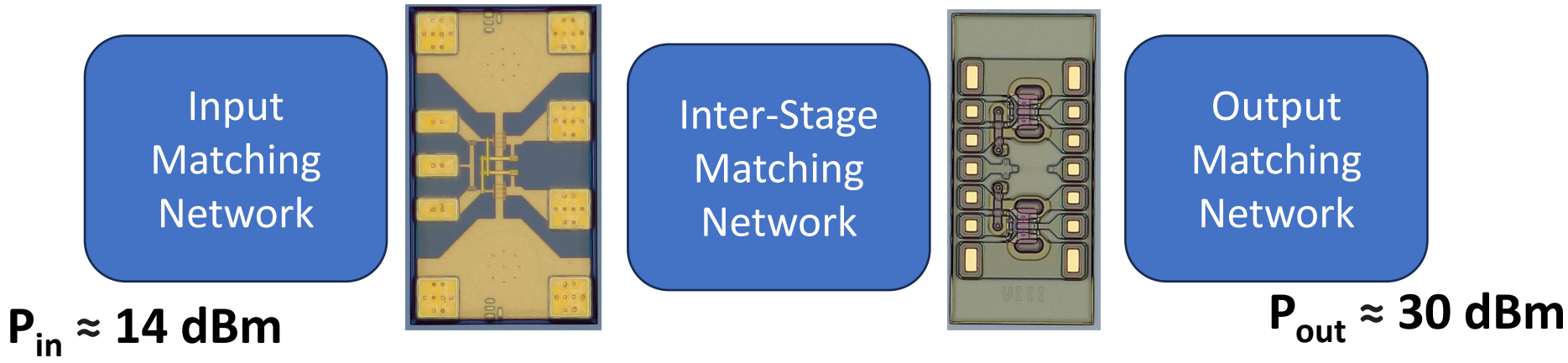
Interposer Design




Schematic Design

# Towards InP / GaN Amplifier

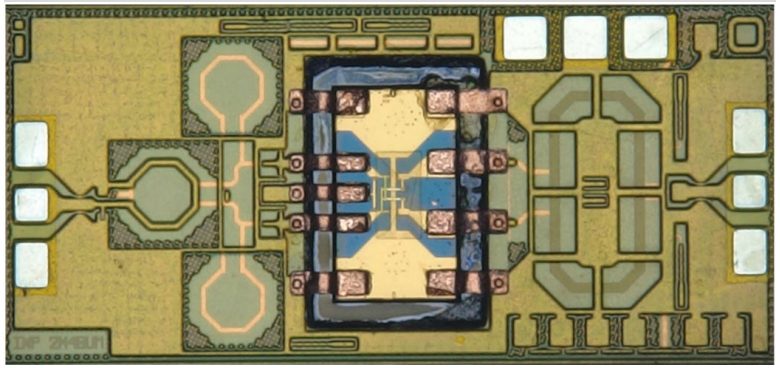
- InP HBTs were explored for a high-bandwidth pre-driver
- GaN HEMTs were explored for a high-power output stage
- Ka-band design

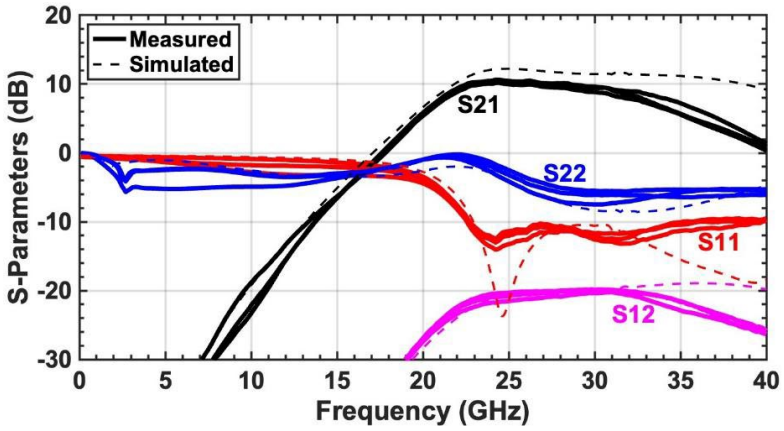


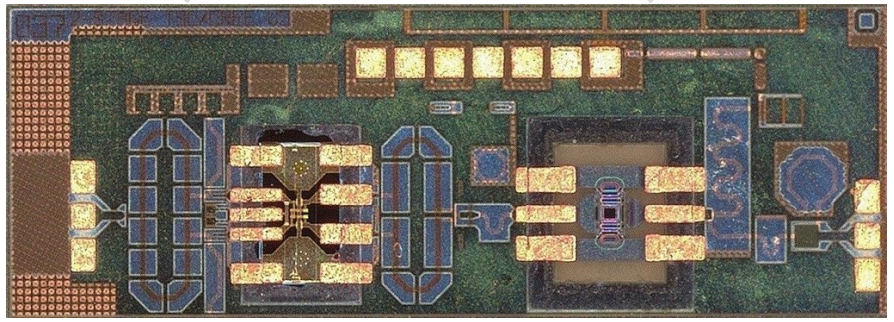
# Mix-and-Match Pseudolithic Integrated Circuits

- InP/GaN actives simultaneously integrated onto a passive silicon interposer

**InP HBT Pre-driver**

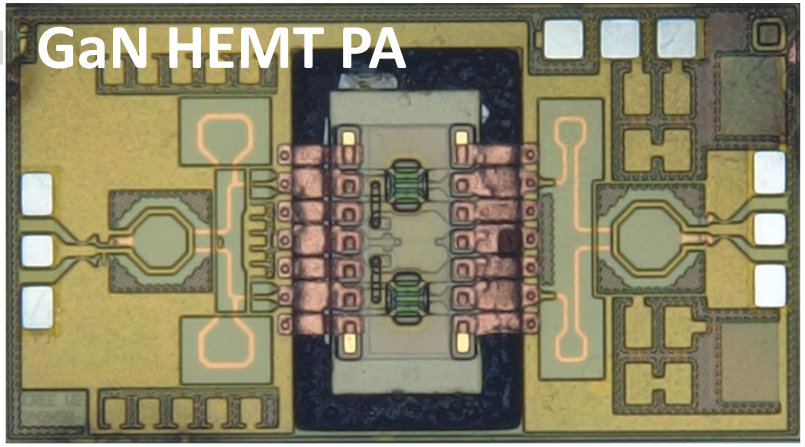


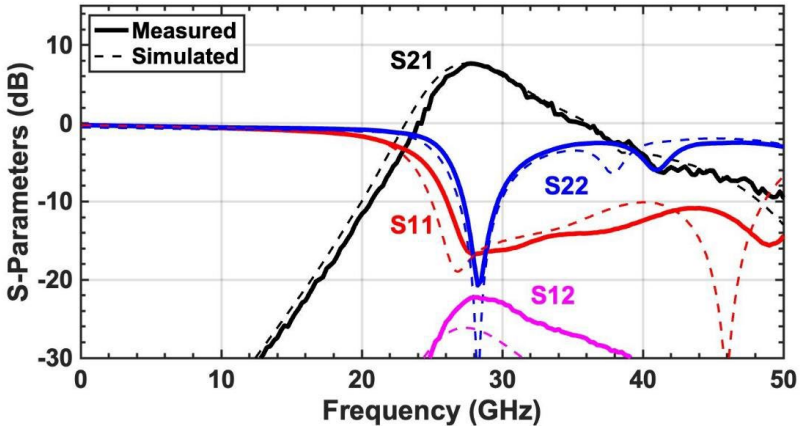


*World's first InP/GaN multistage integrated amplifier at 28 GHz*

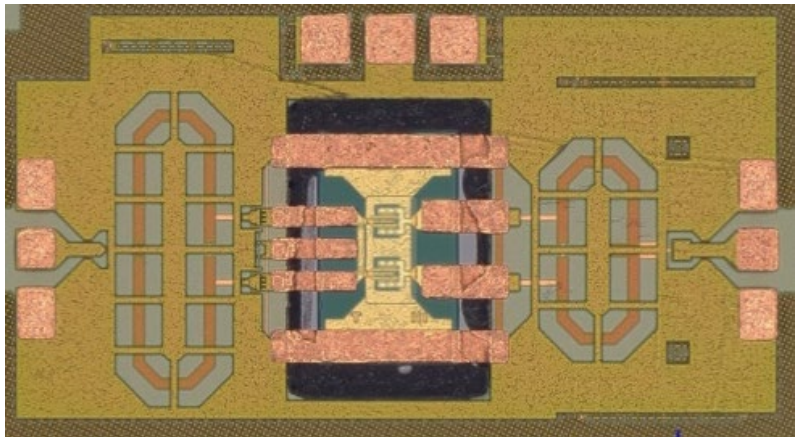
**GaN HEMT PA**

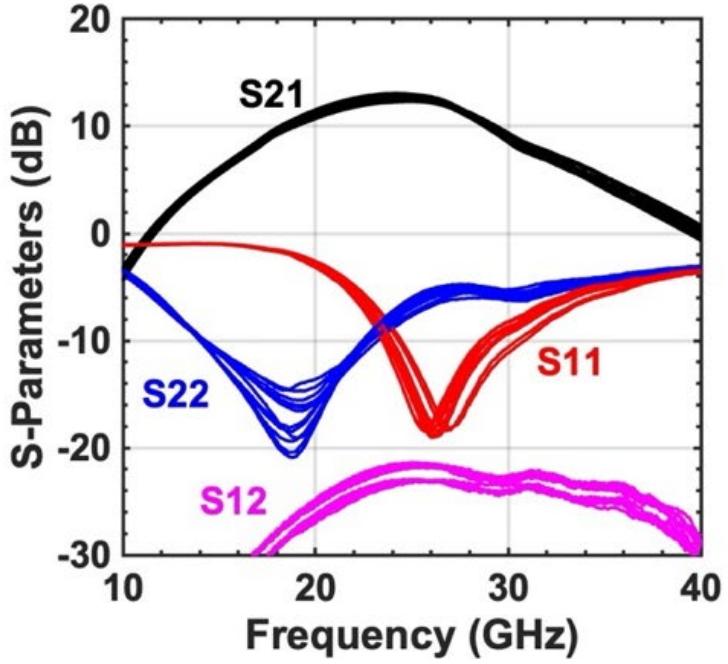


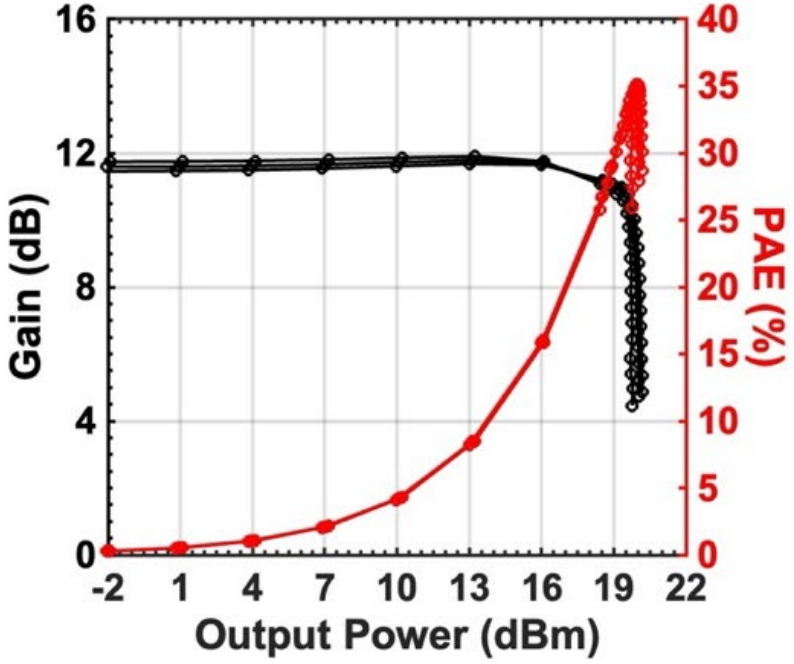


# Another Example - InP 250-nm HBT PA

- Mature 250-nm InP HBT technology
- More than 13 dB gain per stage
- Excellent gain compression
- PAE exceeding 35%






J. Kim et. al, RFIC 2024

*World's first InP/GaN multistage integrated amplifier.*

# TRX Circuit Performance Targets

| Bands | | X (8-12) | | Ku (12-18) | | K (18-27) | | Ka (27-40) | E (71-86) |
|---|---|---|---|---|---|---|---|---|---|
| Transmit | Psat (W) | 2 | 5 | 2 | 4 | 2 | 4 | 2 | 1 |
| | Gain (dB) | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 |
| | PAE (%) | 50 | 45 | 40 | 38 | 38 | 35 | 30 | 15 |
| Receive | NF (dB) | 1.2 | 1.2 | 1.5 | 1.5 | 2 | 2 | 2.5 | 3 |
| | Gain (dB) | 15 | 15 | 15 | 15 | 18 | 18 | 20 | 25 |
| | DC Power (mW) | 10 | 10 | 15 | 15 | 30 | 30 | 20 | 400* |
| * with I/Q down converter and multplier chain | | | | | | | | | |

# X+ CMOS as a Key Differentiation

# CMOS Capabilities within III-V Amplifiers

I. **Built-in self-test (BIST):** By building self-test with analog signals and/or digital scan chains, the health of a heterogeneously integrated solution can be assessed without costly test.

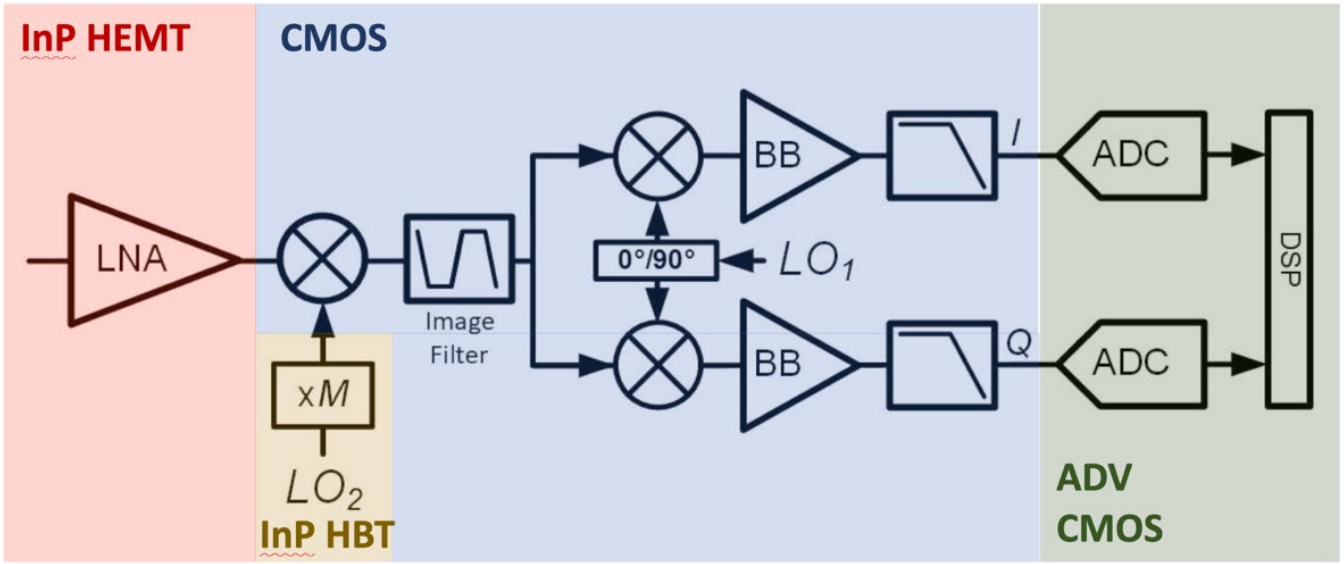
II. **Biasing and power management:** CMOS nodes support biasing circuits that trim devices locally rather than requiring external monitoring and compensates device-to-device variation and circuit yield.

III. **RF signal blocks:** Mature CMOS processes are capable of being used for a variety of applications up to 90 GHz.

IV. **Signal processing:** Digital signal processing is introduced by using different CMOS IP blocks, possibly as chiplets, and incorporated into the solution.

# E-band Receiver

- PseudolithIC is demonstrating multi-technology capabilities at E-band 71-86 GHz for new levels of performance.
- InP HEMT give path to 2-dB noise figure
- InP HBTs offer high multiplier conversion gain and output power
- RF CMOS for I/Q downconverter.




Will be presented at IEEE IMS "A CMOS-Enabled Heterogeneously-Integrated InP HEMT W-band LNA with 2.8-dB Noise Figure at 7.7-dB Gain and 4.5mW $P_{DC}$"

# Conclusions

- Mix and Match integration for millimeter-wave applications unlocks new performance capabilities
  - Power Amplifier, Low Noise Amplifier, Switch
  - Transmit/receive modules
- Low-cost silicon platform supports rapid prototyping iterations and product development (Accelerate Lab to Fab)
- Excellent Thermal Dissipation
- X+CMOS offers exciting opportunities for mix and match of compound semiconductors with analog, digital and RF circuits.