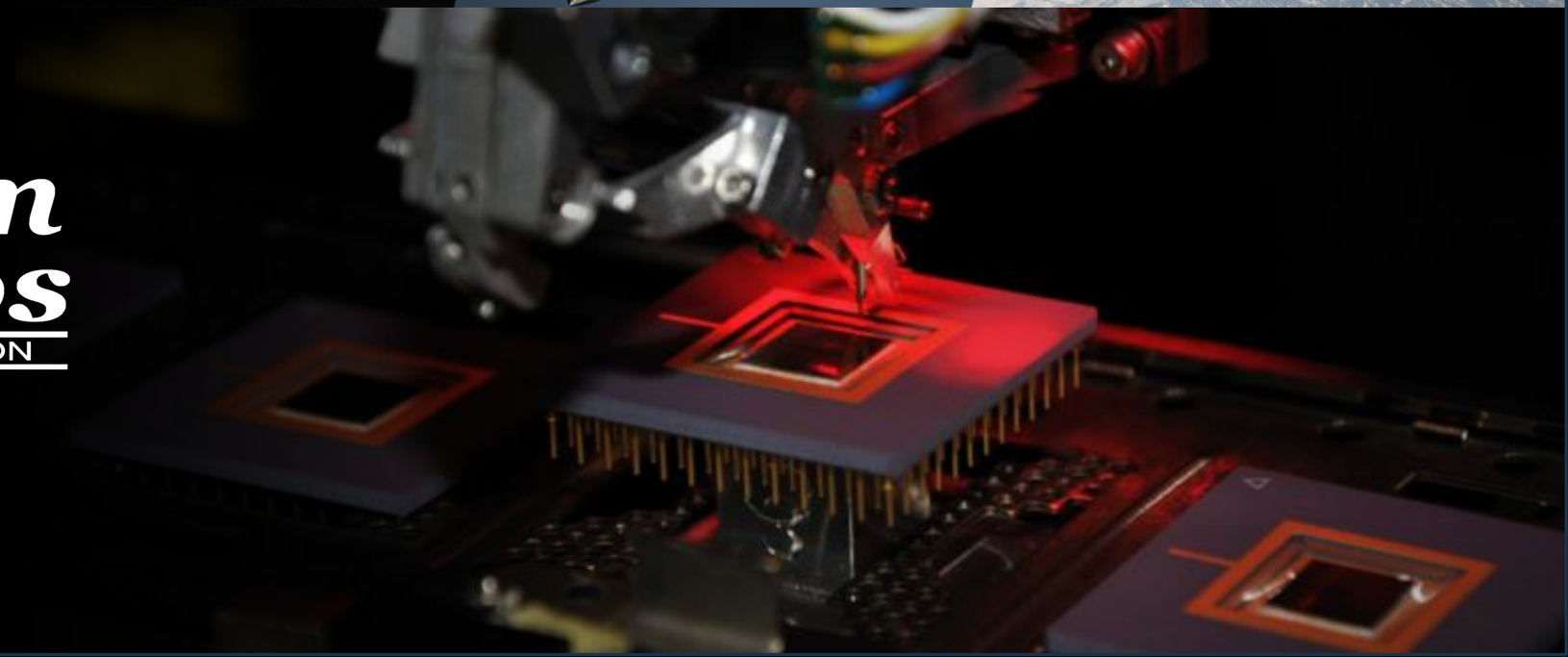
Lessons Learned from Buying Commercial wafers for MIL Project

Golden Altos CORPORATION



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Chair of JC-13 Committee: Government Liaison

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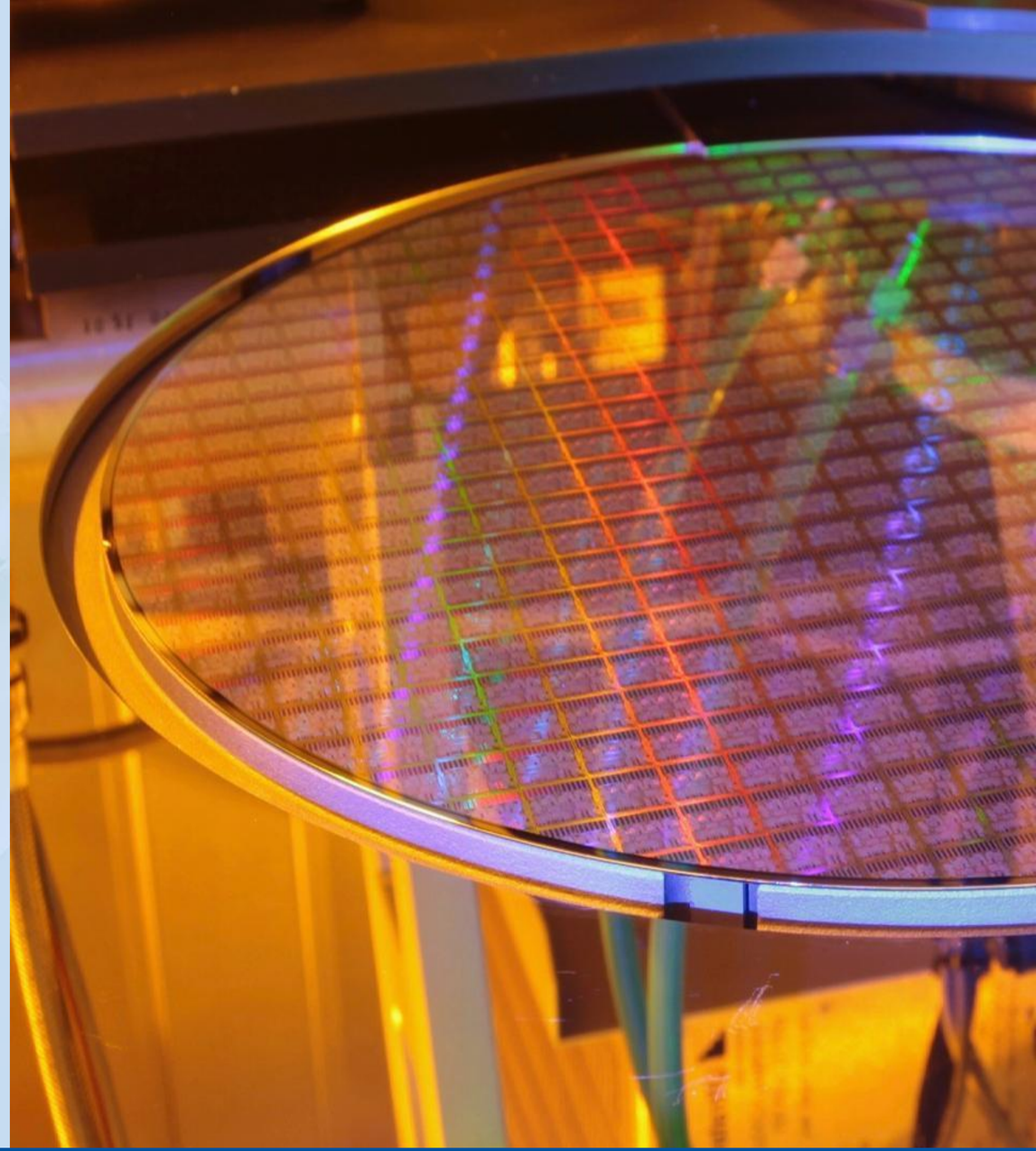
What Drives the Semiconductor Market?

Commercial Goods Drive Market

- Rapid Innovation
- Economies of Scale
- Volume Feeds the Fabs
- Die Area Remains King
- Return on Investment
- Wafer Real Estate
- Fab Must Monitor Process



Historical Perspective

From the start, Military and Aerospace could drive the semiconductor industry. How? $$$

First Integrated Circuits (ICs)

- Slower than discrete solutions / low integration
- Expensive

Aerospace & Military Systems

- Reduced power consumption
- Smaller size

Commercial World

- Used discretes and/or tubes
- Digital not important

IC Designs & Longevity

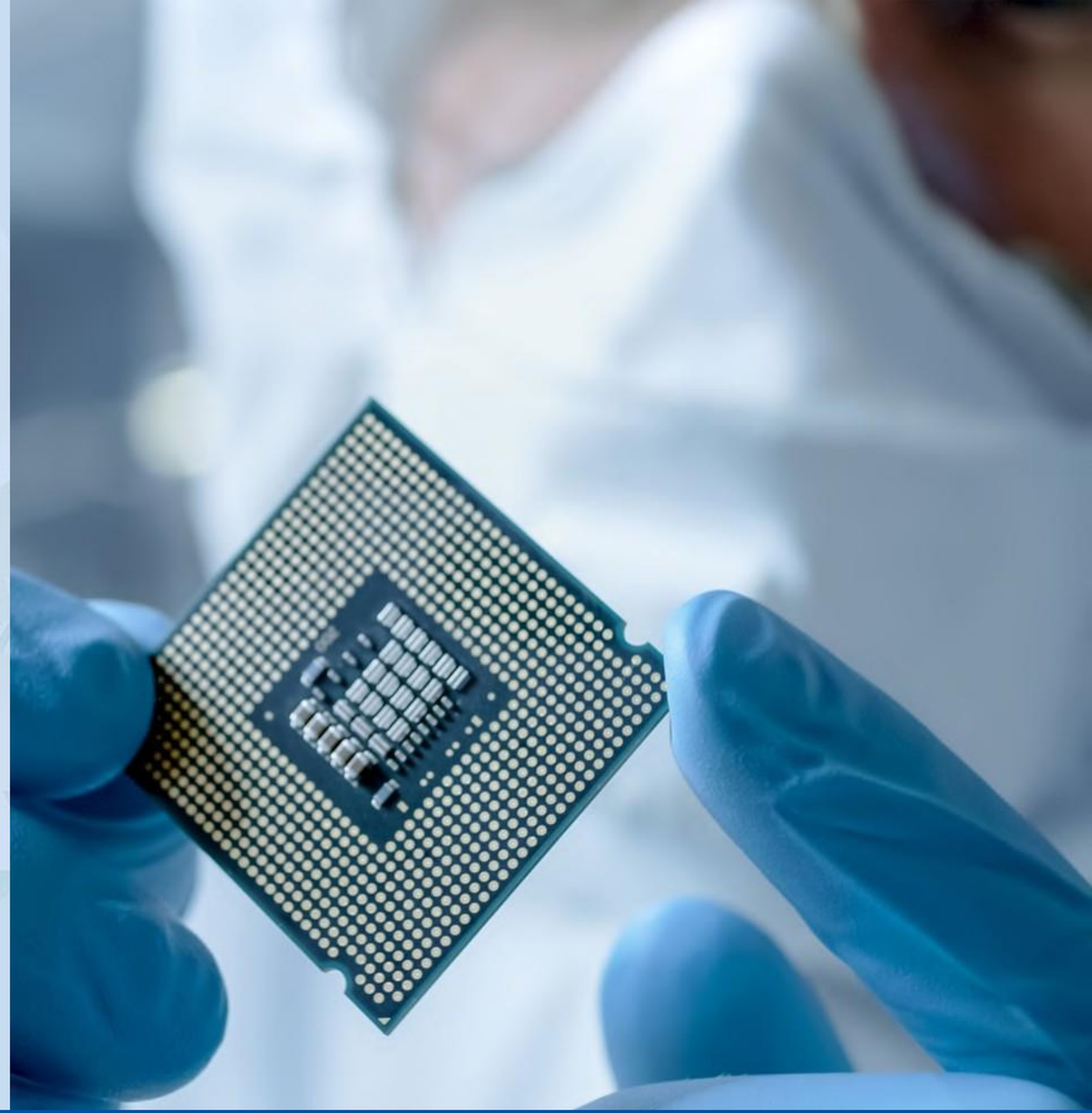
Aerospace & Military No Longer the Driving Factor

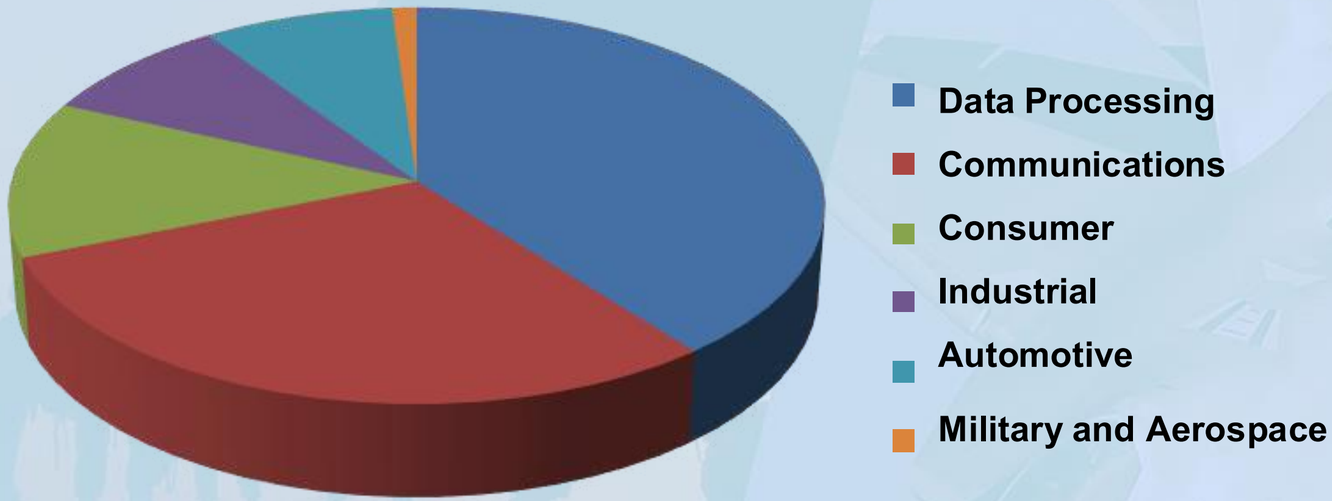
New Designs follow the commercial world

- Wheel reinvention not cost effective
- Market-drive advanced devices not typically offered in hermetic packaging include:
  - Networking controllers, tranceivers
  - Multimedia audio/video processors

QML Manufacturers aren't driven directly by the commercial world

- Device longevity a prime consideration





Semiconductor Market

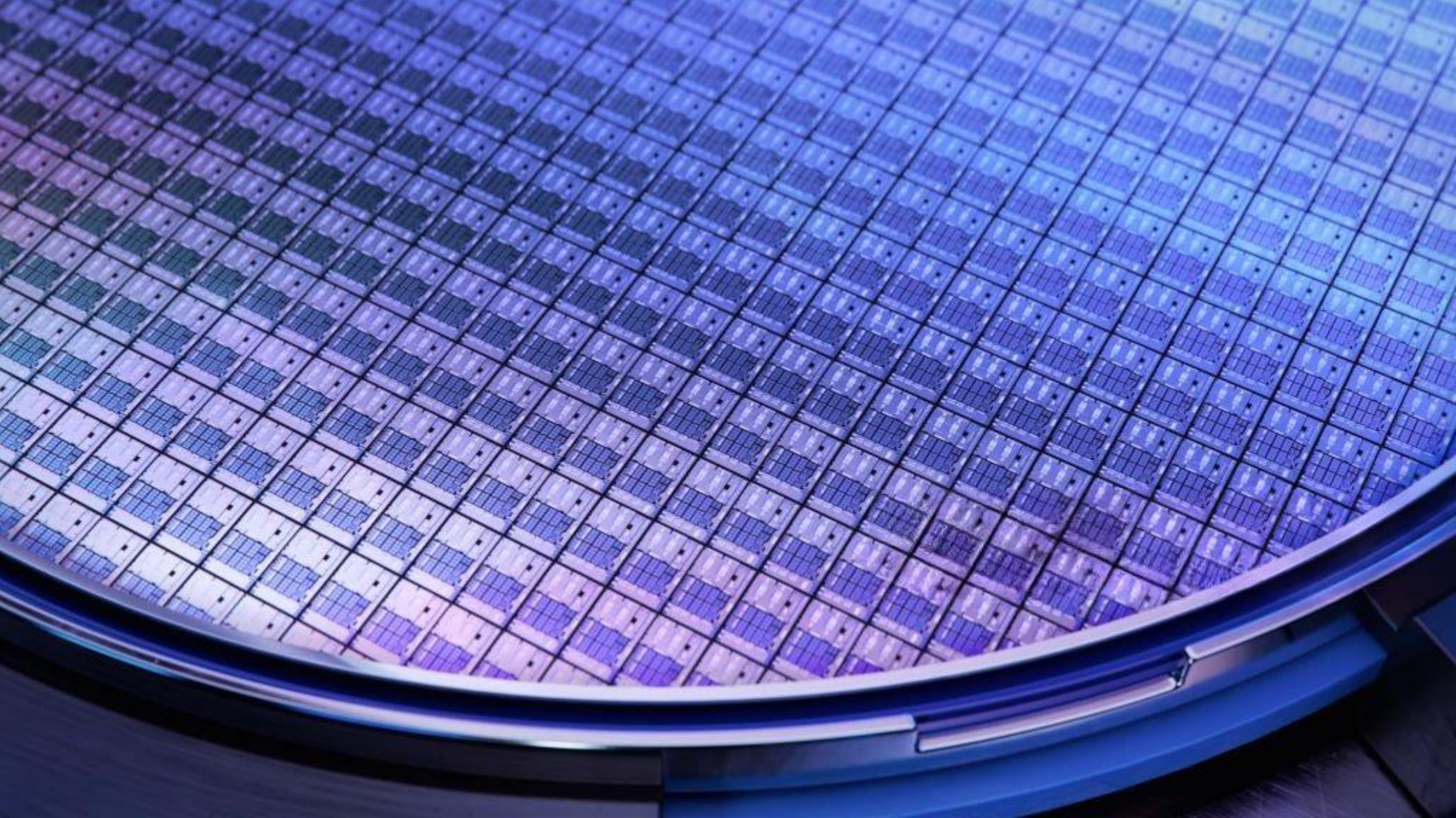
QML Hermetic ICs (Integrated Circuits) occupy a unique initial cost point in the $409 billion semiconductor market (World Semiconductor Trade Statistics, November 2019)

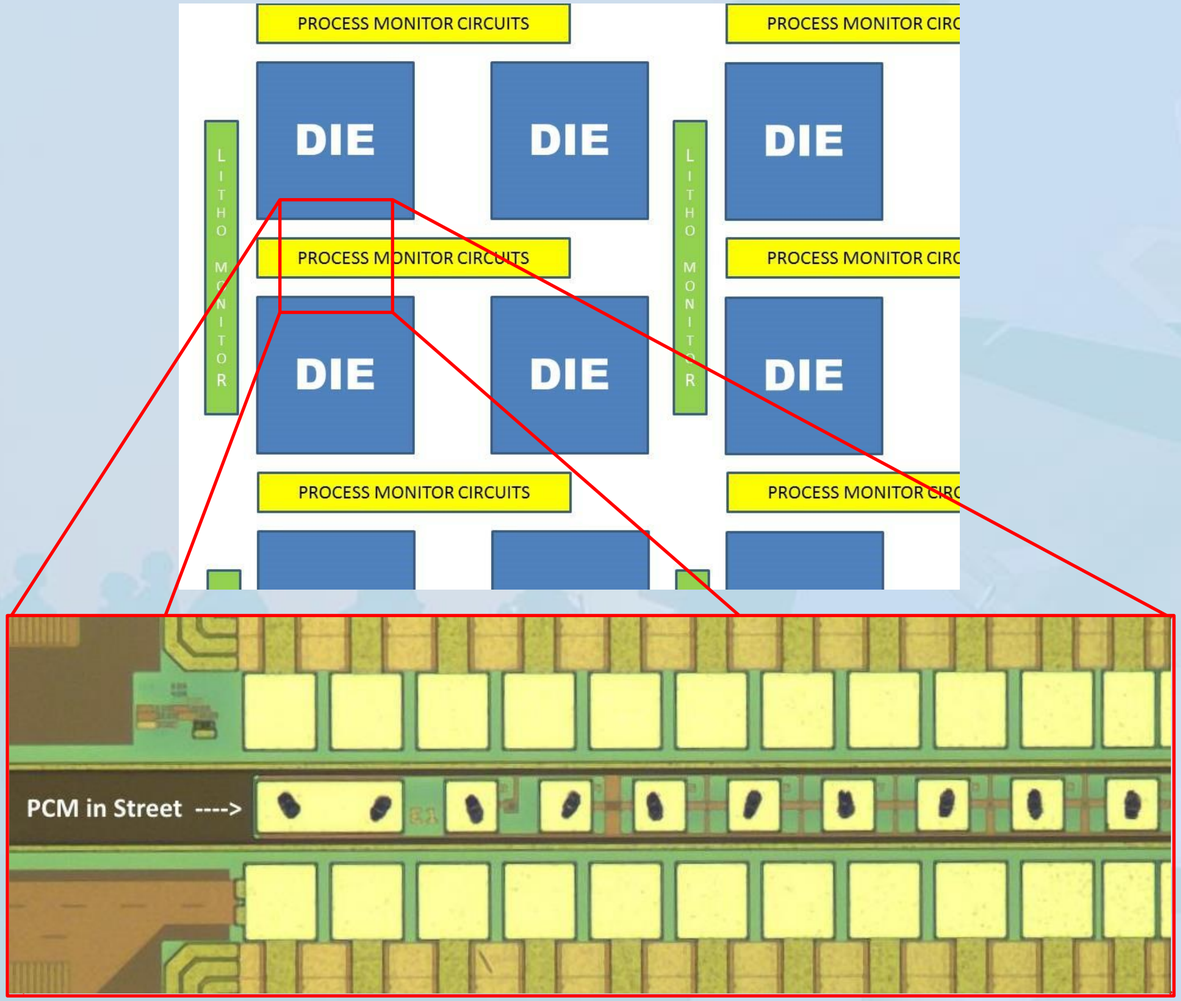
Cost always a concern. What drives that cost?

- Low Volumes (<1%)
- Stringent Quality Requirements
- Sporadic Purchasing Requirements

Approaches to reducing costs include:

- Commercial Off-The-Shelf (COTS)
- Upscreened Parts
- Using commercial die for hi-rel





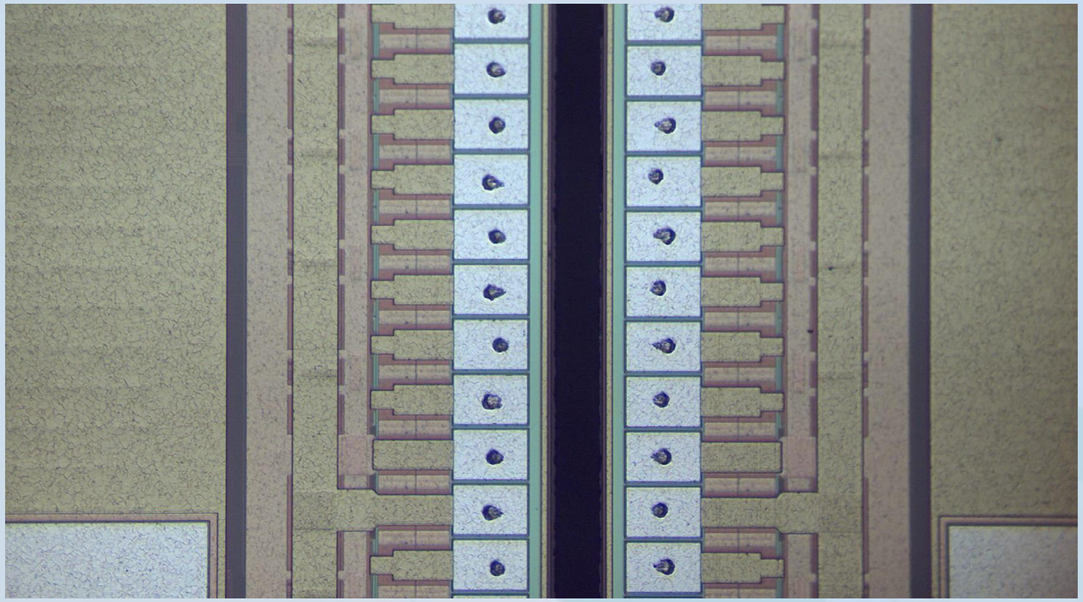
Process Control Monitors (PCMs)

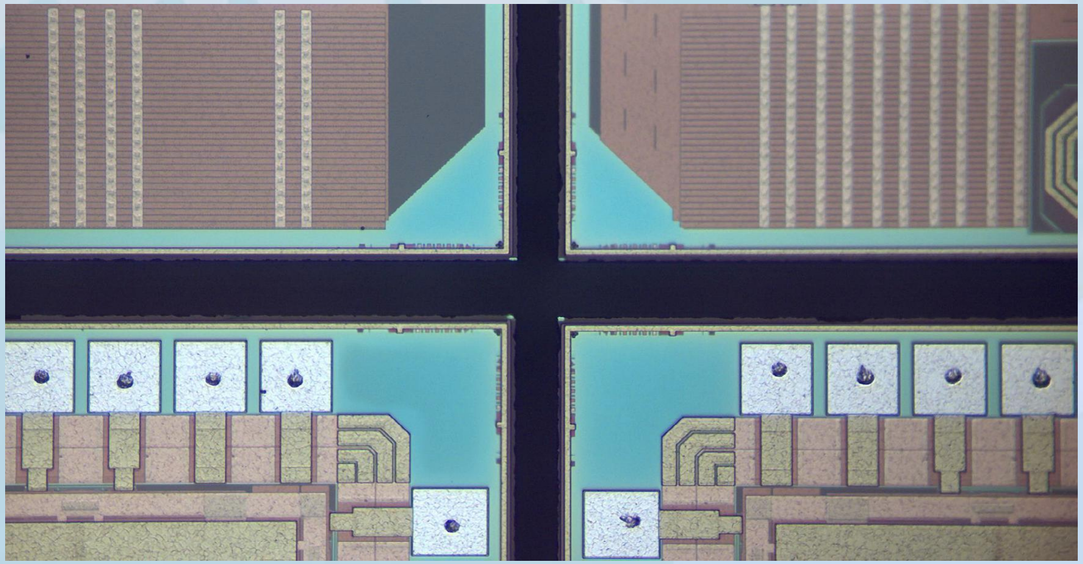
Test Circuitry in the Wafer Streets

Commercial & Industrial Market Influences:

- Increased yield to maximize productivity
- Reduced Cost

Hermetic packages require the removal of PCM while Plastic Encapsulated Microcircuits (PEMs) do not





Saw Solution

Single Cut with Wide Blade

- Blade and Travel Speed Critical
- Alignment tight between dice
- Wider Blade generates far more silicon dust than other options
    - Surfactant
    - Water Pressure

Double Rows of PCMs

Single Cut with Wider Blade?
- Chip Outs Become Worse
- Too Much Silicon Dust

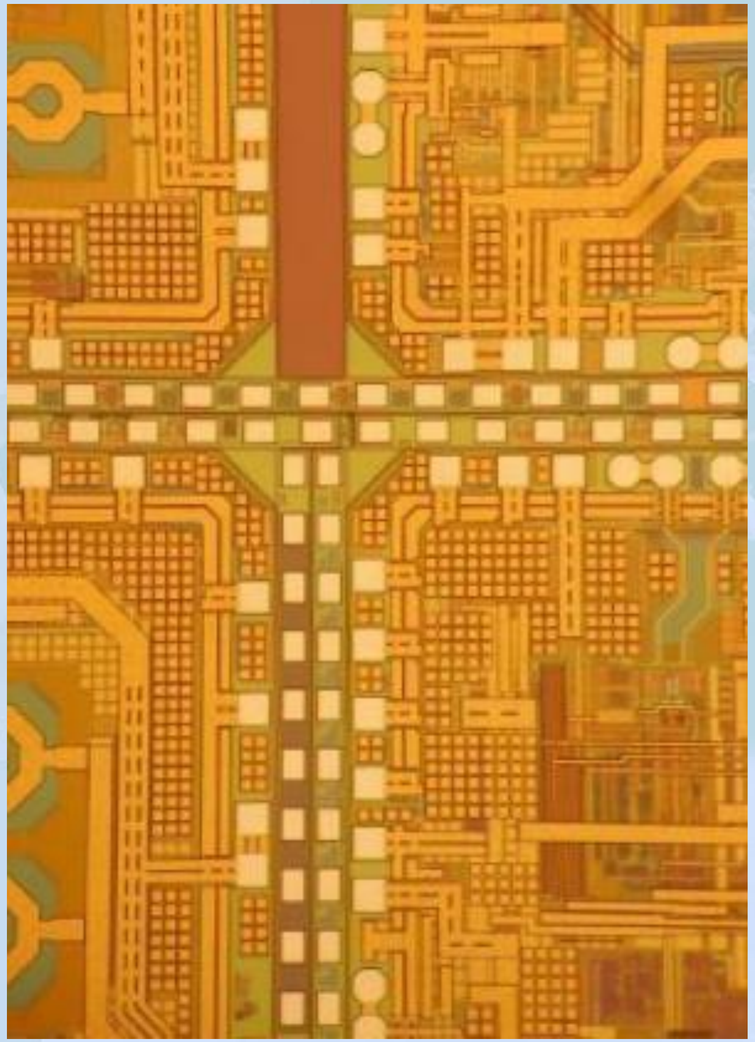
Narrow Blade Down the Middle?
- Not Enough Room

Remove a Single Row Leaving the Other Intact
- Similar to Previous Technique
- Same Issues / Concerns

Remove a Single Row
- But Which One?

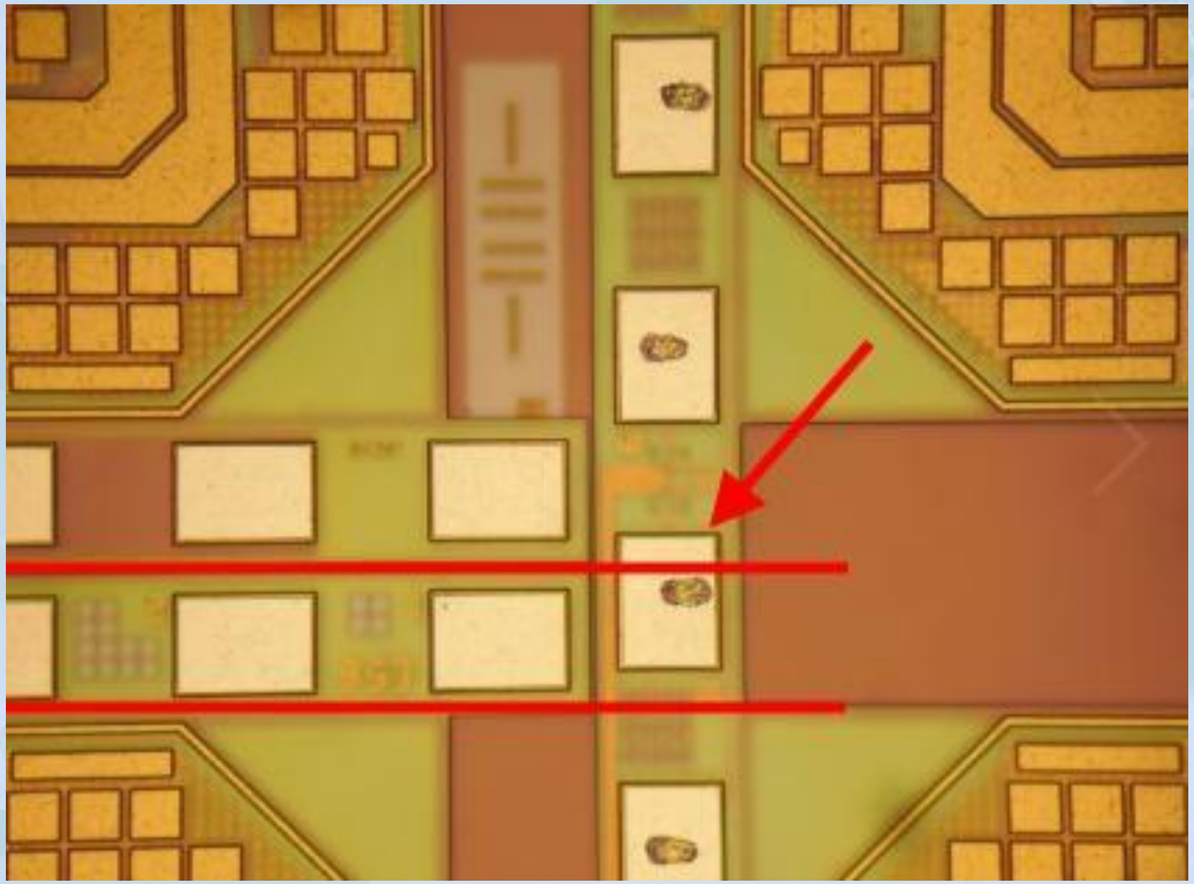
PCM Patterns Repeat in Both X and Y
- Not Tied to Die Size

Intersections Will Vary Across the Reticle



Double Rows of PCMs

- Intersections Can Be Problematic
- Cut on Either X-row Leaves Possible Displaced Metal
- Some Die From Certain Wafer Locations Might Not Be Usable for Space



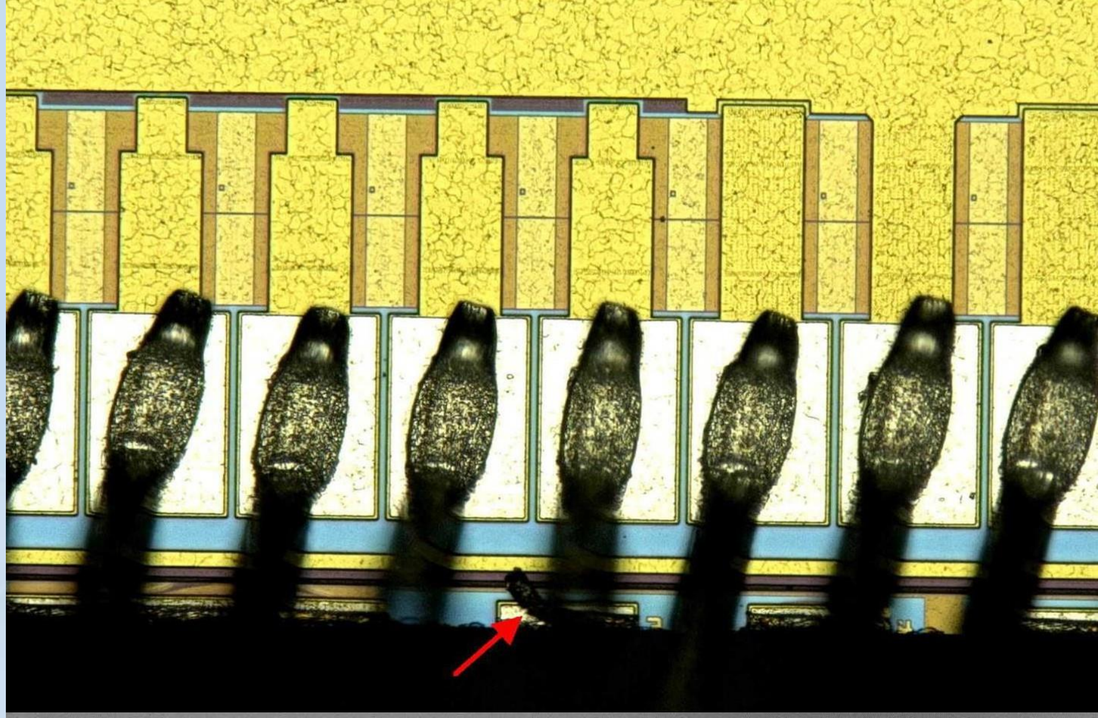
Saw Streets

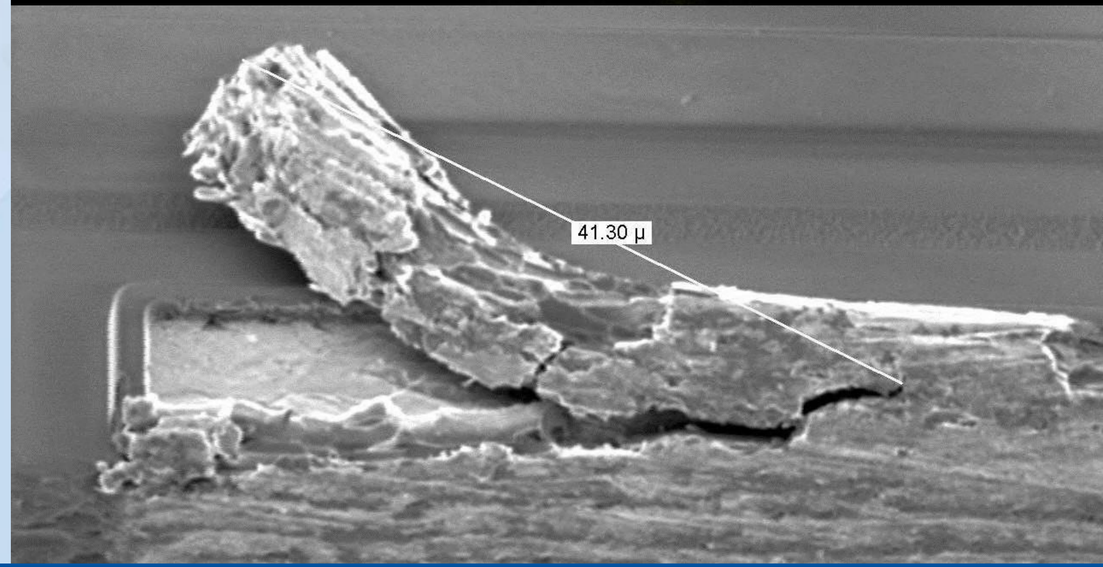
Cut Through PCM

- Disturbed Metal from Probe Pads

Plastic Encapsulation Traps this Metal

No-go for Hermetic Devices





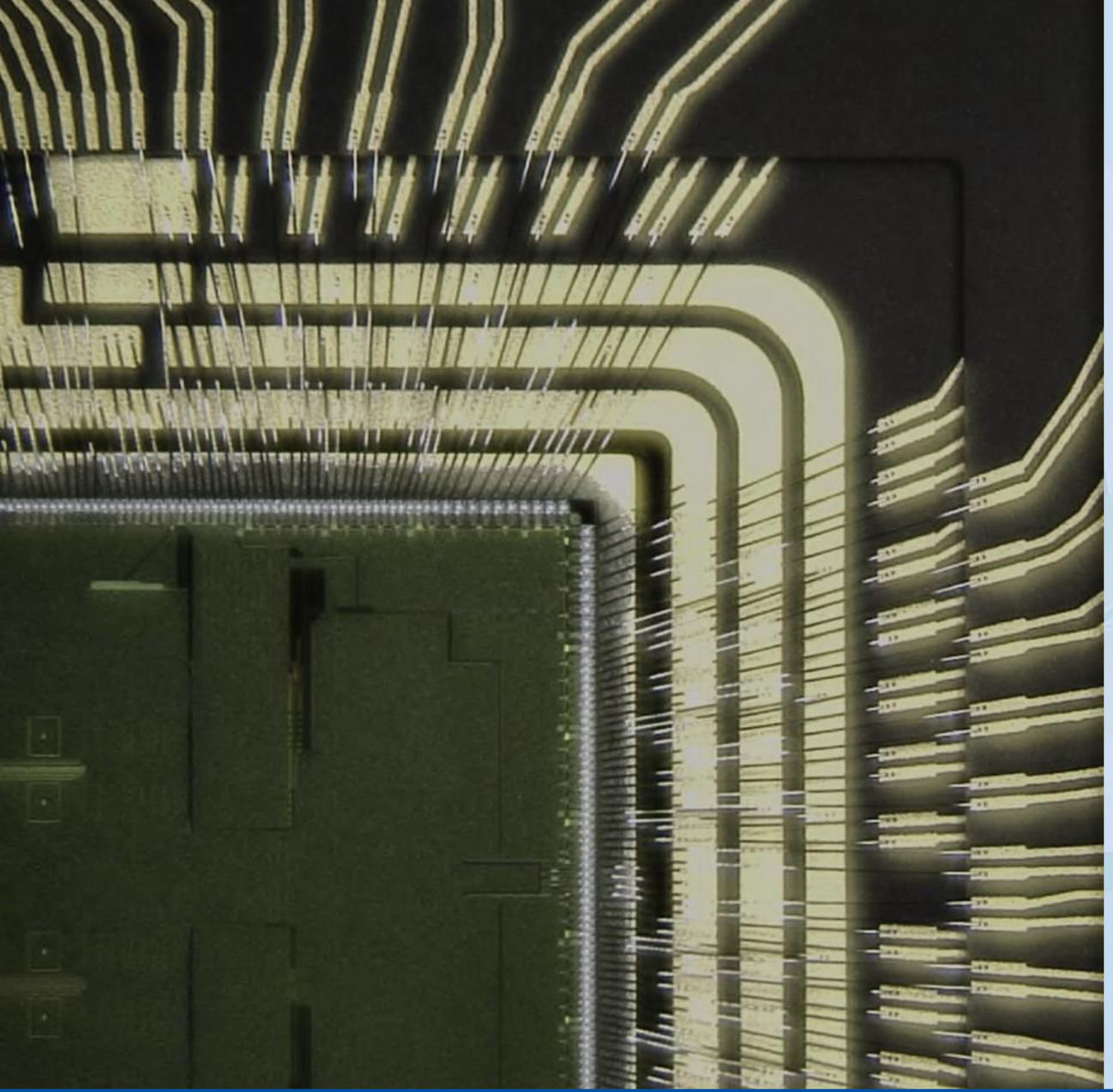
Gold & Aluminum Bonding Issues

Gold Bonding

- Plastic packages typically will use gold ball bond
- Bond angles greater than 30° do not affect the adjacent bond- wires exit the top of the ball bond and will not touch an adjacent wire, bond pad, or bond

Aluminum Bonding

- Aluminum wedge bonds are larger in dimesion than gold ball bonds
- Bond angles play a critical role in wedge bonds due to their physical structure



Wirebond Process Change

Solutions for Hermetic Package Assembly:

- Package layout redesign
- Smaller footprint wedges
- Changing the bond sequence from forward to reverse bonding

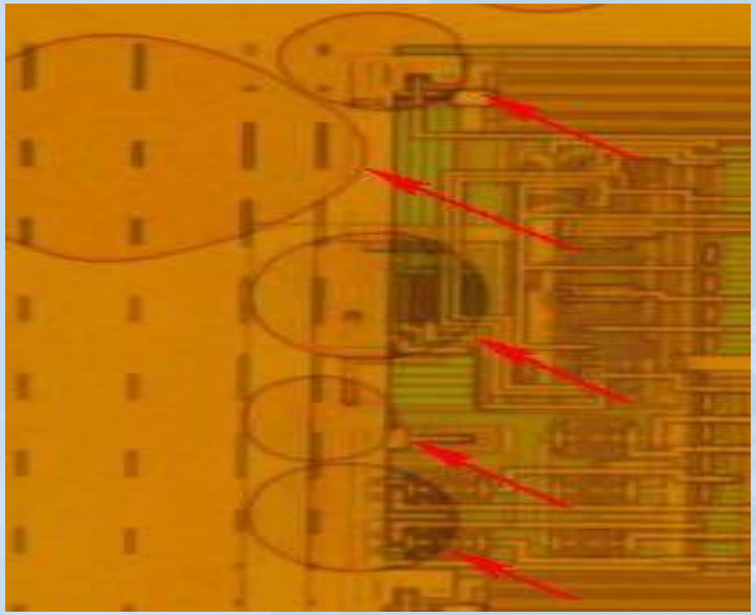
Other Electrical Considerations

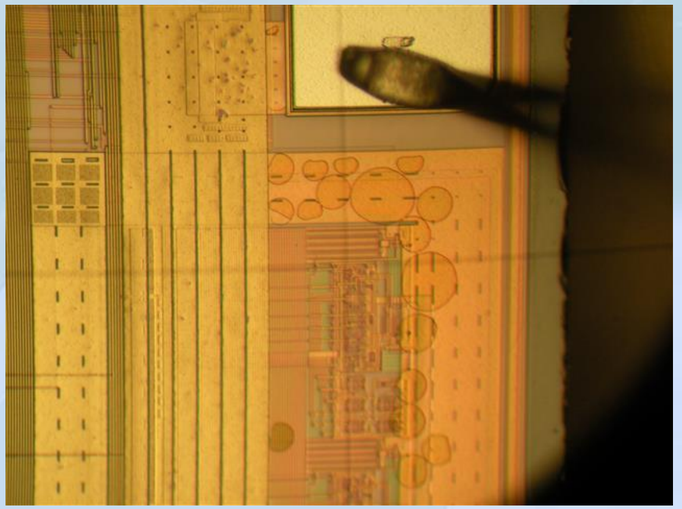
- Signal pairs where the impedance must be matched forces the length of these wire to be of similar dimension.

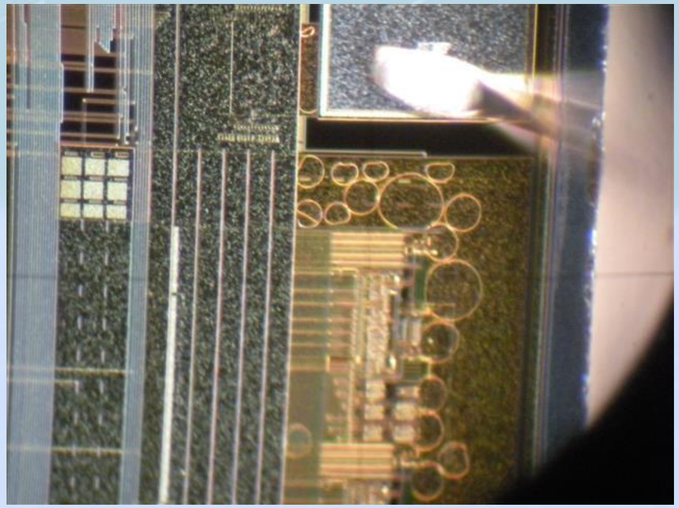
Package Seal Issues

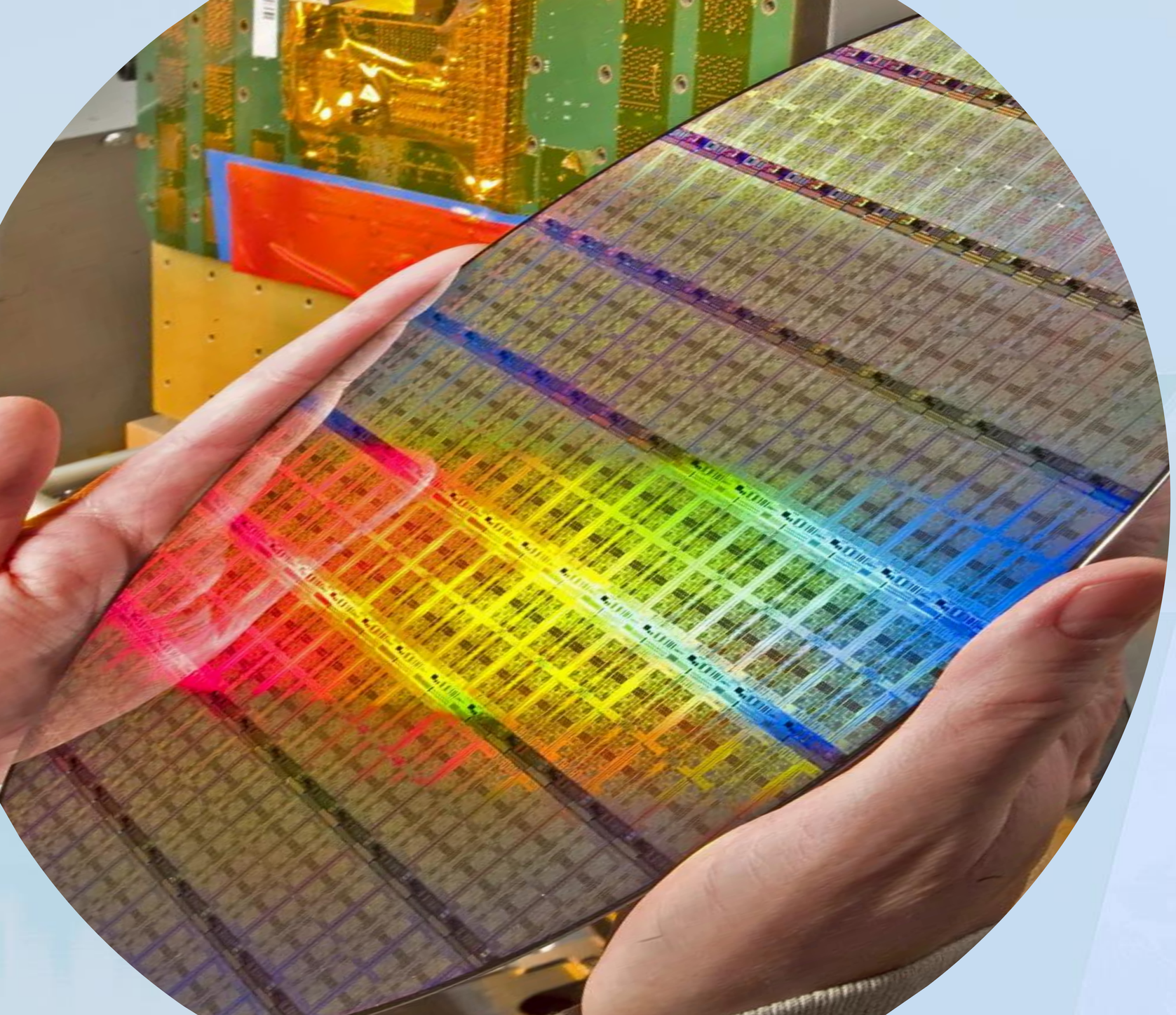
Die Coating

- Added during the wafer fabrication process
- Coating is used for additional protection of the circuitry from mechanical stresses caused by plastic encapsulation
- Die coat materials can be temperature sensitive and peel off or blister under high temperatures (typically greater than 300°C)







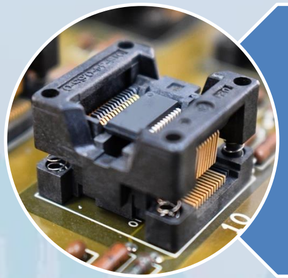


Company Profile

Our Services

Hermetic Assembly

- High reliability - Onshore - Monolithic – Hybrid
- Quick turn prototype or engineering lots and volume production
- Commercial, Military or Space level builds



Burn-in Services

- Board Design and Manufacturing
- Complete Burn-in with all standard environmental conditions
- Low volume qualification and high volume production

Qualification Services

- MIL-STD-883
- JEDEC-STD-22
- MIL-PRF-19500
- MIL-STD-750
- MIL-STD-202

Material Procurement

- Wafers, Dice, Packages, Lids, Pre-assembled Parts

Wafer Preparation

- Backgrinding, Inspection, Saw, Plating

Monolithic and Hybrid Hermetic Assemble

- Engineering Samples
- Space Flight Units

Qualification Testing

- Groups A, B, C, & D

Electrical Testing

Upscreening

Construction Analysis

Onshore Manufacturing

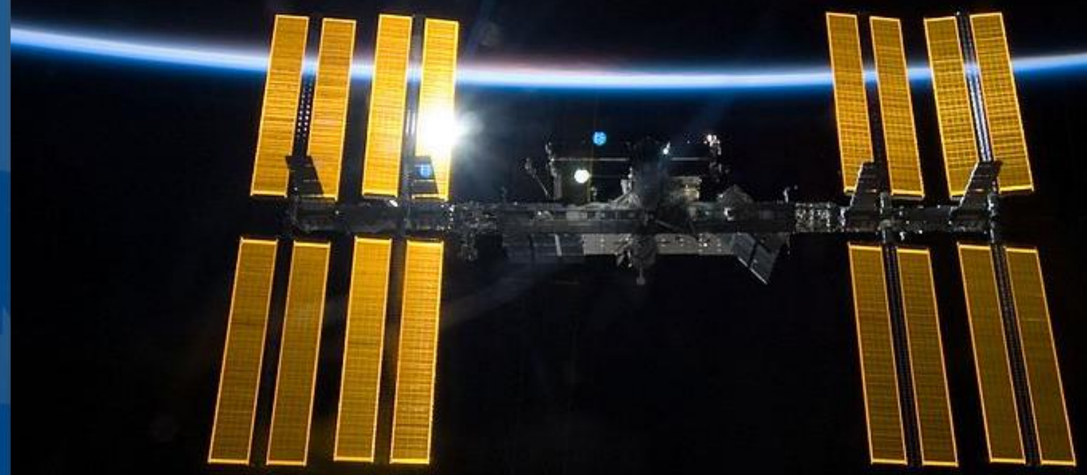
Located in Silicon Valley

Fremont, CA

Assembly Clean Room

Clean Room ISO Class 5 (Class 100)

What we do and how we do it matters



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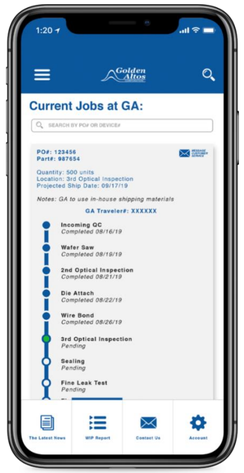

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