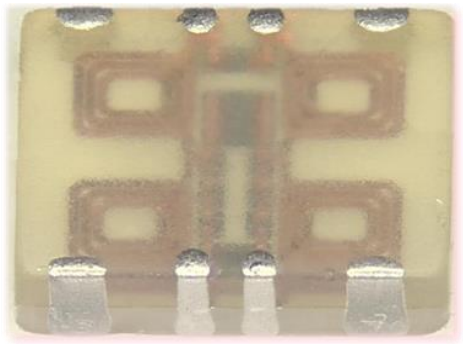
CMSE 2025

Integrated Thin Film Passive Components:

A New Option for Miniature Flight Electronics



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Outline

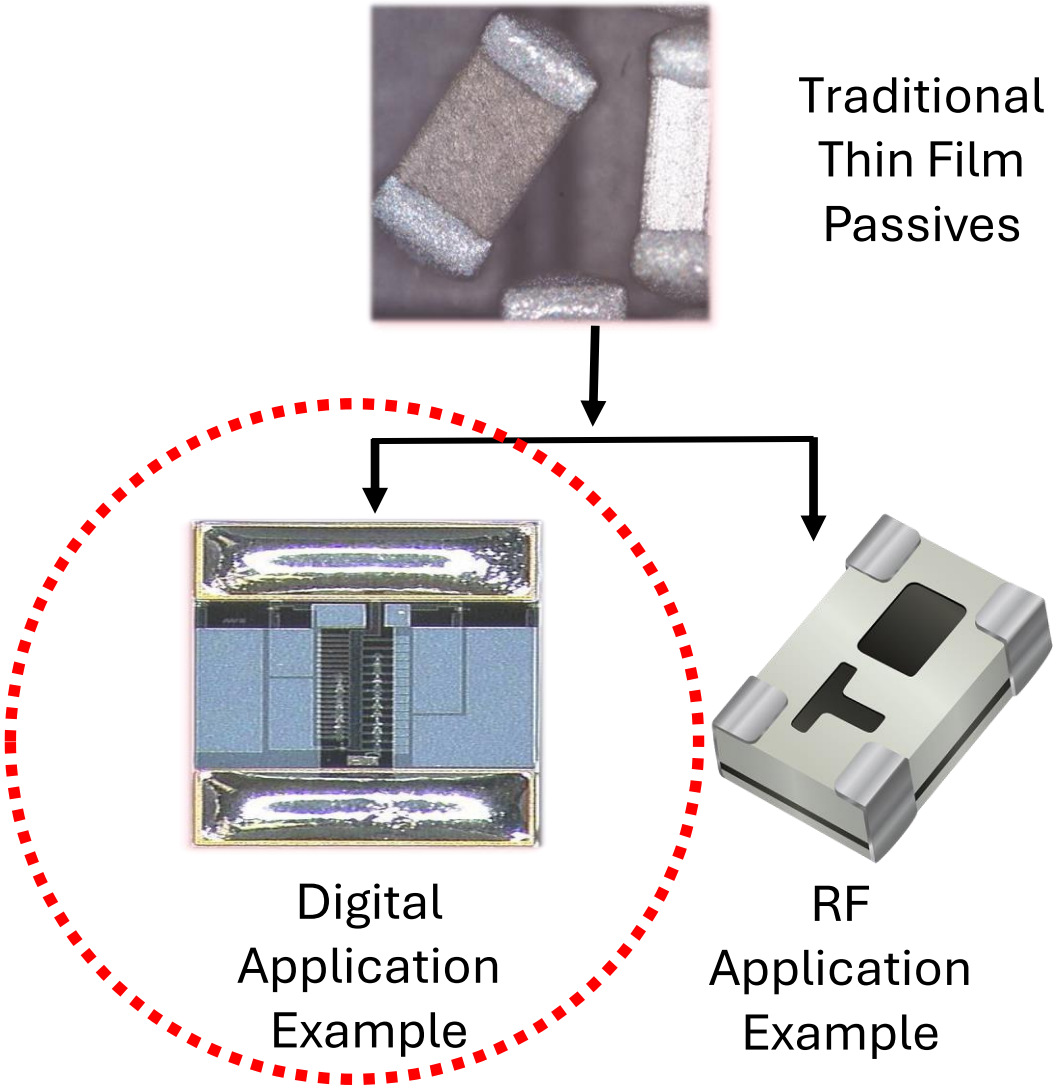
<u>Thin Film passives components advantages:</u>

- Size
- Weight
- Stable & repeatable electrical response

Review the state of **<u>integrated</u>** Thin film options:

Document & Discuss current state of the art integration

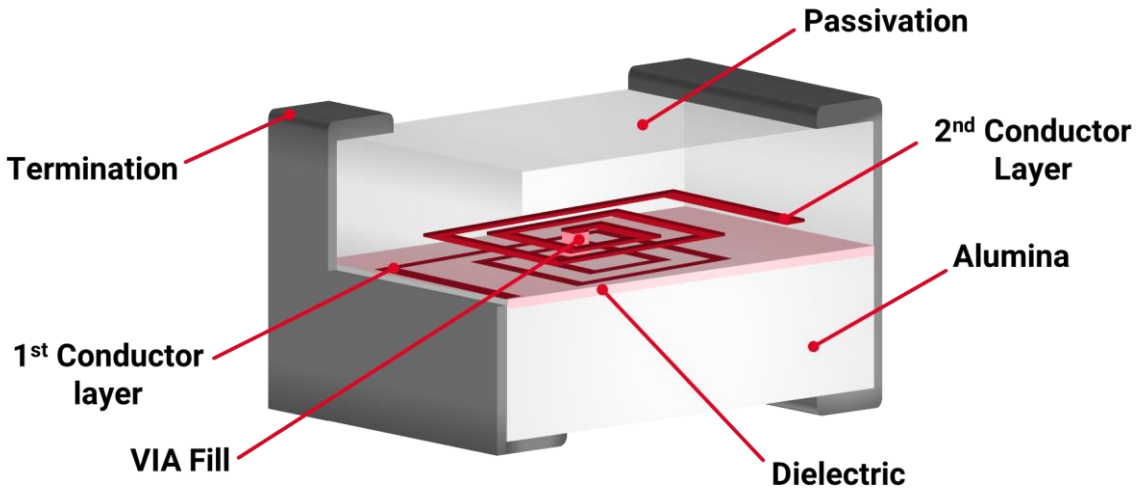
Summary



Thin Film Structures

- » Ultra Tight Tolerances Capacitors
- » Ultra Tight Tolerance Inductors
- » High directivity Miniature size Directional Couplers
- » Wide Band Couplers
- » Smallest 3dB 90° Couplers

StructureS Advanced from simple plates to:



- » High-Power Band-Pass Filters
- » High Power Low Pass Filters
- » High Power High Pass Filters
- » Industry's Lowest Current Ratings Fuses
- » High Frequency (> 20Ghz) Strip Line Couplers and Band Pass Filters

How did we get here: Thin Film Technology

Thin-Film production is unlike MLCC wet or dry processes

Class 1000 clean rooms, with class 100 laminar-flow hood work areas

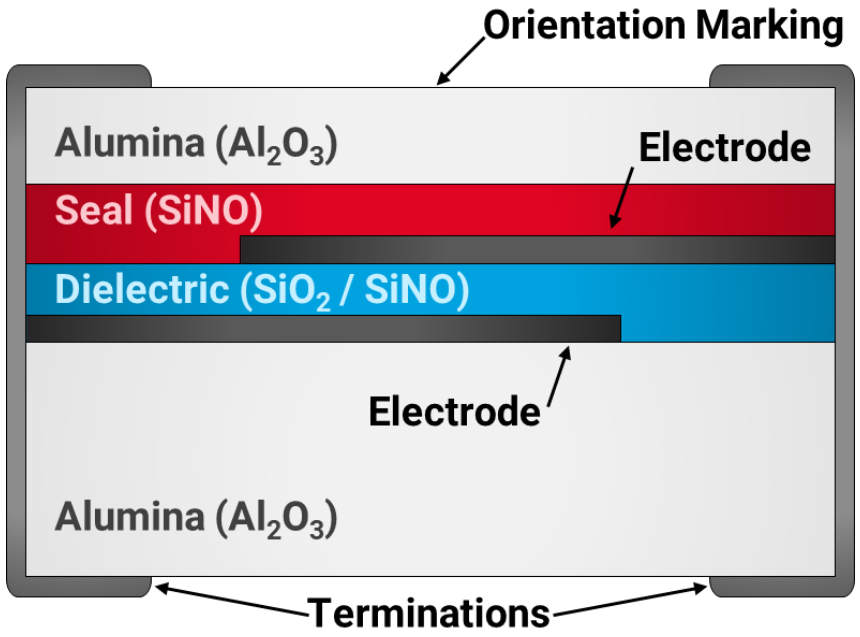
High vacuum metal deposition systems for high-purity electrode construction

Photolithography equipment for line definition down to 2.0µm accuracy

Plasma-enhanced CVD for various dielectric depositions

High accuracy, microprocessor-controlled dicing saws for chip separation

High speed, high accuracy sorting to ensure strict tolerance adherence.



Thin Film Discrete Capacitors

State of technology:

Super repeatable RF parameters at working frequency

Sizes: 0201 / 0402 / 0603 / 0805

Ultra **Tight Tolerances:** ±0.01pF (**Z**), ±0.02pF (**P**), ±0.03pF (**Q**)

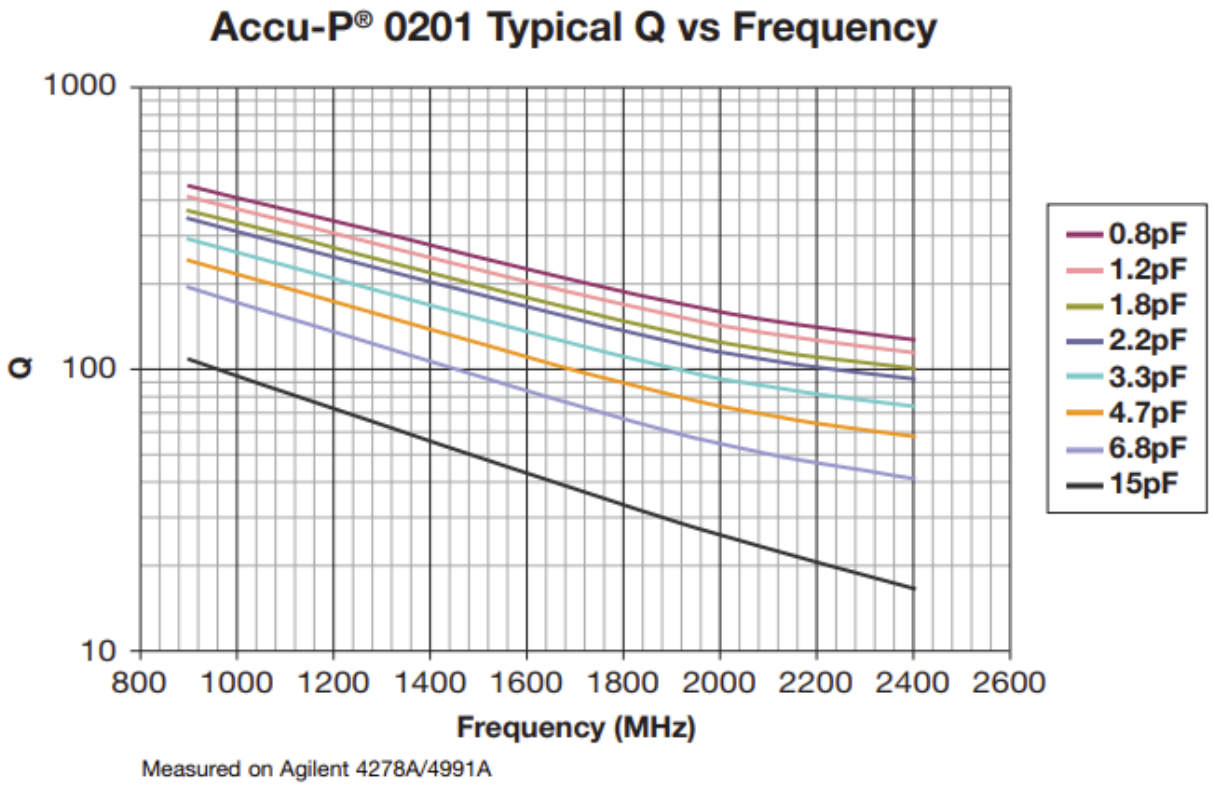
Capacitance Values Start as Low as **0.05pF**

Intermediate capacitance values

High **Q** / Low **ESR**

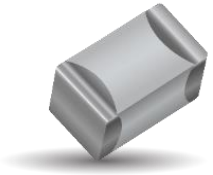
Meets or exceeds the requirements of AEC-Q200-3

0201	0402	0603	0805	1210
0.05 - 22 pF	0.05 - 68 pF	0.05 - 39 pF	0.1 - 68 pF	0.1 - 47 pF



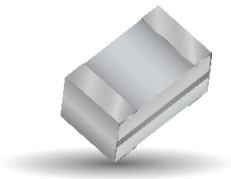
Discrete Capacitor Electrical Advantage

3.3pF MLC

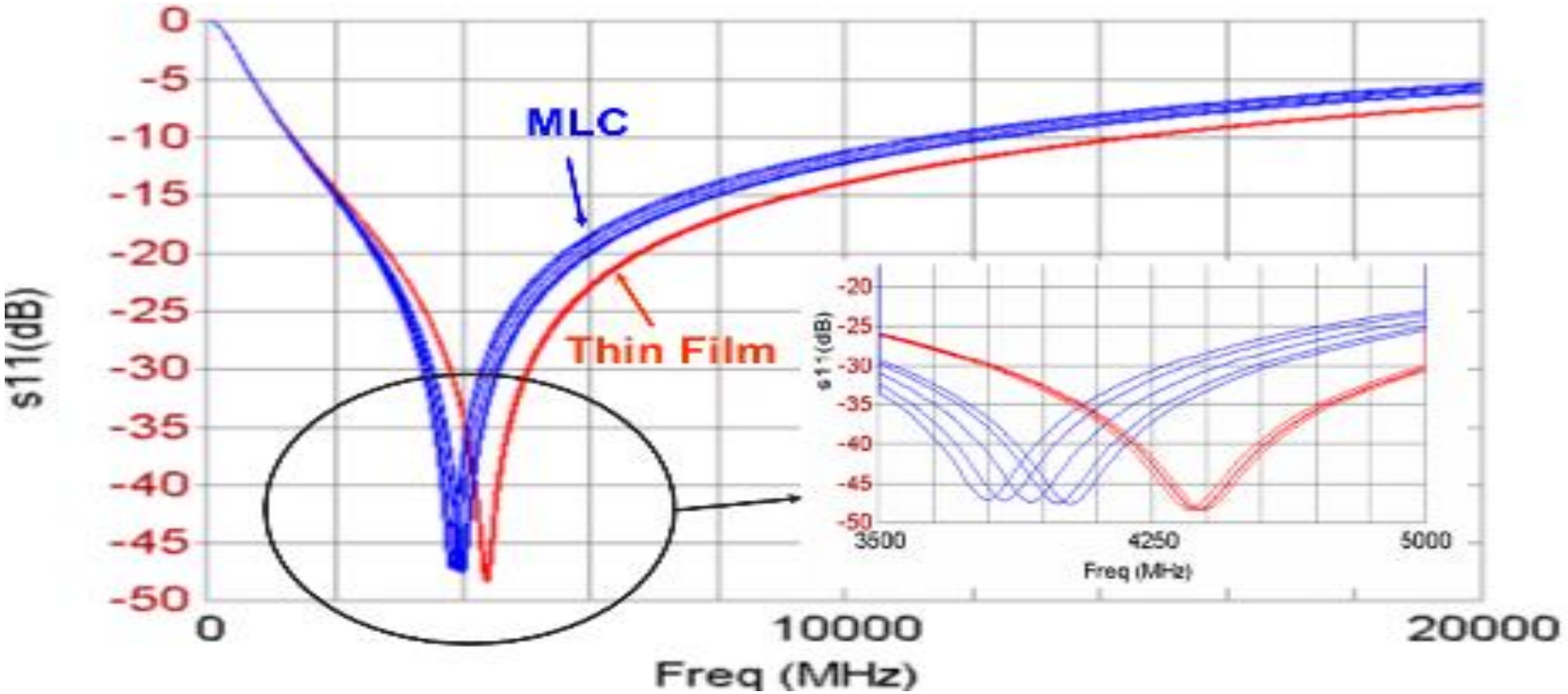


VS

3.3pF Thin Film



Repeatable RF Performance



Thin Film Discrete Inductors

State of technology:

Sizes: 0201 / 0402 / 0603 / 0805

Ultra Tight Tolerances **A**(±0.05nH), **B**(±0.1nH), **C**(±0.2nH), **F**(1%) and **G**(2%)

High **Q** Factor and High SRF

High Power Dissipation

Repeatable Performance at High Frequencies

Meets or exceeds the requirements of AEC-Q200-3

	Accu-L	AL	AS	LCWC	LCCI
Type	Thin Film	Air Core	Air Core	Wire Wound Chip	Multi-Layer Ceramic
Temperature	-55°C To +125°C	-40°C To +125°C	-40°C To +125°C	-40°C To +125°C	-40°C To +85°C
Size	0201, 0402, 0603, 0805	0605, 1212, 1516, 2523	0806, 0807, 0908	0402, 0603, 0805, 1008, 1210, 1812	0201, 0402, 0603
SRF	1.4 - 35 GHz	0.49 - 12.5 GHz	2.5 - 5.2 GHz	0.14 - 12500 GHz	0.4 - 10 GHz
DCR	0.04 - 1 Ω	0.0011 - 0.09 Ω	0.0034 - 0.01 Ω	0.03 - 3350 Ω	0.05 - 3.2 Ω
Inductance	0.33 - 22 nH	1.65 - 538 nH	5.5 - 27.3 nH	1 - 15000 nH	0.3 - 270 nH
Q	7 - 60	87 - 145	60 - 130	15 - 80	4 - 12
Current	150 - 2000 mA $_{(IDC)}$	1.5 - 4 A$_{(Ir)}$	2.7 - 4.4 A $_{(Ir)}$	**Size: 0402 - 1008** 30 - 1360 mA $_{(IDC)}$ **Size: 1210 - 1812** 150 - 1500 mA$_{(Irms)}$	120 - 1000 mA$_{(Irms)}$

Technology to combine:

Typical Substrate Properties

Nominal (Typical) Properties	Al_2O_3 99.6%	Al_2O_3 96.0%	Fused Silica	BeO 99.5%	AlN	Glass Borosilicate	P- Silicon Boron Doped	N++ Silicon Arsenic
Loss Tangent @ 10 GHz	0.0002	0.0002	0.0001	0.0003	0.001	0.003	N/A	N/A
Thermal Conductivity (W/mK)	25.5	24.7	1.38	280	170	1.16	150	150

Resistor Technology

Thin Film Resistors	SiCr	TaN
Typical Sheet Resistivity (ohm/sq)	500-1300	10-100
TCR (ppm/°C -25 to 125°C))	±50; ±100: ±250	-100 to -150
Min Tolerance (Corresponding Greater Value)	0.5% or 0.1Ω	0.5% or 0.1Ω

Capacitor Materials Typical Values

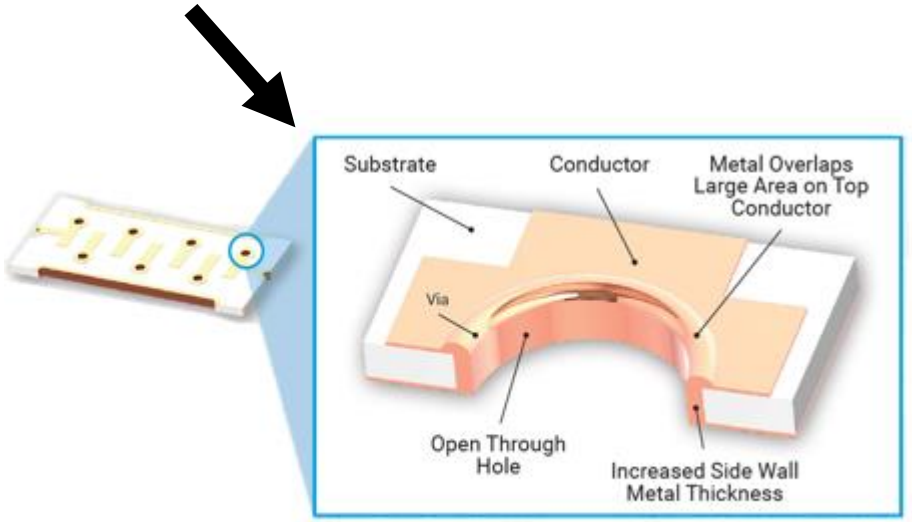
Material	SiN	SiON	SiO_2	BCB	PI
Range	1-500pF	1-500pF	1-500pF	1-50pF	0.5-10pF
Tolerance Value Dependent	±5%	±5%	±5%	±20%	±20%
Stability (TCC)	±60 ppm/°C	±60 ppm/°C	±30 ppm/°C	±42 ppm/°C	±100 ppm/°C
BDV (v/µm)	300	600	1000	300	200

Technology to combine:

	Thickness (µm)	
Metal	Min	Max
TaN (Resistive)	0.03	0.15
SiCr (Resistive)	0.03	0.15
TiW	0.03	0.15
Cr	0.03	0.15
NiV	0.1	0.75
Al	0.1	1
	1	2.5
Au	0.1	1
	1	5
Cu	1	2.5
Plated Ni	0.5	1
	1	4
Plated Au	0.75	1
	1	15
Plated Cu	2.5	50
Plated Metal Stack	-	75
Line Width: Plated Thickness Ratio	N/A	N/A

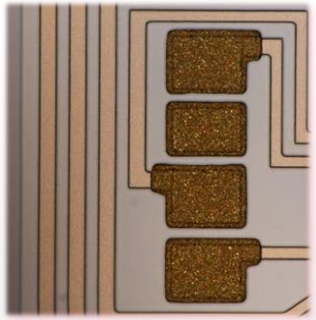
+

VIAs	C
Vias	Min
Via Diameter (D)	125µm
Via Aspect Ratio (D:T)	0.6:1
Via Spacing (Center to Center)	150µm + D
Pad Size Around Via	150µm + D
Circumference to Edge Distance	T
Via Center	-
Substrates Available	-



Termination Styles

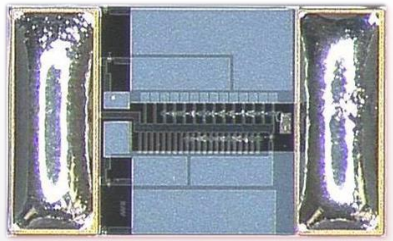
Au Wire-bond



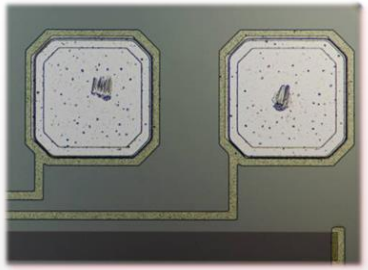
Surface Mount
(single I/O pair)

Castellated Via
(AlN, Alumina, and BeO)

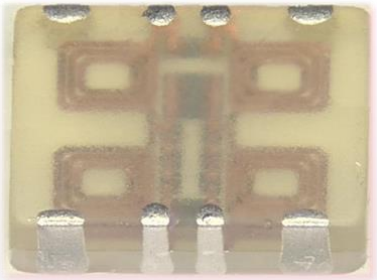
Land Grid Array



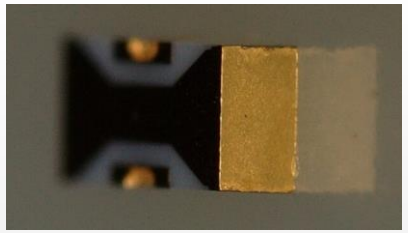
Al Wire-bond



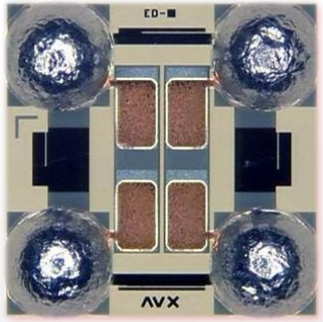
Surface Mount
(Striped, multiple I/Os)



Edge Wrap



Ball Grid Array



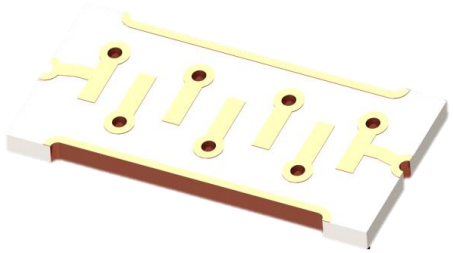
Design Considerations

Substrates Options

- Aluminum Nitride (AlN)
- Alumina (Al_2O_3)
- Silicon
- Glass
- Quartz
- Beryllium Oxide (BeO)

Sputtered & Plated Metals Options

- Gold
- Copper
- Aluminum
- Nickel



Conductor Metal Stack

TiW – Adhesion layer

Copper Conductor Layer ~8um

Nickel Layer ~1um

Gold Layer ~1um

- Thicker gold is required for wirebonding

Dielectric Materials

- Silicon Oxynitride (SiON)
- Silica SiO_2
- Benzo cyclobutene (BCB)
- Polyimide (PI)

Resistive Materials

- SiCr
- TaN

Solder Barrier Options

Exposed Nickel on Conductor Metal Stack

- Oxidation creates natural solder barrier
- 50um length minimum required
    - Width follows Conductor rules

Dielectric Material as Solder Barrier

Outcome 1: 2 / 2.5D Interposer

Lumped Elements Integrated on Chip

- Inductors, Capacitors, and Resistors

External Components Attached

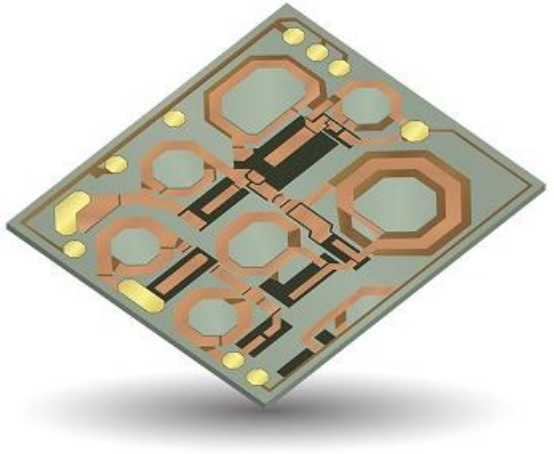
- Solderable pads or Wirebondable attachments

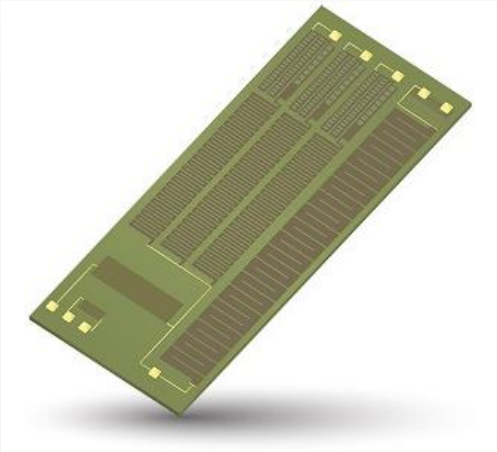
Vias

- Front and Backside processing (AlN, Alumina, BeO)

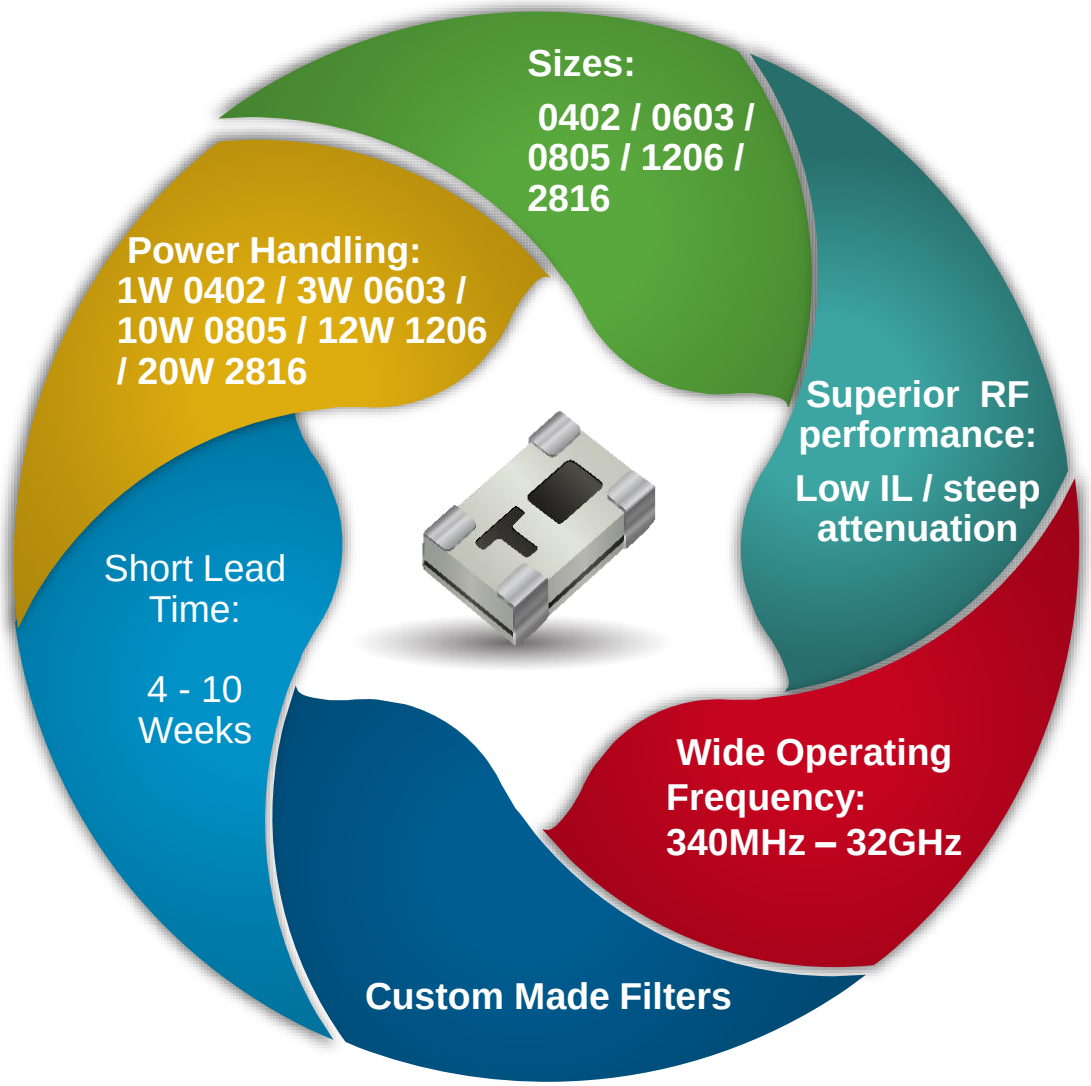
Savings

- Fewer components
  - Reduces weight
  - Reduces work and rework time
- Improves component matching
- Decrease size
  - X and Y dimensions reduced by component stacking
  - Z dimension could grow, but thin materials available





Outcome 2: High Power RF Devices



Benefits:

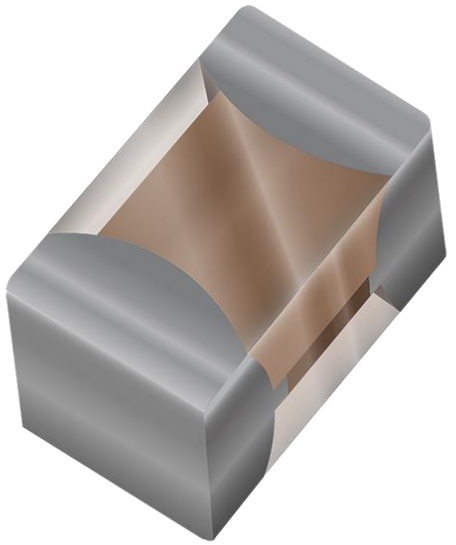
- No performance variance with temperature changes
- High power rating in small form factor
- High part-to-part and lot-to-lot repeatability
- Miniature size
- Short lead time – non LTCC process

	0402	0603	0805	1206	2816
Dimensions (mm)	1 x 0.58	1.6 x 0.84	2.03 x 1.55	3.1 x 1.6	7 x 4
Weight (mg)	1	1.73	10.8	15.57	131

Outcome 3: High Density Passive

Example 1:

Die size: 6.386 x 5.572 mm
Thickness: 127 um
27 resistors (resistors occupy 15% of the die space)
Weight ~ 12 mg

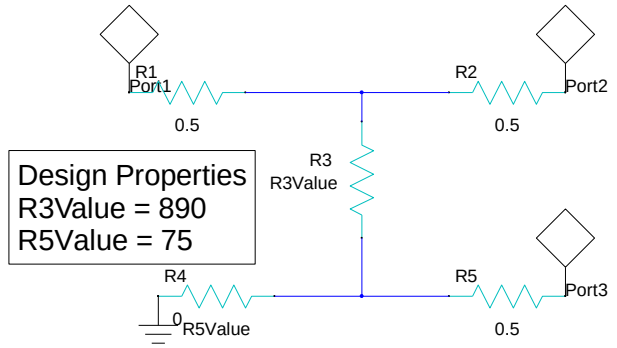


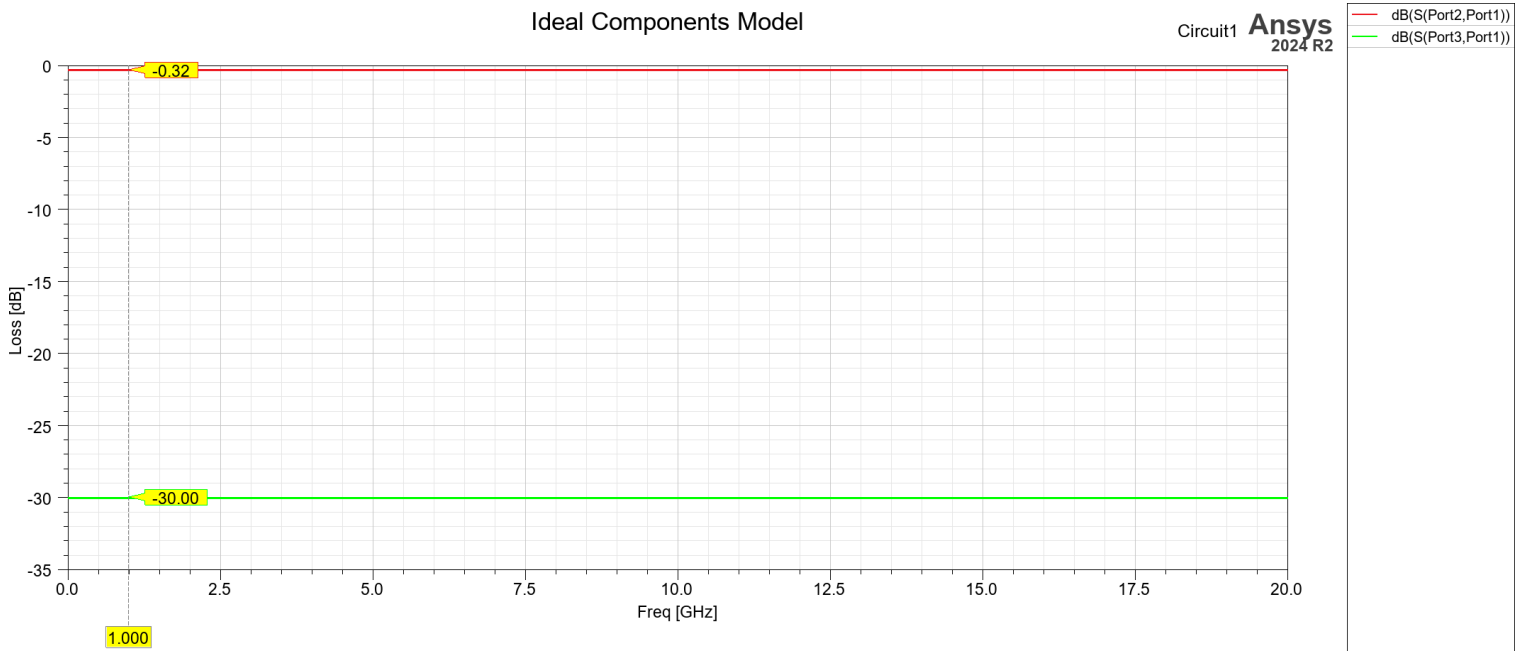
High Density Passive	Equivalent Discrete part
27 resistors in 1 package	27 discrete resistor
~ 5.32 mm^2 in optimized design	Board area 8 mm^2 plus routing
127*u*m	230*u*m
~ 3 mg in optimized design	~ 6 mg

Real World Design Comparison Custom Resistor Divider

Ideal Circuit

- Looking at a design for a 30dB resistor divider
- R3 needs to dissipate enough power to handle the 30dB drop
  - Estimated 500mW rating required
- Estimated ideal circuit shown

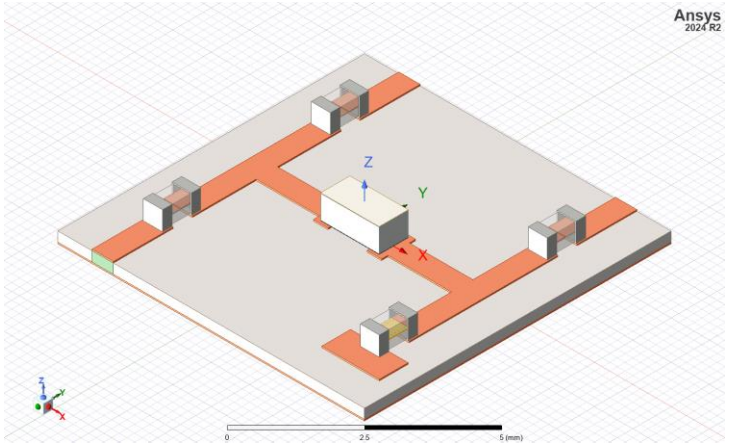


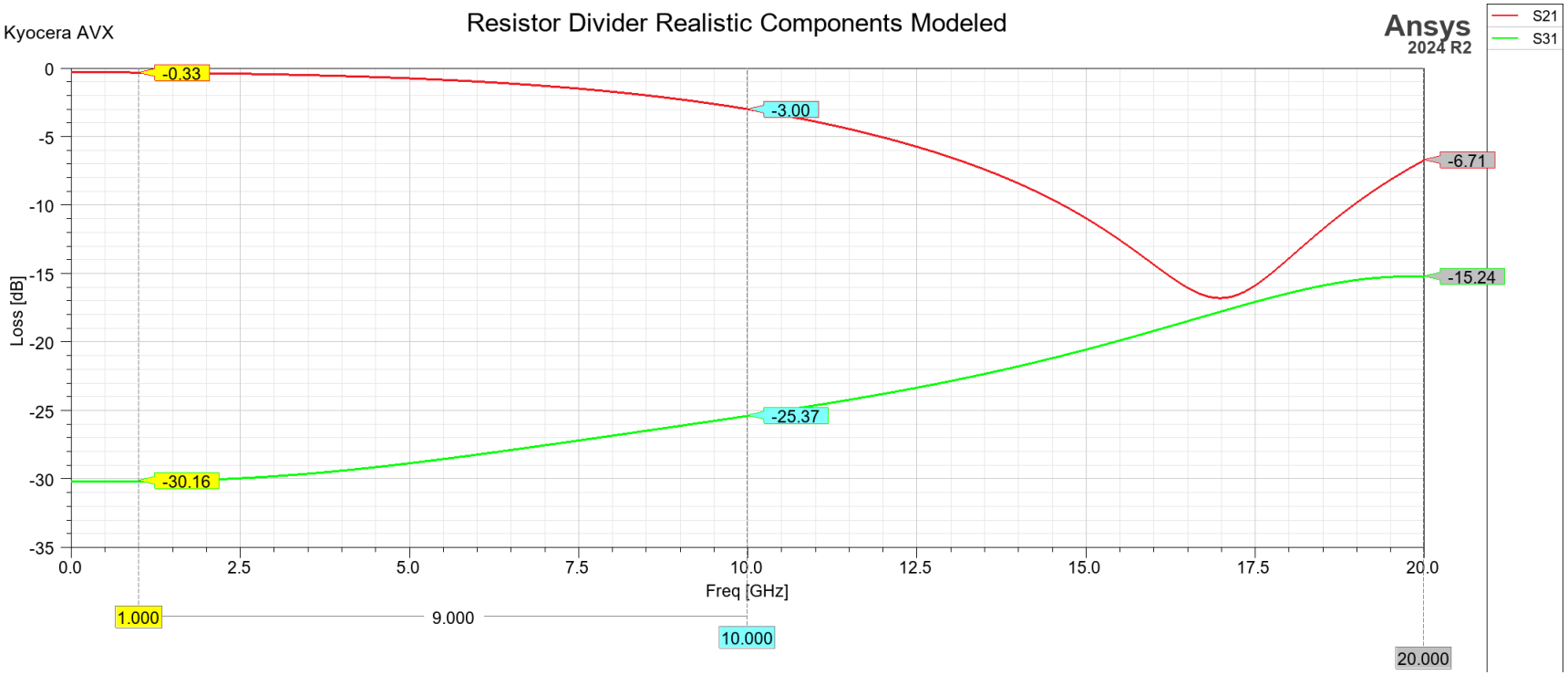


Real World Design Comparison Custom Resistor Divider

COTS Components and Equivalents

- Model uses COTS components
  - 0.5ohm resistors based on Kyocera-AVX UBR style design
    - Generic resistor with 0.5 ohm resistance
  - 75 ohm resistor is Kyocera-AVX UBR design
    - This is a COTS broadband component
  - 890 ohm resistor is based on Kyocera-AVX CR style design
    - Power handling exceeded UBR style's capability
    - 0603 style flip chip resistor with AlN was used
      - Power rating would exceed 500mW
- Model shows 30dB attenuation at 1GHz, and 25dB attenuation at 10GHz

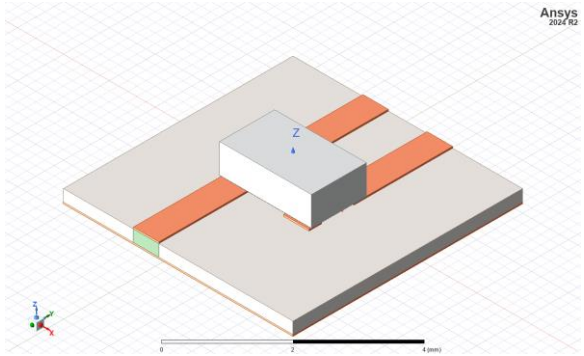


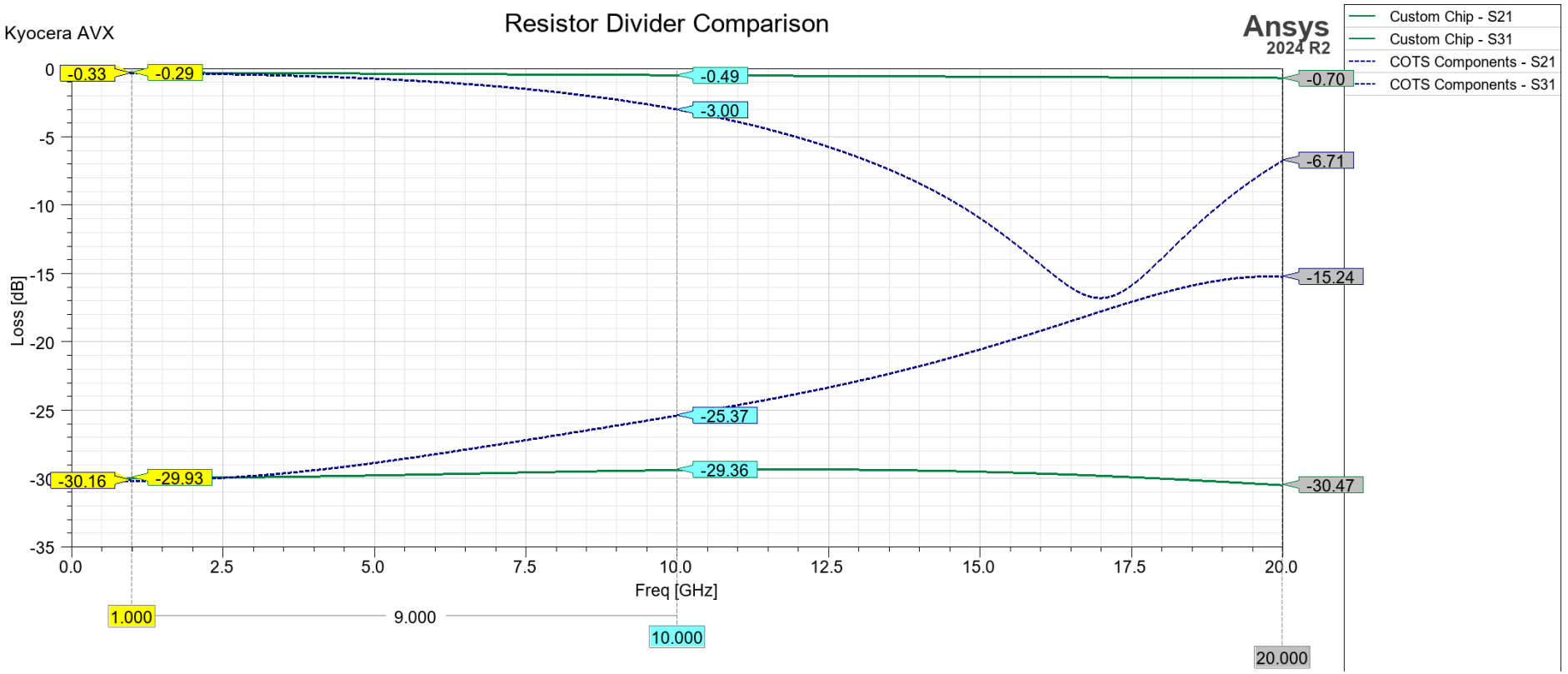


Real World Design Comparison Custom Resistor Divider

Custom Chip Design

- Single chip with all 5 resistors included
- Reduces parasitics by including in 1 chip
- RF Performance extended through 20 GHz
- Size of chip for simulation is 0805
- Flip chip style component
- Preliminary design
  - Needs to be verified with production
  - Could be modified based on customer requirements
- COTS parts – Dash line – Blue
- Custom Chip – Solid Line - Green





Summary

Thin Film integration technology advantages:

- Past discrete part design created highly efficient complex structures
- Integrated designs are quickly created by large simulation data base
- Broad material options exist for integrated designs
- Integration can take the form of RF Interposer or ‘Digital’ structures
- Substrate and component options exist
- Thin film line and oxide accuracies enable low loss, tight response
- Smaller, lighter structures with better electrical response are created