THE EVOLUTION OF MOORE'S LAW THROUGH CHIPLETIZED ARCHITECTURES

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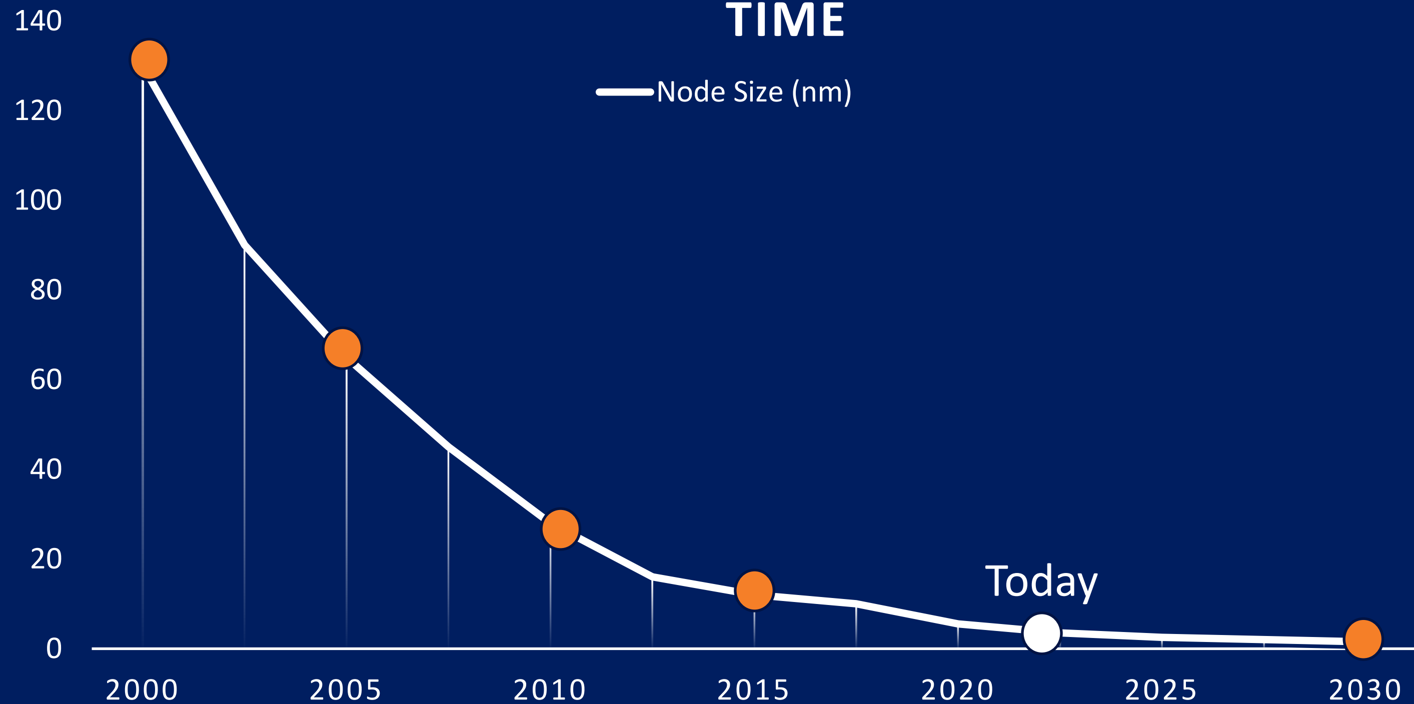
Moore's Law

We have left the transistor shrinking phase of Moore's Law



Moore's Law

- Doubling the number of transistors per chip roughly every two years

Future of Moore's Law

- Increasingly difficult to maintain exponential improvements
  - R&D and capital investments
  - Cost of transistors (design, verification, test, and fabrication)
  - As transistor's shrink, performance trade-offs between analog and digital are increasing
- Chipletized architectures allow the focus on the right node for the specific capability

...and we have entered the next phase of Moore's Law through chipletized architectures

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The future of Moore’s Law looks promising with chipletized architectures

- Moore predicted chipletized architectures as the next phase on his last page
- High speed chip-to-chip communications (AIB & UCIe)
- Enables mixed foundries, process nodes, and IP sources
- Specialized System in Packages (SiP)
- Leading semiconductor companies are already moving to heterogeneous 2.5D solutions

MONOLITHIC CHIP

A singular piece of silicon, constructed as a unit

I/O
GRAPHICS/IMAGING
COMMS
CPU CORES
MEMORY

CHIPLETS

A heterogeneous collection of "chiplets" integrated as one device

10 NM Chiplet
10 NM Chiplet
14 NM Chiplet
14 NM Chiplet
22 NM Chiplet
I/O
GRAPHICS/IMAGING
COMMS
CPU CORES
MEMORY

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Geopolitical and supply chain constraints are also impacting Moore's Law

- Globalization has migrated Advanced Packaging to the Pacific Rim for decades
- Current geopolitics is driving instability in the region and increasing the risk of access to leading edge microelectronics and packaging capabilities
- This has created substantial risks to western countries as they strategically modernize
- At the same time, Advanced Packaging is more critical in solutions as we transition to Heterogeneous Integrated (HI) architectures enabling processing to move to the sensor edge

Mercury Systems is focused on reshoring Advanced Packaging for critical microelectronics

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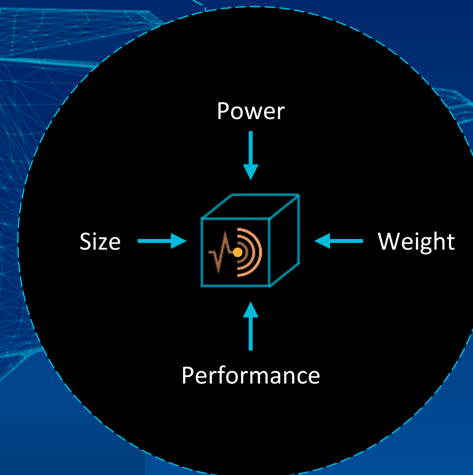
Microelectronics is disrupting the market to solve the edge processing challenges

EDGE PROCESSING CHALLENGE

Processing more data in real time
at the sensor aperture
for decision superiority



SENSOR PROCESSING DRIVERS

This is what drives the revolution.

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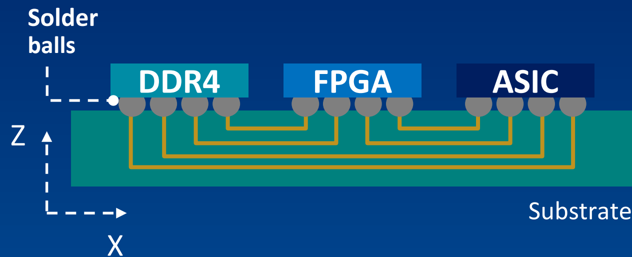
Evolution of packaging technology, simplified

2D SYSTEM-IN-PACKAGE

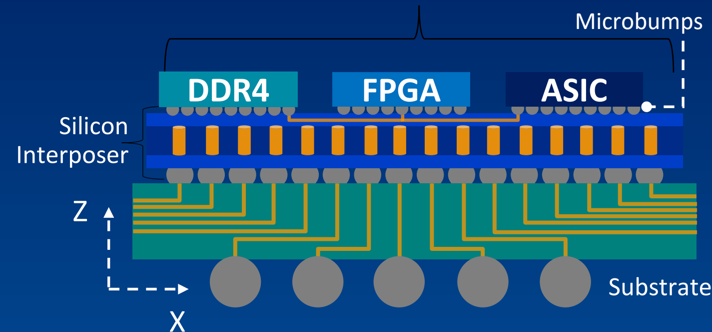
Medium-density interconnects



- In production today in commercial and defense markets

2.5D SYSTEM-IN-PACKAGE

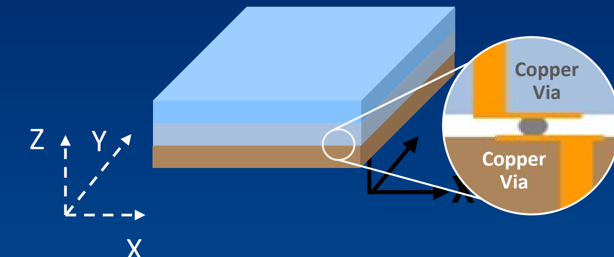
High-density flip chip die



- In production today in commercial and market; Mercury will be the first to commercialize for defense

3D SYSTEM-IN-PACKAGE

Vertically stacked high-density flip chip die



- Not yet in production in the commercial market

Increasing compute density with advanced packaging technology

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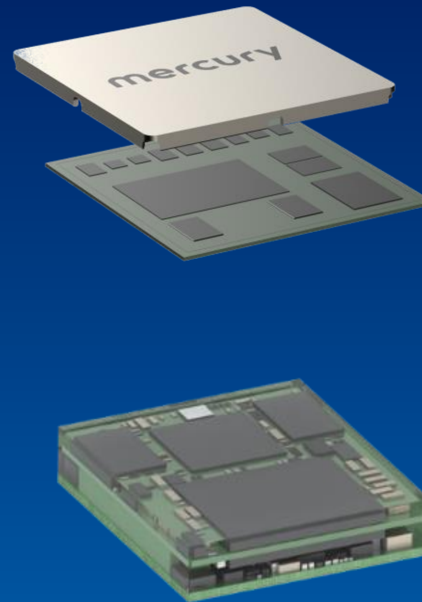
Mercury brings advanced commercial technology to A&D solutions with heterogeneous integration

COMPONENT FLEXIBILITY

- DDR & Flash Memory
- FPGA, CPU, GPU Processing
- ADC, DAC Components
- Power Management Circuitry
- Analog Integrated Circuits

SIP PACKAGE EXAMPLES



THE BENEFITS

- Lower size, weight and power
- Customizable per unique program requirements, unlike custom silicon
- Lower NRE vs. custom silicon
- Faster time to market vs. custom silicon
- Shorten customer development time
- Ruggedized for military use

Customer selects the optimal combination of components for design into the package

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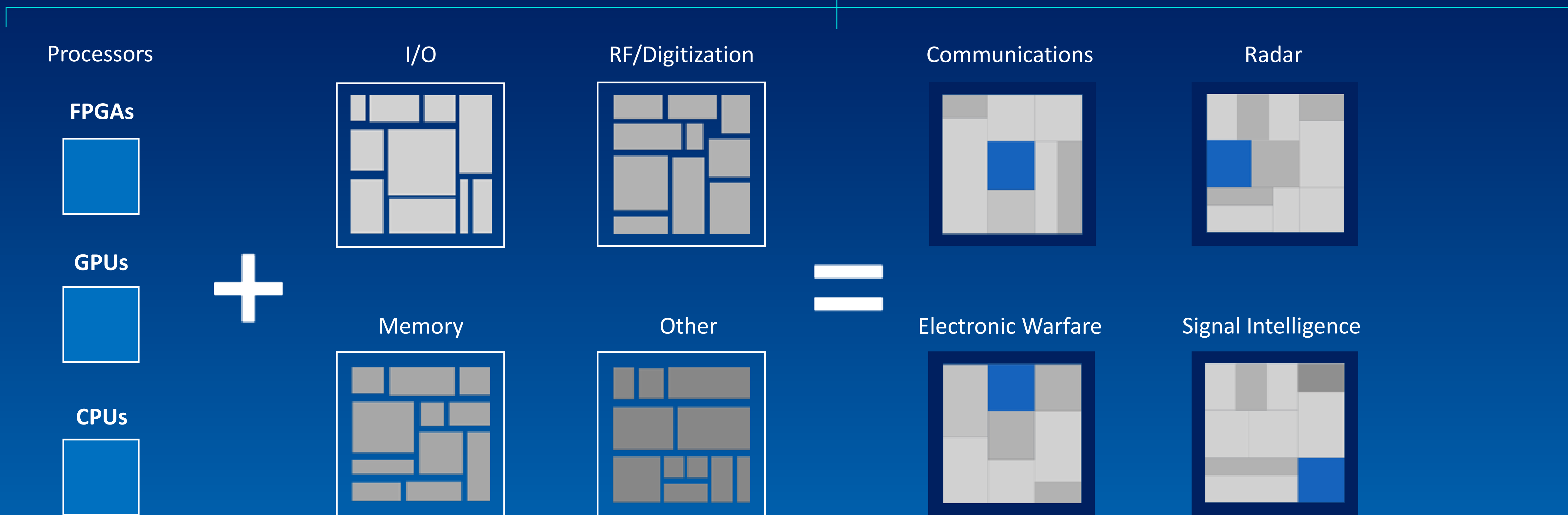
This game-changing capability will enable new applications at a rapid pace



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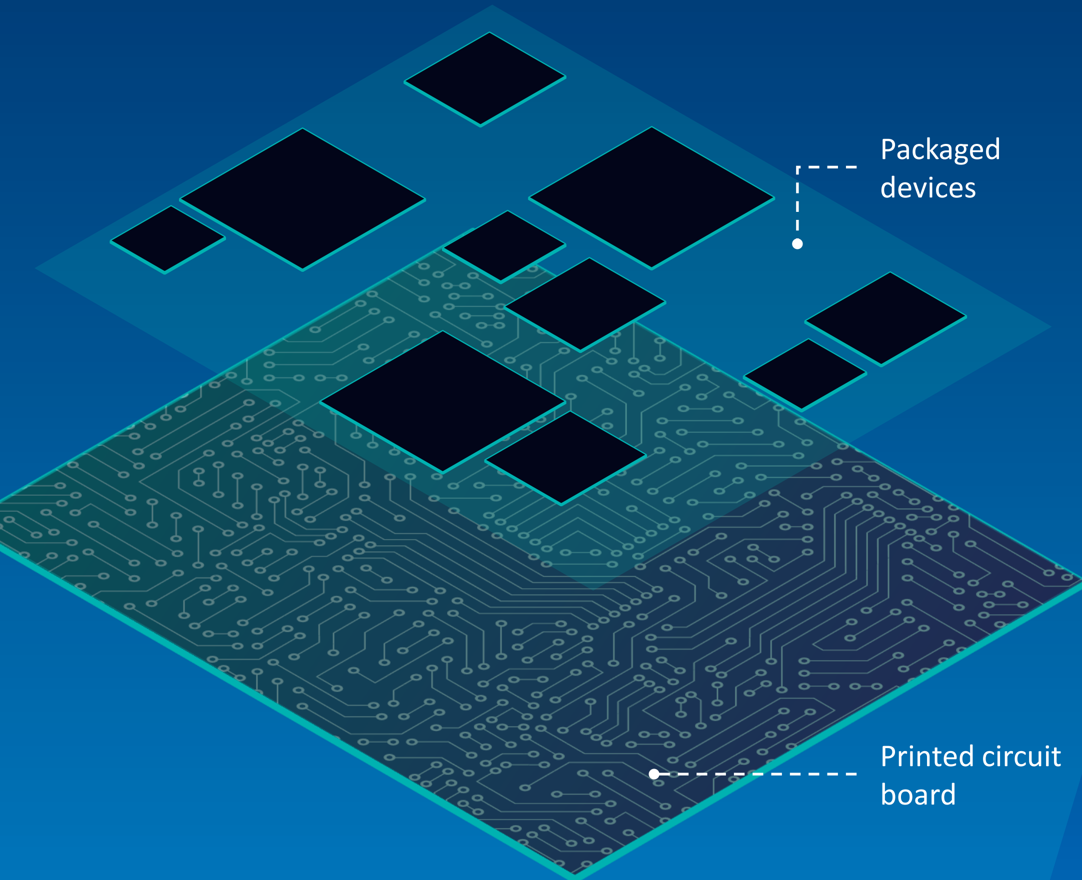
Chip scale vs. board scale integration evolution

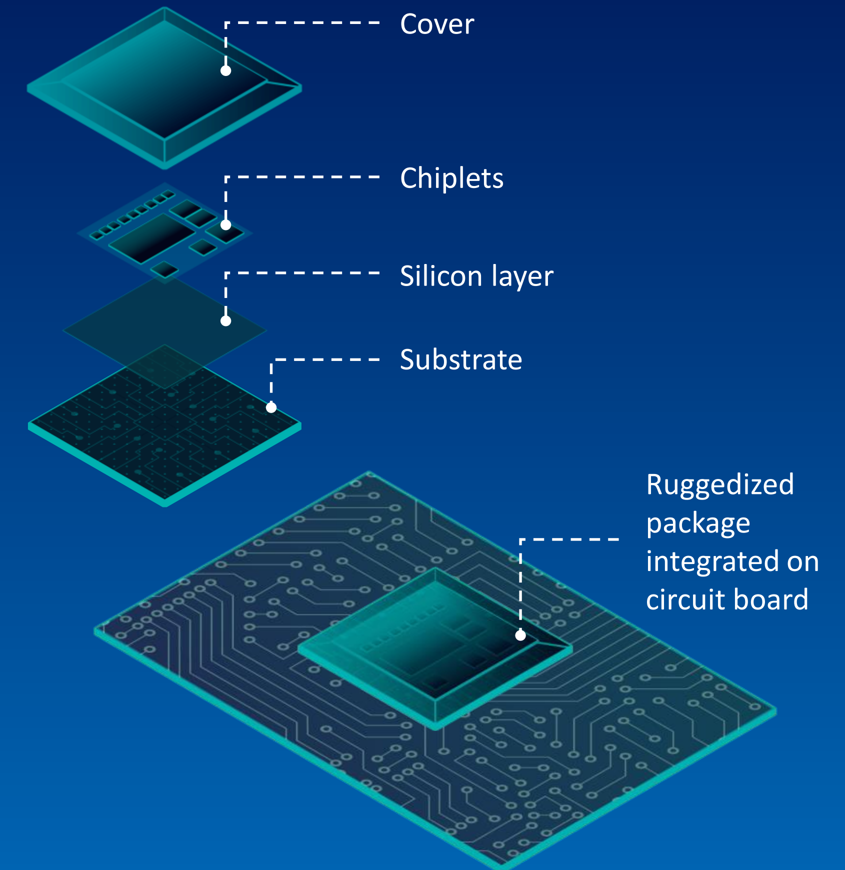
TRADITIONAL BOARD-LEVEL INTEGRATION



MERCURY'S CHIP SCALE INTEGRATED SOLUTIONS

Up to
80%
Reduction in board size

100%
Increase in chip-to-chip communication speed



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Mercury Vision: Chiplet Based Store Front

Mercury Store Front

- ITAR
- DFAR contracts
- Trusted design and processes
- Classified design and/or processes
- Security
- Unique IP
- Unique processes
- Merchant supplier focused on DoD
- Merchant semiconductor partnerships
- Access to leading edge silicon
- Low-volume/high-mix production
- Rugged environments
- Integrated solutions (CCA & subsystem level)

Standard Parts	Derivative Parts	Fully Custom Parts
Heterogeneous Chip/Chiplets Access/Library	Security IP Mercury Third Party Library	Customer Chip/Chiplets and/or Security IP
MIL-SPEC Environments	Program Modified Environments	Program Unique Environments
COTS Boards	Modified COTS Boards	Unique Form Factors and/or Integrated Subassemblies

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- 2,500 employees who design/build microelectronics and computers for aerospace and defense
- Provide within supply chain and direct to government
- Commercial business model, investing 11-13% of annual revenue in R&D
- Our content is deployed on 300+ programs, including on 38 MDAPs

Mercury solutions deployed on 300+ programs with 25+ primes

Aerospace & Defense Platform and Systems Electronics Content

C4I	JLTV	WIN-T	BLACKHAWK	A330 MRTT	Aegis
Sensor & Effector Mission Systems	F-16	Reaper/Gorgon Stare	Triton	LTAMDS	Aegis
	F-35	C-130	Global Hawk	Badger/Buzzard	SEWIP
	Stormbreaker	PGK	MALD-J	Paveway	SM2/3/6

Primes

AIRBUS
BAE
BOEING
GA
L3HARRIS
LEONARDO
LOCKHEED
NORTHROP
RAYTHEON
SAIC
SNC
THALES

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Chipletized Architectures Are the Future, But Before We Get There….

Challenges & Opportunities

Mature Chiplet Ecosystem

Industry should continue to work towards standardization of chip-to-chip communications to enable sustainable business model

Onshore Access to State-of-the-Art Interposers & Substrates

Build up onshore manufacturers that can support lower volumes and high mix for the DoD while reducing cycling time

Process Design Kit for Package Assembly

Automated tools for customers to select from a library of chiplets to create producible System in Packages (SiPs)

Device Enablement & Support

Sustainable business model that supports diversity of chipletized architectures for different consumers

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