



Legacy Program Engineering Stock Validation and Counterfeit Inspection



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Outline

- ❑ Component History & Storage- *Reason for analysis request*
- ❑ Physical assessment- *Inspection and Analysis of packaging & subject components*
- ❑ Additional assessments- *Analysis required for recertification*
- ❑ Findings and Recommendations

Component History, Analysis Request

- ✓ Qty. 104 CPLD*/PLCC** components sent to Failure Analysis from program engineering Laboratory
- ✓ Moisture Barrier Bag opened at some unknown point in time, exposed to ambient temperature & humidity
- ✓ Package marked as **MSL 3**: Solder parts \leq 168 hours from the time the package is opened, Storage shelf life = 12 months
- ✓ Original supplier seal date is: 02/07/2012. Parts will be soldered onto the CCA, per design intent
- ✓ Components are obsolete and unavailable. Quantity needed for a 20-lot spares CCA build (4 devices per CCA)
- ✓ **Request:** Determine if components are useable and can be baked out and re-sealed IAW J-STD-033
- ✓ Initial Inspection noted lead formation & insertion marks on components, Provenance assessment required
- ✓ Due to the length of time the components were exposed to ambient temperature & humidity, Solderability assessment is required

**CPLD = Complex Programmable Logic Device*

***PLCC = Plastic Leaded Chip Carrier (4 sided SMT J-Lead Device)*

Component is obsolete & unavailable in the supply chain. Needed for a 20 lot spares board build

Component Provenance

- ✓ **Device Type:** 44 Pin J-Lead, Plastic Encapsulated Microcircuit (PEM), CPLD
- ✓ **Preliminary Inspection:** Original supplier probe test marks and contact marks from the J-Lead frame fabrication process noted
- ✓ **Insertion Marks:** Additional contact marks and lead deformation suggest components were inserted into a socket, to be programmed or tested, considered evidence of prior use
- ✓ **Counterfeit Reports:** Several incidences previously reported for Non-conformance & counterfeiting for this supplier's device type. A counterfeit report summary was obtained from Silicon expert, then compared to an Internal RTX counterfeit database tool
- ✓ **Additional Engineer QA Inputs:**
 - Seal is 2012. The devices inside appear to be 'used' in the sense that they have insertion scratch marks
 - CPLD went End Of Life in 2011 Per PDN issued October 26, 2011
 - Program maintained paperwork from approved Franchised Distributor who acquired the parts directly from the supplier as part of an end of life quantity buy. Includes C of C and original pertinent purchasing paperwork
 - Engineering lab has original CPLD programming stations, these devices were tested and programmed as part of the initial LRIP production builds and were consumed, as needed

Counterfeit database assessment and origination summary on following slides

Counterfeit Report Summary- *Silicon Expert, Supplier & GIDEP*

Part Number	Manufacturer	Notification Date	Counterfeit Methods	Description	Source
XC95216-15HQ208I	XILINX INC	JAN 21,2015	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)	LEADS ARE BENT, AND SHOW SIGNS OF PREVIOUS USE.	https://download.siliconexpert.com/pdfs/2015/3/5/8/12/15/26/xil_/manual/8014.pdf
XC95144-10PQ160I	XILINX INC	MAR 03,2014	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)	Markings on the base of the lead.	https://download.siliconexpert.com/pdfs/2015/9/6/6/57/5/377/xil_/manual/7612.pdf
XC9572-15TQ100I	XILINX INC	MAY 15,2017	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)		
XC9572-10TQG100I	XILINX INC	MAR 22,2016	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)	LEADS ARE BENT.EVIDENCE OF REMARKING, AFTER BLACKTOP WAS REMOVED, SANDING MARKS PRESENT. EVIDENCE OF RETINNING AS THERE IS NO LEAD FORMATION MARKS OR EXPOSED COPPER.	https://download.siliconexpert.com/pdfs/2016/3/23/8/29/17/746/xil_/manual/9114.pdf
XC9536-10VQG44I	Xilinx. Inc	MAY 14,2018	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)		Please Contact GIDEP for Document # [AAN-U-18-313]
XC95216-10PQ160I					
XC95144-15TQ100C	Xilinx Inc.	AUG 01,2013	Same Supplier, New Parts (Unknown Third party manufacturer looklike part from the same affected supplier)		Please Contact GIDEP for Document # [CEW-P-13-01]
XC9536-10VQ44I	Xilinx Inc.	OCT 09,2013	Same Supplier, New Parts (Unknown Third party manufacturer looklike part from the same affected supplier)		Please Contact GIDEP for Document # [C9Y-A-14-01]
XC9536-10VQG44I	Xilinx	AUG 13,2019	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)		Please Contact GIDEP for Document # [X9-A-19-07]
XC95216-15HQ208I	XILINX INC	JAN 21,2015	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)	LEADS ARE BENT, AND SHOW SIGNS OF PREVIOUS USE.	https://download.siliconexpert.com/pdfs/2015/5/19/7/35/40/848/xil_/manual/8014.pdf
XCR3128XL-7CS144I	Xilinx Inc.	DEC 01,2011	Different Supplier, Old Parts (Unknown Third party use Old part from different supplier than the affected one)		Please Contact GIDEP for Document # [R6-P-12-01]
XC95144-15PQ160C	XILINX INC	MAR 17,2014	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)	Staining on the top surface. Bent leads.	https://download.siliconexpert.com/pdfs/2015/8/18/8/15/4/88/xil_/manual/7676.merged.pdf
XC95108-15TQG100I	Xilinx	JUL 15,2015	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)		Please Contact GIDEP for Document # [AAN-U-15-268]
XC95288XV-6TQ144C					
XCR3512XL-12FT256I					
XC9572-15PC44C	Xilinx Inc.	AUG 03,2020	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)		Please Contact GIDEP for Document # [A2C-A-20-01]
XC95288XV-6TQ144C	Xilinx, Inc.	JAN 14,2016	Same Supplier, Old Parts (Unknown Third party use Old part from the same affected supplier)		Please Contact GIDEP for Document # [x9-a-16-02]

CPLD Part Number has NO Counterfeit Incidences. Compared to Internal RTX tool, no findings

Origination Summary- *Packing List & Inspection Report*

Original Packlist from approved Franchised Distributor

- Included Inspection results, quantities ordered and what was received

Purchase Order paperwork

- Including approved FD supplier Certificate of Compliance (CofC)
- Additional paperwork, showing acquisition of EOL product from the

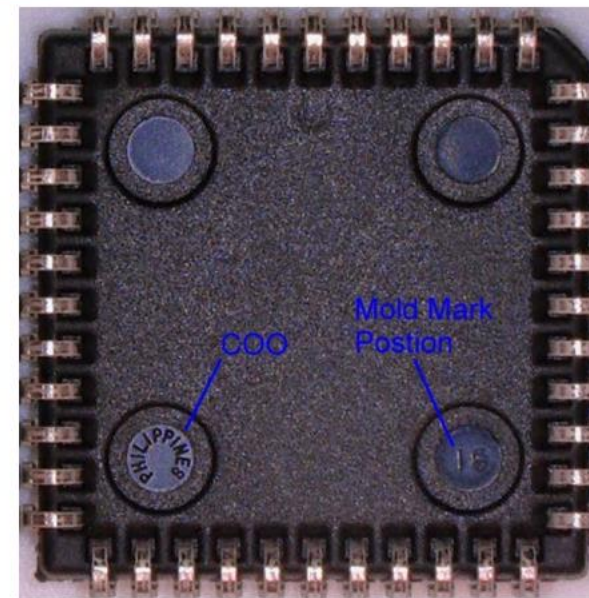
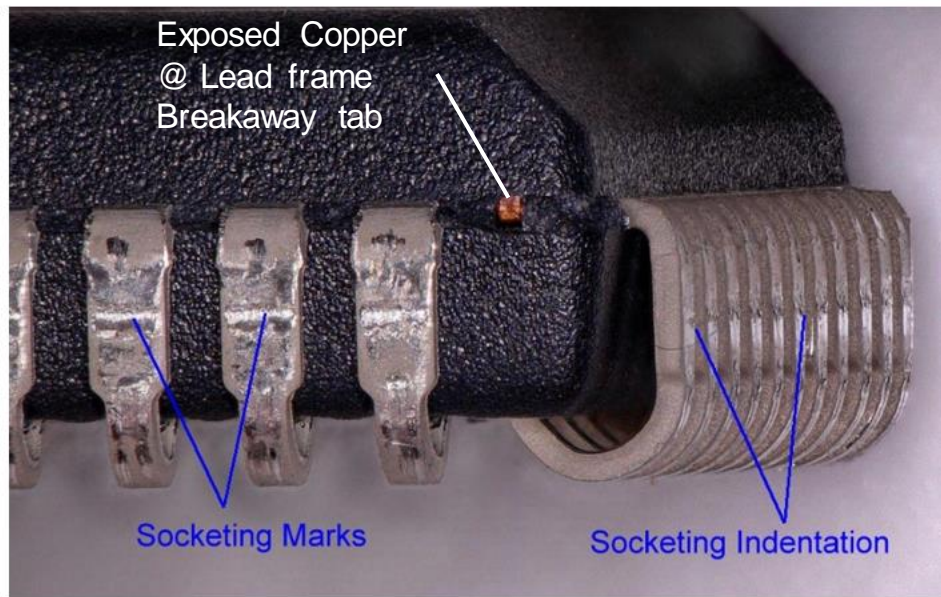
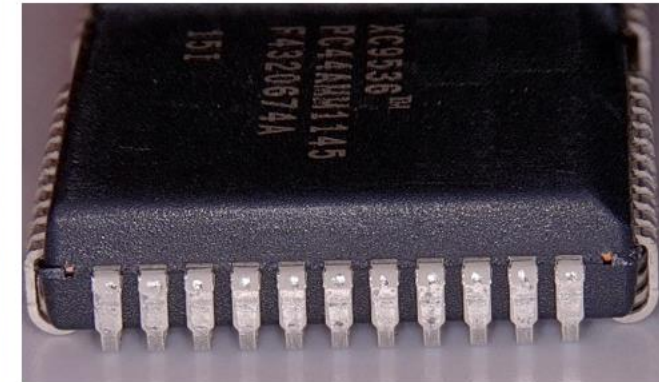
Original Receiving Inspection Report

- Included inspection summary & date of inspection
- Additional aftermarket inspection requirements applied

Traceability Back to the Original Component Manufacturer (OCM) **ESTABLISHED**

Optical Inspection- *External Construction*

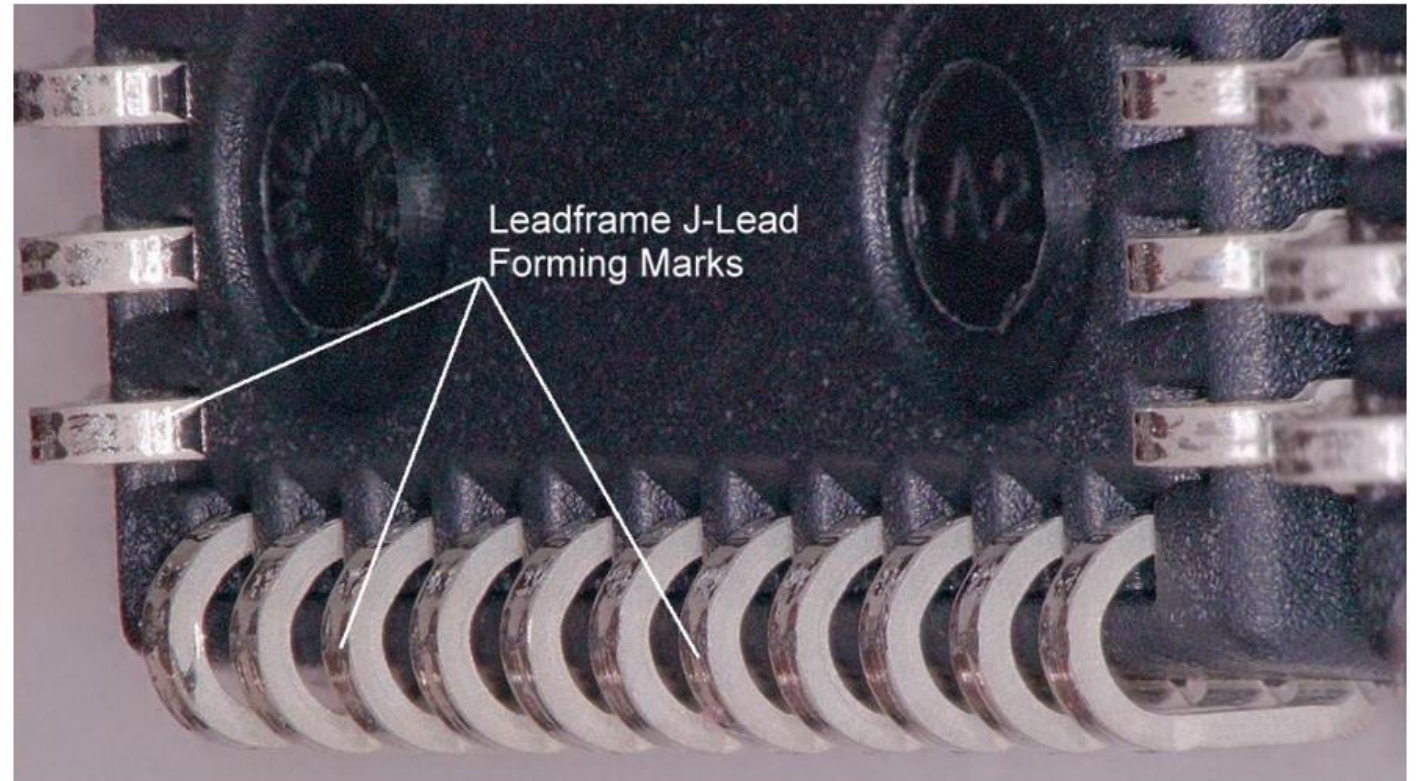
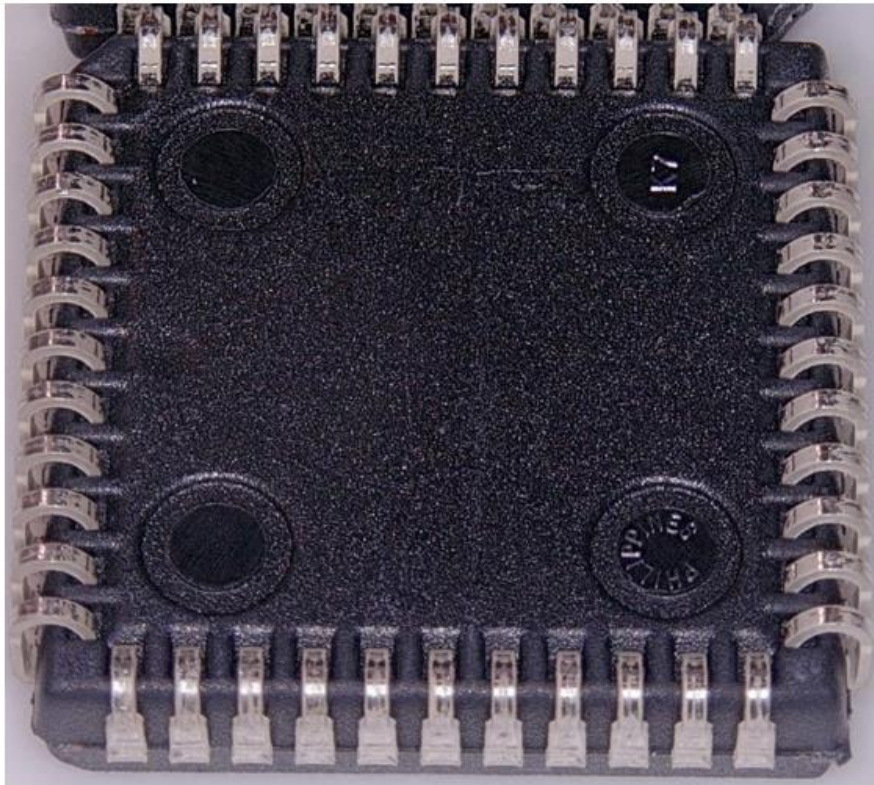
Images owned by Raytheon Technologies



Qty. 104 Components visually inspected. Consistent construction, COO marks & EOL date codes

Optical Inspection- *External Construction*

Images owned by Raytheon Technologies



XRF: Lead frame is a Tin/Lead electroplate finish, Nickel Barrier & Copper basis metal

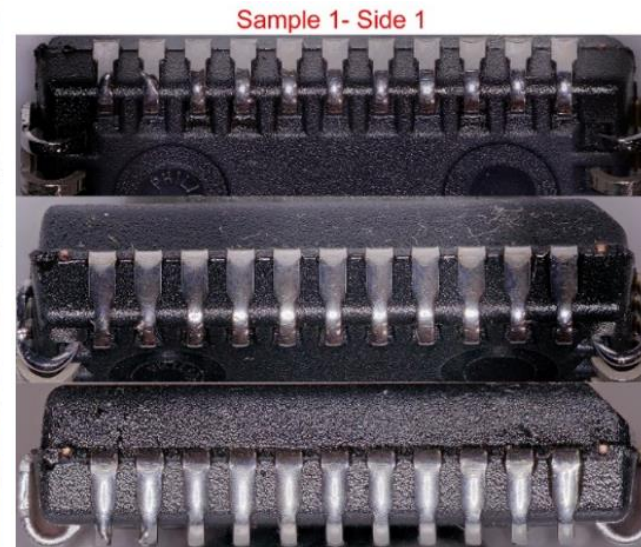
Leads not heavily oxidized. Marks due to J-lead formation & socketing for programming / test

Solderability- *Determine condition of plating & Basis Metal (Cu)*

Images owned by Raytheon Technologies

Setup: Samples tested on 2 of 4 sides; 22 leads per device, 66 total. Pre-flux with 45° angle dip

Solder Sample Test Setup



Pass/Fail Criteria: All leads MUST have > 95% coverage, without blistering, peeling, or signs of de-wetting due to contamination or corrosion defects

Qty. 3 Samples randomly selected for destructive test. TEST IAW J-STD-002E ; Method 4.2.1 Test A.

Solderability- *Determine condition of plating & Basis Metal (Cu)*

Images owned by Raytheon Technologies

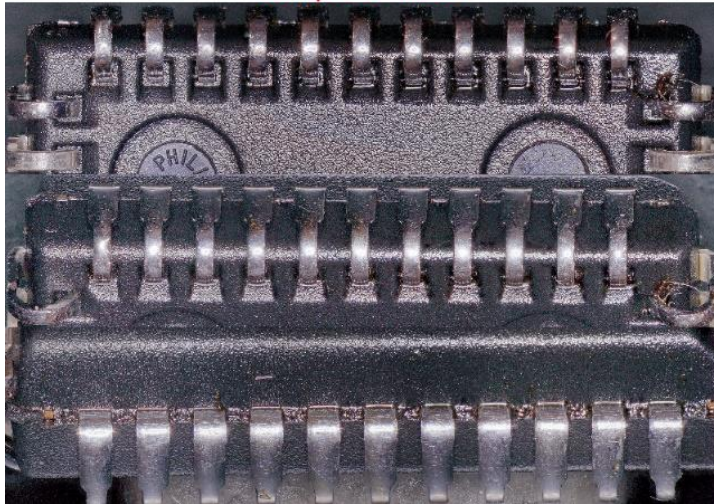
Sample 2- Side 1



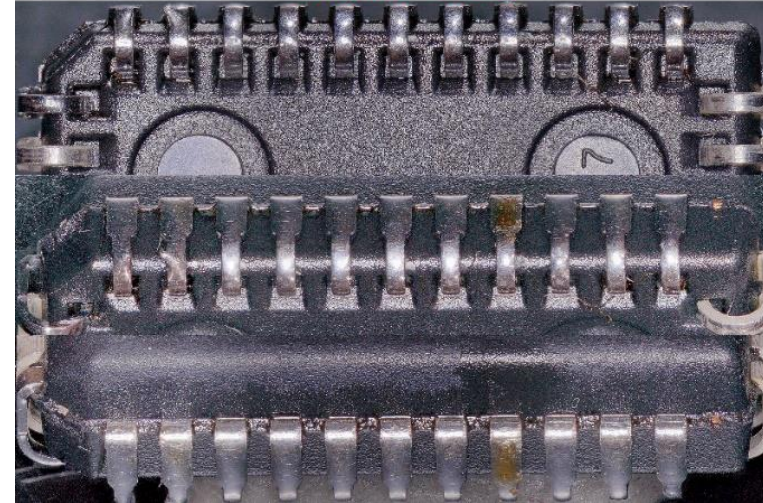
Sample 2- Side 2



Sample 3- Side 1



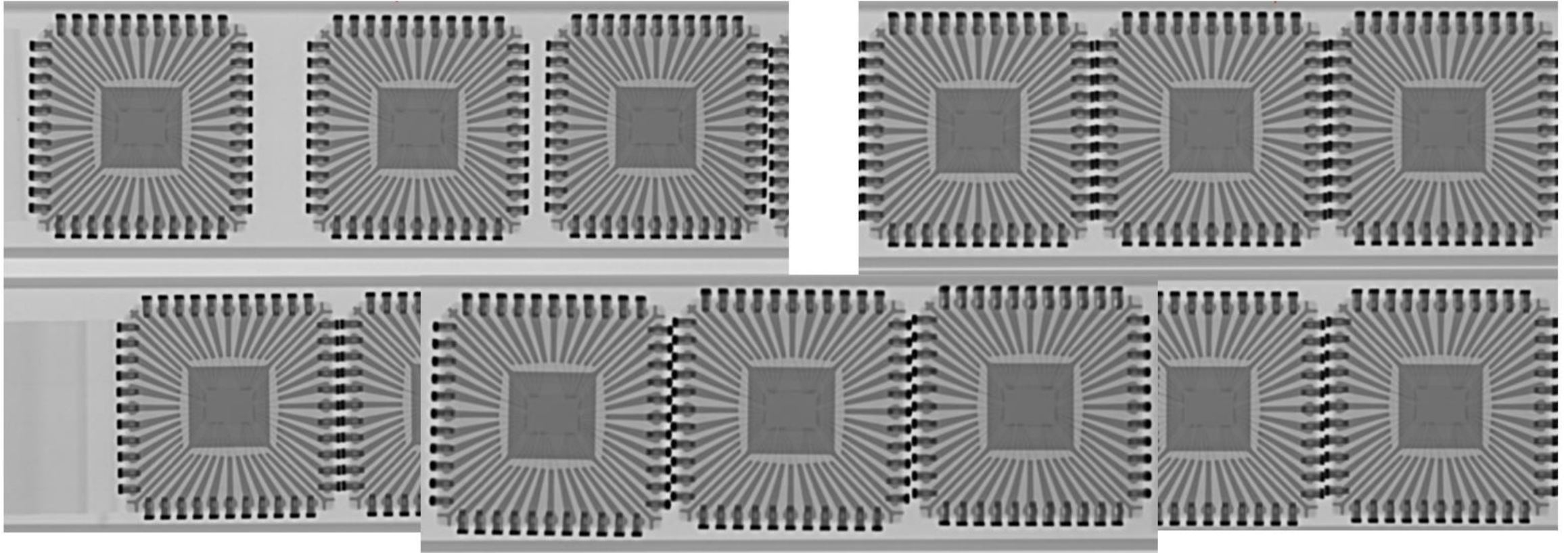
Sample 3- Side 2



All leads (66) on Three Samples showed >99% coverage. Lead re-plating is **NOT** Required.

X-ray- *Cursory Internal Inspection*

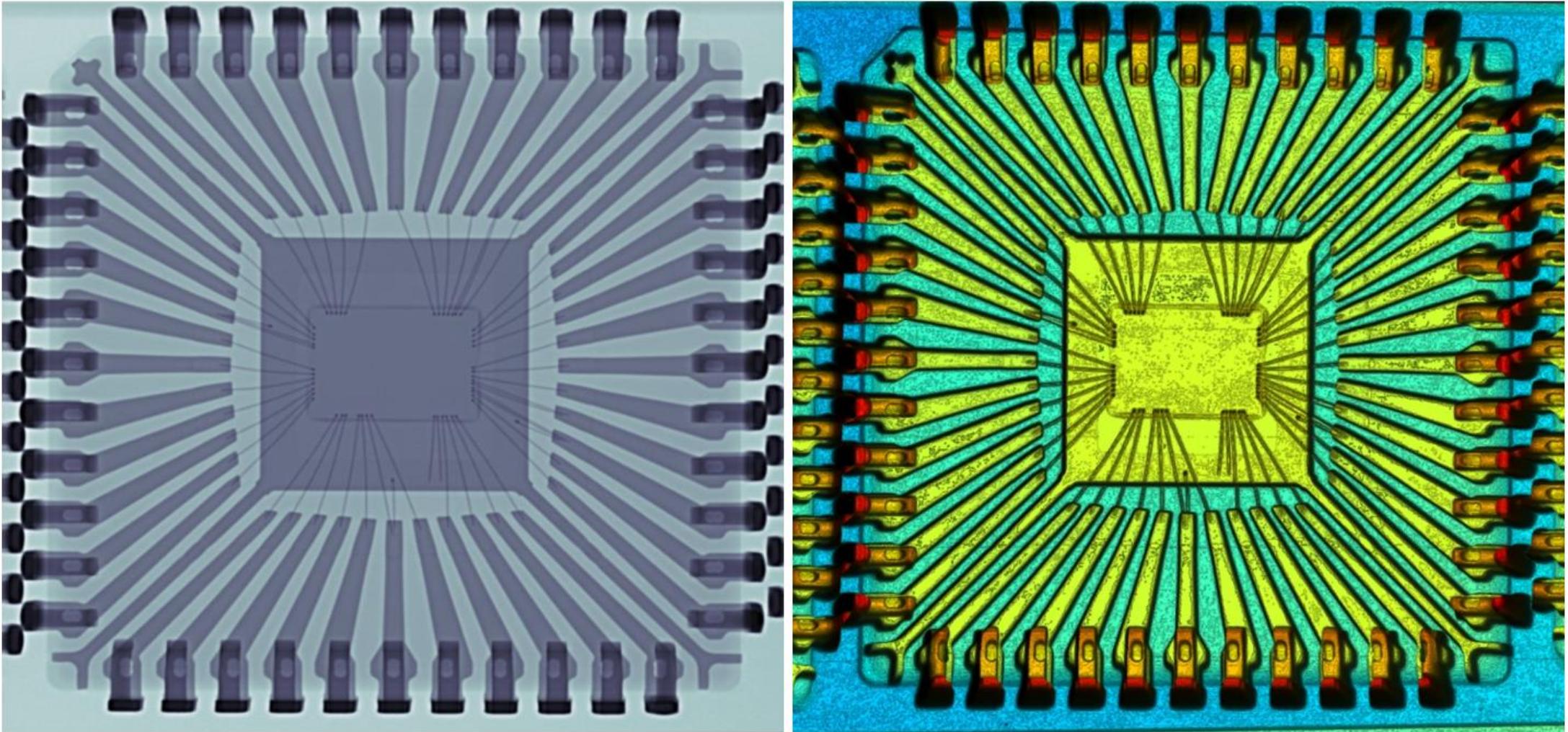
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3 lot sites were selected for X-ray. Showed consistent lead frame, die & wire bond construction

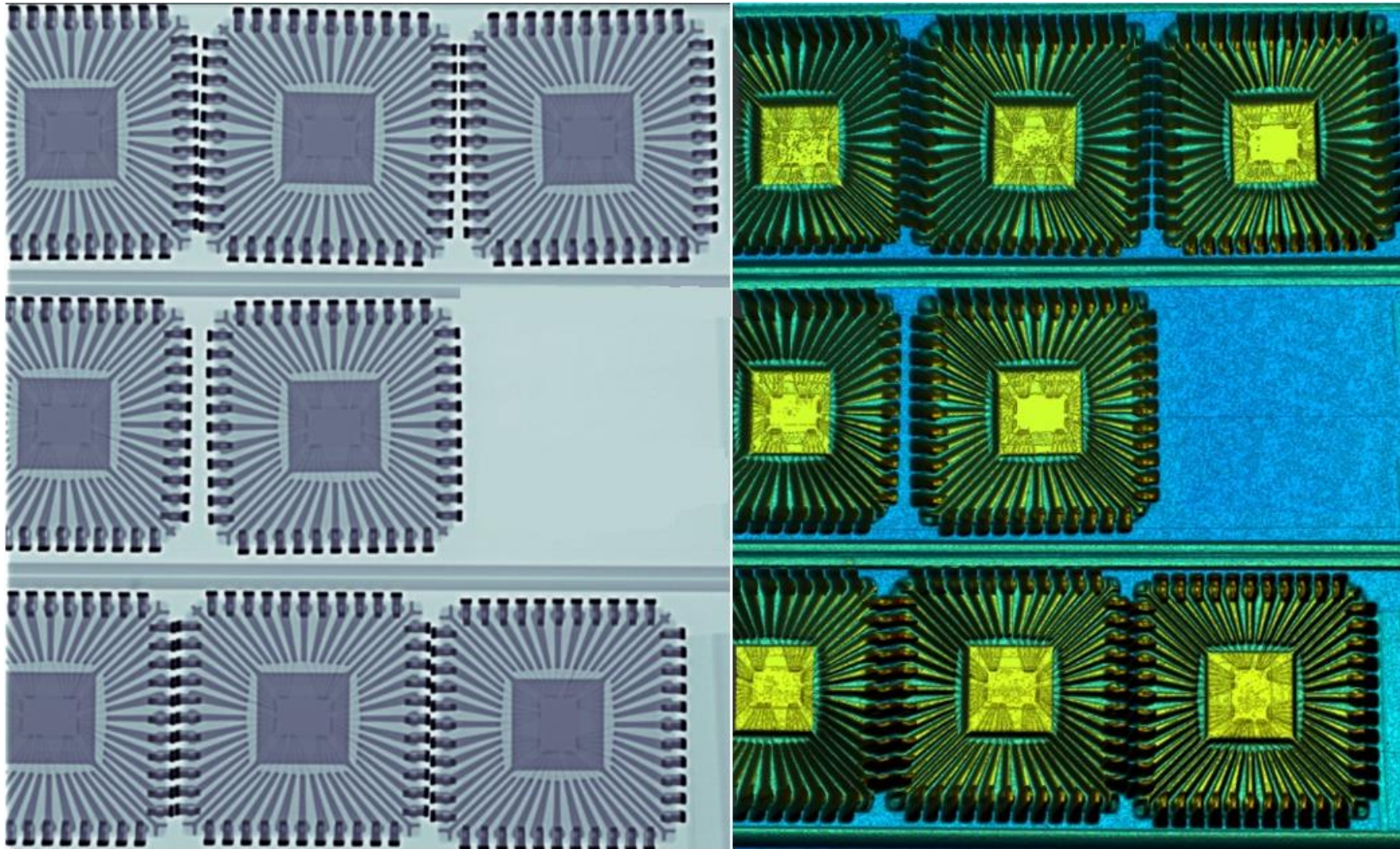
X-ray- *Detail imaging & 3D rendering highlight consistent construction*

Images owned by Raytheon Technologies



3 lot sites were selected for X-ray. Showed consistent lead frame, die & wire bond construction

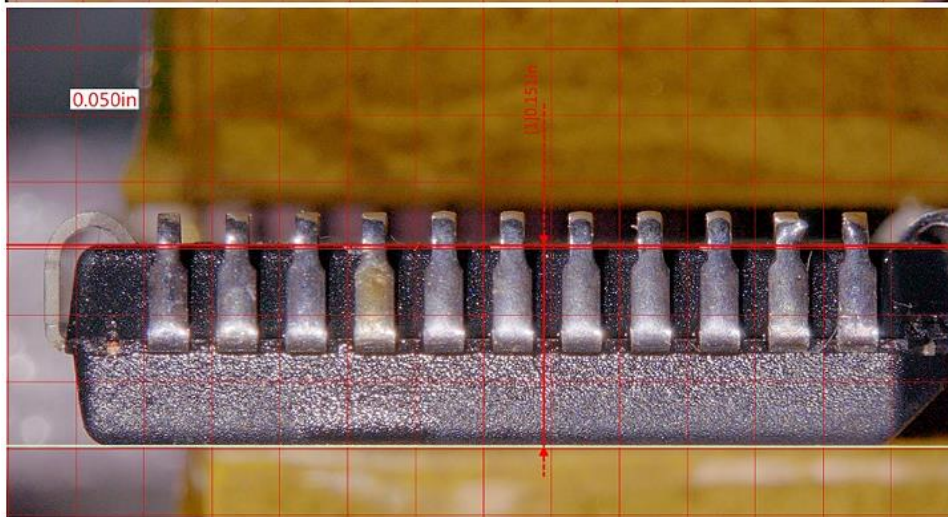
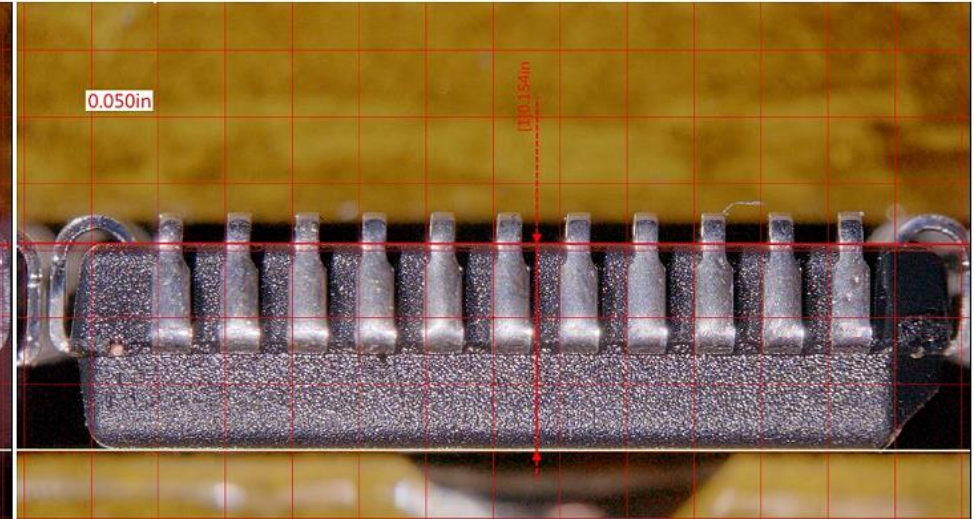
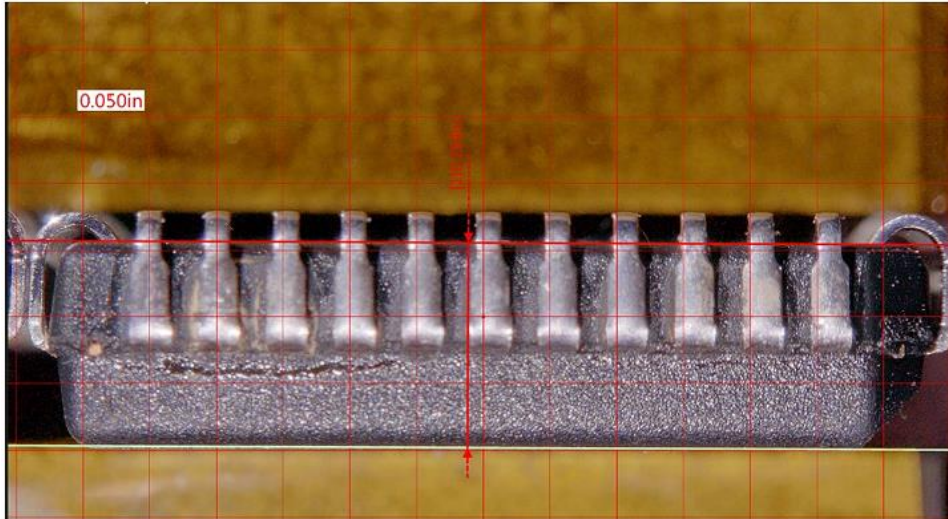
X-ray- *Detail imaging & 3D rendering highlight consistent construction*



*Images owned by
Raytheon Technologies*

3 lot sites were selected for X-ray. NO Issues encountered during internal inspection

Component Thickness- *Determine bake out time IAW J-STD-033D*



Thickness Calculation

S1. 0.154 in.

S2. 0.154 in.

S3. 0.151 in.

 $0.459 \text{ in.} / 3 = 0.1530 \text{ in.}$

$\text{XC9536-15PC441} = 3.8862 \text{ mm}$

*Images owned by
Raytheon Technologies*

Physical dimensional measurements are inline with supplier datasheet

Component Bake out Calculation- IAW J-STD-033D; Table 4.1, Pg. 9

IPC/JEDEC J-STD-033D

Table 4-1 Reference Conditions for Drying Mounted or Unmounted SMD Packages
(User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125 °C + 10/-0 °C < 5% RH		Bake @ 90 °C + 8/-0 °C ≤ 5% RH		Bake @ 40 °C + 5/-0 °C ≤ 5% RH	
XC9536-15PC441 = 3.8862 mm Thickness > 2.0 mm ≤ 4.5 mm (see Note 5)	2	48 hours	48 hours	10 days	7 days	79 days	67 days
	2a	48 hours	48 hours	10 days	7 days	79 days	67 days
	3	48 hours	48 hours	10 days	8 days	79 days	67 days
	4	48 hours	48 hours	10 days	10 days	79 days	67 days
	5	48 hours	48 hours	10 days	10 days	79 days	67 days
	5a	48 hours	48 hours	10 days	10 days	79 days	67 days

Remaining Qty. 101 components are to be baked out at 125°C for 48 hours

Monitored Bake out Process- IAW J-STD-033D

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Completed Bake out after 48 hours @ 125°C. Product Stabilized to 30°C for 2 hours

Reseal Process for Storage- IAW J-STD-033D & J-STD-020

Sealed in Moisture Barrier bag (MBB), with Desiccant & Humidity Indicator Card

Images owned by Raytheon Technologies

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL 2
If blank, see adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at $\leq 40^{\circ}\text{C}$ and $\leq 90\%$ relative humidity (RH)

2. Peak package body temperature: 285 $^{\circ}\text{C}$
If blank, see adjacent bar code label

3. After bag is opened, devices that will be subjected to reflow solder or other temperature process must be

a) Mounted within: 168 hours of factory conditions
If blank, see adjacent bar code label
 $\leq 30^{\circ}\text{C}/60\%\text{RH}$, or

b) Stored per J-STD-033

4. Devices require bake, before mounting, if:

a) Humidity Indicator Card reads $>10\%$ for level 2a - 5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$

b) 3a or 3b are not met

5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: FEB 07 2012
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL 3
If blank, see adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at $\leq 40^{\circ}\text{C}$ and $\leq 90\%$ relative humidity (RH)

2. Peak package body temperature: 225 $^{\circ}\text{C}$
If blank, see adjacent bar code label

3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must

a) Mounted within: 168 hours of factory conditions
If blank, see adjacent bar code label
 $\leq 30^{\circ}\text{C}/60\%$

b) stored at $\leq 10\%$ RH

4. Devices require bake, before mounting, if:

a) Humidity indicator card is $> 10\%$ when read at $23 \pm 5^{\circ}\text{C}$

b) 3a or 3b not met

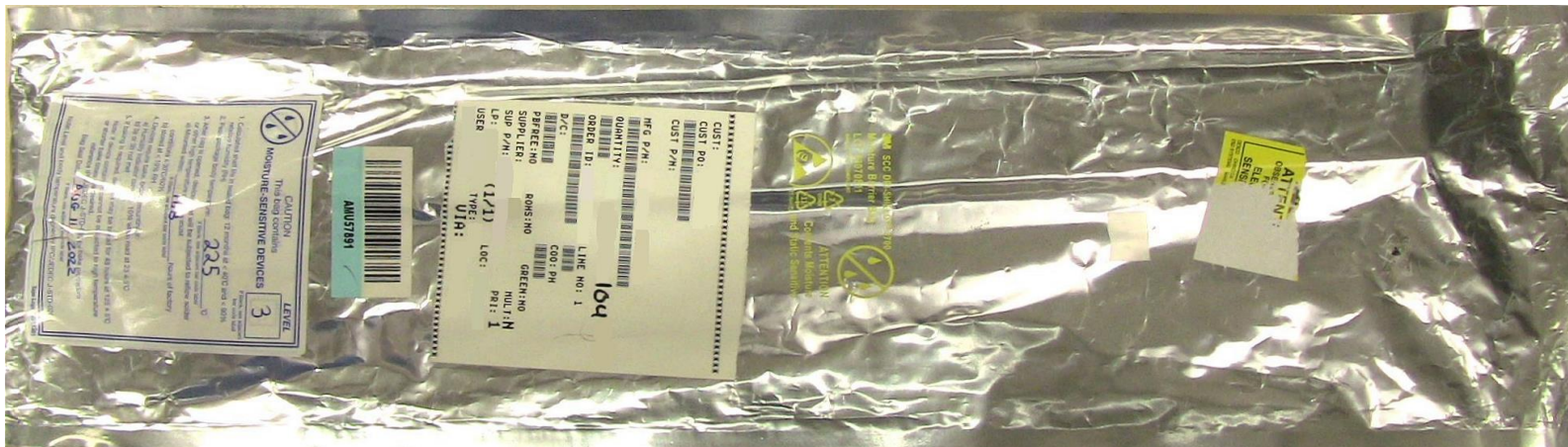
5. If baking is required, devices may be baked for 48 hours at $125 \pm 5^{\circ}\text{C}$

Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: Aug 11, 2022
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020

Tape Logic® #DL17-81



Bake out date documented with label applied; New Desiccant & HIC sealed with components

Results Summary- *Components pass all Requirements*

FINDINGS:

Task	STATUS	Findings & comments
2.0 Provenance	Complete	Original paperwork provided from Franchised Distributor. Shows acquisition of DC 1145 Components from supplier, No CF Incidences for this part number. Engineering QA team provided additional detail.
3.0 Optical Inspection	Complete	Components appear to be new / un-used stock. J-Leads compressed with contact marks, established these were likely socketed for test & programming (CPLD)
4.0 X-ray Fluorescence	Complete	PLCC lead frames are electroplated with Tin-Lead plating, Nickel barrier & Copper basis metal
5.0 Solderability	Complete	Per J-STD-002E, Method 4.2.1, TEST A. Qty. 3 Components allocated for test. (2) Sides assessed, Qty. 66 Leads total. PASSED. Requirement > 95% Coverage. Measured > 99%
6.0 Cursory X-ray	Complete	All components have consistent construction with no voiding, wire bond, lead frame or part to part variability issues
7.0 Component Thickness	Complete	Average Component thickness is: 0.1530 in. (3.8862 mm), required for bake out time calculation
8.0 Bake out Calculation	Complete	Per J-STD-033D, Table 4.1. PEM requires 48 hours (2 days) @ 125 Deg. C.
9.0 Monitored Bake out	Complete	Completed in monitored oven; 8/8 to 8/10. 1H Ramp Up – 48H Dwell – 1H Ramp Dn
10.0 Reseal Process	Complete	Resealed with Desiccant, Humidity Card and MSD Label, RTX Stores Logistics assisting.

Components will be subjected to Solder reflow, Internal Test, Programming and extended Functional Test as part of the NHA process

Recommendation: Components passed all Inspection steps and are re-certified for use

Thank you!

Questions???