Multi-Project Wafer Sort and Inspection Applications

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Outline:

1) Introduction
    a) Outline
    b) Multi-Project Wafer Scope
        i) Definition
        ii) Drivers for MPW Processing
            (1) Low Volume of Chips Required
            (2) Reduces NRE Costs
            (3) Decreases Time to Market
        iii) Applications for MPW Processing
            (1) III-V Materials (GaAs, GaN, InP), SiC
            (2) Wafer Level Packaging
            (3) Technologies (RF and Power Management, MEMS, Optoelectronics)
            (4) Industries (Defense, Aerospace, Medical, Automotive)
    c) Multi-Project Wafer Processing Challenges
        i) Multiple Passes Required
            (1) Hardware Set
            (2) Inspection Criteria
        ii) Advances in Singulation Technology (Plasma Dicing, Stealth Dicing)
        iii) Wafer Map Limitations
2) Multi-Project Wafer Sort
    a) Hardware
        i) Universal Eject Heads
        ii) Pick-up Tip Types
    b) Wafer Mapping
        i) Formats (SEMI E142, Royce XML)
        ii) Requirements (product type, reticle geometry)
    c) Output Set-up
3) Multi-Project Wafer Inspection
    a) Program Requirements (Die Alignment, Inspection Criteria)
    b) Inspection Surface Considerations (Top, Underside, Edge)
    c) Dynamic Inspection Program Control
        i) Programs defined for each part in wafer map
        ii) Automatic program switching during sorting
4) Role of Die ID in MPW Sort and Inspection
    a) Embedded in Wafer Map

    b) Read via OCR during Inspection

5) Future Discussion
    a) Industry Direction
    b) Limitations of Existing Approaches
    c) Research and Development Areas
6) Conclusion
7) Q&A