Passive Components and Integration for Power and RF Modules

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Course Summary

Passive component advances and integration is becoming the key for ultra-thin and high-performance electronic systems. This talk will review advances in integrated passives in all three categories – surface-assembled ultra-thin IPDs, package-inserted IPDs and package- or wafer-embedded thinfilm passives.

Inductors and capacitors are critical storage components in power converters. Their large size is, however, a major bottleneck for module integration and efficient power management. High-density passives can migrate the power converter close to the load. This can lead to lower losses and more efficient and granular power delivery. Emerging nanoscale and thinfilm components provide unique opportunities to enhance volumetric densities, reduce losses and integrate components close to the chip. These passives are either formed with substrate- or wafer-compatible processes, or pre-fabricated and inserted as integrated passive devices (IPDs) to form 3D power packages. The first part of the presentations deals with advances in power passives for high efficiency and power handling.

Passive-active integration for emerging RF (1-77 GHz) packaging will be covered in the second part of the talk. Glass provides unique opportunities for High Q passives in diplexer IPDs and embedded matching networks. Integrated nonreciprocal components, tunable components, EMI shielding or noise isolation with 3D copper and nanomagnetic structures can further enhance the component densities and realize true heterogeneous system integration. Advances in passive integration with additive manufacturing techniques such as inkjet and 3D printing with lower cost and higher on-demand customization will also be reviewed.

Instructor Bio

P. Markondeya Raj is a Research Professor and Associate Research Director with the 3D Systems Packaging Research Center (PRC), Georgia Institute of Technology, Atlanta, USA. His expertise is in the areas of packaging of electronic systems, power-supply component integration on silicon, glass and organic substrates for power conversion and integrity, RF/5G components, integrated RF and power modules and fine-pitch interconnections. He coauthored about 280 publications, which includes 14 books, 8 patents with others pending. He received more than 25 “Best Paper” awards for his conference and journal publications. He is the Co-chair for IEEE CPMT Nanopackaging technical committee and US CPMT representative for IEEE Nanotechnology Council. He is also the Past Chair for the “High-speed, Wireless & Components” thrust in the CPMT, Electronics and Component Technology Conference (ECTC), and Associate Editor for the Transactions of CPMT and Associate Editor for IEEE Nanotechnology Magazine. He received his PhD from Rutgers University in 1999 in Ceramic Engineering, MS from the Indian Institute of Science, Bangalore (1995) and BS from the Indian Institute of Technology, Kanpur (1993).