Advanced Integrated Circuit Packaging and Reliability Issues

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Course Summary

This short course provides a holistic understanding of all aspects of reliability failure mechanisms of an advanced IC packages. It covers advanced packaging technologies such as Flip Chip BGA, Wafer Level packages, 2.5D/3D Packages and Cu pillar and wirebonding; and their reliability failure modes and design solution.

1. Advanced packaging technologies and reliability failure mechanisms
    a. Advanced packaging technologies including FCBGA, WLCSP, WLP, SiP, 2.5D/3D TSV and Non TSV based 2.5D packaging
    b. TSV, Interposer and Cu Pillar Bump Related Failures
    c. Solder bump migration failure under combined electrical current, thermal mechanical stress and temperature changes
    d. Cu wirebonding long term reliability
    e. Warpage and board level Solder joint reliability
    f. Package reliability design
2. Chip to package interaction (CPI)
    a. CPI effects during package assembly processes
    b. CPI effects in field application
    c. CPI simulations
    d. CPI qualification
    e. Quantitative CPI reliability
    f. Electrical CPI
    g. Chip Board Package Interaction

Instructor Bio

Dr. Richard RAO is currently a Fellow of Microsemi Corp, a lead supplier of high reliability integrate circuit, located in southern California, USA and an elected Senior Member of IEEE. He is responsible for the corporate reliability and advanced packaging solutions. His focus is to find the advanced packages to meet the high performance, high reliability and high power semiconductor ICs; to study the new failure modes and mechanisms of cutting edge Silicon and packaging technologies as well as to develop design for reliability solutions for advanced circuits, packaging and chip to package interaction. He has a Ph.D. degree in solid mechanics of materials from the University of Science and Technology of China, the most prestigious university in China. Prior to joining Microsemi in 2004, Dr. Rao held various academic and technical positions in reliability physics and engineering. He was an associate professor at University of Science and Technology of China, a research fellow at Northwestern University, Evanston, IL, USA and a National Science and Technology Board Research Fellow of Singapore. He also held senior and principal technical positions in Motorola Electronics and Ericsson Inc. He has published over 30 papers on reliability physics and applications and a main contributor of several JEDEC standards. He is a technical committee member of IRPS (International Reliability and Physics Symposium) and ECTC (Electronics Component and Technology Conference). He is a frequent speaker to IRPS, ECTC, ISQED (International Symposium on Quality Electronics Design), ASME Symposiums and a keynote speaker to ICEPT and International Conf on System on Chip, etc. Dr. Rao has over 20 years' hands on experience and knowledge in silicon to package to system integration such as HKMG and FinFET, high performance FCBGA/CSP,WLP, 2.5D/3D, chip to package to board interaction, board and system level reliability physics and applications. He has conducted professional development courses on advanced IC reliability to both industrial and academic worlds.