

# **Modeling and Characterization of the Power Distribution Network and High Speed Signaling for a 3D Integrated Micro Scale System**

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The design of the power distribution network for a modern FPGA SoC integrated into a system presents a number of challenging requirements. The inductance of the traces, bulk and local energy storage requirements and response times must be considered. Multiple power rails in digital, analog and RF domains are typical, increasing the crosstalk and noise between the domains – which can degrade overall system performance.

In this presentation, The power distribution network, high speed JESD-204 transceiver interconnect and RF Subsystem will be modeled and characterized for a three-dimensional system composed of an FPGA SoC, Memory, Analog RF silicon die and additional discrete components. The system implements more than 15 different power domains at multiple voltage levels in a multi-layer sub 20mm on a side rectangular footprint.

The primary FPGA SoC die, associated power management and other components in the first silicon plane are integrated onto an ultra-low CTE polymer interposer with 3 layers of copper interconnect. The memory, analog and other components are integrated on a second silicon plane interconnected to the primary silicon plane. The 3D power distribution network for the 0.95V digital core logic on the primary FPGA and the 1.8V supply for the JESD-204 transceivers will be extracted and modeled with SPICE. Also, the JESD-204 transceivers and associated interconnect will be modeled, extracted and characterized at over 10 Gigabaud/sec.

The ultra-low CTE interposer is closely matched to silicon to allow extremely high density interconnect between the die on each silicon plane. The semiconductor die are tightly abutted to each other as well as to the discrete components. The power distribution network on the interposer is similar to the multi-layer orthogonal mesh topology on semiconductor die. This is substantially different from the power planes typically used in PCBs. The power mesh contains multiple power rails in multiple regions on each silicon plane. An overall 3D system topology with these attributes can provide a substantial improvement to the performance of the power distribution network and hence the overall system performance.