Packaging and Heterogeneous Integration During and Post Moore's Law Era

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Semiconductor and systems landscape is changing dramatically. Moore's Law is no longer valid since cost reduction as the next node is introduced with higher transistor density is not possible anymore. In addition, limits are being seen in front end due to high leakage and in the backend due to higher RC delays.

The driving engines for electronic systems, on the other hand, are also changing dramatically to smart robotic systems with artificial intelligence along with wearable, wireless healthcare, wireless networks, new era in self driving and ultra-high power automotive electronics requiring high-temperature electronics with highest reliability

In the post Moore's Law era, Georgia Tech believes package integration must enable better devices in the short term and better systems with highest functional density and lowest SWaP in the long term.

To address the above needs, heterogeneous package integration (HPI) has begun with Si-based packaging and integration so far. It is an excellent 1st step. The next generation of HPI, however must be dramatically different: 1) The integration must happen at package level and not at board level, as it is currently 2) Such an HPI package must be assembled on board directly without another package in between, as with current Si packaging 3) Since the HPI package will be larger than 10 mm in size and since current HPIs are produced in 300 mm size wafers, cost-effective HPIs need to come from> 510 mm size panels. 4) HPIs must be designed with true 3D architectures in contrast to current 2.5D and 3D. The 2.5D is not best for shortest interconnect length, whereas current 3D stcking with TSVs has two problems--- 1) TSVs in logic ICs taking too much real estate for power and signals and high thermal dissipation from logic ICs through the stack.The other improvement is to do with HPI material properties. Si has high electrical loss, high dielectric constant, and low resistivity— all undesirable. . As RDL is scaled down further to increase I/O density, it becomes increasingly resistive leading to higher RC delays. The other enhancement is to do with the ideal CTE of ~7ppm/C for large 20-50mm HPI packages, to achieve both chip and board level reliabilities simultaneously. Si CTE is 3ppm/C, ideal for chip but not for board, and Si interposers need an additional BGA package, therefore, making Si-based HPIs a four-level hierarchy, making the interconnections even larger and the systems even bulkier.

Georgia Tech proposes an alternative 3D architecture for next generation of HPI that addresses all the above needs and combines both package and system into one, dramatically improving performance, reliability, cost and size--- both for commercial and military.

This new 3D system architecture leads to ultra-small SWAP systems for military applications.

Prof. Rao Tummala is a Distinguished and Endowed Chair Professor at Georgia Tech in USA. He is well known as an industrial technologist, technology pioneer, and educator. Prior to joining Georgia Tech, he was Director of Advanced Packaging at IBM and an IBM Fellow, pioneering such major technologies as the industry's first plasma display and the first and next two generations of 100 chip multi-chip packaging. He is the father of LTCC and System-on-Package (SOP) technologies. As an educator, Prof. Tummala was instrumental in setting up the largest Academic Center funded by NSF as NSF Engineering Research Center in Electronic Systems at Georgia Tech, producing more than 1500 engineers, with an integrated approach to research, education and industry collaborations with companies in US, Europe, Japan, Korea andTaiwan. He has published 800 technical papers and invented many technologies that resulted in over 110 patents, wrote the first modern textbook in packaging, Microelectronics Packaging Handbook(1988); the 1st undergrad textbook, Fundamentals of Microsystem Packaging (2001); and the 1st book introducing the concept of SOP, Introduction to System-on-Package(2006). He received more than 50 Industry, Academic and Professional Society awards. He is a member of NAE and IEEE Fellow.