MIL-PRF-ATM Development

JEDEC JC 13.7 and SAE CE-12 Task Group

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Introduction

- MIL-PRF-ATM (Advanced Technology Microcircuit) is intended to provide an avenue to introduce advanced packaged ICs with through silicon via (TSV) and other integration technologies into the Military and Space QML system
- MIL-PRF-ATM works alongside MIL-PRF-38535 (Integrated Circuits) and MIL-PRF-38534 (Hybrids) to ensure there is a path for EEE components using these integration methods to be included in the QML system

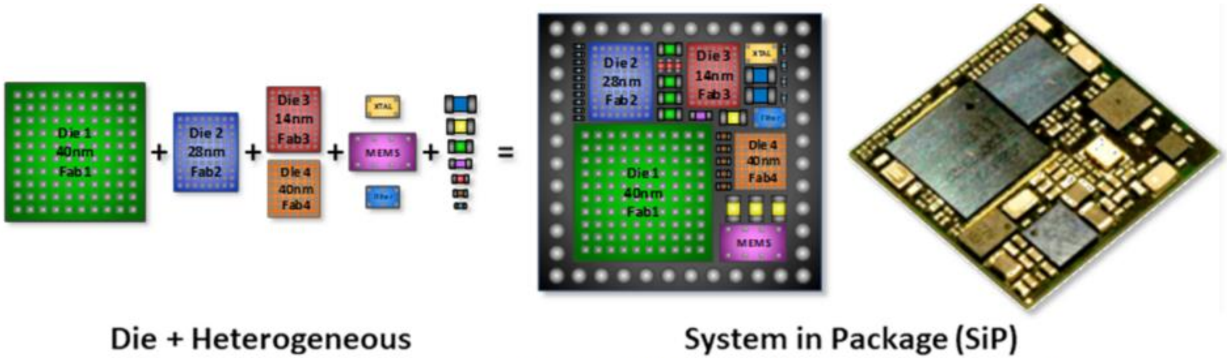

Figure 6. Heterogeneous Integration and System in Package (SiP). Source: ASE

[Ref: Heterogeneous Integration Roadmap - IEEE Electronics Packaging Society]

- Foundational elements from 38535 and 38534 are merged with OEM addressed degradation modes and mechanisms to provide a path to demonstrate technology capabilities and reliability for military and space usage
- >2D technologies are typically unique to an OEM leading to much more reliance upon OEMs to identify degradation mechanisms associated with the fabrication and packaging technologies used

Structure applied to standardize the non-standard

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- Technology and OEM agnostic outline levels applied to enable stand alone requirement definition (Limited technologies specifically not addressed (PICs))
- Modes and Mechanism applicability leveraging known issues (JEP122, JESD158, etc.) with justification and supporting test data
  - Qualification reliant upon OEM data
  - Advanced product data package (APDP) (replacement for PIDTP in 38535) communication vehicle
- Independent verification through test challenged by signal density and time/cost
  - Test assumed at element level and higher
  - OEMs required to provide access to “critical” signals including those impacting these signals
  - Industry standards (IEEE 1838, BoW, UCIe, etc.) leveraged whenever available

Integration level	Designation	Description
1	Product or Device	QML listed product that is a packaged device with applicable QML marking
2	Integrated element	Elements within a product that are integrated onto the fan out surface, interposer, or other applicable technology.
3	Stacked element	Elements stacked into a configuration that allows integration with the fan out technology to be implemented. Stacked elements may or may not be able to be independently packaged or tested. Stacking processes may occur at a foundry or within an associated fabrication process.
4	Element	Lowest level of integration addressed by this standard. Elements are where lot definitions begin. Elements may be passives within a package or various active die that are included in stacks.
5	Sub-element	Sub-elements are made up of chiplets or related technologies that are integrated through 2 or 3 dimensional methods onto a wafer. These sub-elements may have communications or other functions that are buried within the element that are stacked and integrated to form the final ATM product.
6	Chiplet	Chiplets are functional elements that are circuit blocks a manufacturer of ATM products may leverage from their own or third party intellectual property libraries to form sub-elements. Chiplet technology may or may not be available for detailed evaluation by QA.

OEM’s relied upon to demonstrate mode / mechanism applicability

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- Varying technologies (materials, nodes, etc.) within the same package combined with the need to identify applicable degradation modes leads to OEM’s needing to identify and justify which modes are applicable and how these have been addressed
  - Modes / mechanisms range from physical and construction (thermal mechanical and radiation induced) to application (design and process selection)
- Challenged by existing mechanism models and testing approaches built upon 2D construction
  - Radiation: impact of complex designs with multiple secondary interactions
  - Reliability: legacy part (35/34) reliability primarily implied through passing series of tests. Limited objective criteria to evaluate reliability of >2D construction through simulation and modeling
  - Qualification: defining a set of minimum tests and data to prove a part is qualified given that each OEM technology and fabrication processes may vary
- Applicability of process or step level mechanism verification (models, simulations, testing, etc.) to a fully integrated part using multiple technologies within the same package
  - Over what range of criteria is testing required? Over what temperature ranges and how to best measure temperatures within devices operating in range of applications? How many parts are required in each test to verify test methods, quality or reliability goals, repeatability, etc.?

Reliability considerations

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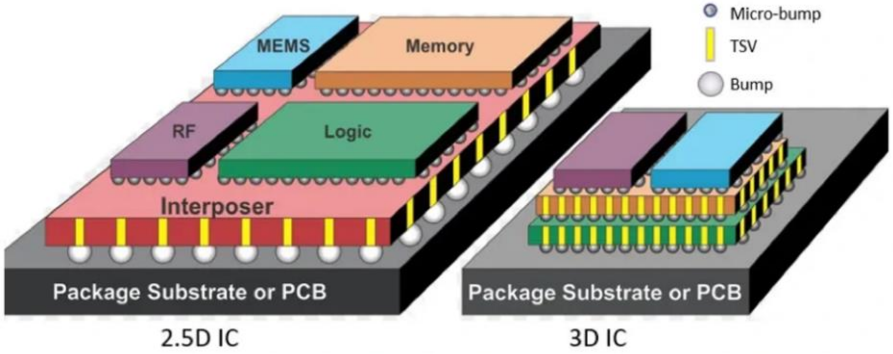
- Legacy approach to reliability for military standard parts focused on screening
  - 44K device hours assuming 15 year operation for steady state life testing
- Several issues exist in using this as an assumed reliability goal
  - Few space programs today have a design life of 15 years (Is 44K device hours the right target?)
  - Temperature capabilities (-55 to 125C) for technologies and fabrication methods may very
  - Junction temperature and activation energy may be different for each technology used
  - No consideration for embedded FW/SW or associated faults
- Result: reliability considerations and definitions may need to evolve to view these “parts” as “systems”

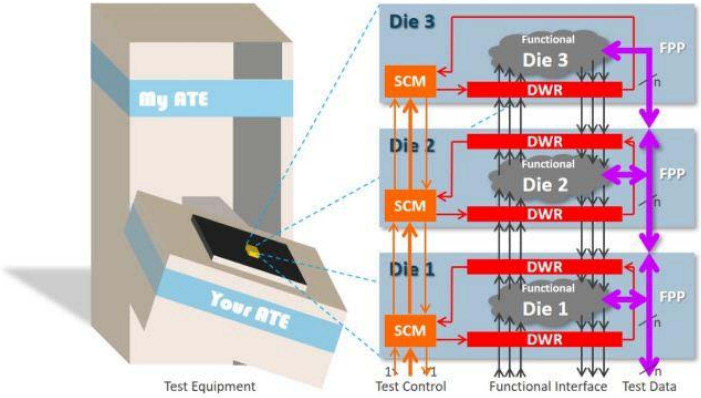


Source https://techovedas.com/what-is-2d-2-5d-3d-packaging-of-integrated-chips/

- Life limiting mechanisms may not be able to be fully tested at integrated system level
  - Output may be limited by comm failures
  - Stacks may not be configured for independent packaging and testing
  - Interposers / mechanical separation may limit energy transmission for mechanism activation
- Challenge: Impacts legacy definitions of “lot” and what a “known good die” (KGD) means in the context of an integrated system

Radiation considerations

- Existing radiation test standards and approaches may be insufficient to characterize fully integrated ATM devices, especially by third party organizations that do not have access to detailed OEM design information
  - Identification of sensitive volumes as compared to critical signals or outputted signals
  - Emerging test standards (IEEE 1838, etc.) may help close the test and metrology gaps
- Material layers generate secondary particles resulting in difficulty identifying the root cause or susceptibility of effects (Assuming methods to characterize effects independently are used)
  - Chiplets and 3rd party IP blocks pose separate problem due to "black box" design approaches
  - Comm protocols may leverage standards (BoW, UCIe, etc.) or use proprietary protocols



Source https://www.eetimes.com/ieee-1838-allows-test-access-to-every-die-in-3d-ic-stack/

- Correction circuitry may obscure effects depending on read out timescales and applications
  - Technology or fabrication unique methods, including test circuits, may be needed to understand impacts
  - Some functions may be invisible at package level
- Legacy interpretation of RHA certification may be challenged

Additional issues being considered for incorporation

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- Applicability and value of including passive elements
  - SOCs, SIPs, etc. may integrate passives in the construction of the device, but this is a different approach than traditional hybrids
  - Criteria for passive element qualification / screening may not align with technology needs
- Supply chain and cybersecurity demands
  - Supply chain and cybersecurity is a continuing source of concern for the user community with limited to no mention of it in military standard product design or procurement docs
  - Manufacturers perform mitigation activities in various ways throughout the product lifecycle making a standard requirement set difficult to define and verify
  - Supply chain and cyber risks are orthogonal considerations to product qualification resulting is complication in using existing part class structures to address these risks
- Verification vs. application specific testing
  - 3DIC's may have multiple internal clock domains complicating verification testing
  - "Nominal" configuration and test results may have limited applicability to application
  - Specification sheet performance may be impacted by multiple internal critical signals susceptible to usage and environment unique degradation modes
  - Acceptance criteria may not be able to address range of usage conditions

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Qualification and Test Considerations

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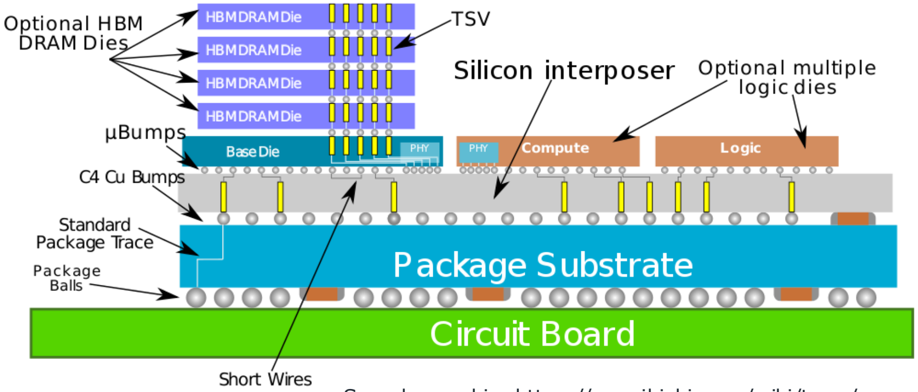
- Qualification challenged by multiple levels of integration, test, and degradation modes
  - Qualification at one level may not apply to a higher level of integration
  - "Known good die" has different meanings and different approaches
  - Qualification may need to include technology, fabrication process, and other elements that it does not today
- Verification activities (optical, electrical, etc.) exist at multiple integration levels challenging legacy QML product flow assumptions
  - OEM defined screening flows
  - "Product changes" (PCNs, etc.) may take on different meaning
  - Proprietary nature of technologies may require NDAs or other methods for users to understand how technologies are applied



Sample graphic: https://en.wikichip.org/wiki/tsmc/cowos

- Qualification, test time and cost significantly impacted by device complexity
  - Parts are now systems with all that implies
- Post procurement testing or analysis may require teaming with OEMs to have context and understanding of test results considering design and integration approaches

Gaps to closure of MIL-PRF-ATM

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- Identifying minimum viable specification and qualification data set from element to packaged part
  - Integration level unique tests including data capture and evaluation within reasonable cost / time
  - Number and type of tests required to justify degradation modes and mechanisms (sampling)
  - Applicability of standards and impact when they are not used (DfT, EDA, tests, comm, etc.)
  - Model / simulation verification and validation, especially as applicable to EDA tools and design rules
- Impact and path forward for legacy test and evaluation approaches
  - Analyses: WCCA, FMEA, etc. and applicability
  - Test: Burn-in, life test, etc. and applicability given functional and application variance
  - Test methods: MIL-STD-883 update(s) and impact to usage
- User impacts:
  - Non-NDA access to information for evaluation and decision making
  - Applicability of de-rating, numerical reliability, etc. to usage of devices
  - Methods to evaluate application specific performance without significant test cost and schedule
- New issues that may need to be evaluated:
  - Cyber and other requirements and evaluation methods without application specific information
  - Software bills of material (SBOMs) and related elements
  - Radiation evaluation criteria for SEE with multiple secondaries and/or identifying evaluation criteria

Thank you

Questions?