KYOCERA AVX

ACCELERATING INNOVATION

CMSE 2025

Advancements of Stacked Capacitors for Military and Flight Applications

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Stacked Capacitor Technology

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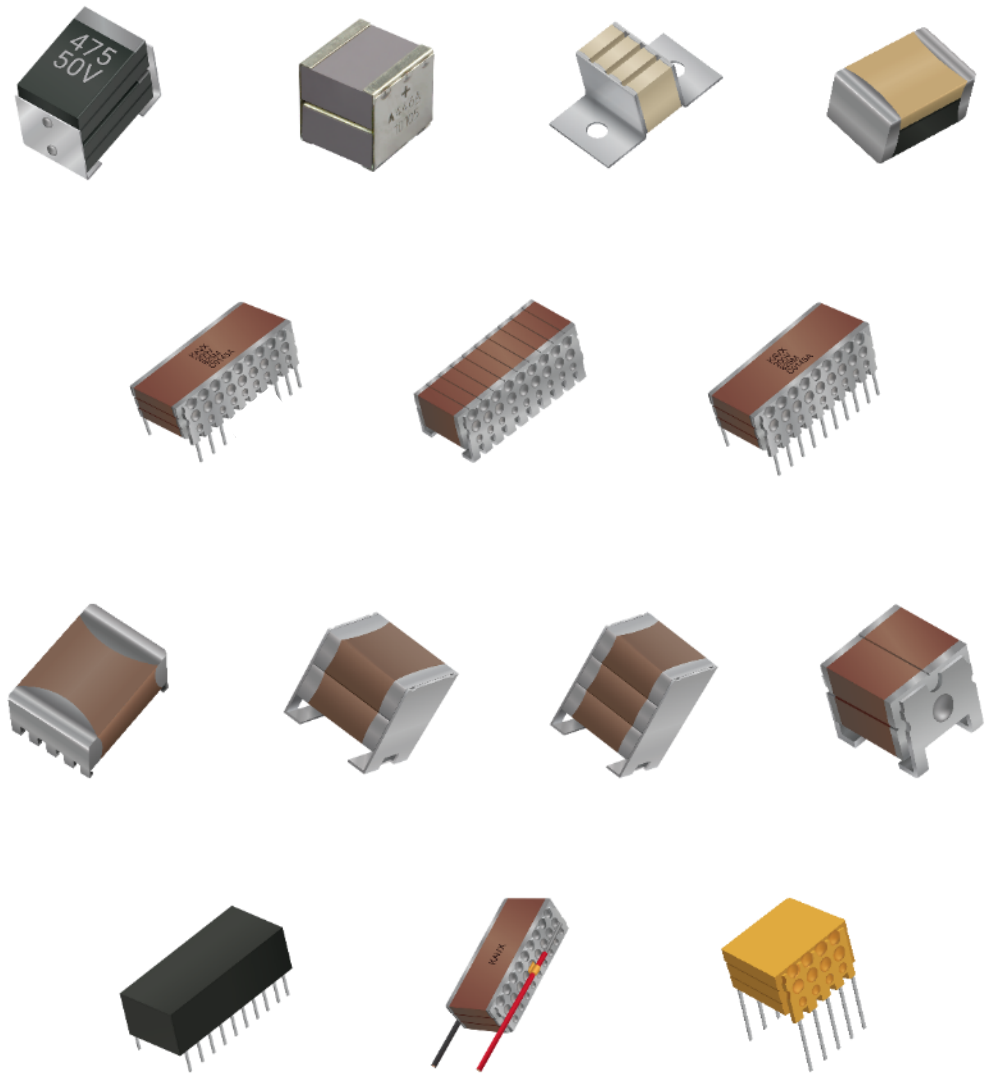
Why Stacked Capacitor Technology?



STACKING ADVANTAGES:

- Increased capacitance in a given XY board area (capacitors)
- Increased RMS current in a given XY board area (capacitors)
- Reduced Inductance per µF/mm^2
- Improved Frequency Response Characteristics
- Reduced ESR, leading to optimized performance
- Allows mixed technology in stacks (Capacitor/Circuit Protection)
- Potential shock and vibration mitigation
- Potential active device mounting on top of stacks

STACKING DISADVANTAGES:

- Potential shock and vibration issues
- Not applicable for low height profile circuitry

Stacked Solid Tantalum Introduction

Capacitor Background – Stacked $TaMn0_2$

	TCP
	
Qualification	COTS+
Temperature	-55°C to +125°C
Voltage Rating @85°C	6 - 50V
3016	9.4 - 660µF
3032	18.8 - 1980µF

- Discrete components qualify under MIL-PRF 55365/11
- Available in 2, 4, or 6 stack module
- Terminations available in hot solder dipped and gold plated
- Space grade module ideal for DC-to-DC converters, SMPS, or any application requiring stable, high CV, and low leakage current

- Tables below clearly depict how adding one capacitor to the stack can double capacitance and RMS current handling while also minimizing ESR by over 2X.

	TCP Stack (2X)
	
Qualification	DLA 09009
Temperature	-55°C to +125°C
Voltage Rating @85°C	50V
Capacitance	9.4 µF
ESR @ 100 kHz	200 mΩ
I_{RMS} @25°C	1.22 A
I_{RMS} @85°C	1.1 A
I_{RMS} @125°C	0.49 A

	CWR29 & TAZ COTS+
	
Qualification	MIL-55365/11
Temperature	-55°C to +125°C
Voltage Rating @85°C	50V
Capacitance	4.7 µF
ESR @ 100 kHz	500 mΩ
I_{RMS} @25°C	0.55 A
I_{RMS} @85°C	0.49 A
I_{RMS} @125°C	0.22 A

Stacked Tantalum Polymer Introduction

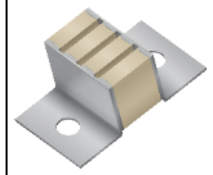
Capacitor Background – Hermetically Stacked Tantalum Polymer

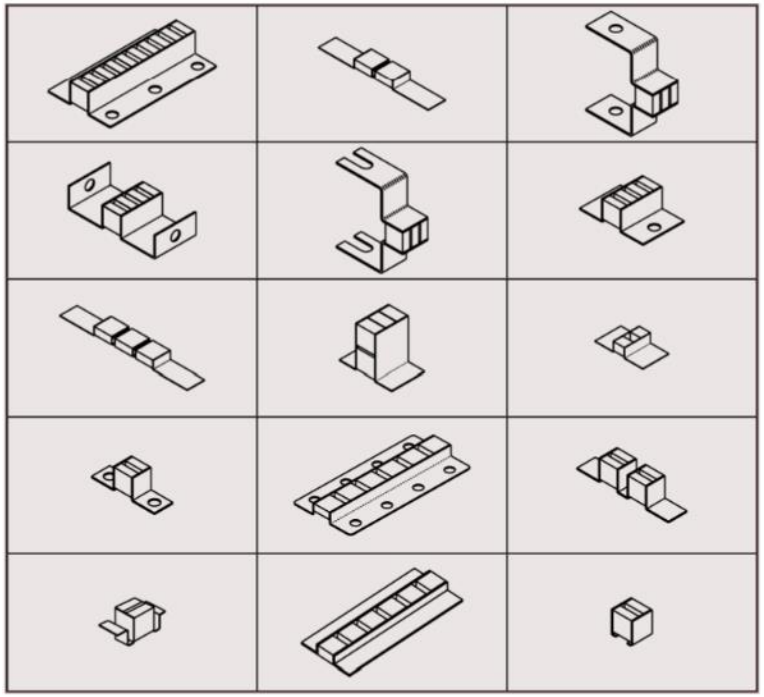
	TCH (2X)
	
Qualification	COTS+/MIL-PRF 327000*
Temperature	-55°C to +125°C
Voltage Rating @85°C	10 - 100V
ESR @100 kHz	30-100 mΩ
I_{RMS} @ 25°C	2 – 3.65 A
I_{RMS} @ 85°C	1.8 – 3.29 A
I_{RMS} @ 125°C	0.8 – 1.46 A
4649	44 - 660µF

- First Polymer capacitor to ever be used in a space mission (Chandrayaan-3 Lunar Mission)
- Ultra-low ESR
- Hermetically sealed, suited for Hi-Rel aerospace and defense applications
- Higher RMS current and Voltage handling compared to TaMn02
- Less derating needed compared to TaMn02 technology
- Being qualified under MIL-PRF 32700

Advanced Ceramic Capacitor Introduction

Capacitor Background – RF Stack

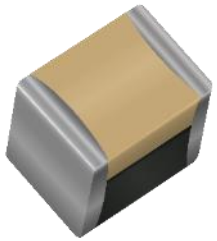
	100B/C/E Module 900C Module
	
Qualification	COTS+/DLA
Temperature	-55°C to +175°C
Voltage Rating @85°C	50V – 10kV
Capacitance 100 Series	1 – 5100 pF
Capacitance 900 Series	0.01 – 1 µF



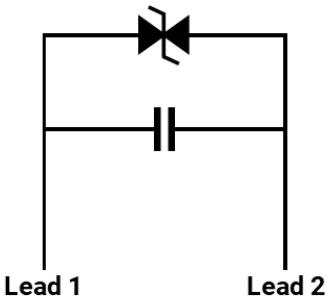
- Primarily used for DC blocking, filtering, decoupling and impedance matching on high power, RF applications
- Very High Q and power handling capabilities
- Both vertical and horizontal stack/mounting options in either series, parallel, or a combination.
- Extremely low ESL/ESR

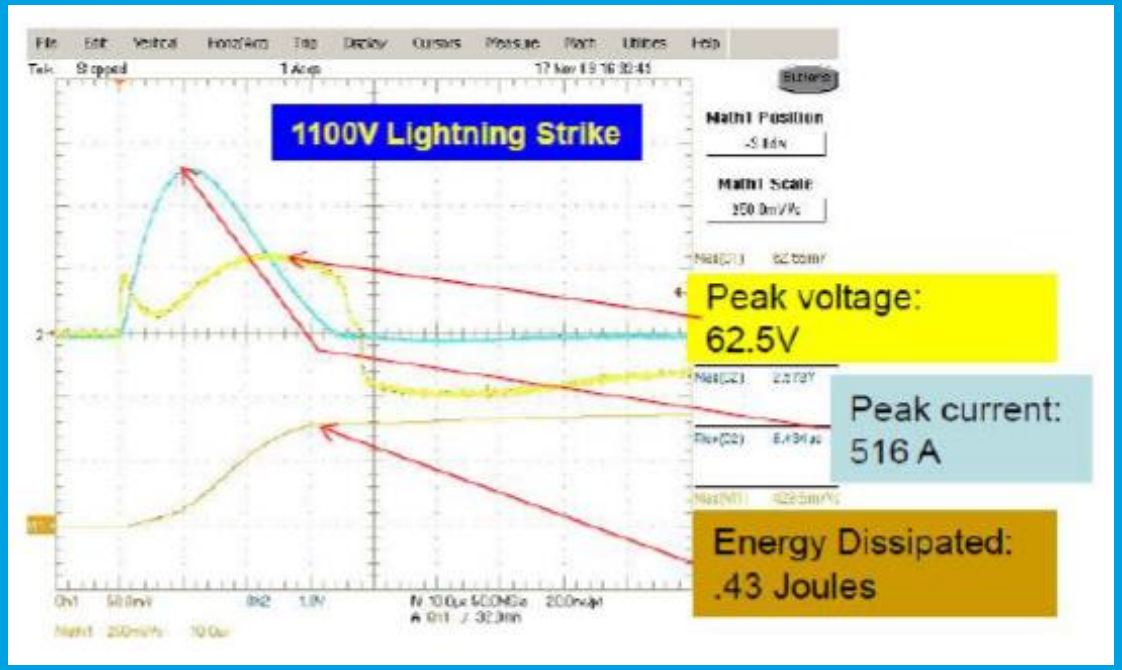
Advanced Ceramic Capacitor

Capacitor Background – MLCC/MLV Stack

	CapGuard
	
Qualification	Standard / Auto
Temperature	-55°C to +125°C
Working Voltage	18 - 60 V_{DC}
Energy	1.2 - 1.6 J
Clamping Voltage	42 - 120 V
$V_{B\ Nom}$	25 - 76 V
1210	0.012 - 0.1 µF

- MLCC X7R to mitigate EMI
- Multi Layer Varistor (MLV) to mitigate ESD strikes
- Comes in Surface Mount Technology (SMT) or Radial footprint

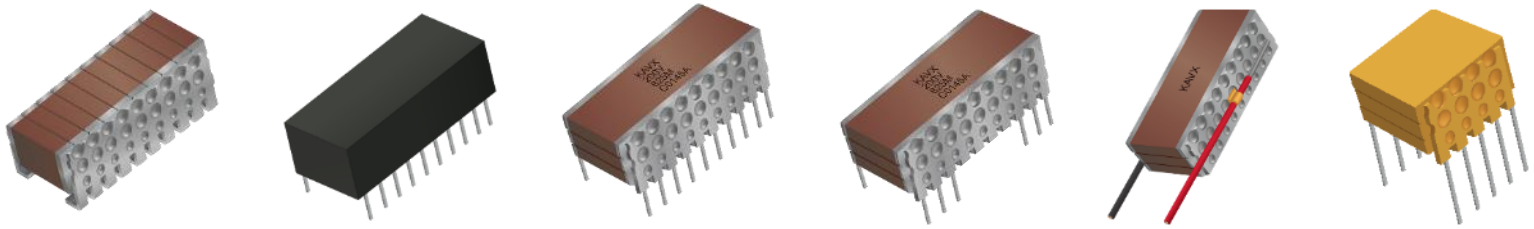




RTCA DO-160 Testing Data

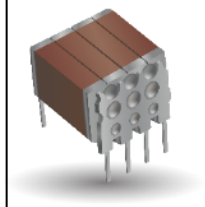
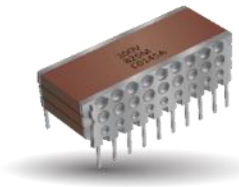
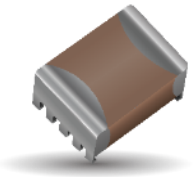
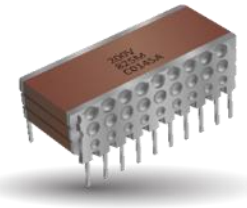
- 1100 V lighting strike test
- Multiple strikes at 500 Amperes peak current
- Peak voltage limited to 62.5 V

Stacked PME Ceramic Capacitor Introduction

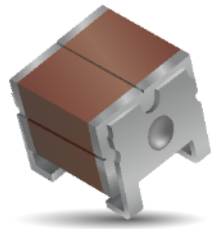
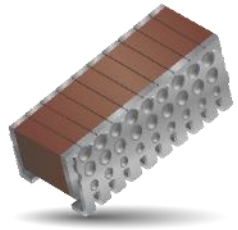
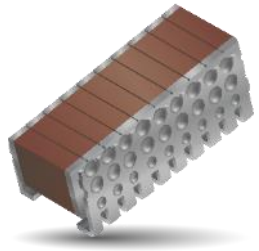


- Wide array of options for PME stacks
- Vertical & horizontal stacks, encapsulated, through hole or surface mount options available
- Select Discrete capacitors adhere to MIL-PRF 32535
- Select Stacks adhere to MIL-PRF 49470/1 (unencapsulated) MIL-PRF 49470/2 (encapsulated)
- Testing standards “B” or highest reliability level “T” available
- Many custom configurations are also available from select Manufacturers
- More offerings in either standard or automotive qualified range are also available

Stacked PME Ceramic Capacitor Introduction

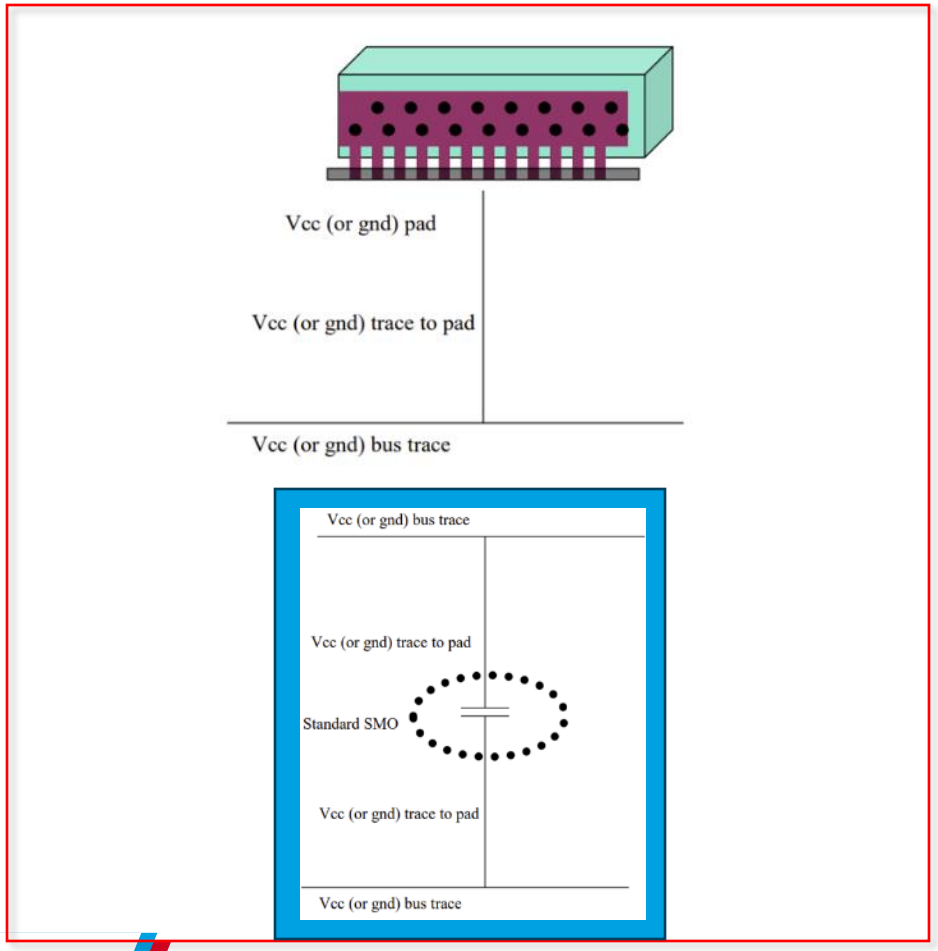
	CV	CH	RM	HV	SMM / RMM	SMX	MH	RH		SM	
											
Qualification	Standard	Standard	Standard	Standard	Standard	Standard	Standard / AEC-Q200	Standard	Standard / AEC-Q200	Standard	MIL-PRF-49470
Type	Vertical	Horizontal	Horizontal	Horizontal	Horizontal	Horizontal	Horizontal	Horizontal	Horizontal	Horizontal	Horizontal
# of Leads per Side	1 - 2	2 - 14	3 - 20	3 - 11	3 - 10	3 - 20	2	3 - 5	2	3 - 20	3 - 20
Temperature	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +200°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Dielectric	X7R	X7R	X7R, NP0/C0G	N1500, NP0/C0G, X7R	X7R	X7R, NP0/C0G	X7R	X7R	X7R	N1500, NP0/C0G, X7R	BP, BQ, BR, BX
Voltage Rating	50 - 500V	50 - 500V	50 - 500V	1KV - 5KV	50 - 500V	50 - 500V	25 - 100V	25 - 500V	25 - 500V	50 - 500V	25 - 500V
Capacitance	0.12 - 68 µF	0.12 - 180 µF	0.5 - 400 µF	0.0007 - 5.50 µF	0.56 - 120 µF	0.01 - 270 µF	2.2 - 22 µF	0.047 - 47 µF	2.2 - 68 µF	0.01 - 390 µF	0.01 - 270 µF
Length	0.150 - 0.583”	0.342 - 1.598”	0.25 - 2.05”	0.25 - 1.14”	0.25 - 1.05”	0.25 - 2.05”	0.20 - 0.32”	0.270 - 0.535”	0.213”	0.25 - 2.155”	0.224 - 2.075”
Width	0.417 - 0.893”	0.362 - 0.944”	0.30 - 1.35”	0.30 - 2.16”	0.30 - 0.50”	0.30 - 1.35”	0.279 - 0.295”	0.30 - 0.586”	0.283”	0.30 - 1.43”	0.30 - 1.35”
Height	0.342 - 0.850”	0.150 - 0.583”	0.12 - 0.65”	0.12 - 0.65”	0.12 - 0.60”	0.12 - 0.65”	-	0.058 - 0.08”	0.047 - 0.071”	0.12 - 0.80”	0.12 - 0.65”
Total Height MIN.	-	-	0.185”	0.185”	0.175”	0.185”	0.124”	0.192”	0.181”	0.185”	-
Total Height MAX.	-	-	0.77”	0.77”	0.665”	0.825”	0.148”	0.323”	0.295”	0.815”	-

Stacked PME Ceramic Capacitor Introduction

	ST10 / RT10			ST12 / RT12		ST20 / RT20		
								
Temperature	-55°C to +125°C			-55°C to +125°C		-55°C to +125°C		
ESL	~1.2nH			~0.61nH		~1nH		
Voltage Rating	25	50	100	50	100	25V	50V	100V
2119	82µF	18µF & 39µF	8.2µF					
3830						68µF	27µF	14µF
4325				18µF	8.2µF			
5830						100µF	47µF	22µF
6325				27µF	12µF			
110025				50µF	22µF			
110030						220µF	100µF	47µF

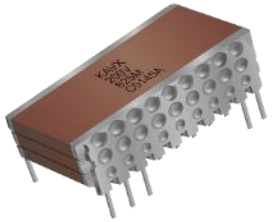
Stacked PME Low Inductance Options

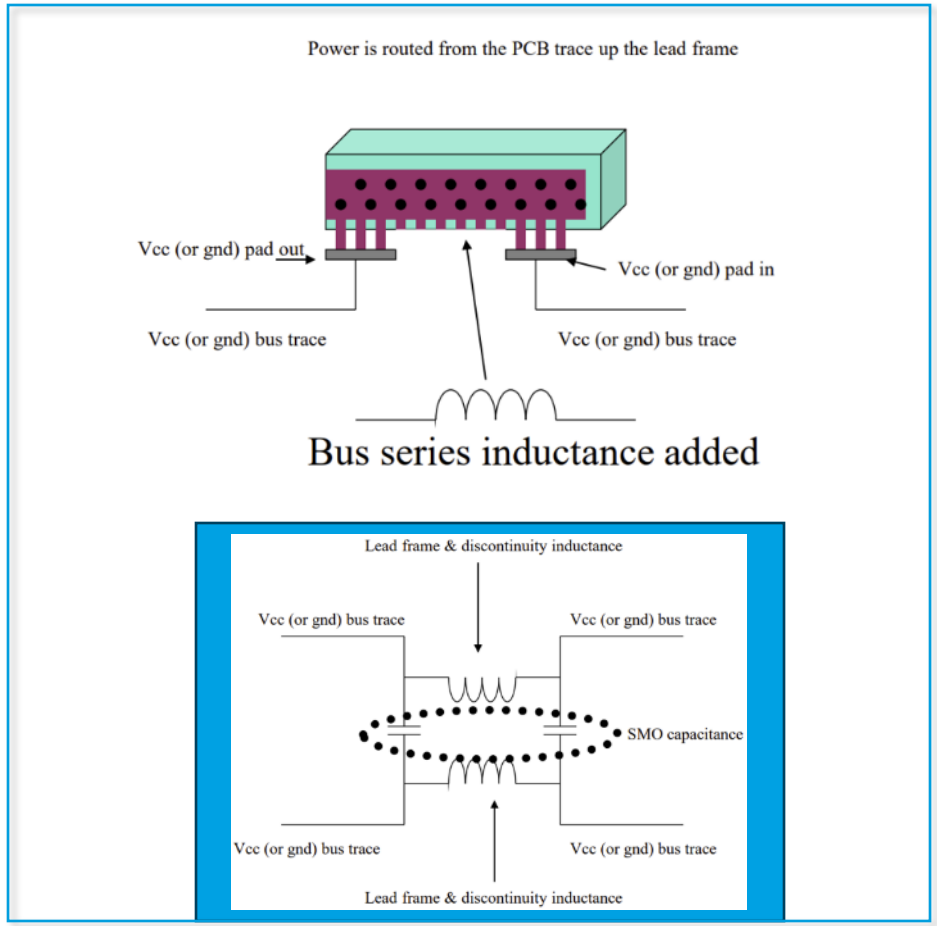
Standard Configuration



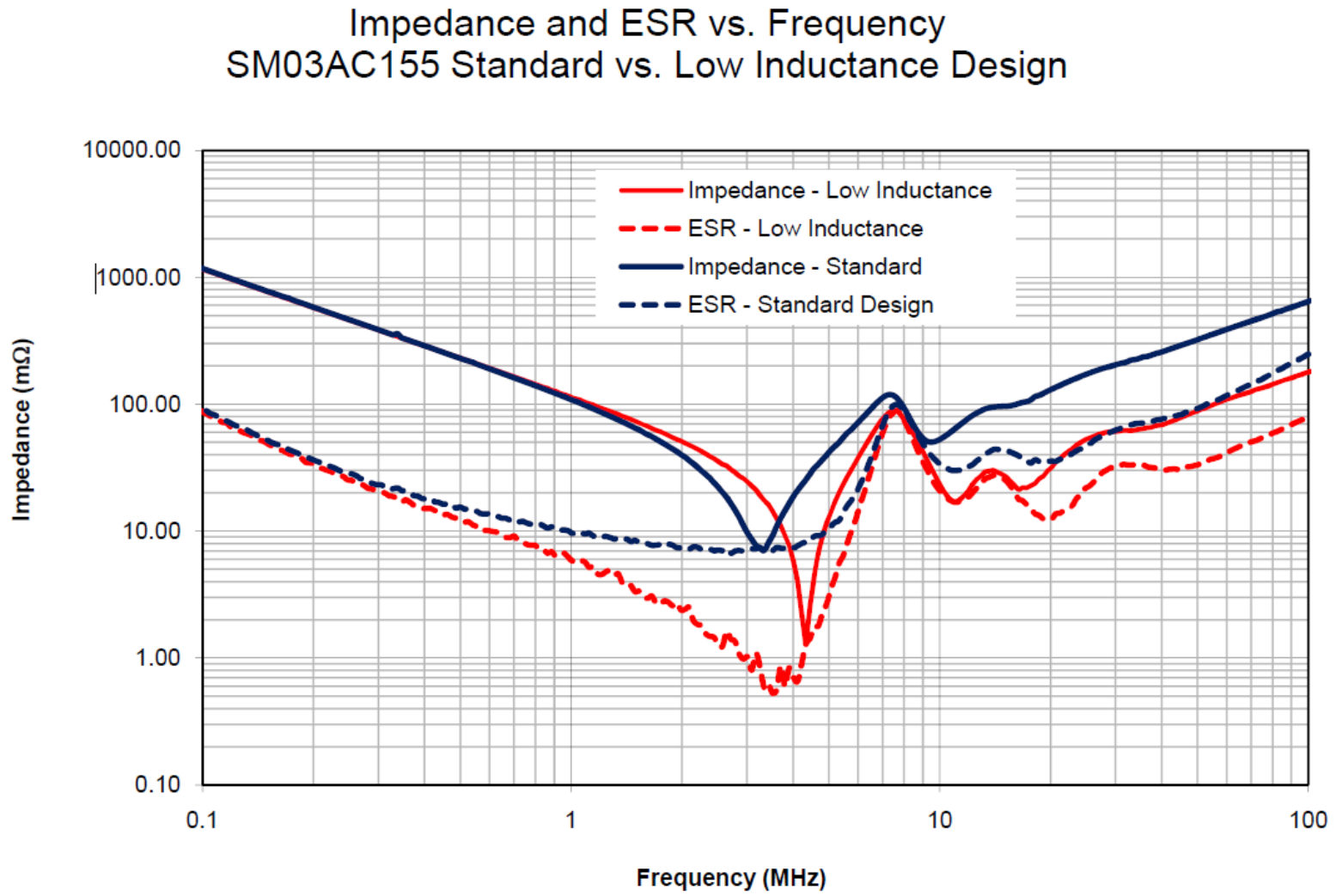
Optimize

Low Inductance Configuration



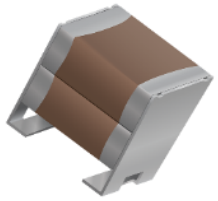
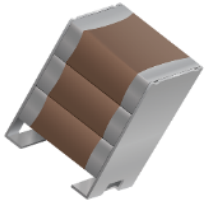


PME Stack Configuration Data



Stacked BME Ceramic Capacitor Introduction

Capacitor Background – BME MLCC Stack

	Horizontal BME Stack (2X)			Horizontal BME Stack (3X)			Vertical BME Stack (3X/5X/10X)		
									
Standard	DSCC 25007			Pending DSCC 25007			Pending DSCC 25007		
Temperature	-55°C to +125°C			-55°C to +125°C			-55°C to +125°C		
Dielectric	X7R			X7R			X7R		
Voltage Rating	10/16/25 V	50 V	100 V	10/16/25 V	50 V	100 V	10/16/25 V	50 V	100 V
Capacitance	27µF - 47 µF	18µF & 22µF	8.2µF & 10µF	56µF & 68µF	27µF - 47µF	12µF - 18µF	68µF - 220µF	33µF - 120µF	18µF - 68µF
L/W/H mm (in)	7.2 (0.283)	5.4 (0.213)	7.5 (0.296)	7.2 (0.283)	5.4 (0.213)	10.4 (0.410)			

- High Current Handling capability
- 100% Group A tested under DSCC
- Input/Output Filtering Hi-Rel applications

- All BME X7R 2220 capacitors come from a MIL-PRF 32535 qualified production facility
- Can be finished in either J, L, or Paddle (single foot) type lead frame
- Initial range consists of 2 to 3 horizontal placed caps or 3 to 10 vertically oriented
- Sn/Pb finished lead frames

DSCC 25007 Drawing

DRAFT DATED 29 October 2024

1. SCOPE

1.1 Scope. This drawing describes the general requirements for stacked ceramic capacitors.

1.2 Part or Identifying Number (PIN). The complete PIN is as follows:

25XXX	B	103	K	J	B
Performance specification number	Voltage (see 1.2.1)	Capacitance (see 1.2.2)	Capacitance tolerance (see 1.2.3)	Configuration (see 1.2.4)	Group B testing option (see 1.2.5)

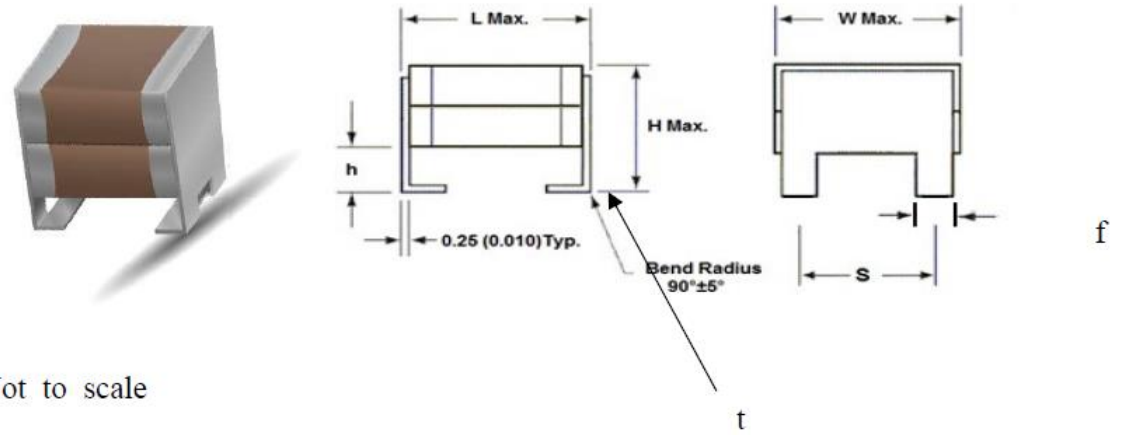
TABLE III. Group A inspection.

Inspection	Requirement paragraph	Sampling procedure
Subgroup 1		
Thermal shock and voltage conditioning 1/	3.3.3	100% inspection
Insulation resistance (at +125°C)	3.3.4	
Dielectric withstanding voltage (at +25°C)	3.3.5	
Insulation resistance (at +25°C)	3.3.4	
Capacitance (at +25°C)	3.2.1	
Dissipation factor (at +25°C)	3.3.6	
Subgroup 2		
Visual and mechanical examination:	3.3.7	13 samples
Physical dimensions	Figure 1	0 failures
Workmanship	3.8	
Subgroup 3		
Solderability	3.3.8	3 samples 0 failures

TABLE IV. Group B inspection.

Inspection	Requirement paragraph	Sampling procedure
Subgroup 1		
Thermal shock (mounted)	3.3.3.1	12 samples 1 failure
Life	3.3.9	
Subgroup 2		
Resistance to soldering heat		12 samples 0 failures
Temperature humidity bias	3.3.11	
Subgroup 3		
Destructive physical analysis	3.3.12	3 samples 0 failures

Horizontal Dimension , mm (inch)



Not to scale

Max Stack Length, L	Max Stack Width , W	Profile Height , h	Lead frame feet distance , S	Lead frame feet, t	Lead frame feet width , f	Max Stack Height x 2 Chip Stack, H	Max Stack Height x 3 Chip Stack ,H
7.2 (0.283)	5.4 (0.213)	1.50 ±0.30 (0.059 ±0.012)	2.54 ±0.30 (0.108 ±0.012)	1.50 ±0.10 (0.059 ±0.004)	1.45±0.30 (0.057 ±0.012)	7.5 (0.296)	10.4 (0.410)

Thermal Shock Group A 20 cycles , Group B 100 Cycle Life

Life Group A 168 - 264 hours 2 x RV

Group B 1000 hours 2 x RV

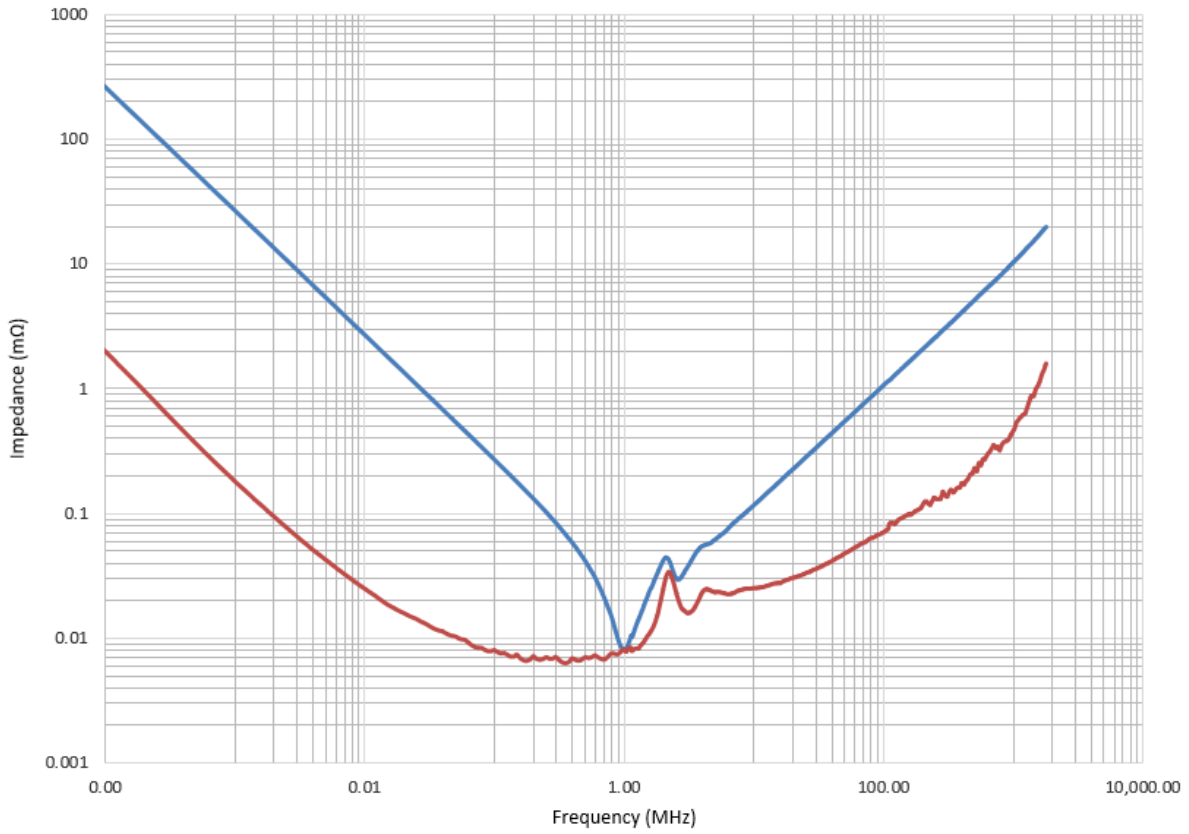
Stacked BME vs PME Comparison

	Prototype DSCC (M32535) BME 100 Volt ~10 µf Dimensions	Standard Mil 49470 PME 100 Volt ~10 µf Dimensions
Length	7 mm	26 mm
Width	5.5 mm	12 mm
Stack Height	7.5 mm	6 mm
Volume	289mm³ / 0.017 inch³	1872 mm³ / 0.114 inch³
Weight	0.75 grams	9.3 grams
Self Resonance	1.04 MHz	720 kHz

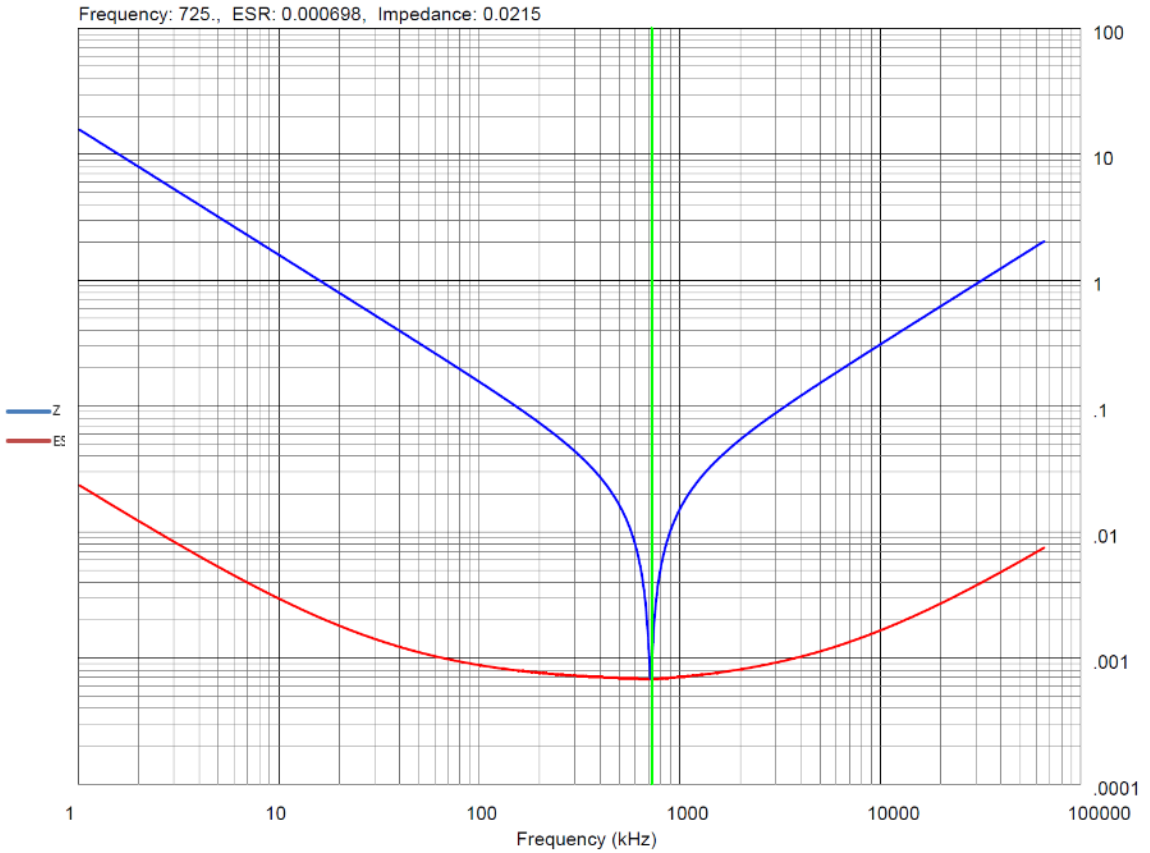
*dimensions are approximations

BME/PME Stack Z & ESR Vs Frequency Data

BME
100V, 10 µF Stack Z & ESR vs Freq
[SRF = 1.04 MHz]

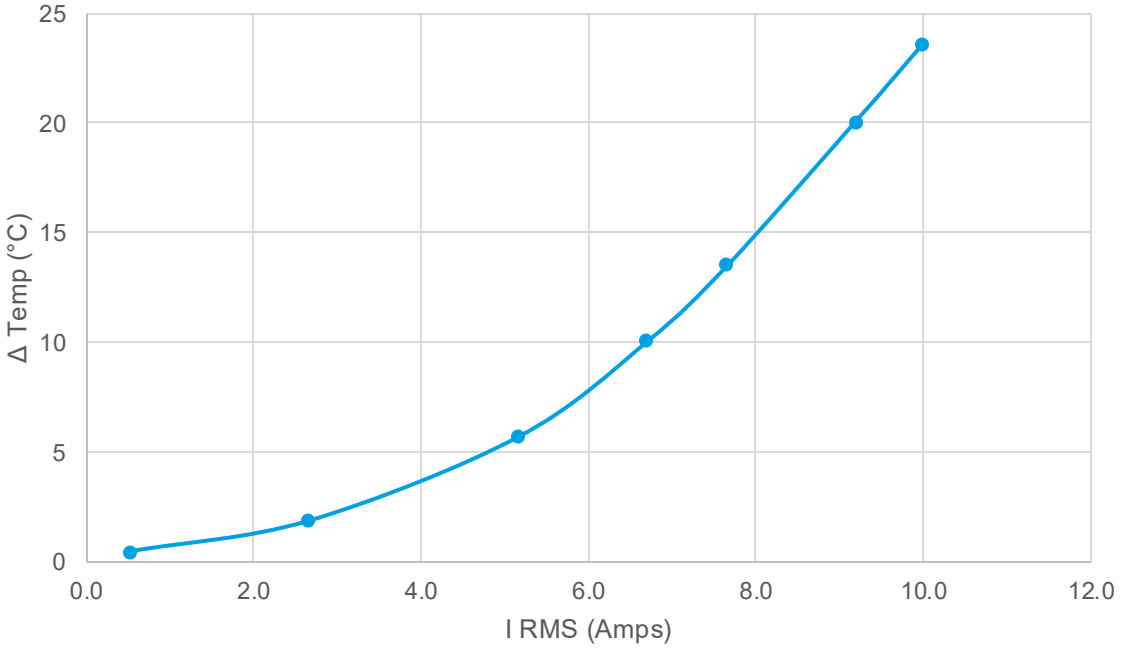


PME
100V, 10 µF Stack Z & ESR vs Freq
[SRF = 725 kHz]

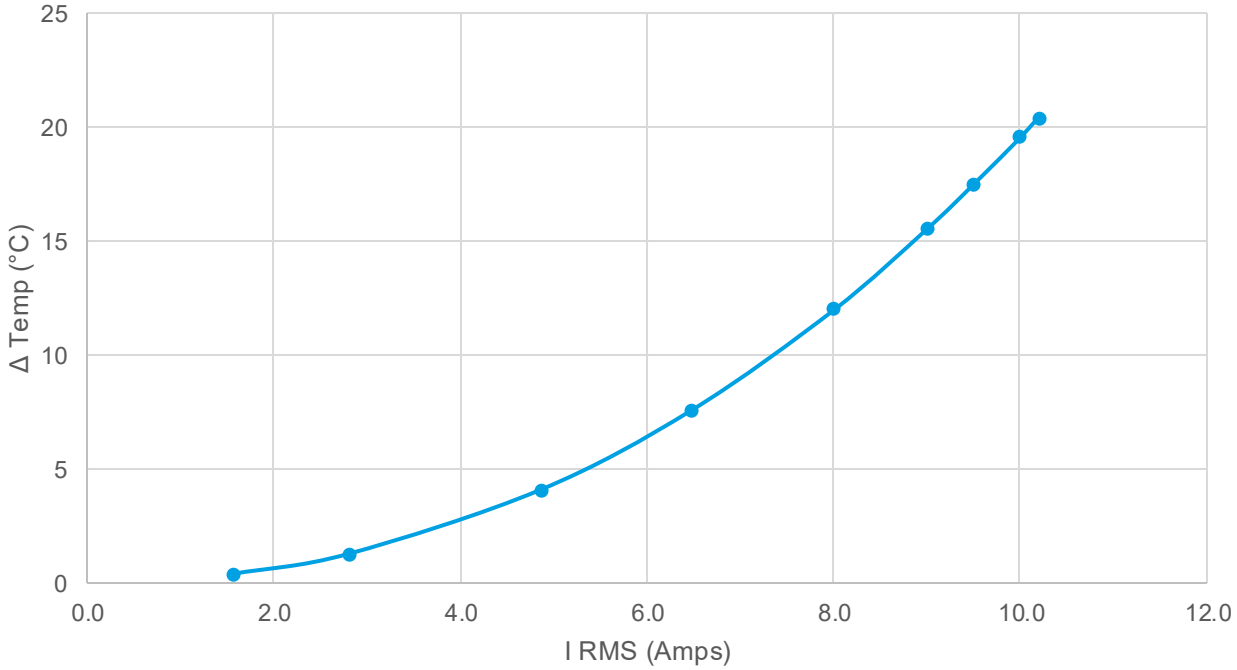


Stacked BME Ceramic Capacitor Introduction

BME Temperature Rise vs. Current - 100 kHz



PME Temperature Rise vs. Current - 100 kHz



→ **BME stack is 1/6 of the volume of PME stack**

Stacked Capacitor Technology Summary

- In general, Stacked Technology can be used to:
  - Reduce Board Space in the X & Y
  - Improve Shock and Vibration performance
  - Improve Frequency Response characteristics
  - Much more!

- Where to use each technology of stacked components:

Technology	Where to Use
Tantalum	High Capacitance / Small Footprint
Polymer	High Capacitance / Small Footprint + Higher Voltage
Ceramic	Low ESR, Low Current, or Higher Ripple Current
RF Ceramic	High Power & High Frequency
Varistor	EMI and ESD Mitigation

THANK YOU.

KYOCERA AVX

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